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April 2016

74LVX3245
8-Bit, Dual-Supply Translating Transceiver with 3-State Outputs

Features

- Bidirectional Interface Between 3 V and 5 V Buses
- Inputs Compatible with TTL Level
- 3 V Data Flow at A-Port and 5 V Data Flow at B-Port
- Outputs Source / Sink: 24 mA
- Guaranteed Simultaneous Switching Noise Level and Dynamic Threshold Performance
- Implements Proprietary EMI Reduction Circuitry
- Functionally Compatible with the 74 Series 245

Description

The 74LVX3245 is a dual-supply, 8-bit translating transceiver designed to interface between a 3 V bus and a 5 V bus in a mixed 5 V supply environment. The Transmit/ Receive ($T/\overline{R}$) input determines the direction of data flow. Transmit (active-HIGH) enables data from A-ports to B-ports; receive (active-LOW) enables data from B-ports to A-ports. The output enable input, when HIGH, disables both A- and B-ports by placing them in a high-impedance condition. The A-port interfaces with the 3 V bus; the B-port interfaces with the 5 V bus.

The 74LVX3245 is suitable for mixed-voltage applications, such as notebook computers using 3.3 V CPU and 5V peripheral components.

Related Resources

- *AN-5001 — Using Fairchild's LVX Low-Voltage Dual-Supply CMOS Translating Transceivers*

Ordering Information

Part Number	Operating Temperature Range	Package	Packing Method
74LVX3245QSC	-40 to +85°C	24-Lead Quarter-Size Outline Package (QSOP), JEDEC MO-137, 0.150" Wide	Tubes
74LVX3245QSCX			Tape and Reel
74LVX3245MTC		24-Lead Thin-Shrink Small-Outline Package (TSSOP), JEDEC MO-153, 4.4 mm Wide	Tubes
74LVX3245MTCX			Tape and Reel

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Logic Symbol

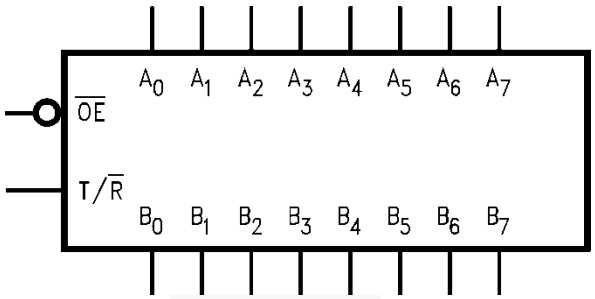

Figure 1. Logic Symbol

Pin Configuration

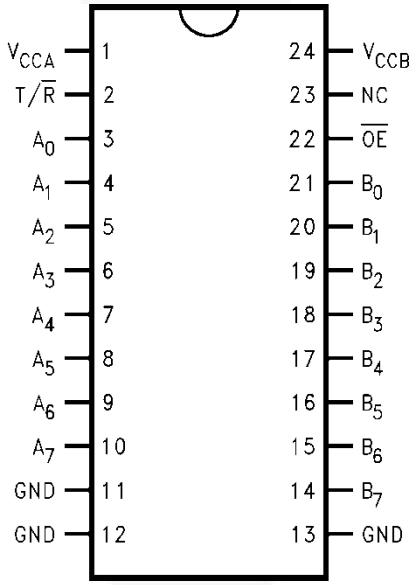

Figure 2. Pin Configuration

Pin Definitions

Pin #	Name	Description
1	V_{CCA}	Supply Voltage
2	T/$\overline{R}$	Transmit/Receive Input
3, 4, 5, 6, 7, 8, 9, 10	A_0, A_1, A_2, A_3, A_4, A_5, A_6, A_7	Port-A Inputs or 3-State Outputs
11, 12, 13	GND	Ground
14, 15, 16, 17, 18, 19, 20, 21	B_7, B_6, B_5, B_4, B_3, B_2, B_1, B_0	Port-B Inputs or 3-State Outputs
22	/OE	Output Enable Input
23	NC	No Connect
24	V_{CCB}	Supply Voltage

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Logic Diagram

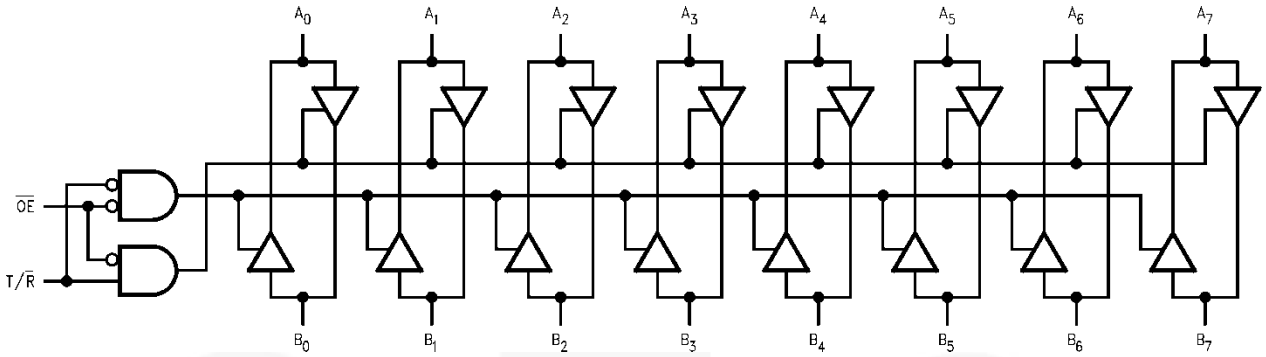

Figure 3. Logic Diagram

Table 1. Truth Table

Inputs		Outputs
/OE	**T/$\overline{R}$**	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	HIGH-Z State

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

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Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter			Min.	Max.	Unit
V_{CCA}, V_{CCB}	Supply Voltage			-0.5	7.0	V
V_{IN}	DC Input Voltage; (/OE, T/$\overline{R}$)			-0.5	V_{CCA} +0.5	V
$V_{I/O}$	DC Input / Output Voltage		A_n	-0.5	V_{CCA} to +0.5	V
			B_n	-0.5	V_{CCB} to +0.5	
I_{IN}	DC Input Diode Current (/OE and T/$\overline{R}$)				±20	mA
I_{OK}	DC Output Diode Current				±50	mA
I_O	DC Output Source or Sink Current				±50	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	Output Pin			±50	mA
		Maximum Current at	I_{CCA}		±100	
			I_{CCB}		±200	
T_{STG}	Storage Temperature Range			-65	+150	°C
I_{SINK}	DC Latch-Up Source or Sink Current				±300	mA
T_J	Maximum Junction Temperature Under Bias				+150	°C
ESD	Electrostatic Discharge Capability	Human Body Model, JESD22-A114			2500	V

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter		Min.	Max.	Unit
V_{CCA}	Supply Voltage		2.7	3.6	V
V_{CCB}			4.5	5.5	
V_I	Input Voltage (/OE and T/$\overline{R}$)		0	V_{CCA}	V
$V_{I/O}$	DC Input / Output Voltage	A_n	0	V_{CCA}	V
		B_n	0	V_{CCB}	
T_A	Operating Temperature, Free Air		-40	+85	°C
$\Delta t / \Delta V$	Minimum Input Edge Rate (V_{IN} from 30 to 70% of V_{CC}, V_{CC} at 3.0 V, 4.5 V, and 5.5 V)			8	ns/V

Note:

1. Unused pins (inputs and I/O's) must be held HIGH or LOW. They may not float.

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DC Electrical Characteristics

Symbol	Parameter		Conditions	V_{CCA} (V)	V_{CCB} (V)	T_A= -25°C	T_A=-40 to+85°C		Unit
						Typ.	Guaranteed Limits		
V_{IHA}	Minimum HIGH Level Input Voltage	A_n, T/$\overline{R}$, /OE	$V_{OUT} \leq 0.1$ V or $\geq V_{CC}$ - 0.1 V	3.6	5.0		2.0	2.0	V
				2.7	5.0		2.0	2.0	
V_{IHB}		B_n		3.3	4.5		2.0	2.0	
				3.3	5.5		2.0	2.0	
V_{ILA}	Minimum LOW Level Input Voltage	A_n, T/$\overline{R}$, /OE	$V_{OUT} \leq 0.1$ V or $\geq V_{CC}$ - 0.1 V	3.6	5.0		0.8	0.8	V
				2.7	5.0		0.8	0.8	
V_{ILB}		B_n		3.3	4.5		0.8	0.8	
				3.3	5.5		0.8	0.8	
V_{OHA}	Minimum HIGH Level Output Voltage		I_{OUT}=-100 µA	3.0	4.5	2.99	2.90	2.90	V
			I_{OH}=-24 mA	3.0	4.5	2.65	2.35	2.25	
			I_{OH}=-12 mA	2.7	4.5	2.50	2.30	2.20	
			I_{OH}=-24 mA	2.7	4.5	2.30	2.10	2.00	
V_{OHB}			I_{OUT}=-100 µA	3.0	4.5	4.50	4.40	4.40	
			I_{OH}=-24 mA	3.0	4.5	4.25	3.86	3.76	
V_{OLA}	Minimum LOW Level Output Voltage		I_{OUT}=100 µA	3.0	4.5	0.002	0.100	0.100	V
			I_{OH}=24 mA	3.0	4.5	0.210	0.360	0.440	
			I_{OH}=12 mA	2.7	4.5	0.110	0.360	0.440	
			I_{OH}=24 mA	2.7	4.5	0.220	0.420	0.500	
V_{OLB}			I_{OUT}=100 µA	3.0	4.5	0.002	0.100	0.100	
			I_{OH}=24 mA	3.0	4.5	0.180	0.360	0.440	
I_{IN}	Maximum Input Leakage Current; /OE, T/$\overline{R}$		V_{IN}=V_{CCB}, GND	3.6	5.5		±0.1	±1.0	µA
I_{OZA}	Maximum 3-State Output Leakage; A_n		V_{IN}=V_{IL}, V_{IH}; /OE= V_{CCA}; V_O=V_{CCA}, GND	3.6	5.5		±0.5	±5.0	µA
I_{OZB}	Maximum 3-State Output Leakage; B_n		V_{IN}=V_{IL}, V_{IH}; /OE= V_{CCA}; V_O=V_{CCB}, GND	3.6	5.5		±0.5	±5.0	µA
ΔI_{CC}	Maximum I_{CCT}/Input at	B_n	V_{IN}=V_{CCB}-2.1 V	3.6	5.5	1.00	1.35	1.50	mA
		A_n, T/$\overline{R}$, /OE	V_{IN}=V_{CCA}-0.6 V	3.6	5.5		0.35	0.50	
I_{CCA}	Quiescent V_{CCA} Supply Current		A_n=V_{CCA} or GND, B_n=V_{CCB} or GND, /OE=GND, T/$\overline{R}$ =GND	3.6	5.5		5	50	µA
I_{CCB}	Quiescent V_{CCB} Supply Current		A_n=V_{CCA} or GND, B_n=V_{CCB} or GND, /OE=GND, T/$\overline{R}$ =V_{CCA}	3.6	5.5		8	80	

Continued on the following page…

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DC Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	V_{CCA} (V)	V_{CCB} (V)	T_A= -25°C	T_A=-40 to+85°C		Unit
					Typ.	Guaranteed Limits		
V_{OLPA}	Quiet Output Maximum Dynamic V_{OL}[2, 3]		3.3	5.0		0.8		V
V_{OLPB}			3.3	5.0		1.5		
V_{OLVA}	Quiet Output Minimum Dynamic V_{OL}[2, 3]		3.3	5.0		-0.8		V
V_{OLVB}			3.3	5.0		-1.2		
V_{IHDA}	Minimum HIGH Level Dynamic Input Voltage[2, 4]		3.3	5.0		2.0		V
V_{IHDB}			3.3	5.0		2.0		
V_{ILDA}	Maximum LOW Level Dynamic Input Voltage[2, 4]		3.3	5.0		0.8		V
V_{ILDB}			3.3	5.0		0.8		

Notes:

2. Worst-case package.
3. Maximum number of outputs defined as (n). Data inputs are driven 0 V to V_{CC} level; one output at GND.
4. Maximum number of data inputs (n) switching. (n-1) inputs switching 0 V to V_{CC} level. Input-under-test switching; V_{CC} level to threshold (V_{IHD}), 0V to threshold (V_{ILD}), f=1 MHz.

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AC Electrical Characteristics

Symbol	Parameter	T_A=+25°C, C_L=50 pF, V_{CCA}=3.3 V[5], V_{CCB}=5.0 V[6]			T_A=-40 to +85°C, C_L=50 pF, V_{CCA}=3.3 V[5], V_{CCB}=5.0 V[6]		T_A=-40 to +85°C, C_L=50 pF, V_{CCA}=2.7 V, V_{CCB}=5.0 V		Unit
		Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{PHL}, t_{PLH}	Propagation Delay A to B	1.0	5.4	8.0	1.0	8.5	1.0	9.0	ns
		1.0	5.6	7.5	1.0	8.0	1.0	8.5	
	Propagation Delay B to A	1.0	5.1	7.5	1.0	8.0	1.0	8.5	
		1.0	5.7	7.5	1.0	8.0	1.0	8.5	
t_{PZL}, t_{PZH}	Output Enable Time /OE to B	1.0	4.8	8.0	1.0	8.5	1.0	9.0	ns
		1.0	6.3	8.5	1.0	9.0	1.0	9.5	
	Output Enable Time /OE to A	1.0	6.3	8.5	1.0	9.0	1.0	9.5	
		1.0	6.8	9.0	1.0	9.5	1.0	10.0	
t_{PHZ}, t_{PLZ}	Output Disable Time /OE to B	1.0	5.3	7.5	1.0	8.0	1.0	8.5	ns
		1.0	4.2	7.0	1.0	7.5	1.0	8.0	
	Output Disable Time /OE to A	1.0	5.3	8.0	1.0	8.5	1.0	9.0	
		1.0	3.7	6.5	1.0	7.0	1.0	7.5	
t_{OSHL}, t_{OSLH}	Output to Output Skew, Data to Output[7]		1.0	1.5		1.5		1.5	ns

Notes:

5. Voltage range 3.3 V is 3.3 V ± 0.3 V.
6. Voltage range 5.0 V is 5.0 V ± 0.5 V.
7. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}). Parameter guaranteed by design.

Capacitance

Symbol	Parameter		Conditions	Typ.	Unit
C_{IN}	Input Capacitance		V_{CC} = Open	4.5	pF
$C_{I/O}$	Input / Output Capacitance		V_{CCA} = 3.3 V, V_{CCB} = 5.0 V	15	pF
C_{PD}	Power Dissipation Capacitance[8]	A to B	V_{CCA} = 3.3 V, V_{CCB} = 5.0 V	55	pF
		B to A		40	

Note:

8. C_{PD} is measured at 10 MHz.

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8-Bit Dual-Supply Translating Transceiver

The 74LVX3245 is a dual-supply device capable of bi-directional signal translation. This level shifting ability provides an efficient interface between low-voltage CPU local bus with memory and a standard bus defined by 5 V I/O levels. The device control inputs can be controlled by the low-voltage CPU and core logic or a bus arbitrator with 5 V I/O levels.

Manufactured on a sub-micron CMOS process, the 74LVX3245 is ideal for mixed voltage applications such as notebook computers using 3.3 V CPUs and 5 V peripheral devices.

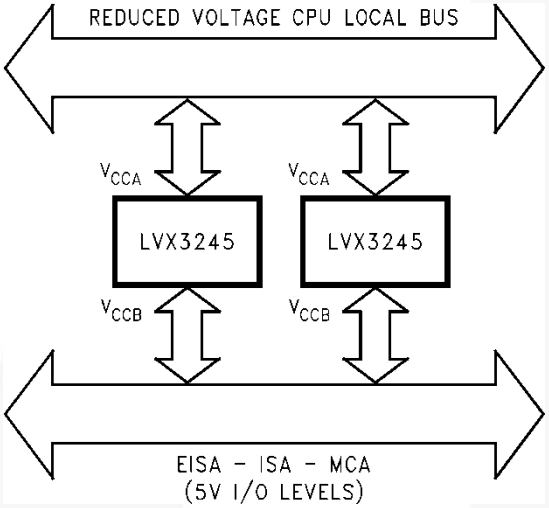

Figure 4. Application Example

Power-Up Considerations

To ensure that the system does not experience unnecessary I_{CC} current draw, bus contention, or oscillations during power up; the following guidelines should be followed to *(refer to Table 2)*:

- Power up the control side of the device first (V_{CCA}).
- /OE should ramp with or ahead of V_{CCA}. This helps guard against bus contention.
- The Transmit/Receive (T/$\overline{R}$) control pin should ramp with V_{CCA}. This ensures that the A-port data pins are configured as inputs. With V_{CCA} receiving power first, the I/O port should be configured as an input to help guard against bus contention and oscillations.
- A-side data inputs should be driven to a valid logic level. This prevents excessive current draw.

The above steps ensure that there are no bus contentions or oscillations, and therefore no excessive current draw occurs during the power-up cycling. These steps help prevent possible damage to the translator devices and potential damage to other system components.

Table 2. Low Voltage Translator Power-Up Sequencing

Device	V_{CCA}	V_{CCB}	T/$\overline{R}$	/OE	A-Side I/O	B-Side I/O	Floatable Pin Allowed
74LVX3245	3 V (Power-Up First)	5 V Configurable	Ramp with V_{CCA}	Ramp with V_{CCA}	Logic 0 V or V_{CCA}	Outputs	No

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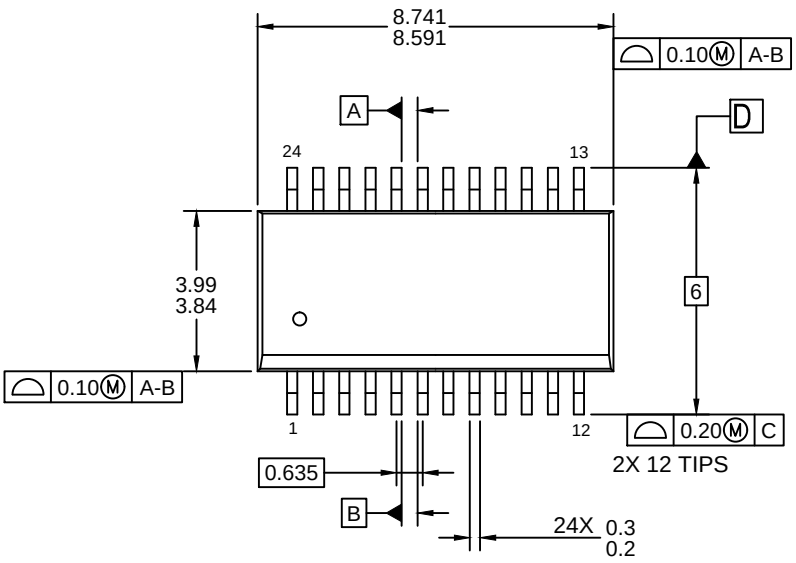
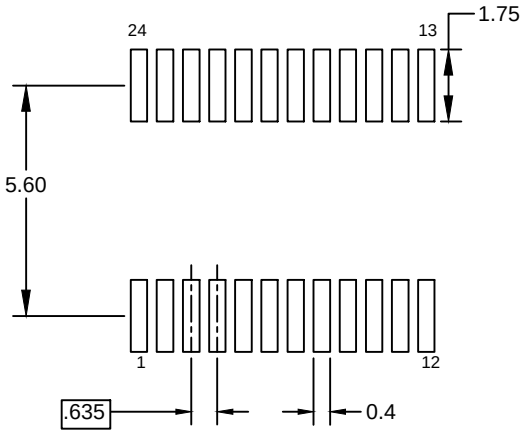


TOP VIEW

0.178 M C A-B D



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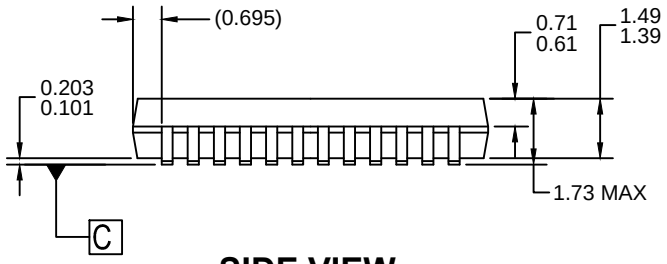

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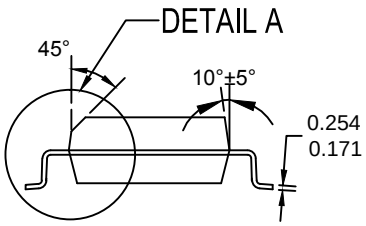
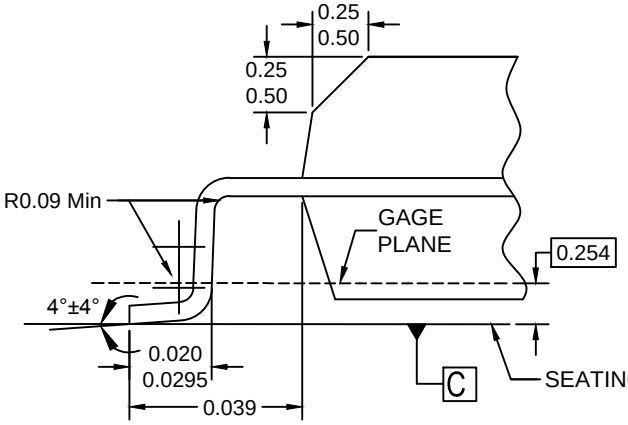


END VIEW



DETAIL A

NOTES :

A. THIS PACKAGE CONFORMS TO JEDEC M0-137 VARIATION AE

B. ALL DIMENSIONS ARE IN MILLIMETERS

C. DIMENSIONING AND TOLERANCES PER ANSI Y14.5M, 2009.

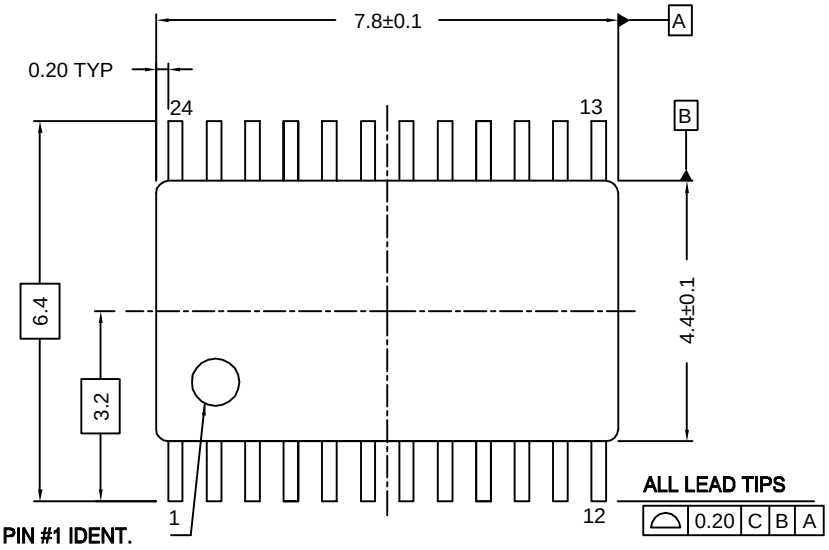
D. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS

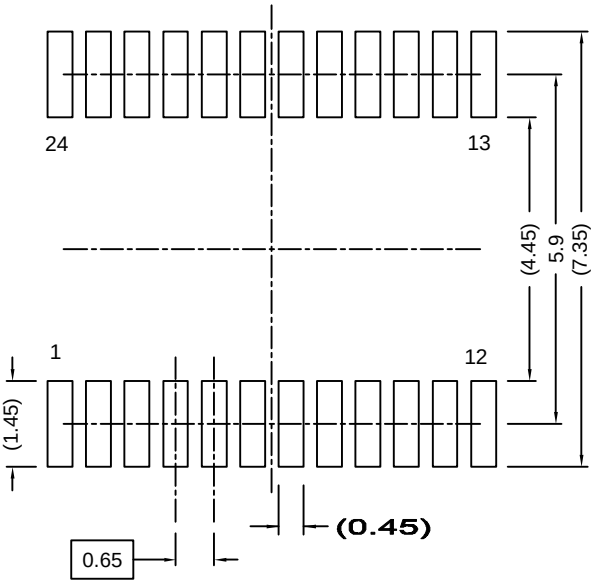
E. LAND PATTERN STANDARD: SOP63P600X175-24M.

F. DRAWING FILE NAME: MKT-MQA24rev3

FAIRCHILD

REVISIONS				
LTR	DESCRIPTION	EDCN	DATE	BY/APP'D
4	CHANGE TO FSPM DRAWING FORMAT N LEAD SHIFT TOL. FROM 0.13MM TO 0.10MM	ECN-MTC24REV4	21/12/2006	H.ALLEN





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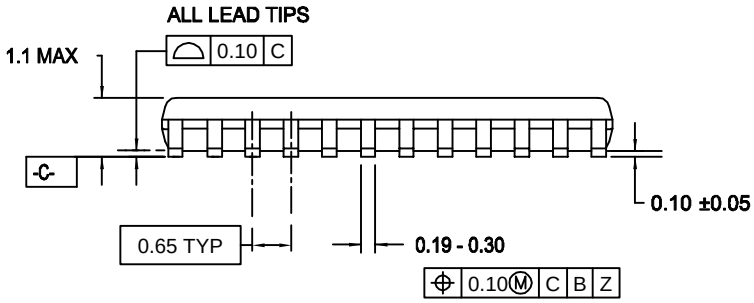

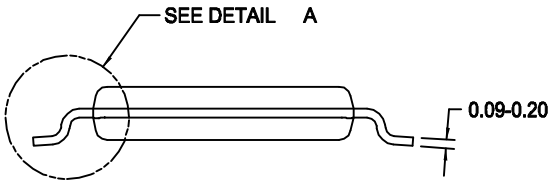

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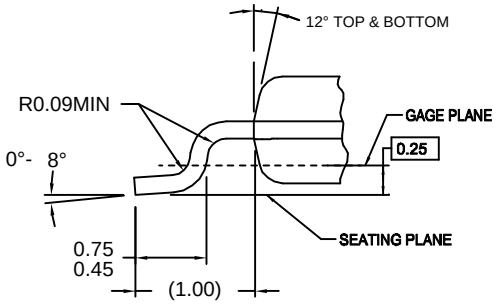

DETAIL A

NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AD, DATE 10/97.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1994

E. DRAWING FILE NAME: MTC24REV4

MTC24REV4

APPROVALS	DATE
DRAWN FEITAN	8-10-99
DFTG. CHK. H.ALLEN	21-12-2006
ENGR. CHK.	

FAIRCHILD SEMICONDUCTOR™ Bayan Lepas, FIZ, 11900, Penang, Malaysia.

24LD, TSSOP, JEDEC MO-153, 4.4MM WIDE

PROJECTION	SCALE	SIZE	DRAWING NUMBER	REV
INCH [MM]	N/A	A4	MKT-MTC24	4

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