# RX62N Group, RX621 Group
Renesas MCUs

R01DS0052EJ0140
Rev.1.40
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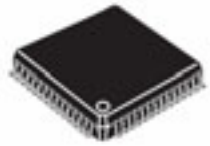
## 100 MHz 32-bit RX MCU with FPU, 165 DMIPS, up to 512-Kbyte Flash, Ethernet, USB 2.0 Full-Speed Host/Function/OTG, CAN, 12-bit ADC, TFT-LCD, RTC, up to 14 communication channels

## Features



TFLGA85 7 × 7 mm, 0.65 mm pitch
TFLGA145 9 × 9 mm, 0.65 mm pitch
LFBGA176 13 × 13 mm, 0.8 mm pitch

LQFP100 14 × 14 mm, 0. 5mm pitch
LQFP144 20 × 20 mm, 0.5 mm pitch

### ■ 32-bit RX CPU Core

- Delivers 165 DMIPS at a maximum operating frequency of 100 MHz
- Single Precision 32-bit IEEE-754 Floating Point
- Accumulator: 32 × 32 to 64-bit result, one instruction
- Mult/Divide Unit, 32 × 32 Multiply in one CPU clock for multiple instructions
- Interrupt response in as few as 5 CPU clock cycles
- CISC-Harvard Architecture with 5-stage pipeline
- Variable length instructions, ultra compact code
- Supports the Memory Protection Unit (MPU)
- Background JTAG debug plus high-speed trace

### ■ Low Power Design and Architecture

- 2.7V to 3.6V operation from a single supply
- 480 µA/MHz Run Mode with all peripherals on
- Deep Software Standby Mode with RTC
- Four low power modes

### ■ Main Flash Memory, no Wait-State

- 100 MHz operation, 10 nsec read cycle
- No wait states for read at full CPU speed
- 256K, 384K, 512K Byte size options
- For Instructions or Operands
- Programming from USB, SCI, JTAG, user code

### ■ Data Flash Memory

- Up to 32K Bytes with 30K Erase Cycles
- Background Erase/Program does not stall CPU

### ■ SRAM, no Wait-State

- 64K or 96K Byte size options
- For Operands or Instructions
- Back-up retention in Deep Software Standby Mode

### ■ DMA

- Four fully programmable internal DMA channels
- Two EXDMA channels for external-to-external transfers
- Data Transfer Controller (DTC)

### ■ Reset and Supply Management

- Power-On Reset (POR) monitor/generator
- Low Voltage Detect (LVD) with precision setting

### ■ System Clocking with Clock Monitoring

- External crystal, 8 MHz to 14 MHz to Internal PLL
- PLL source to system, USB, and Ethernet
- Internal 125 kHz LOCO for IWDT
- External crystal, 32 kHz for RTC

### ■ Real Time Clock

- Full calendar function, BCD format

### ■ Two Independent Watchdog Timers

- 125-kHz LOCO operation

### ■ Up to 14 Communication Interfaces

- USB 2.0 Full-Speed interfaces with PHY (2 ch)
  Supports Host/Function/OTG
  10 endpoints for types: Control, Interrupt, Bulk, Isochronous
- Ethernet MAC 10/100 Mbps, Half or Full Duplex Supported. (1 ch)
  Dedicated DMA with 2-Kbyte transmit and receive FIFOs.
  RMII or MII interface to external PHY
- CAN ISO11898-1, supports 32 mailboxes (1 ch)
- SCI channels: Asynchronous, clock sync, smartcard, and 9-bit modes (6 ch)
- $I^2C$ interfaces up to 1 M bps, SMBus support (2 ch)
- RSPI (2 ch)

### ■ External Address Space

- Eight CS areas (8 × 16 Mbytes)
- 128-Mbyte SDRAM area
- 8-/16-/32-bit bus space selectable for each area

### ■ TFT-LCD up to WQVGA resolution

### ■ Up to 20 Extended Function Timers

- 16-bit MTU2
  Input capture, Output Compare, PWM output, phase count mode (12 ch)
- 8-bit TMR (4 ch)
- 16-bit CMT (4 ch)

### ■ 1-MHz ADC units with two combination choices

- 12-bit × 8 ch. unit with single sample/hold circuit
- or (2) 10-bit × 4 ch units each with a sample/hold circuit
- AD-converted value addition mode (12-bit A/D converter)

### ■ 10-bit DAC, 2 channels

### ■ Up to 128 GPIO

- 5 V tolerant, Open-Drain, Internal Pull-up

### ■ Operation Temp

- –40°C to +85°C

# 1. Overview

## 1.1 Outline of Specifications

Table 1.1 lists the specifications in outline, and Table 1.2 lists the functions of products.

**Table 1.1 Outline of Specifications (1 / 4)**

| Classification | Module/Function | Description |
|---|---|---|
| CPU | CPU | ・ Maximum operating frequency: 100 MHz<br>・ 32-bit RX CPU<br>・ Minimum instruction execution time: One instruction per state (cycle of the system clock)<br>・ Address space: 4-Gbyte linear<br>・ Register set of the CPU<br>General purpose: Sixteen 32-bit registers<br>Control: Nine 32-bit registers<br>Accumulator: One 64-bit register<br>・ Basic instructions: 73<br>・ Floating-point instructions: 8<br>・ DSP instructions: 9<br>・ Addressing modes: 10<br>・ Data arrangement<br>Instructions: Little endian<br>Data: Selectable as little endian or big endian<br>・ On-chip 32-bit multiplier: 32 x 32 → 64 bits<br>・ On-chip divider: 32 / 32 → 32 bits<br>・ Barrel shifter: 32 bits<br>・ Memory-protection unit (MPU) |
| | FPU | ・ Single precision (32-bit) floating point<br>・ Data types and floating-point exceptions in conformance with the IEEE754 standard |
| Memory | ROM | ・ ROM capacity: 512 Kbytes (max.)<br>・ Two on-board programming modes<br>Boot mode (The user MAT is programmable via the SCI and USB.)<br>User program mode<br>・ Parallel programmer mode (for off-board programming) |
| | RAM | RAM capacity: 96 Kbytes (max.) |
| | Data flash | Data flash capacity: 32 Kbytes |
| MCU operating modes | | ・ Single-chip mode, on-chip ROM enabled expansion mode, and on-chip ROM disabled expansion mode (software switching) |
| Clock | Clock generation circuit | ・ Two circuits: Main clock oscillator and subclock oscillator<br>・ Internal oscillator: Low-speed on-chip oscillator<br>・ Structure of a PLL frequency synthesizer and frequency divider for selectable operating frequency<br>・ Oscillation stoppage detection<br>・ Independent frequency-division and multiplication settings for the system clock (ICLK), peripheral module clock (PCLK), and external bus clock (BCLK)<br>The CPU and other bus masters run in synchronization with the system clock (ICLK): 8 to 100 MHz<br>Peripheral modules run in synchronization with the peripheral module clock (PCLK): 8 to 50 MHz<br>・ Devices connected to the external bus run in synchronization with the external bus clock (BCLK pin): 8 to 50 MHz*1 |
| Reset | | ・ Pin reset, power-on reset, voltage-monitoring reset, watchdog timer reset, independent watchdog timer reset, and deep software standby reset |
| Voltage detection circuit | | ・ When the voltage on VCC falls below the voltage detection level (Vdet), an internal reset or internal interrupt is generated. |
| Low power consumption | Low power consumption facilities | ・ Module stop function<br>・ Four low power consumption modes<br>Sleep mode, all-module clock stop mode, software standby mode, and deep software standby mode |

**Table 1.1 Outline of Specifications (2 / 4)**

| Classification | Module/Function | Description |
|---|---|---|
| Interrupt | Interrupt control unit | ・Peripheral function interrupts: 146 sources<br>・External interrupts: 16 (pins IRQ0 to IRQ15)<br>・Non-maskable interrupts: 3 (the NMI pin, oscillation stop detection interrupt, and voltage-monitoring interrupt)<br>・Sixteen levels specifiable for the order of priority |
| | User break controller (as an optional function) | ・Two breakpoint channels<br>・Address breaks in fetch cycles are specifiable (enabling ROM correction) |
| External bus extension | | ・The external address space can be divided into nine areas (CS0 to CS7, SDCS), each with independent control of access settings.<br>Capacity of each area: 16 Mbytes (CS0 to CS7), 128 Mbytes (SDCS)<br>A chip-select signal (CS0# to CS7#, SDCS#) can be output for each area.<br>Each area is specifiable as an 8-, 16-, or 32-bit bus space (however, only 176-pin versions support 32-bit bus spaces).<br>The data arrangement in each area is selectable as little or big endian (only for data).<br>・SDRAM interface connectable<br>・Bus format: Separate buses<br>・Wait control<br>・Write buffer facility |
| DMA | DMA controller | ・4 channels<br>・Three transfer modes: Normal transfer, repeat transfer, and block transfer<br>・Activation sources: Software trigger, external interrupts, and interrupt requests from peripheral functions |
| | EXDMA controller | ・2 channels<br>・Four transfer modes: Normal transfer, repeat transfer, block transfer, and cluster transfer<br>・Single-address transfer enabled with the EDACK signal<br>・Capable of direct data transfer to TFT LCD panels<br>・Activation sources: Software trigger, external DMA transfer requests (EDREQ), and interrupt requests from peripheral functions |
| | Data transfer controller | ・Three transfer modes: Normal transfer, repeat transfer, and block transfer<br>・Activation sources: Software trigger, external interrupts and interrupt requests from peripheral functions |
| I/O ports | Programmable I/O ports | ・I/O ports for the 176-pin LFBGA/145-pin TFLGA/144-pin LQFP/100-pin LQFP/85-pin TFLGA<br>・I/O pins: 126/103/103/72/58<br>・Input pins: 2/2/2/2/2<br>・Pull-up resistors: 56/44/44/40/28<br>・Open-drain outputs: 35/33/33/27/23<br>・5-V tolerance: 11/11/11/7/6 |
| Timers | Multi-function timer pulse unit | ・(16 bits x 6 channels) x 2 units<br>・Time bases for the 12 16-bit timer channels can be provided via up to 32 pulse-input/output lines and six pulse-input lines<br>・Select from among eight counter-input clock signals for each channel (PCLK/1, PCLK/4, PCLK/16, PCLK/64, MTCLKA, MTCLKB, MTCLKC, MTCLKD) other than channel 5, for which only four signals are available.<br>・Input capture function<br>・21 output compare/input capture registers<br>・Pulse output mode<br>・Complementary PWM output mode<br>・Reset synchronous PWM mode<br>・Phase-counting mode<br>・Generation of triggers for A/D converter conversion |
| | Port output enable | ・Controls the high-impedance state of the MTU's waveform output pins |

**Table 1.1 Outline of Specifications (3 / 4)**

| Classification | Module/Function | Description |
|---|---|---|
| Timers | Programmable pulse generator | ・(4 bits x 4 groups) x 2 units<br>・Pulse output with the MTU output as a trigger<br>・Maximum of 32-bit pulse output possible |
| | 8-bit timers | ・(8 bits x 2 channels) x 2 units<br>・Select from among seven internal clock signals (PCLK, PCLK/2, PCLK/8, PCLK/32, PCLK/64, PCLK/1024, PCLK/8192) and one external clock signal<br>・Capable of output of pulse trains with desired duty cycles or of PWM signals<br>・The 2 channels of each unit can be cascaded to create a 16-bit timer<br>・Generation of triggers for A/D converter conversion<br>・Capable of generating baud-rate clocks for SCI5 and SCI6 |
| | Compare match timer | ・(16 bits x 2 channels) x 2 units<br>・Select from among four internal clock signals (PCLK/8, PCLK/32, PCLK/128, PCLK/512) |
| | Watchdog timer | ・8 bits x 1 channel<br>・Select from among eight counter-input clock signals (PCLK/4, PCLK/64, PCLK/128, PCLK/512, PCLK/2048, PCLK/8192, PCLK/32768, PCLK/131072)<br>・Switchable between watchdog timer mode and interval timer mode |
| | Independent watchdog timer | ・14 bits x 1 channel<br>・Counter-input clock: Dedicated on-chip oscillator |
| Realtime clock | | ・Clock source: Subclock<br>・Time/calendar<br>Interrupt sources: Alarm interrupt, periodic interrupt, and carry interrupt |
| Communication function | Ethernet controller | ・Input and output of Ethernet/IEEE 802.3 frames<br>・Transfer at 10 or 100 Mbps<br>・Full- and half-duplex modes<br>・MII (Media Independent Interface) or RMII (Reduced Media Independent Interface) as defined in IEEE 802.3u<br>・Detection of Magic Packets™* or output of a "wake-on-LAN" signal (WOL)<br>・Compliance with flow control as defined in IEEE 802.3x standards<br>Note: * Magic Packet™ is a registered trademark of Advanced Micro Devices, Inc. |
| | DMA controller for Ethernet controller | ・Alleviation of CPU loads by the descriptor control method<br>・Transmission FIFO: 2 Kbytes; Reception FIFO: 2 Kbytes |
| | USB 2.0 host/ function module | ・Includes a UDC (USB Device Controller) and transceiver for USB 2.0<br>・Single port (176-pin products: two ports)<br>・Compliance with the USB 2.0 specification<br>・Transfer rate: Full speed (12 Mbps)<br>・Self-power mode and bus power are selectable<br>・OTG (On the Go) operation is possible<br>・Incorporates 2 Kbytes of RAM as a transfer buffer |
| | Serial communications interfaces | ・6 channels<br>・Serial communications modes:<br>Asynchronous, clock synchronous, and smart-card interface<br>・Multi-processor communications function<br>・On-chip baud rate generator allows selection of the desired bit rate<br>・Choice of LSB-first or MSB-first transfer<br>・Average transfer rate clock can be input from TMR timers for SCI5 and SCI6 |

**Table 1.1 Outline of Specifications (4 / 4)**

| Classification | Module/Function | Description |
|---|---|---|
| Communication function | I²C bus interfaces | ・ 2 channels (100-pin version: 1 channel)<br>・ Communications formats<br>I²C bus format/SMBus format<br>Master/slave selectable (For multi-master operation) |
| | CAN module | ・ 1 channel<br>・ 32 mailboxes |
| | Serial peripheral interfaces | ・ 2 channels<br>・ RSPI transfer facility<br>Using the MOSI (master out, slave in), MISO (master in, slave out), SSL (slave select), and RSPI clock (RSPCK) signals enables serial transfer through SPI operation (four lines) or clock-synchronous operation (three lines)<br>Capable of handling serial transfer as a master or slave<br>・ Data formats<br>Switching between MSB first and LSB first<br>The number of bits in each transfer can be changed to any number of bits from 8 to 16, or to 20, 24, or 32 bits.<br>128-bit buffers for transmission and reception<br>Up to four frames can be transmitted or received in a single transfer operation (with each frame having up to 32 bits)<br>・ Buffered structure<br>・ Double buffers for both transmission and reception<br>・ Max. transfer rate<br>In master mode: 18 Mbps<br>In slave mode: 6.25 Mbps |
| 12-bit A/D converter<br>10-bit A/D converter | | ・ 12 bits x 1 unit (1 unit x 8 channels) or 10 bits x 2 units (2 units x 4 channels);<br>12- and 10-bit A/D converters can be exclusively used.<br>・ 10- or 12-bit resolution<br>・ Conversion time: 1.0 μs per channel (in operation with PCLK at 50 MHz)<br>・ Two operating modes<br>Single mode<br>Scan mode (one-cycle scan mode or continuous scan mode)<br>・ Sample-and-hold function<br>・ Three ways to start A/D conversion<br>Conversion can be started by software, a conversion start trigger from a timer (MTU or TMR), or an external trigger signal.<br>・ Self-diagnostic functions |
| D/A converter | | ・ 2 channels (1 channel for 100-pin products)<br>・ 10-bit resolution<br>・ Output voltage: 0 V to VREFH |
| CRC calculator | | ・ CRC code generation for arbitrary amounts of data in 8-bit units<br>・ Select any of three generating polynomials:<br>$X^8 + X^2 + X + 1$, $X^{16} + X^{15} + X^2 + 1$, or $X^{16} + X^{12} + X^5 + 1$.<br>・ Generation of CRC codes for use with LSB-first or MSB-first communications is selectable. |
| Operating frequency | | 8 to 100 MHz |
| Power supply voltage | | VCC = PLLVCC = AVCC = 2.7 to 3.6V, VREFH = 2.7 to AVCC |
| Operating temperature | | –40 to +85°C |
| Package | | 176-pin LFBGA (PLBG0176GA-A), 145-pin TFLGA (PTLG0145JB-A),<br>144-pin LQFP (PLQP0144KA-A), 100-pin LQFP (PLQP0100KB-A)*2<br>85-pin TFLGA (PTLG0085JA-A)*2,*3 |

Note 1. For products in the 100-pin LQFP and 85-pin TFLGA, the synchronizing frequency is 8 to 25 MHz.
Note 2. The 100-pin LQFP and 85-pin TFLGA do not support the SDRAM area controller and EXDMA controller.
Note 3. The 85-pin TFLGA does not support the port-output enabling.

**Table 1.2 Functions of RX62N Group and RX621 Group Products**

| Functions | | RX62N Group | | | | | | | | RX621 Group | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | R5F562NxBxxx* | | | | R5F562NxAxxx* | | | | R5F5621xBxxx* | | | | |
| Package | | 176-pin LFBGA | 145-pin TFLGA | 144-pin LQFP | 100-pin LQFP | 176-pin LFBGA | 145-pin TFLGA | 144-pin LQFP | 100-pin LQFP | 176-pin LFBGA | 145-pin TFLGA | 144-pin LQFP | 100-pin LQFP | 85-pin TFLGA |
| External bus | SDRAM area controller | O | | | — | O | | | — | O | | | — | |
| DMA | DMA controller | O | | | | O | | | | O | | | | |
| | EXDMA controller | O | | | — | O | | | — | O | | | — | |
| | Data transfer controller | O | | | | O | | | | O | | | | |
| Timers | Multi-function timer pulse unit | O | | | | O | | | | O | | | | |
| | Port output enable | O | | | | O | | | | O | | | | — |
| | Programmable pulse generator | O | | | | O | | | | O | | | | |
| | 8-bit timers | O | | | | O | | | | O | | | | |
| | Compare match timer | O | | | | O | | | | O | | | | |
| | Realtime clock | O | | | | O | | | | O | | | | |
| | Watchdog timer | O | | | | O | | | | O | | | | |
| | Independent watchdog timer | O | | | | O | | | | O | | | | |
| Communication function | Ethernet controller/ DMA controller for Ethernet controller | O | | | | O | | | | — | | | | |
| | USB 2.0 host/function module | O | | | | O | | | | O | | | | |
| | Serial communications interfaces | O | | | | O | | | | O | | | | |
| | $I^2C$ bus interfaces | O | | | | O | | | | O | | | | |
| | CAN module | O | | | | — | | | | O | | | | |
| | Serial peripheral interfaces | O | | | | O | | | | O | | | | |
| A/D converter | | O | | | | O | | | | O | | | | |
| D/A converter | | O | | | | O | | | | O | | | | |
| CRC calculator | | O | | | | O | | | | O | | | | |

[Legend]
O: Supported, —: Not supported
Note: * For details on part numbers, see Table 1.3.

## 1.2 List of Products

Table 1.3 is a list of products, and Figure 1.1 shows how to read the product part no.

**Table 1.3 List of Products**

| Group | Part No. | Package | ROM Capacity | RAM Capacity | Data Flash | Operating Frequency (Max.) |
|---|---|---|---|---|---|---|
| RX62N | R5F562N8BDBG | PLBG0176GA-A | 512 Kbytes | 96 Kbytes | 32 Kbytes | 100 MHz |
| | R5F562N8BDLE | PTLG0145JB-A | 512 Kbytes | 96 Kbytes | 32 Kbytes | 100 MHz |
| | R5F562N8BDFB | PLQP0144KA-A | 512 Kbytes | 96 Kbytes | 32 Kbytes | 100 MHz |
| | R5F562N8BDFP | PLQP0100KB-A | 512 Kbytes | 96 Kbytes | 32 Kbytes | 100 MHz |
| | R5F562N7BDBG | PLBG0176GA-A | 384 Kbytes | 64 Kbytes | 32 Kbytes | 100 MHz |
| | R5F562N7BDLE | PTLG0145JB-A | 384 Kbytes | 64 Kbytes | 32 Kbytes | 100 MHz |
| | R5F562N7BDFB | PLQP0144KA-A | 384 Kbytes | 64 Kbytes | 32 Kbytes | 100 MHz |
| | R5F562N7BDFP | PLQP0100KB-A | 384 Kbytes | 64 Kbytes | 32 Kbytes | 100 MHz |
| | R5F562N8ADBG | PLBG0176GA-A | 512 Kbytes | 96 Kbytes | 32 Kbytes | 100 MHz |
| | R5F562N8ADLE | PTLG0145JB-A | 512 Kbytes | 96 Kbytes | 32 Kbytes | 100 MHz |
| | R5F562N8ADFB | PLQP0144KA-A | 512 Kbytes | 96 Kbytes | 32 Kbytes | 100 MHz |
| | R5F562N8ADFP | PLQP0100KB-A | 512 Kbytes | 96 Kbytes | 32 Kbytes | 100 MHz |
| | R5F562N7ADBG | PLBG0176GA-A | 384 Kbytes | 64 Kbytes | 32 Kbytes | 100 MHz |
| | R5F562N7ADLE | PTLG0145JB-A | 384 Kbytes | 64 Kbytes | 32 Kbytes | 100 MHz |
| | R5F562N7ADFB | PLQP0144KA-A | 384 Kbytes | 64 Kbytes | 32 Kbytes | 100 MHz |
| | R5F562N7ADFP | PLQP0100KB-A | 384 Kbytes | 64 Kbytes | 32 Kbytes | 100 MHz |
| RX621 | R5F56218BDBG | PLBG0176GA-A | 512 Kbytes | 96 Kbytes | 32 Kbytes | 100 MHz |
| | R5F56218BDLE | PTLG0145JB-A | 512 Kbytes | 96 Kbytes | 32 Kbytes | 100 MHz |
| | R5F56218BDFB | PLQP0144KA-A | 512 Kbytes | 96 Kbytes | 32 Kbytes | 100 MHz |
| | R5F56218BDFP | PLQP0100KB-A | 512 Kbytes | 96 Kbytes | 32 Kbytes | 100 MHz |
| | R5F56218BDLD | PTLG0085JA-A | 512 Kbytes | 96 Kbytes | 32 Kbytes | 100 MHz |
| | R5F56217BDBG | PLBG0176GA-A | 384 Kbytes | 64 Kbytes | 32 Kbytes | 100 MHz |
| | R5F56217BDLE | PTLG0145JB-A | 384 Kbytes | 64 Kbytes | 32 Kbytes | 100 MHz |
| | R5F56217BDFB | PLQP0144KA-A | 384 Kbytes | 64 Kbytes | 32 Kbytes | 100 MHz |
| | R5F56217BDFP | PLQP0100KB-A | 384 Kbytes | 64 Kbytes | 32 Kbytes | 100 MHz |
| | R5F56217BDLD | PTLG0085JA-A | 384 Kbytes | 64 Kbytes | 32 Kbytes | 100 MHz |
| | R5F56216BDBG | PLBG0176GA-A | 256 Kbytes | 64 Kbytes | 32 Kbytes | 100 MHz |
| | R5F56216BDLE | PTLG0145JB-A | 256 Kbytes | 64 Kbytes | 32 Kbytes | 100 MHz |
| | R5F56216BDFB | PLQP0144KA-A | 256 Kbytes | 64 Kbytes | 32 Kbytes | 100 MHz |
| | R5F56216BDFP | PLQP0100KB-A | 256 Kbytes | 64 Kbytes | 32 Kbytes | 100 MHz |
| | R5F56216BDLD | PTLG0085JA-A | 256 Kbytes | 64 Kbytes | 32 Kbytes | 100 MHz |

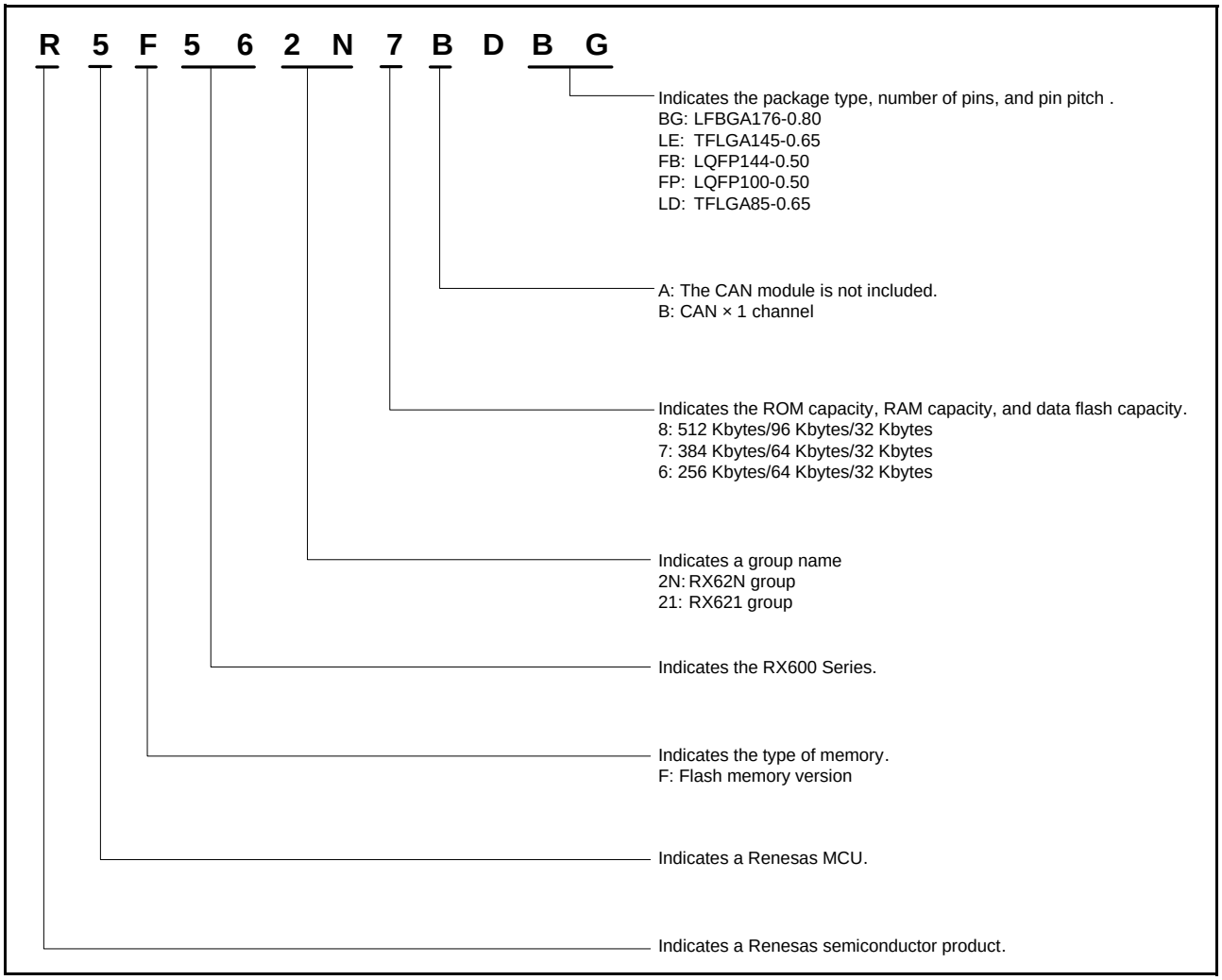
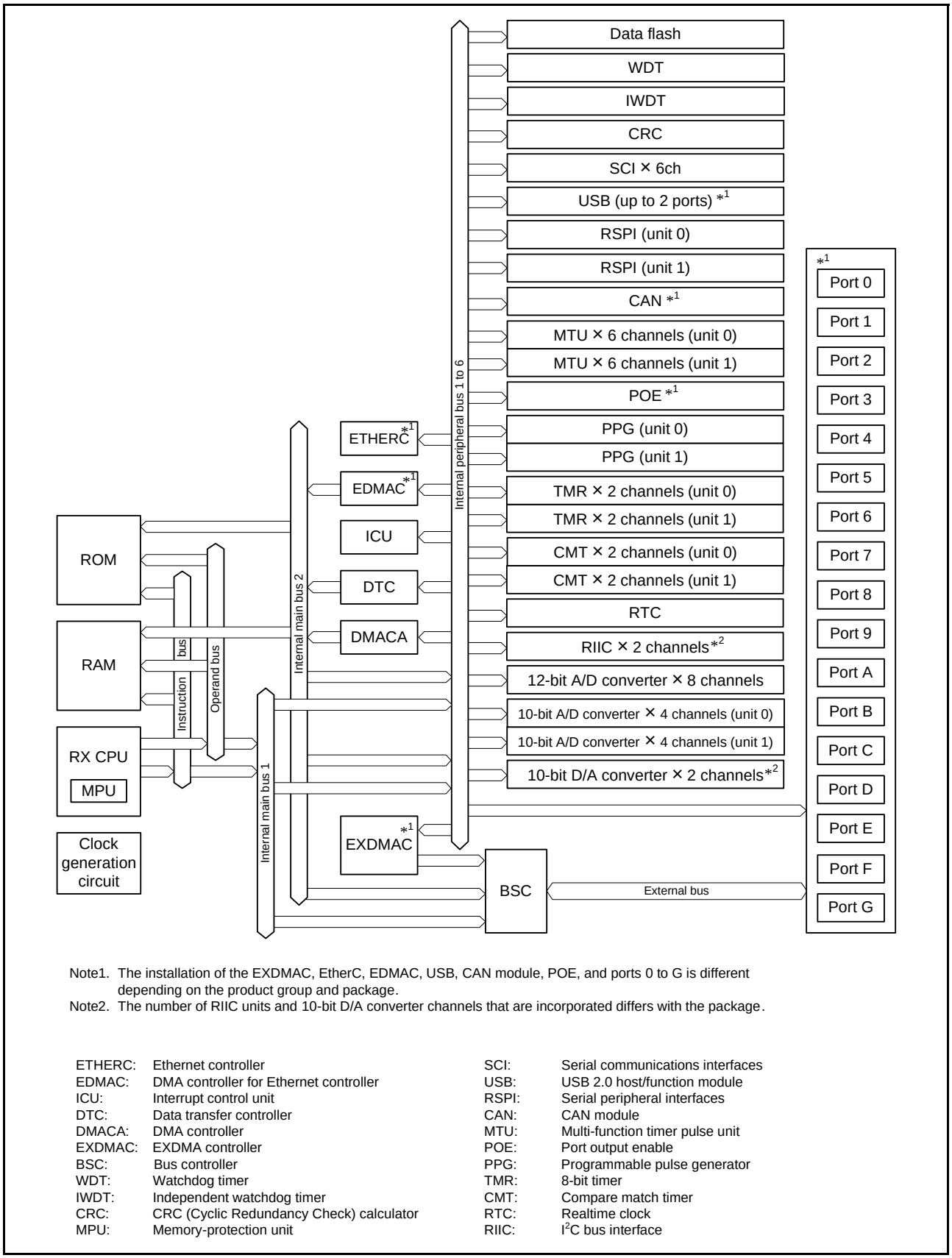



**Figure 1.1 How to Read the Product Part No.**

## 1.3 Block Diagram

Figure 1.2 shows a block diagram.




Note1. The installation of the EXDMAC, EtherC, EDMAC, USB, CAN module, POE, and ports 0 to G is different depending on the product group and package.
Note2. The number of RIIC units and 10-bit D/A converter channels that are incorporated differs with the package.

| | | | |
|---|---|---|---|
| ETHERC: | Ethernet controller | SCI: | Serial communications interfaces |
| EDMAC: | DMA controller for Ethernet controller | USB: | USB 2.0 host/function module |
| ICU: | Interrupt control unit | RSPI: | Serial peripheral interfaces |
| DTC: | Data transfer controller | CAN: | CAN module |
| DMACA: | DMA controller | MTU: | Multi-function timer pulse unit |
| EXDMAC: | EXDMA controller | POE: | Port output enable |
| BSC: | Bus controller | PPG: | Programmable pulse generator |
| WDT: | Watchdog timer | TMR: | 8-bit timer |
| IWDT: | Independent watchdog timer | CMT: | Compare match timer |
| CRC: | CRC (Cyclic Redundancy Check) calculator | RTC: | Realtime clock |
| MPU: | Memory-protection unit | RIIC: | $I^2C$ bus interface |

**Figure 1.2 Block Diagram**

## 1.4 Pin Assignments

Figure 1.3 to Figure 1.9 show the pins assignments. Table 1.4 to Table 1.8 show the list of pins and pin functions.

| | A | B | C | D | E | F | G | H | J | K | L | M | N | P | R | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 15 | PE1 | P70 | PE6 | P65 | P67 | PG5 | PA1 | PA3 | PA6 | PB0 | VCC | PB2 | PB5 | PB7 | P75 | 15 |
| 14 | P63 | PE2 | PE5 | PE7 | P66 | PA0 | PG6 | PA4 | PA7 | P72 | PB3 | PB6 | P73 | PC1 | P77 | 14 |
| 13 | P61 | P64 | PE3 | PE4 | VCC | PG3 | VCC | PA2 | PA5 | P71 | PB4 | VCC | P74 | P76 | P80 | 13 |
| 12 | PD7 | P62 | PE0 | VSS | PG2 | PG4 | VSS | PG7 | VSS | PB1 | VSS | PC0 | PC2 | PC4 | PC7 | 12 |
| 11 | PG0 | P60 | VCC | VSS | | | | | | | | P81 | PC3 | P82 | P83 | 11 |
| 10 | PD4 | PD6 | PD5 | PG1 | | | | | | | | PC6 | PC5 | P50 | P53 | 10 |
| 9 | PD3 | P97 | VCC | VSS | | | | | | | | VSS | VCC | P84 | P85 | 9 |
| 8 | PD2 | P96 | P94 | P95 | | | | | | | | P51 | P52 | VCC_ USB | USB1_ DP | 8 |
| 7 | PD0 | PD1 | P92 | P93 | | | | | | | | P54 | P10 | P56 | USB1_ DM | 7 |
| 6 | P90 | P91 | VCC | VSS | | | | | | | | P55 | P57 | VCC_ USB | VSS_ USB | 6 |
| 5 | P46 | P47 | P40 | P43 | | | | | | | | P11 | P15 | P13 | USB0_ DP | 5 |
| 4 | P45 | P44 | P07 | P41 | VSS | VSS | MDE | RES# | P34 | PF4 | P30 | VSS | P17 | P14 | USB0_ DM | 4 |
| 3 | P42 | VREFL | P05 | VCC | BSCANP | VCL | MD0 | VCC | PF3 | PF0 | VCC | P22 | P20 | P16 | P12 | 3 |
| 2 | AVCC | VREFH | P03 | P01 | CNVSS | WDTOVF# | MD1 | P35 | P32 | P31 | P27 | P25 | P23 | PLLVCC | PLLVSS | 2 |
| 1 | AVSS | P02 | P00 | EMLE | XCIN | XCOUT | VSS | XTAL | EXTAL | P33 | PF2 | PF1 | P26 | P24 | P21 | 1 |
| | A | B | C | D | E | F | G | H | J | K | L | M | N | P | R | |

RX62N Group
RX621 Group
PLBG0176GA-A
(176-pin LFBGA)
(Upper perspective view)

: NC pin

**Figure 1.3 Pin Assignment of the 176-Pin LFBGA**

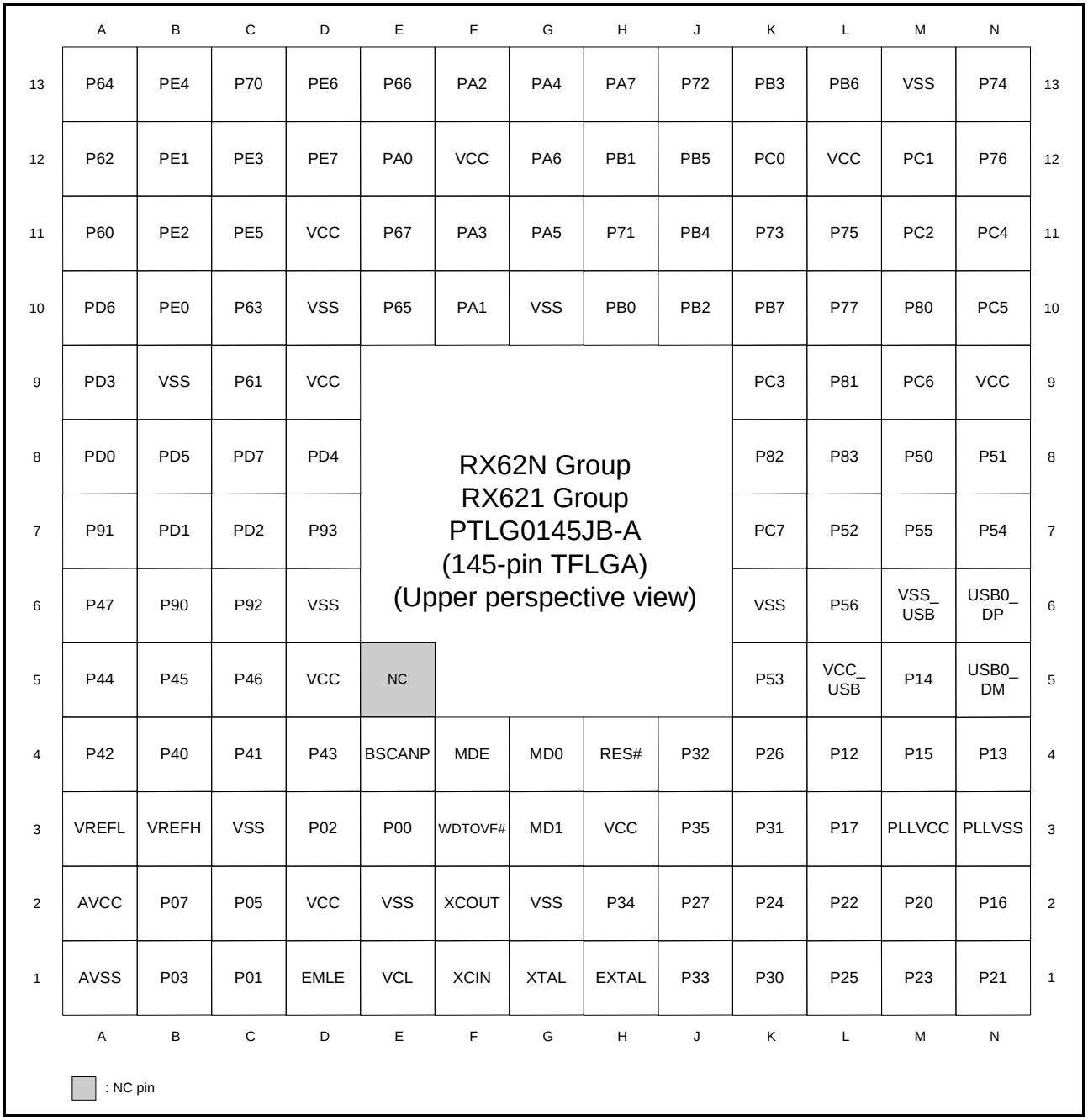



**Figure 1.4 Pin Assignment of the 145-Pin TFLGA**

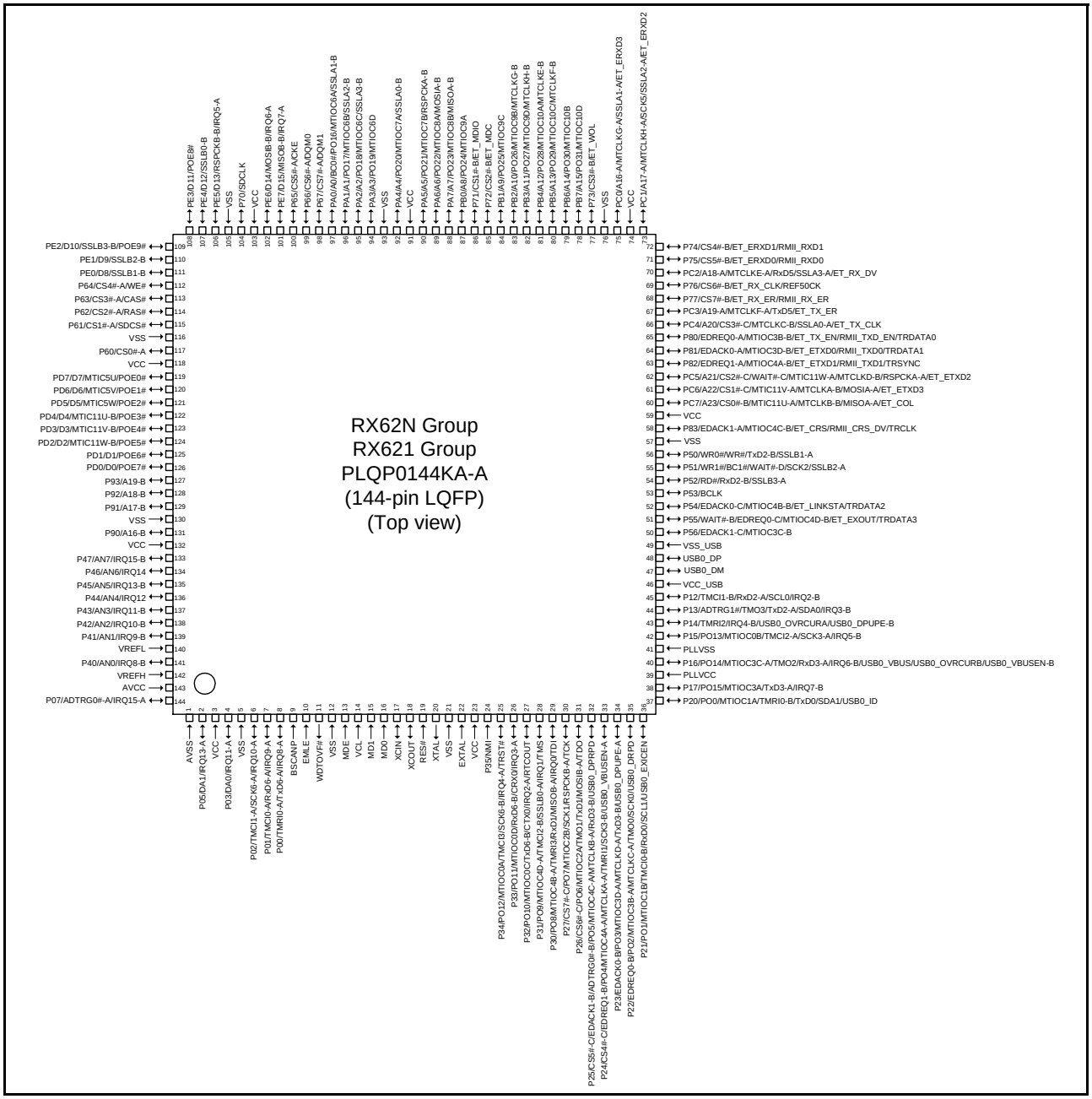



**Figure 1.5 Pin Assignment of the 144-Pin LQFP**

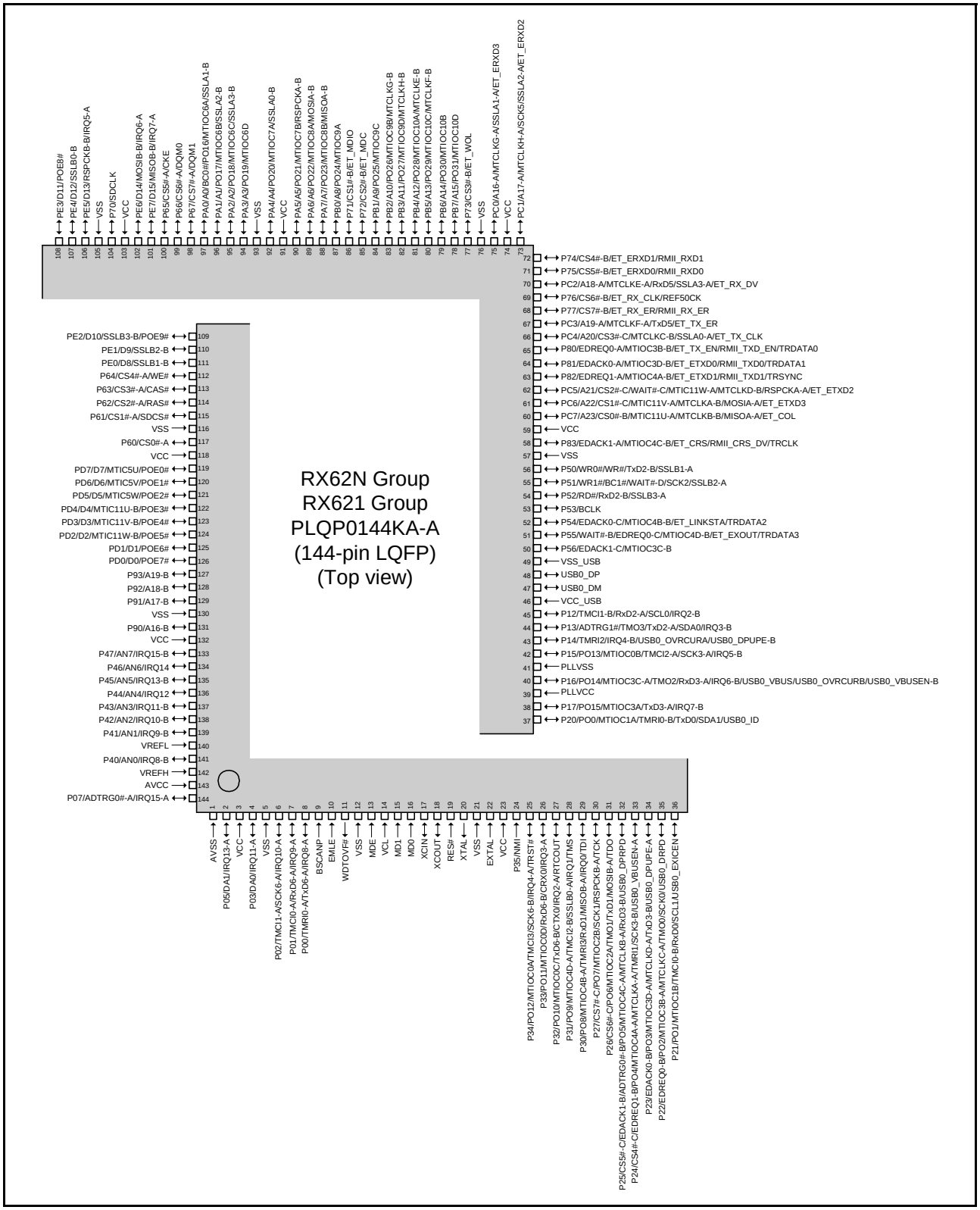



**Figure 1.6 Pin Assignment of the 144-Pin LQFP (Assistance Diagram)**

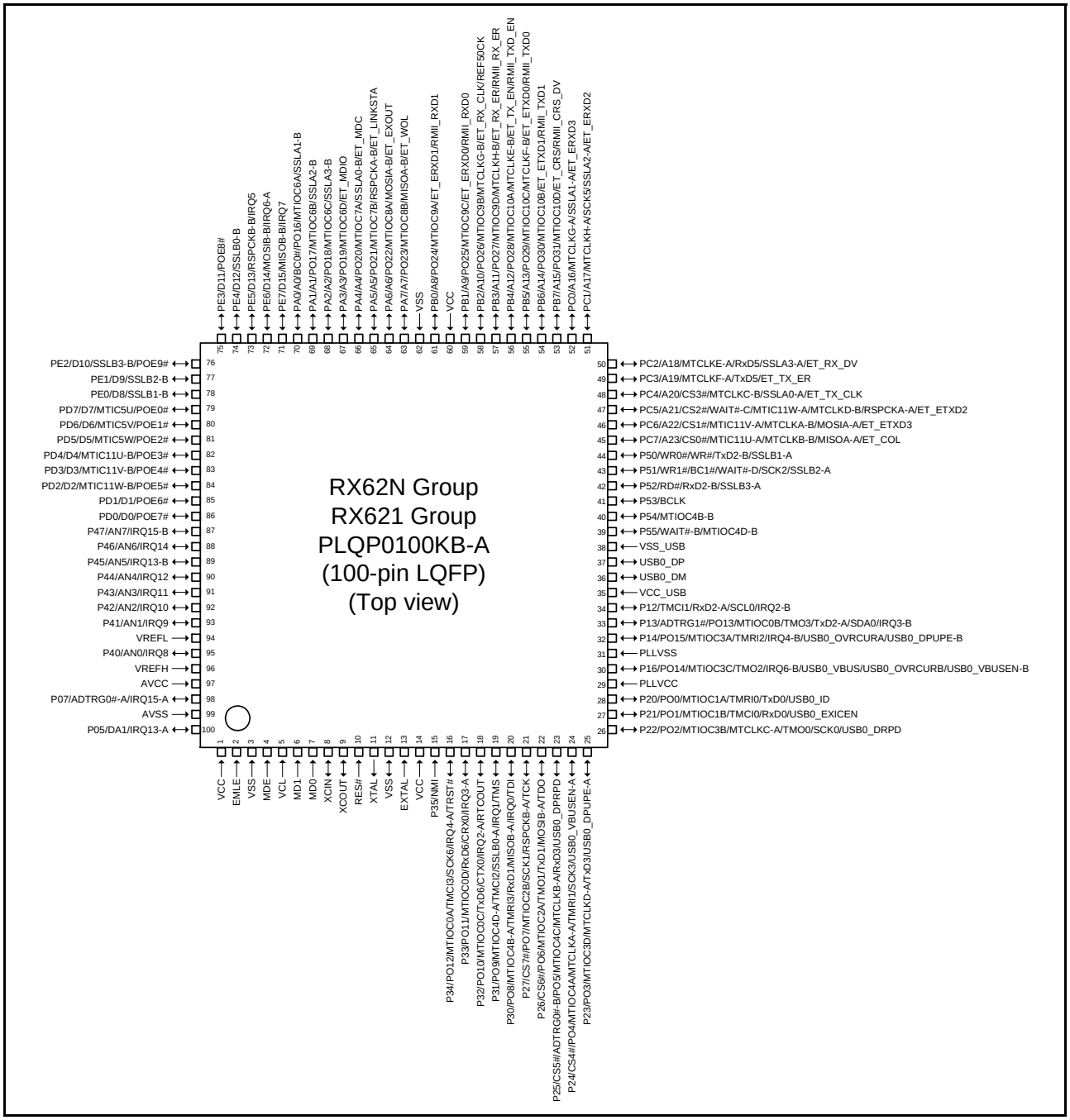



**Figure 1.7 Pin Assignment of the 100-Pin LQFP**

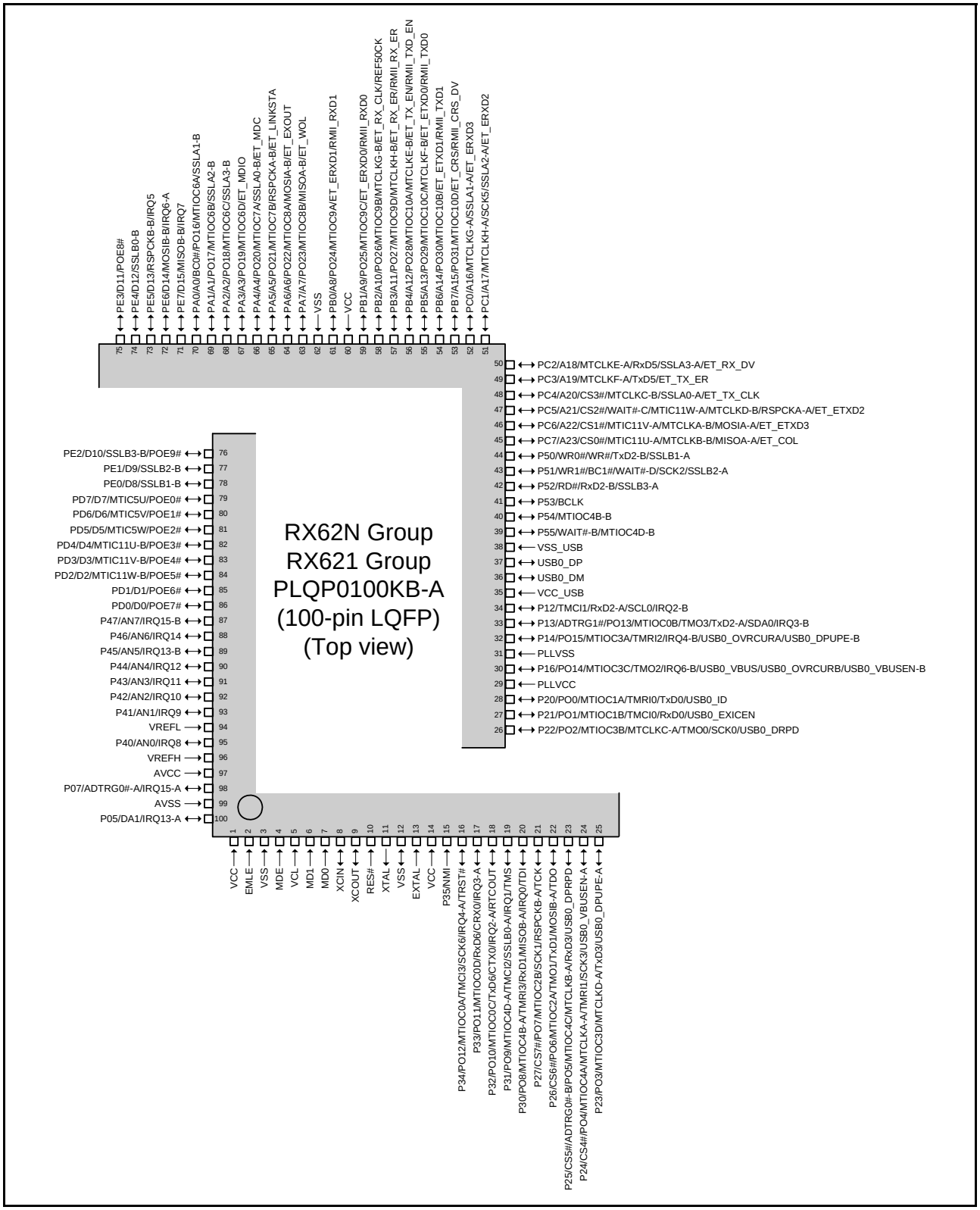



**Figure 1.8 Pin Assignment of the 100-Pin LQFP (Assistance Diagram)**

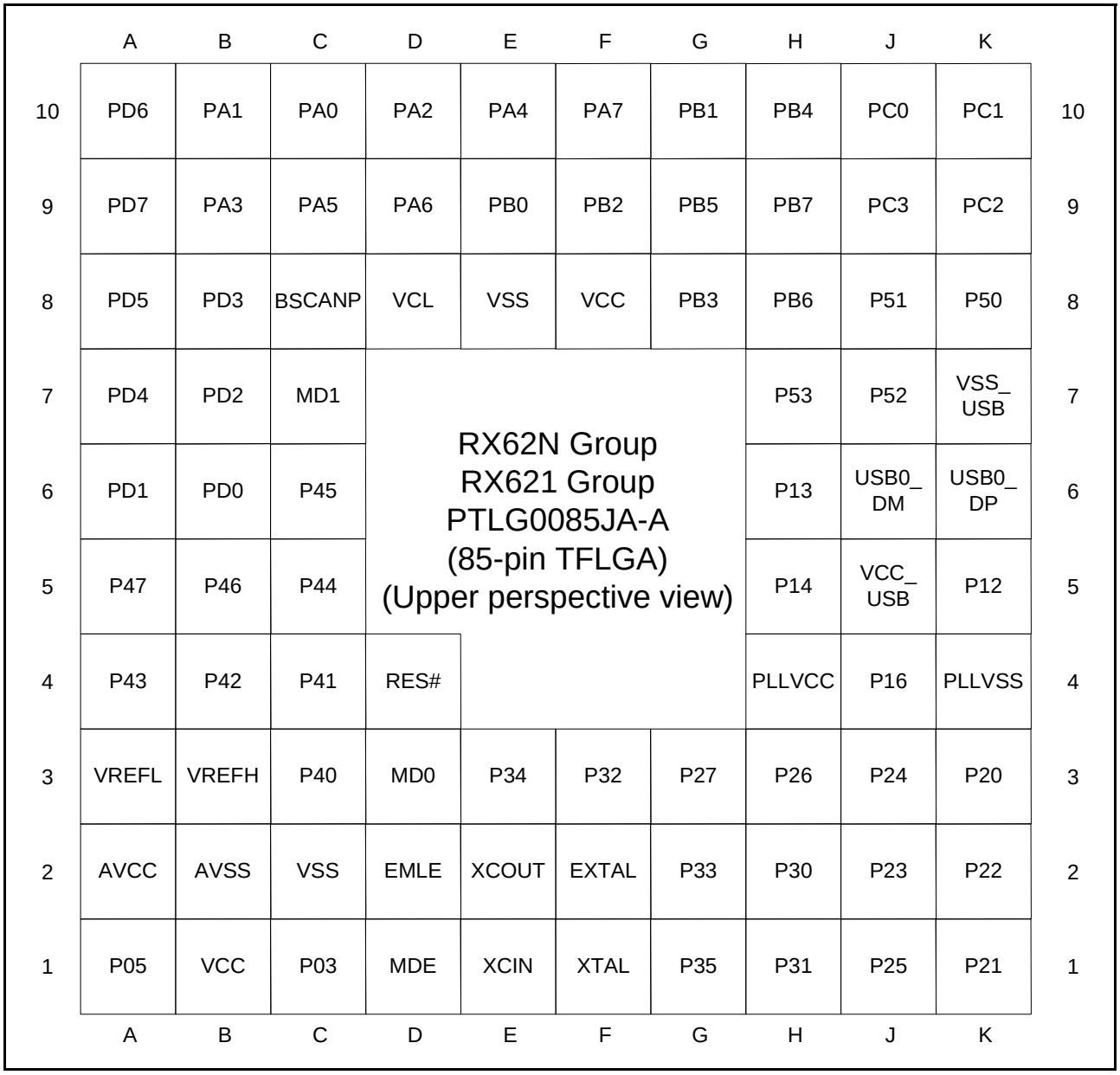



**Figure 1.9 Pin Assignment of the 85-Pin TFLGA**

**Table 1.4 List of Pins and Pin Functions (176-Pin LFBGA) (1 / 6)**

| Pin No. 176-Pin LFBGA | Power Supply Clock System Control | I/O Port | External Bus EXDMAC | ETHERC EDMAC | USB | Timers (MTU, TMR, PPG, POE, WDT) | Communi-cation (SCI, CAN, RSPI, RIIC) | Others |
|---|---|---|---|---|---|---|---|---|
| A1 | AVSS | | | | | | | |
| A2 | AVCC | | | | | | | |
| A3 | | P42 | | | | | | IRQ10-B/AN2 |
| A4 | | P45 | | | | | | IRQ13-B/AN5 |
| A5 | | P46 | | | | | | IRQ14/AN6 |
| A6 | | P90 | D16/A16-B | | | | | |
| A7 | | PD0 | D0 | | | POE7# | | |
| A8 | | PD2 | D2 | | | MTIC11W-B/ POE5# | | |
| A9 | | PD3 | D3 | | | MTIC11V-B/ POE4# | | |
| A10 | | PD4 | D4 | | | MTIC11U-B/ POE3# | | |
| A11 | | PG0 | D24 | | | | | |
| A12 | | PD7 | D7 | | | MTIC5U-B/ POE0# | | |
| A13 | | P61 | CS1#-A/ SDCS# | | | | | |
| A14 | | P63 | CS3#-A/ CAS# | | | | | |
| A15 | | PE1 | D9 | | | | SSLB2-B | |
| B1 | | P02 | | | | TMCI1-A | SCK6-A | IRQ10-A |
| B2 | VREFH | | | | | | | |
| B3 | VREFL | | | | | | | |
| B4 | | P44 | | | | | | IRQ12/AN4 |
| B5 | | P47 | | | | | | IRQ15-B/AN7 |
| B6 | | P91 | D17/A17-B | | | | | |
| B7 | | PD1 | D1 | | | POE6# | | |
| B8 | | P96 | D22/A22-B | | | | | |
| B9 | | P97 | D23/A23-B | | | | | |
| B10 | | PD6 | D6 | | | MTIC5V-B/ POE1# | | |
| B11 | | P60 | CS0#-A | | | | | |
| B12 | | P62 | CS2#-A/ RAS# | | | | | |
| B13 | | P64 | CS4#-A/ WE# | | | | | |
| B14 | | PE2 | D10 | | | POE9# | SSLB3-B | |
| B15 | SDCLK | P70 | | | | | | |
| C1 | | P00 | | | | TMRI0-A | TxD6-A | IRQ8-A |
| C2 | | P03 | | | | | | IRQ11-A/DA0 |
| C3 | | P05 | | | | | | IRQ13-A/DA1 |
| C4 | | P07 | | | | | | IRQ15-A/ ADTRG0#-A |
| C5 | | P40 | | | | | | IRQ8-B/AN0 |

**Table 1.4 List of Pins and Pin Functions (176-Pin LFBGA) (2 / 6)**

| Pin No. 176-Pin LFBGA | Power Supply Clock System Control | I/O Port | External Bus EXDMAC | ETHERC EDMAC | USB | Timers (MTU, TMR, PPG, POE, WDT) | Communi-cation (SCI, CAN, RSPI, RIIC) | Others |
|---|---|---|---|---|---|---|---|---|
| C6 | VCC | | | | | | | |
| C7 | | P92 | D18/A18-B | | | | | |
| C8 | | P94 | D20/A20-B | | | | | |
| C9 | VCC | | | | | | | |
| C10 | | PD5 | D5 | | | MTIC5W-B/ POE2# | | |
| C11 | VCC | | | | | | | |
| C12 | | PE0 | D8 | | | | SSLB1-B | |
| C13 | | PE3 | D11 | | | POE8# | | |
| C14 | | PE5 | D13 | | | | RSPCKB-B | IRQ5-A |
| C15 | | PE6 | D14 | | | | MOSIB-B | IRQ6-A |
| D1 | EMLE | | | | | | | |
| D2 | | P01 | | | | TMCI0-A | RxD6-A | IRQ9-A |
| D3 | VCC | | | | | | | |
| D4 | | P41 | | | | | | IRQ9-B/AN1 |
| D5 | | P43 | | | | | | IRQ11-B/AN3 |
| D6 | VSS | | | | | | | |
| D7 | | P93 | D19/A19-B | | | | | |
| D8 | | P95 | D21/A21-B | | | | | |
| D9 | VSS | | | | | | | |
| D10 | | PG1 | D25 | | | | | |
| D11 | VSS | | | | | | | |
| D12 | VSS | | | | | | | |
| D13 | | PE4 | D12 | | | | SSLB0-B | |
| D14 | | PE7 | D15 | | | | MISOB-B | IRQ7-A |
| D15 | | P65 | CS5#-A/ CKE | | | | | |
| E1 | XCIN | | | | | | | |
| E2 | CNVSS | | | | | | | |
| E3 | BSCANP | | | | | | | |
| E4 | VSS | | | | | | | |
| E12 | | PG2 | D26 | | | | | TRDATA0 |
| E13 | VCC | | | | | | | |
| E14 | | P66 | CS6#-A/ DQM0 | | | | | |
| E15 | | P67 | CS7#-A/ DQM1 | | | | | |
| F1 | XCOUT | | | | | | | |
| F2 | | | | | | WDTOVF# | | |
| F3 | VCL | | | | | | | |
| F4 | VSS | | | | | | | |
| F12 | | PG4 | D28 | | | | | TRSYNC |
| F13 | | PG3 | D27 | | | | | TRDATA1 |
| F14 | | PA0 | A0/BC0#/ DQM2 | | | MTIOC6A/ PO16 | SSLA1-B | |

**Table 1.4 List of Pins and Pin Functions (176-Pin LFBGA) (3 / 6)**

| Pin No. 176-Pin LFBGA | Power Supply Clock System Control | I/O Port | External Bus EXDMAC | ETHERC EDMAC | USB | Timers (MTU, TMR, PPG, POE, WDT) | Communi-cation (SCI, CAN, RSPI, RIIC) | Others |
|---|---|---|---|---|---|---|---|---|
| F15 | | PG5 | D29 | | | | | TRCLK |
| G1 | VSS | | | | | | | |
| G2 | MD1 | | | | | | | |
| G3 | MD0 | | | | | | | |
| G4 | MDE | | | | | | | |
| G12 | VSS | | | | | | | |
| G13 | VCC | | | | | | | |
| G14 | | PG6 | D30 | | | | | TRDATA2 |
| G15 | | PA1 | A1/DQM3 | | | MTIOC6B/ PO17 | SSLA2-B | |
| H1 | XTAL | | | | | | | |
| H2 | | P35 | | | | | | NMI |
| H3 | VCC | | | | | | | |
| H4 | RES# | | | | | | | |
| H12 | | PG7 | D31 | | | | | TRDATA3 |
| H13 | | PA2 | A2 | | | MTIOC6C/ PO18 | SSLA3-B | |
| H14 | | PA4 | A4 | | | MTIOC7A/ PO20 | SSLA0-B | |
| H15 | | PA3 | A3 | | | MTIOC6D/ PO19 | | |
| J1 | EXTAL | | | | | | | |
| J2 | | P32 | | | | MTIOC0C/ PO10/ RTCOUT | CTX0/ TxD6-B | IRQ2-A |
| J3 | | PF3 | | | | | | TMS |
| J4 | | P34 | | | | MTIOC0A/ TMCI3-B/ PO12 | SCK6-B | IRQ4-A |
| J12 | VSS | | | | | | | |
| J13 | | PA5 | A5 | | | MTIOC7B/ PO21 | RSPCKA-B | |
| J14 | | PA7 | A7 | | | MTIOC8B/ PO23 | MISOA-B | |
| J15 | | PA6 | A6 | | | MTIOC8A/ PO22 | MOSIA-B | |
| K1 | | P33 | | | | MTIOC0D/ PO11 | CRX0/ RxD6-B | IRQ3-A |
| K2 | | P31 | | | USB1_DPRPD | MTIOC4D-A/ TMCI2-B/ PO9 | SSLB0-A | IRQ1-A |
| K3 | | PF0 | | | | | TxD1-B | TDO |
| K4 | | PF4 | | | | | | TRST# |
| K12 | | PB1 | A9 | | | MTIOC9C/ PO25 | | |
| K13 | | P71 | CS1#-B | ET_MDIO | | | | |
| K14 | | P72 | CS2#-B | ET_MDC | | | | |

**Table 1.4 List of Pins and Pin Functions (176-Pin LFBGA) (4 / 6)**

| Pin No. 176-Pin LFBGA | Power Supply Clock System Control | I/O Port | External Bus EXDMAC | ETHERC EDMAC | USB | Timers (MTU, TMR, PPG, POE, WDT) | Communi-cation (SCI, CAN, RSPI, RIIC) | Others |
|---|---|---|---|---|---|---|---|---|
| K15 | | PB0 | A8 | | | MTIOC9A/ PO24 | | |
| L1 | | PF2 | | | | | RxD1-B | TDI |
| L2 | | P27 | CS7#-C | | USB1_EXICEN | MTIOC2B/ PO7 | RSPCKB-A/ SCK1-A | |
| L3 | VCC | | | | | | | |
| L4 | | P30 | | | USB1_DRPD | MTIOC4B-A/ TMRI3-B/ PO8 | MISOB-A/ RxD1-A | IRQ0-A |
| L12 | VSS | | | | | | | |
| L13 | | PB4 | A12 | | | MTIOC10A/ MTCLKE-B/ PO28 | | |
| L14 | | PB3 | A11 | | | MTIOC9D/ MTCLKH-B/ PO27 | | |
| L15 | VCC | | | | | | | |
| M1 | | PF1 | | | | | SCK1-B | TCK |
| M2 | | P25 | CS5#-C/ EDACK1-B | | USB0_DPRPD | MTIOC4C-A/ MTCLKB-A/ PO5 | RxD3-B | ADTRG0#-B |
| M3 | | P22 | EDREQ0-B | | USB0_DRPD | MTIOC3B-A/ MTCLKC-A/ TMO0/ PO2 | SCK0 | |
| M4 | VSS | | | | | | | |
| M5 | | P11 | | | USB1_VBUSEN-A | MTIC5V-A/ TMCI3-A | SCK2-A | IRQ1-B |
| M6 | | P55 | WAIT#-B/ EDREQ0-C | ET_EXOUT | | MTIOC4D-B | | |
| M7 | | P54 | EDACK0-C | ET_LINKSTA | | MTIOC4B-B | | |
| M8 | | P51 | WR1#/ BC1#/ WAIT#-D | | | | SSLB2-A/ SCK2-B | |
| M9 | VSS | | | | | | | |
| M10 | | PC6 | A22-A/ CS1#-C | ET_ETXD3 | | MTIC11V-A/ MTCLKA-B | MOSIA-A | |
| M11 | | P81 | EDACK0-A | ET_ETXD0/ RMII_TXD0 | | MTIOC3D-B | | |
| M12 | | PC0 | A16-A | ET_ERXD3 | | MTCLKG-A | SSLA1-A | |
| M13 | VCC | | | | | | | |
| M14 | | PB6 | A14 | | | MTIOC10B/ PO30 | | |
| M15 | | PB2 | A10 | | | MTIOC9B/ MTCLKG-B/ PO26 | | |
| N1 | | P26 | CS6#-C | | USB1_ID | MTIOC2A/ TMO1/ PO6 | MOSIB-A/ TxD1-A | |

**Table 1.4 List of Pins and Pin Functions (176-Pin LFBGA) (5 / 6)**

| Pin No. 176-Pin LFBGA | Power Supply Clock System Control | I/O Port | External Bus EXDMAC | ETHERC EDMAC | USB | Timers (MTU, TMR, PPG, POE, WDT) | Communi-cation (SCI, CAN, RSPI, RIIC) | Others |
|---|---|---|---|---|---|---|---|---|
| N2 | | P23 | EDACK0-B | | USB0_DPUPE-A | MTIOC3D-A/ MTCLKD-A/ PO3 | TxD3-B | |
| N3 | | P20 | | | USB0_ID | MTIOC1A/ TMRI0-B/ PO0 | SDA1/ TxD0 | |
| N4 | | P17 | | | USB1_VBUS/ USB1_OVRCURB/ USB1_VBUSEN-B | MTIOC3A/ PO15 | TxD3-A | IRQ7-B |
| N5 | | P15 | | | USB1_OVRCURA/ USB1_DPUPE-B | MTIOC0B/ TMCI2-A/ PO13 | SCK3-A | IRQ5-B |
| N6 | | P57 | WAIT#-A/ WR3#/ BC3#/ EDREQ1-C | | | | | |
| N7 | | P10 | | | USB1_DPUPE-A | MTIC5W-A/ TMRI3-A | | IRQ0-B |
| N8 | | P52 | RD# | | | | SSLB3-A/ RxD2-B | |
| N9 | VCC | | | | | | | |
| N10 | | PC5 | A21-A/ CS2#-C/ WAIT#-C | ET_ETXD2 | | MTIC11W-A/ MTCLKD-B | RSPCKA-A | |
| N11 | | PC3 | A19-A | ET_TX_ER | | MTCLKF-A | TxD5 | |
| N12 | | PC2 | A18-A | ET_RX_DV | | MTCLKE-A | SSLA3-A/ RxD5 | |
| N13 | | P74 | CS4#-B | ET_ERXD1/ RMII_RXD1 | | | | |
| N14 | | P73 | CS3#-B | ET_WOL | | | | |
| N15 | | PB5 | A13 | | | MTIOC10C/ MTCLKF-B/ PO29 | | |
| P1 | | P24 | CS4#-C/ EDREQ1-B | | USB0_VBUSEN-A | MTIOC4A-A/ MTCLKA-A/ TMRI1/ PO4 | SCK3-B | |
| P2 | PLLVCC | | | | | | | |
| P3 | | P16 | | | USB0_VBUS/ USB0_OVRCURB/ USB0_VBUSEN-B | MTIOC3C-A/ TMO2/ PO14 | RxD3-A | IRQ6-B |
| P4 | | P14 | | | USB0_OVRCURA/ USB0_DPUPE-B | TMRI2 | | IRQ4-B |
| P5 | | P13 | | | | TMO3 | SDA0/ TxD2-A | IRQ3-B/ ADTRG1# |
| P6 | VCC_USB | | | | | | | |

**Table 1.4 List of Pins and Pin Functions (176-Pin LFBGA) (6 / 6)**

| Pin No. 176-Pin LFBGA | Power Supply Clock System Control | I/O Port | External Bus EXDMAC | ETHERC EDMAC | USB | Timers (MTU, TMR, PPG, POE, WDT) | Communi-cation (SCI, CAN, RSPI, RIIC) | Others |
|---|---|---|---|---|---|---|---|---|
| P7 | | P56 | WR2#/ BC2#/ EDACK1-C | | | MTIOC3C-B | | |
| P8 | VCC_USB | | | | | | | |
| P9 | | P84 | | | | | | |
| P10 | | P50 | WR0#/ WR# | | | | SSLB1-A/ TxD2-B | |
| P11 | | P82 | EDREQ1-A | ET_ETXD1/ RMII_TXD1 | | MTIOC4A-B | | |
| P12 | | PC4 | A20-A/ CS3#-C | ET_TX_CLK | | MTCLKC-B | SSLA0-A | |
| P13 | | P76 | CS6#-B | ET_RX_CLK/ REF50CK | | | | |
| P14 | | PC1 | A17-A | ET_ERXD2 | | MTCLKH-A | SSLA2-A/ SCK5 | |
| P15 | | PB7 | A15 | | | MTIOC10D/ PO31 | | |
| R1 | | P21 | | | USB0_EXICEN | MTIOC1B/ TMCI0-B/ PO1 | SCL1/ RxD0 | |
| R2 | PLLVSS | | | | | | | |
| R3 | | P12 | | | | MTIC5U-A/ TMCI1-B | SCL0/ RxD2-A | IRQ2-B |
| R4 | | | | | USB0_DM | | | |
| R5 | | | | | USB0_DP | | | |
| R6 | VSS_USB | | | | | | | |
| R7 | | | | | USB1_DM | | | |
| R8 | | | | | USB1_DP | | | |
| R9 | | P85 | | | | | | |
| R10 | BCLK | P53 | | | | | | |
| R11 | | P83 | EDACK1-A | ET_CRS/ RMII_CRS_DV | | MTIOC4C-B | | |
| R12 | | PC7 | A23-A/ CS0#-B | ET_COL | | MTIC11U-A/ MTCLKB-B | MISOA-A | |
| R13 | | P80 | EDREQ0-A | ET_TX_EN/ RMII_TXD_EN | | MTIOC3B-B | | |
| R14 | | P77 | CS7#-B | ET_RX_ER/ RMII_RX_ER | | | | |
| R15 | | P75 | CS5#-B | ET_ERXD0/ RMII_RXD0 | | | | |

**Table 1.5 List of Pins and Pin Functions (145-Pin TFLGA) (1 / 5)**

| Pin No. 145-Pin TFLGA | Power Supply Clock System Control | I/O Port | External Bus EXDMAC | ETHERC EDMAC | USB | Timers (MTU, TMR, PPG, POE, WDT) | Communi-cation (SCI, CAN, RSPI, RIIC) | Others |
|---|---|---|---|---|---|---|---|---|
| A1 | AVSS | | | | | | | |
| A2 | AVCC | | | | | | | |
| A3 | VREFL | | | | | | | |
| A4 | | P42 | | | | | | IRQ10-B/AN2 |
| A5 | | P44 | | | | | | IRQ12/AN4 |
| A6 | | P47 | | | | | | IRQ15-B/AN7 |
| A7 | | P91 | A17-B | | | | | |
| A8 | | PD0 | D0 | | | POE7# | | |
| A9 | | PD3 | D3 | | | MTIC11V-B/ POE4# | | |
| A10 | | PD6 | D6 | | | MTIC5V/ POE1# | | |
| A11 | | P60 | CS0#-A | | | | | |
| A12 | | P62 | CS2#-A/ RAS# | | | | | |
| A13 | | P64 | CS4#-A/ WE# | | | | | |
| B1 | | P03 | | | | | | IRQ11-A/DA0 |
| B2 | | P07 | | | | | | IRQ15-A/ ADTRG0#-A |
| B3 | VREFH | | | | | | | |
| B4 | | P40 | | | | | | IRQ8-B/AN0 |
| B5 | | P45 | | | | | | IRQ13-B/AN5 |
| B6 | | P90 | A16-B | | | | | |
| B7 | | PD1 | D1 | | | POE6# | | |
| B8 | | PD5 | D5 | | | MTIC5W/ POE2# | | |
| B9 | VSS | | | | | | | |
| B10 | | PE0 | D8 | | | | SSLB1-B | |
| B11 | | PE2 | D10 | | | POE9# | SSLB3-B | |
| B12 | | PE1 | D9 | | | | SSLB2-B | |
| B13 | | PE4 | D12 | | | | SSLB0-B | |
| C1 | | P01 | | | | TMCI0-A | RxD6-A | IRQ9-A |
| C2 | | P05 | | | | | | IRQ13-A/DA1 |
| C3 | VSS | | | | | | | |
| C4 | | P41 | | | | | | IRQ9-B/AN1 |
| C5 | | P46 | | | | | | IRQ14/AN6 |
| C6 | | P92 | A18-B | | | | | |
| C7 | | PD2 | D2 | | | MTIC11W-B/ POE5# | | |
| C8 | | PD7 | D7 | | | MTIC5U/ POE0# | | |
| C9 | | P61 | CS1#-A/ SDCS# | | | | | |

**Table 1.5 List of Pins and Pin Functions (145-Pin TFLGA) (2 / 5)**

| Pin No. 145-Pin TFLGA | Power Supply Clock System Control | I/O Port | External Bus EXDMAC | ETHERC EDMAC | USB | Timers (MTU, TMR, PPG, POE, WDT) | Communi-cation (SCI, CAN, RSPI, RIIC) | Others |
|---|---|---|---|---|---|---|---|---|
| C10 | | P63 | CS3#-A/ CAS# | | | | | |
| C11 | | PE5 | D13 | | | | RSPCKB-B | IRQ5-A |
| C12 | | PE3 | D11 | | | POE8# | | |
| C13 | SDCLK | P70 | | | | | | |
| D1 | EMLE | | | | | | | |
| D2 | VCC | | | | | | | |
| D3 | | P02 | | | | TMCI1-A | SCK6-A | IRQ10-A |
| D4 | | P43 | | | | | | IRQ11-B/AN3 |
| D5 | VCC | | | | | | | |
| D6 | VSS | | | | | | | |
| D7 | | P93 | A19-B | | | | | |
| D8 | | PD4 | D4 | | | MTIC11U-B/ POE3# | | |
| D9 | VCC | | | | | | | |
| D10 | VSS | | | | | | | |
| D11 | VCC | | | | | | | |
| D12 | | PE7 | D15 | | | | MISOB-B | IRQ7-A |
| D13 | | PE6 | D14 | | | | MOSIB-B | IRQ6-A |
| E1 | VCL | | | | | | | |
| E2 | VSS | | | | | | | |
| E3 | | P00 | | | | TMRI0-A | TxD6-A | IRQ8-A |
| E4 | BSCANP | | | | | | | |
| E5 | (N.C) | | | | | | | |
| E10 | | P65 | CS5#-A/ CKE | | | | | |
| E11 | | P67 | CS7#-A/ DQM1 | | | | | |
| E12 | | PA0 | A0/BC0# | | | MTIOC6A/ PO16 | SSLA1-B | |
| E13 | | P66 | CS6#-A/ DQM0 | | | | | |
| F1 | XCIN | | | | | | | |
| F2 | XCOUT | | | | | | | |
| F3 | | | | | | WDTOVF# | | |
| F4 | MDE | | | | | | | |
| F10 | | PA1 | A1 | | | MTIOC6B/ PO17 | SSLA2-B | |
| F11 | | PA3 | A3 | | | MTIOC6D/ PO19 | | |
| F12 | VCC | | | | | | | |
| F13 | | PA2 | A2 | | | MTIOC6C/ PO18 | SSLA3-B | |
| G1 | XTAL | | | | | | | |
| G2 | VSS | | | | | | | |

**Table 1.5 List of Pins and Pin Functions (145-Pin TFLGA) (3 / 5)**

| Pin No. 145-Pin TFLGA | Power Supply Clock System Control | I/O Port | External Bus EXDMAC | ETHERC EDMAC | USB | Timers (MTU, TMR, PPG, POE, WDT) | Communi-cation (SCI, CAN, RSPI, RIIC) | Others |
|---|---|---|---|---|---|---|---|---|
| G3 | MD1 | | | | | | | |
| G4 | MD0 | | | | | | | |
| G10 | VSS | | | | | | | |
| G11 | | PA5 | A5 | | | MTIOC7B/ PO21 | RSPCKA-B | |
| G12 | | PA6 | A6 | | | MTIOC8A/ PO22 | MOSIA-B | |
| G13 | | PA4 | A4 | | | MTIOC7A/ PO20 | SSLA0-B | |
| H1 | EXTAL | | | | | | | |
| H2 | | P34 | | | | MTIOC0A/ TMCI3/ PO12 | SCK6-B | IRQ4-A/ TRST# |
| H3 | VCC | | | | | | | |
| H4 | RES# | | | | | | | |
| H10 | | PB0 | A8 | | | MTIOC9A/ PO24 | | |
| H11 | | P71 | CS1#-B | ET_MDIO | | | | |
| H12 | | PB1 | A9 | | | MTIOC9C/ PO25 | | |
| H13 | | PA7 | A7 | | | MTIOC8B/ PO23 | MISOA-B | |
| J1 | | P33 | | | | MTIOC0D/ PO11 | CRX0/ RxD6-B | IRQ3-A |
| J2 | | P27 | CS7#-C | | | MTIOC2B/ PO7 | RSPCKB-A/ SCK1 | TCK |
| J3 | | P35 | | | | | | NMI |
| J4 | | P32 | | | | MTIOC0C/ PO10/ RTCOUT | CTX0/ TxD6-B | IRQ2-A |
| J10 | | PB2 | A10 | | | MTIOC9B/ MTCLKG-B/ PO26 | | |
| J11 | | PB4 | A12 | | | MTIOC10A/ MTCLKE-B/ PO28 | | |
| J12 | | PB5 | A13 | | | MTIOC10C/ MTCLKF-B/ PO29 | | |
| J13 | | P72 | CS2#-B | ET_MDC | | | | |
| K1 | | P30 | | | | MTIOC4B-A/ TMRI3/ PO8 | RxD1/ MISOB-A | IRQ0/ TDI |
| K2 | | P24 | CS4#-C/ EDREQ1-B | | USB0_VBUSEN-A | MTIOC4A-A/ MTCLKA-A/ TMRI1/PO4 | SCK3-B | |
| K3 | | P31 | | | | MTIOC4D-A/ TMCI2-B/ PO9 | SSLB0-A | IRQ1/ TMS |

**Table 1.5 List of Pins and Pin Functions (145-Pin TFLGA) (4 / 5)**

| Pin No. 145-Pin TFLGA | Power Supply Clock System Control | I/O Port | External Bus EXDMAC | ETHERC EDMAC | USB | Timers (MTU, TMR, PPG, POE, WDT) | Communi-cation (SCI, CAN, RSPI, RIIC) | Others |
|---|---|---|---|---|---|---|---|---|
| K4 | | P26 | CS6#-C | | | MTIOC2A/ TMO1/ PO6 | MOSIB-A/ TxD1 | TDO |
| K5 | BCLK | P53 | | | | | | |
| K6 | VSS | | | | | | | |
| K7 | | PC7 | A23/ CS0#-B | ET_COL | | MTIC11U-A/ MTCLKB-B | MISOA-A | |
| K8 | | P82 | EDREQ1-A | ET_ETXD1/ RMII_TXD1 | | MTIOC4A-B | | TRSYNC |
| K9 | | PC3 | A19-A | ET_TX_ER | | MTCLKF-A | TxD5 | |
| K10 | | PB7 | A15 | | | MTIOC10D/ PO31 | | |
| K11 | | P73 | CS3#-B | ET_WOL | | | | |
| K12 | | PC0 | A16-A | ET_ERXD3 | | MTCLKG-A | SSLA1-A | |
| K13 | | PB3 | A11 | | | MTIOC9D/ MTCLKH-B/ PO27 | | |
| L1 | | P25 | CS5#-C/ EDACK1-B | | USB0_DPRPD | MTIOC4C-A/ MTCLKB-A/ PO5 | RxD3-B | ADTRG0#-B |
| L2 | | P22 | EDREQ0-B | | USB0_DRPD | MTIOC3B-A/ MTCLKC-A/ TMO0/PO2 | SCK0 | |
| L3 | | P17 | | | | MTIOC3A/ PO15 | TxD3-A | IRQ7-B |
| L4 | | P12 | | | | TMCI1-B | SCL0/ RxD2-A | IRQ2-B |
| L5 | VCC_USB | | | | | | | |
| L6 | | P56 | EDACK1-C | | | MTIOC3C-B | | |
| L7 | | P52 | RD# | | | | SSLB3-A/ RxD2-B | |
| L8 | | P83 | EDACK1-A | ET_CRS/ RMII_CRS_DV | | MTIOC4C-B | | TRCLK |
| L9 | | P81 | EDACK0-A | ET_ETXD0/ RMII_TXD0 | | MTIOC3D-B | | TRDATA1 |
| L10 | | P77 | CS7#-B | ET_RX_ER/ RMII_RX_ER | | | | |
| L11 | | P75 | CS5#-B | ET_ERXD0/ RMII_RXD0 | | | | |
| L12 | VCC | | | | | | | |
| L13 | | PB6 | A14 | | | MTIOC10B/ PO30 | | |
| M1 | | P23 | EDACK0-B | | USB0_DPUPE-A | MTIOC3D-A/ MTCLKD-A/ PO3 | TxD3-B | |
| M2 | | P20 | | | USB0_ID | MTIOC1A/ TMRI0-B/ PO0 | SDA1/ TxD0 | |
| M3 | PLLVCC | | | | | | | |

**Table 1.5 List of Pins and Pin Functions (145-Pin TFLGA) (5 / 5)**

| Pin No. 145-Pin TFLGA | Power Supply Clock System Control | I/O Port | External Bus EXDMAC | ETHERC EDMAC | USB | Timers (MTU, TMR, PPG, POE, WDT) | Communi-cation (SCI, CAN, RSPI, RIIC) | Others |
|---|---|---|---|---|---|---|---|---|
| M4 | | P15 | | | | MTIOC0B/ TMCI2-A/ PO13 | SCK3-A | IRQ5-B |
| M5 | | P14 | | | USB0_OVRC URA/ USB0_DPUPE -B | TMRI2 | | IRQ4-B |
| M6 | VSS_USB | | | | | | | |
| M7 | | P55 | WAIT#-B/ EDREQ0-C | ET_EXOUT | | MTIOC4D-B | | TRDATA3 |
| M8 | | P50 | WR0#/ WR# | | | | SSLB1-A/ TxD2-B | |
| M9 | | PC6 | A22/CS1#-C | ET_ETXD3 | | MTIC11V-A/ MTCLKA-B | MOSIA-A | |
| M10 | | P80 | EDREQ0-A | ET_TX_EN/ RMII_TXD_E N | | MTIOC3B-B | | TRDATA0 |
| M11 | | PC2 | A18-A | ET_RX_DV | | MTCLKE-A | SSLA3-A/ RxD5 | |
| M12 | | PC1 | A17-A | ET_ERXD2 | | MTCLKH-A | SSLA2-A/ SCK5 | |
| M13 | VSS | | | | | | | |
| N1 | | P21 | | | USB0_EXICE N | MTIOC1B/ TMCI0-B/ PO1 | SCL1/RxD0 | |
| N2 | | P16 | | | USB0_VBUS/ USB0_OVRC URB/ USB0_VBUSE N-B | MTIOC3C-A/ TMO2/ PO14 | RxD3-A | IRQ6-B |
| N3 | PLLVSS | | | | | | | |
| N4 | | P13 | | | | TMO3 | SDA0/ TxD2-A | IRQ3-B/ ADTRG1# |
| N5 | | | | | USB0_DM | | | |
| N6 | | | | | USB0_DP | | | |
| N7 | | P54 | EDACK0-C | ET_LINKSTA | | MTIOC4B-B | | TRDATA2 |
| N8 | | P51 | WR1#/BC1#/ WAIT#-D | | | | SSLB2-A/ SCK2 | |
| N9 | VCC | | | | | | | |
| N10 | | PC5 | A21/CS2#-C/ WAIT#-C | ET_ETXD2 | | MTIC11W-A/ MTCLKD-B | RSPCKA-A | |
| N11 | | PC4 | A20/CS3#-C | ET_TX_CLK | | MTCLKC-B | SSLA0-A | |
| N12 | | P76 | CS6#-B | ET_RX_CLK/ REF50CK | | | | |
| N13 | | P74 | CS4#-B | ET_ERXD1/ RMII_RXD1 | | | | |

**Table 1.6 List of Pins and Pin Functions (144-Pin LQFP) (1 / 5)**

| Pin No. 144-Pin LQFP | Power Supply Clock System Control | I/O Port | External Bus EXDMAC | ETHERC EDMAC | USB | Timers (MTU, TMR, PPG, POE, WDT) | Communi-cation (SCI, CAN, RSPI, RIIC) | Others |
|---|---|---|---|---|---|---|---|---|
| 1 | AVSS | | | | | | | |
| 2 | | P05 | | | | | | IRQ13-A/DA1 |
| 3 | VCC | | | | | | | |
| 4 | | P03 | | | | | | IRQ11-A/DA0 |
| 5 | VSS | | | | | | | |
| 6 | | P02 | | | | TMCI1-A | SCK6-A | IRQ10-A |
| 7 | | P01 | | | | TMCI0-A | RxD6-A | IRQ9-A |
| 8 | | P00 | | | | TMRI0-A | TxD6-A | IRQ8-A |
| 9 | BSCANP | | | | | | | |
| 10 | EMLE | | | | | | | |
| 11 | | | | | | WDTOVF# | | |
| 12 | VSS | | | | | | | |
| 13 | MDE | | | | | | | |
| 14 | VCL | | | | | | | |
| 15 | MD1 | | | | | | | |
| 16 | MD0 | | | | | | | |
| 17 | XCIN | | | | | | | |
| 18 | XCOUT | | | | | | | |
| 19 | RES# | | | | | | | |
| 20 | XTAL | | | | | | | |
| 21 | VSS | | | | | | | |
| 22 | EXTAL | | | | | | | |
| 23 | VCC | | | | | | | |
| 24 | | P35 | | | | | | NMI |
| 25 | | P34 | | | | MTIOC0A/ TMCI3/ PO12 | SCK6-B | IRQ4-A/ TRST# |
| 26 | | P33 | | | | MTIOC0D/ PO11 | CRX0/ RxD6-B | IRQ3-A |
| 27 | | P32 | | | | MTIOC0C/ PO10/ RTCOUT | CTX0/ TxD6-B | IRQ2-A |
| 28 | | P31 | | | | MTIOC4D-A/ TMCI2-B/ PO9 | SSLB0-A | IRQ1/ TMS |
| 29 | | P30 | | | | MTIOC4B-A/ TMRI3/ PO8 | RxD1/ MISOB-A | IRQ0/ TDI |
| 30 | | P27 | CS7#-C | | | MTIOC2B/ PO7 | RSPCKB-A/ SCK1 | TCK |
| 31 | | P26 | CS6#-C | | | MTIOC2A/ TMO1/ PO6 | MOSIB-A/ TxD1 | TDO |

**Table 1.6 List of Pins and Pin Functions (144-Pin LQFP) (2 / 5)**

| Pin No. 144-Pin LQFP | Power Supply Clock System Control | I/O Port | External Bus EXDMAC | ETHERC EDMAC | USB | Timers (MTU, TMR, PPG, POE, WDT) | Communi-cation (SCI, CAN, RSPI, RIIC) | Others |
|---|---|---|---|---|---|---|---|---|
| 32 | | P25 | CS5#-C/ EDACK1-B | | USB0_DPRPD | MTIOC4C-A/ MTCLKB-A/ PO5 | RxD3-B | ADTRG0#-B |
| 33 | | P24 | CS4#-C/ EDREQ1-B | | USB0_VBUSEN-A | MTIOC4A-A/ MTCLKA-A/ TMRI1/PO4 | SCK3-B | |
| 34 | | P23 | EDACK0-B | | USB0_DPUPE-A | MTIOC3D-A/ MTCLKD-A/ PO3 | TxD3-B | |
| 35 | | P22 | EDREQ0-B | | USB0_DRPD | MTIOC3B-A/ MTCLKC-A/ TMO0/PO2 | SCK0 | |
| 36 | | P21 | | | USB0_EXICEN | MTIOC1B/ TMCI0-B/ PO1 | SCL1/RxD0 | |
| 37 | | P20 | | | USB0_ID | MTIOC1A/ TMRI0-B/ PO0 | SDA1/ TxD0 | |
| 38 | | P17 | | | | MTIOC3A/ PO15 | TxD3-A | IRQ7-B |
| 39 | PLLVCC | | | | | | | |
| 40 | | P16 | | | USB0_VBUS/ USB0_OVRCURB/ USB0_VBUSEN-B | MTIOC3C-A/ TMO2/ PO14 | RxD3-A | IRQ6-B |
| 41 | PLLVSS | | | | | | | |
| 42 | | P15 | | | | MTIOC0B/ TMCI2-A/ PO13 | SCK3-A | IRQ5-B |
| 43 | | P14 | | | USB0_OVRCURA/ USB0_DPUPE-B | TMRI2 | | IRQ4-B |
| 44 | | P13 | | | | TMO3 | SDA0/ TxD2-A | IRQ3-B/ ADTRG1# |
| 45 | | P12 | | | | TMCI1-B | SCL0/ RxD2-A | IRQ2-B |
| 46 | VCC_USB | | | | | | | |
| 47 | | | | | USB0_DM | | | |
| 48 | | | | | USB0_DP | | | |
| 49 | VSS_USB | | | | | | | |
| 50 | | P56 | EDACK1-C | | | MTIOC3C-B | | |
| 51 | | P55 | WAIT#-B/ EDREQ0-C | ET_EXOUT | | MTIOC4D-B | | TRDATA3 |
| 52 | | P54 | EDACK0-C | ET_LINKSTA | | MTIOC4B-B | | TRDATA2 |
| 53 | BCLK | P53 | | | | | | |
| 54 | | P52 | RD# | | | | SSLB3-A/ RxD2-B | |

**Table 1.6 List of Pins and Pin Functions (144-Pin LQFP) (3 / 5)**

| Pin No. 144-Pin LQFP | Power Supply Clock System Control | I/O Port | External Bus EXDMAC | ETHERC EDMAC | USB | Timers (MTU, TMR, PPG, POE, WDT) | Communi-cation (SCI, CAN, RSPI, RIIC) | Others |
|---|---|---|---|---|---|---|---|---|
| 55 | | P51 | WR1#/BC1#/ WAIT#-D | | | | SSLB2-A/ SCK2 | |
| 56 | | P50 | WR0#/ WR# | | | | SSLB1-A/ TxD2-B | |
| 57 | VSS | | | | | | | |
| 58 | | P83 | EDACK1-A | ET_CRS/ RMII_CRS_DV | | MTIOC4C-B | | TRCLK |
| 59 | VCC | | | | | | | |
| 60 | | PC7 | A23/ CS0#-B | ET_COL | | MTIC11U-A/ MTCLKB-B | MISOA-A | |
| 61 | | PC6 | A22/ CS1#-C | ET_ETXD3 | | MTIC11V-A/ MTCLKA-B | MOSIA-A | |
| 62 | | PC5 | A21/CS2#-C/ WAIT#-C | ET_ETXD2 | | MTIC11W-A/ MTCLKD-B | RSPCKA-A | |
| 63 | | P82 | EDREQ1-A | ET_ETXD1/ RMII_TXD1 | | MTIOC4A-B | | TRSYNC |
| 64 | | P81 | EDACK0-A | ET_ETXD0/ RMII_TXD0 | | MTIOC3D-B | | TRDATA1 |
| 65 | | P80 | EDREQ0-A | ET_TX_EN/ RMII_TXD_EN | | MTIOC3B-B | | TRDATA0 |
| 66 | | PC4 | A20/CS3#-C | ET_TX_CLK | | MTCLKC-B | SSLA0-A | |
| 67 | | PC3 | A19-A | ET_TX_ER | | MTCLKF-A | TxD5 | |
| 68 | | P77 | CS7#-B | ET_RX_ER/ RMII_RX_ER | | | | |
| 69 | | P76 | CS6#-B | ET_RX_CLK/ REF50CK | | | | |
| 70 | | PC2 | A18-A | ET_RX_DV | | MTCLKE-A | SSLA3-A/ RxD5 | |
| 71 | | P75 | CS5#-B | ET_ERXD0/ RMII_RXD0 | | | | |
| 72 | | P74 | CS4#-B | ET_ERXD1/ RMII_RXD1 | | | | |
| 73 | | PC1 | A17-A | ET_ERXD2 | | MTCLKH-A | SSLA2-A/ SCK5 | |
| 74 | VCC | | | | | | | |
| 75 | | PC0 | A16-A | ET_ERXD3 | | MTCLKG-A | SSLA1-A | |
| 76 | VSS | | | | | | | |
| 77 | | P73 | CS3#-B | ET_WOL | | | | |
| 78 | | PB7 | A15 | | | MTIOC10D/ PO31 | | |
| 79 | | PB6 | A14 | | | MTIOC10B/ PO30 | | |
| 80 | | PB5 | A13 | | | MTIOC10C/ MTCLKF-B/ PO29 | | |
| 81 | | PB4 | A12 | | | MTIOC10A/ MTCLKE-B/ PO28 | | |

**Table 1.6 List of Pins and Pin Functions (144-Pin LQFP) (4 / 5)**

| Pin No. 144-Pin LQFP | Power Supply Clock System Control | I/O Port | External Bus EXDMAC | ETHERC EDMAC | USB | Timers (MTU, TMR, PPG, POE, WDT) | Communi-cation (SCI, CAN, RSPI, RIIC) | Others |
|---|---|---|---|---|---|---|---|---|
| 82 | | PB3 | A11 | | | MTIOC9D/ MTCLKH-B/ PO27 | | |
| 83 | | PB2 | A10 | | | MTIOC9B/ MTCLKG-B/ PO26 | | |
| 84 | | PB1 | A9 | | | MTIOC9C/ PO25 | | |
| 85 | | P72 | CS2#-B | ET_MDC | | | | |
| 86 | | P71 | CS1#-B | ET_MDIO | | | | |
| 87 | | PB0 | A8 | | | MTIOC9A/ PO24 | | |
| 88 | | PA7 | A7 | | | MTIOC8B/ PO23 | MISOA-B | |
| 89 | | PA6 | A6 | | | MTIOC8A/ PO22 | MOSIA-B | |
| 90 | | PA5 | A5 | | | MTIOC7B/ PO21 | RSPCKA-B | |
| 91 | VCC | | | | | | | |
| 92 | | PA4 | A4 | | | MTIOC7A/ PO20 | SSLA0-B | |
| 93 | VSS | | | | | | | |
| 94 | | PA3 | A3 | | | MTIOC6D/ PO19 | | |
| 95 | | PA2 | A2 | | | MTIOC6C/ PO18 | SSLA3-B | |
| 96 | | PA1 | A1 | | | MTIOC6B/ PO17 | SSLA2-B | |
| 97 | | PA0 | A0/BC0#/ | | | MTIOC6A/ PO16 | SSLA1-B | |
| 98 | | P67 | CS7#-A/ DQM1 | | | | | |
| 99 | | P66 | CS6#-A/ DQM0 | | | | | |
| 100 | | P65 | CS5#-A/ CKE | | | | | |
| 101 | | PE7 | D15 | | | | MISOB-B | IRQ7-A |
| 102 | | PE6 | D14 | | | | MOSIB-B | IRQ6-A |
| 103 | VCC | | | | | | | |
| 104 | SDCLK | P70 | | | | | | |
| 105 | VSS | | | | | | | |
| 106 | | PE5 | D13 | | | | RSPCKB-B | IRQ5-A |
| 107 | | PE4 | D12 | | | | SSLB0-B | |
| 108 | | PE3 | D11 | | | POE8# | | |
| 109 | | PE2 | D10 | | | POE9# | SSLB3-B | |
| 110 | | PE1 | D9 | | | | SSLB2-B | |
| 111 | | PE0 | D8 | | | | SSLB1-B | |

**Table 1.6 List of Pins and Pin Functions (144-Pin LQFP) (5 / 5)**

| Pin No. 144-Pin LQFP | Power Supply Clock System Control | I/O Port | External Bus EXDMAC | ETHERC EDMAC | USB | Timers (MTU, TMR, PPG, POE, WDT) | Communi-cation (SCI, CAN, RSPI, RIIC) | Others |
|---|---|---|---|---|---|---|---|---|
| 112 | | P64 | CS4#-A/ WE# | | | | | |
| 113 | | P63 | CS3#-A/ CAS# | | | | | |
| 114 | | P62 | CS2#-A/ RAS# | | | | | |
| 115 | | P61 | CS1#-A/ SDCS# | | | | | |
| 116 | VSS | | | | | | | |
| 117 | | P60 | CS0#-A | | | | | |
| 118 | VCC | | | | | | | |
| 119 | | PD7 | D7 | | | MTIC5U/ POE0# | | |
| 120 | | PD6 | D6 | | | MTIC5V/ POE1# | | |
| 121 | | PD5 | D5 | | | MTIC5W/ POE2# | | |
| 122 | | PD4 | D4 | | | MTIC11U-B/ POE3# | | |
| 123 | | PD3 | D3 | | | MTIC11V-B/ POE4# | | |
| 124 | | PD2 | D2 | | | MTIC11W-B/ POE5# | | |
| 125 | | PD1 | D1 | | | POE6# | | |
| 126 | | PD0 | D0 | | | POE7# | | |
| 127 | | P93 | A19-B | | | | | |
| 128 | | P92 | A18-B | | | | | |
| 129 | | P91 | A17-B | | | | | |
| 130 | VSS | | | | | | | |
| 131 | | P90 | A16-B | | | | | |
| 132 | VCC | | | | | | | |
| 133 | | P47 | | | | | | IRQ15-B/AN7 |
| 134 | | P46 | | | | | | IRQ14/AN6 |
| 135 | | P45 | | | | | | IRQ13-B/AN5 |
| 136 | | P44 | | | | | | IRQ12/AN4 |
| 137 | | P43 | | | | | | IRQ11-B/AN3 |
| 138 | | P42 | | | | | | IRQ10-B/AN2 |
| 139 | | P41 | | | | | | IRQ9-B/AN1 |
| 140 | VREFL | | | | | | | |
| 141 | | P40 | | | | | | IRQ8-B/AN0 |
| 142 | VREFH | | | | | | | |
| 143 | AVCC | | | | | | | |
| 144 | | P07 | | | | | | IRQ15-A/ ADTRG0#-A |

**Table 1.7 List of Pins and Pin Functions (100-Pin LQFP) (1 / 4)**

| Pin No. 100-Pin LQFP | Power Supply Clock System Control | I/O Port | External Bus | ETHERC EDMAC | USB | Timers (MTU, TMR, PPG, POE) | Communi-cation (SCI, CAN, RSPI, RIIC) | Others |
|---|---|---|---|---|---|---|---|---|
| 1 | VCC | | | | | | | |
| 2 | EMLE | | | | | | | |
| 3 | VSS | | | | | | | |
| 4 | MDE | | | | | | | |
| 5 | VCL | | | | | | | |
| 6 | MD1 | | | | | | | |
| 7 | MD0 | | | | | | | |
| 8 | XCIN | | | | | | | |
| 9 | XCOUT | | | | | | | |
| 10 | RES# | | | | | | | |
| 11 | XTAL | | | | | | | |
| 12 | VSS | | | | | | | |
| 13 | EXTAL | | | | | | | |
| 14 | VCC | | | | | | | |
| 15 | | P35 | | | | | | NMI |
| 16 | | P34 | | | | MTIOC0A/ TMCI3/ PO12 | SCK6 | IRQ4-A/ TRST# |
| 17 | | P33 | | | | MTIOC0D/ PO11 | CRX0/ RxD6 | IRQ3-A |
| 18 | | P32 | | | | MTIOC0C/ PO10/ RTCOUT | CTX0/ TxD6 | IRQ2-A |
| 19 | | P31 | | | | MTIOC4D-A/ TMCI2/ PO9 | SSLB0-A | IRQ1/ TMS |
| 20 | | P30 | | | | MTIOC4B-A/ TMRI3/ PO8 | RxD1/ MISOB-A | IRQ0/ TDI |
| 21 | | P27 | CS7# | | | MTIOC2B/ PO7 | RSPCKB-A/ SCK1 | TCK |
| 22 | | P26 | CS6# | | | MTIOC2A/ TMO1/ PO6 | MOSIB-A/ TxD1 | TDO |
| 23 | | P25 | CS5# | | USB0_DPRPD | MTIOC4C/ MTCLKB-A/ PO5 | RxD3 | ADTRG0#-B |
| 24 | | P24 | CS4# | | USB0_VBUSEN-A | MTIOC4A/ MTCLKA-A/ TMRI1/PO4 | SCK3 | |
| 25 | | P23 | | | USB0_DPUPE-A | MTIOC3D/ MTCLKD-A/ PO3 | TxD3 | |
| 26 | | P22 | | | USB0_DRPD | MTIOC3B/ MTCLKC-A/ TMO0/PO2 | SCK0 | |

**Table 1.7 List of Pins and Pin Functions (100-Pin LQFP) (2 / 4)**

| Pin No. 100-Pin LQFP | Power Supply Clock System Control | I/O Port | External Bus | ETHERC EDMAC | USB | Timers (MTU, TMR, PPG, POE) | Communi-cation (SCI, CAN, RSPI, RIIC) | Others |
|---|---|---|---|---|---|---|---|---|
| 27 | | P21 | | | USB0_EXICEN | MTIOC1B/ TMCI0/ PO1 | RxD0 | |
| 28 | | P20 | | | USB0_ID | MTIOC1A/ TMRI0/ PO0 | TxD0 | |
| 29 | PLLVCC | | | | | | | |
| 30 | | P16 | | | USB0_VBUS/ USB0_OVRCURB/ USB0_VBUSEN-B | MTIOC3C/ TMO2/ PO14 | | IRQ6-B |
| 31 | PLLVSS | | | | | | | |
| 32 | | P14 | | | USB0_OVRCURA/ USB0_DPUPE-B | MTIOC3A/ TMRI2/ PO15 | | IRQ4-B |
| 33 | | P13 | | | | MTIOC0B/ TMO3/ PO13 | SDA0/ TxD2-A | IRQ3-B/ ADTRG1# |
| 34 | | P12 | | | | TMCI1 | SCL0/ RxD2-A | IRQ2-B |
| 35 | VCC_USB | | | | | | | |
| 36 | | | | | USB0_DM | | | |
| 37 | | | | | USB0_DP | | | |
| 38 | VSS_USB | | | | | | | |
| 39 | | P55 | WAIT#-B | | | MTIOC4D-B | | |
| 40 | | P54 | | | | MTIOC4B-B | | |
| 41 | BCLK | P53 | | | | | | |
| 42 | | P52 | RD# | | | | SSLB3-A/ RxD2-B | |
| 43 | | P51 | WR1#/BC1#/ WAIT#-D | | | | SSLB2-A/ SCK2 | |
| 44 | | P50 | WR0#/ WR# | | | | SSLB1-A/ TxD2-B | |
| 45 | | PC7 | A23/ CS0# | ET_COL | | MTIC11U-A/ MTCLKB-B | MISOA-A | |
| 46 | | PC6 | A22/ CS1# | ET_ETXD3 | | MTIC11V-A/ MTCLKA-B | MOSIA-A | |
| 47 | | PC5 | A21/CS2#/ WAIT#-C | ET_ETXD2 | | MTIC11W-A/ MTCLKD-B | RSPCKA-A | |
| 48 | | PC4 | A20/CS3# | ET_TX_CLK | | MTCLKC-B | SSLA0-A | |
| 49 | | PC3 | A19 | ET_TX_ER | | MTCLKF-A | TxD5 | |
| 50 | | PC2 | A18 | ET_RX_DV | | MTCLKE-A | SSLA3-A/ RxD5 | |
| 51 | | PC1 | A17 | ET_ERXD2 | | MTCLKH-A | SSLA2-A/ SCK5 | |
| 52 | | PC0 | A16 | ET_ERXD3 | | MTCLKG-A | SSLA1-A | |

**Table 1.7 List of Pins and Pin Functions (100-Pin LQFP) (3 / 4)**

| Pin No. 100-Pin LQFP | Power Supply Clock System Control | I/O Port | External Bus | ETHERC EDMAC | USB | Timers (MTU, TMR, PPG, POE) | Communi-cation (SCI, CAN, RSPI, RIIC) | Others |
|---|---|---|---|---|---|---|---|---|
| 53 | | PB7 | A15 | ET_CRS/ RMII_CRS_DV | | MTIOC10D/ PO31 | | |
| 54 | | PB6 | A14 | ET_ETXD1/ RMII_TXD1 | | MTIOC10B/ PO30 | | |
| 55 | | PB5 | A13 | ET_ETXD0/ RMII_TXD0 | | MTIOC10C/ MTCLKF-B/ PO29 | | |
| 56 | | PB4 | A12 | ET_TX_EN/ RMII_TXD_EN | | MTIOC10A/ MTCLKE-B/ PO28 | | |
| 57 | | PB3 | A11 | ET_RX_ER/ RMII_RX_ER | | MTIOC9D/ MTCLKH-B/ PO27 | | |
| 58 | | PB2 | A10 | ET_RX_CLK/ REF50CK | | MTIOC9B/ MTCLKG-B/ PO26 | | |
| 59 | | PB1 | A9 | ET_ERXD0/ RMII_RXD0 | | MTIOC9C/ PO25 | | |
| 60 | VCC | | | | | | | |
| 61 | | PB0 | A8 | ET_ERXD1/ RMII_RXD1 | | MTIOC9A/ PO24 | | |
| 62 | VSS | | | | | | | |
| 63 | | PA7 | A7 | ET_WOL | | MTIOC8B/ PO23 | MISOA-B | |
| 64 | | PA6 | A6 | ET_EXOUT | | MTIOC8A/ PO22 | MOSIA-B | |
| 65 | | PA5 | A5 | ET_LINKSTA | | MTIOC7B/ PO21 | RSPCKA-B | |
| 66 | | PA4 | A4 | ET_MDC | | MTIOC7A/ PO20 | SSLA0-B | |
| 67 | | PA3 | A3 | ET_MDIO | | MTIOC6D/ PO19 | | |
| 68 | | PA2 | A2 | | | MTIOC6C/ PO18 | SSLA3-B | |
| 69 | | PA1 | A1 | | | MTIOC6B/ PO17 | SSLA2-B | |
| 70 | | PA0 | A0/BC0# | | | MTIOC6A/ PO16 | SSLA1-B | |
| 71 | | PE7 | D15 | | | | MISOB-B | IRQ7 |
| 72 | | PE6 | D14 | | | | MOSIB-B | IRQ6-A |
| 73 | | PE5 | D13 | | | | RSPCKB-B | IRQ5 |
| 74 | | PE4 | D12 | | | | SSLB0-B | |
| 75 | | PE3 | D11 | | | POE8# | | |
| 76 | | PE2 | D10 | | | POE9# | SSLB3-B | |
| 77 | | PE1 | D9 | | | | SSLB2-B | |
| 78 | | PE0 | D8 | | | | SSLB1-B | |
| 79 | | PD7 | D7 | | | MTIC5U/ POE0# | | |

**Table 1.7 List of Pins and Pin Functions (100-Pin LQFP) (4 / 4)**

| Pin No. 100-Pin LQFP | Power Supply Clock System Control | I/O Port | External Bus | ETHERC EDMAC | USB | Timers (MTU, TMR, PPG, POE) | Communi-cation (SCI, CAN, RSPI, RIIC) | Others |
|---|---|---|---|---|---|---|---|---|
| 80 | | PD6 | D6 | | | MTIC5V/ POE1# | | |
| 81 | | PD5 | D5 | | | MTIC5W/ POE2# | | |
| 82 | | PD4 | D4 | | | MTIC11U-B/ POE3# | | |
| 83 | | PD3 | D3 | | | MTIC11V-B/ POE4# | | |
| 84 | | PD2 | D2 | | | MTIC11W-B/ POE5# | | |
| 85 | | PD1 | D1 | | | POE6# | | |
| 86 | | PD0 | D0 | | | POE7# | | |
| 87 | | P47 | | | | | | IRQ15-B/AN7 |
| 88 | | P46 | | | | | | IRQ14/AN6 |
| 89 | | P45 | | | | | | IRQ13-B/AN5 |
| 90 | | P44 | | | | | | IRQ12/AN4 |
| 91 | | P43 | | | | | | IRQ11/AN3 |
| 92 | | P42 | | | | | | IRQ10/AN2 |
| 93 | | P41 | | | | | | IRQ9/AN1 |
| 94 | VREFL | | | | | | | |
| 95 | | P40 | | | | | | IRQ8/AN0 |
| 96 | VREFH | | | | | | | |
| 97 | AVCC | | | | | | | |
| 98 | | P07 | | | | | | IRQ15-A/ ADTRG0#-A |
| 99 | AVSS | | | | | | | |
| 100 | | P05 | | | | | | DA1/IRQ13-A |

**Table 1.8 List of Pins and Pin Functions (85-Pin TFLGA) (1 / 3)**

| Pin No. 85-Pin TFLGA | Power Supply Clock System Control | I/O Port | External Bus | USB | Timers (MTU, TMR, PPG) | Communi-cation (SCI, CAN, RSPI, RIIC) | Others |
|---|---|---|---|---|---|---|---|
| A1 | | P05 | | | | | DA1/ IRQ13-A |
| A2 | AVCC | | | | | | |
| A3 | VREFL | | | | | | |
| A4 | | P43 | | | | | IRQ11-B/AN3 |
| A5 | | P47 | | | | | IRQ15/ AN7 |
| A6 | | PD1 | D1 | | | | |
| A7 | | PD4 | D4 | | MTIC11U | | |
| A8 | | PD5 | D5 | | MTIC5W | | |
| A9 | | PD7 | D7 | | MTIC5U | | |
| A10 | | PD6 | D6 | | MTIC5V | | |
| B1 | VCC | | | | | | |
| B2 | AVSS | | | | | | |
| B3 | VREFH | | | | | | |
| B4 | | P42 | | | | | IRQ10/ AN2 |
| B5 | | P46 | | | | | IRQ14/ AN6 |
| B6 | | PD0 | D0 | | | | |
| B7 | | PD2 | D2 | | MTIC11W | | |
| B8 | | PD3 | D3 | | MTIC11V | | |
| B9 | | PA3 | A3 | | MTIOC6D/PO19 | | |
| B10 | | PA1 | A1 | | MTIOC6B/PO17 | SSLA2 | |
| C1 | | P03 | | | | | IRQ11-A/DA0 |
| C2 | VSS | | | | | | |
| C3 | | P40 | | | | | IRQ8/ AN0 |
| C4 | | P41 | | | | | IRQ9/ AN1 |
| C5 | | P44 | | | | | IRQ12/ AN4 |
| C6 | | P45 | | | | | IRQ13-B/AN5 |
| C7 | MD1 | | | | | | |
| C8 | BSCANP | | | | | | |
| C9 | | PA5 | A5 | | MTIOC7B/PO21 | RSPCKA | |
| C10 | | PA0 | A0 | | MTIOC6A/PO16 | SSLA1 | |
| D1 | MDE | | | | | | |
| D2 | EMLE | | | | | | |
| D3 | MD0 | | | | | | |
| D4 | RES# | | | | | | |

**Table 1.8 List of Pins and Pin Functions (85-Pin TFLGA) (2 / 3)**

| Pin No. 85-Pin TFLGA | Power Supply Clock System Control | I/O Port | External Bus | USB | Timers (MTU, TMR, PPG) | Communi-cation (SCI, CAN, RSPI, RIIC) | Others |
|---|---|---|---|---|---|---|---|
| D8 | VCL | | | | | | |
| D9 | | PA6 | A6 | | MTIOC8A/PO22 | MOSIA | |
| D10 | | PA2 | A2 | | MTIOC6C/PO18 | SSLA3 | |
| E1 | XCIN | | | | | | |
| E2 | XCOUT | | | | | | |
| E3 | | P34 | | | MTIOC0A/TMCI3/PO12 | SCK6 | IRQ4-A/ TRST# |
| E8 | VSS | | | | | | |
| E9 | | PB0 | A8 | | MTIOC9A/PO24 | | |
| E10 | | PA4 | A4 | | MTIOC7A/PO20 | SSLA0 | |
| F1 | XTAL | | | | | | |
| F2 | EXTAL | | | | | | |
| F3 | | P32 | | | MTIOC0C/PO10/RTCOUT | TxD6/CTX0 | IRQ2-A |
| F8 | VCC | | | | | | |
| F9 | | PB2 | A10 | | MTIOC9B/MTCLKG-B/ PO26 | | |
| F10 | | PA7 | A7 | | MTIOC8B/PO23 | MISOA | |
| G1 | | P35 | | | | | NMI |
| G2 | | P33 | | | MTIOC0D/PO11 | RxD6/CRX0 | IRQ3-A |
| G3 | | P27 | CS7# | | MTIOC2B/PO7 | SCK1/RSPCKB | TCK |
| G8 | | PB3 | A11 | | MTIOC9D/MTCLKH-B/PO27 | | |
| G9 | | PB5 | A13 | | MTIOC10C/MTCLKF-B/PO29 | | |
| G10 | | PB1 | A9 | | MTIOC9C/PO25 | | |
| H1 | | P31 | | | MTIOC4D/TMCI2/PO9 | SSLB0 | IRQ1/ TMS |
| H2 | | P30 | | | MTIOC4B/TMRI3/PO8 | RxD1/MISOB | IRQ0/ TDI |
| H3 | | P26 | CS6# | | MTIOC2A/TMO1/PO6 | TxD1/MOSIB | TDO |
| H4 | PLLVCC | | | | | | |
| H5 | | P14 | | USB0_OVRCURA/USB0_DPUPE-B | MTIOC3A/TMRI2/PO15 | | IRQ4-B |
| H6 | | P13 | | | MTIOC0B/TMO3/PO13 | TxD2-A/SDA0 | IRQ3-B/ ADTRG1# |
| H7 | BCLK | P53 | | | | | |
| H8 | | PB6 | A14 | | MTIOC10B/PO30 | | |
| H9 | | PB7 | A15 | | MTIOC10D/PO31 | | |
| H10 | | PB4 | A12 | | MTIOC10A/MTCLKE-B/PO28 | | |
| J1 | | P25 | CS5# | USB0_DPRPD | MTIOC4C/MTCLKB/PO5 | RxD3 | ADTRG0# |
| J2 | | P23 | | USB0_DPUPE-A | MTIOC3D/MTCLKD/PO3 | TxD3 | |
| J3 | | P24 | CS4# | USB0_VBUSEN-A | MTIOC4A/MTCLKA/TMRI1/ PO4 | SCK3 | |

**Table 1.8 List of Pins and Pin Functions (85-Pin TFLGA) (3 / 3)**

| Pin No. 85-Pin TFLGA | Power Supply Clock System Control | I/O Port | External Bus | USB | Timers (MTU, TMR, PPG) | Communi-cation (SCI, CAN, RSPI, RIIC) | Others |
|---|---|---|---|---|---|---|---|
| J4 | | P16 | | USB0_VBUS/ USB0_OVRCURB/ USB0_VBUSEN-B | MTIOC3C/TMO2/PO14 | | IRQ6 |
| J5 | VCC_USB | | | | | | |
| J6 | | | | USB0_DM | | | |
| J7 | | P52 | RD# | | | RxD2-B/SSLB3 | |
| J8 | | P51 | WAIT# | | | SCK2/SSLB2 | |
| J9 | | PC3 | A19 | | MTCLKF-A | TxD5 | |
| J10 | | PC0 | A16 | | MTCLKG-A | | |
| K1 | | P21 | | USB0_EXICEN | MTIOC1B/TMCI0/PO1 | RxD0/SCL1 | |
| K2 | | P22 | | USB0_DRPD | MTIOC3B/MTCLKC/TMO0/PO2 | SCK0 | |
| K3 | | P20 | | USB0_ID | MTIOC1A/TMRI0/PO0 | TxD0/SDA1 | |
| K4 | PLLVSS | | | | | | |
| K5 | | P12 | | | TMCI1 | RxD2-A/SCL0 | IRQ2-B |
| K6 | | | | USB0_DP | | | |
| K7 | VSS_USB | | | | | | |
| K8 | | P50 | WR0# | | | TxD2-B/SSLB1 | |
| K9 | | PC2 | A18 | | MTCLKE-A | RxD5 | |
| K10 | | PC1 | A17 | | MTCLKH-A | SCK5 | |

## 1.5 Pin Functions

Table 1.8 lists the pin functions.

**Table 1.9 Pin Functions (1 / 7)**

| Classifications | Pin Name | I/O | Description |
|---|---|---|---|
| Power supply | VCC | Input | Power supply pin. Connect it to the system power supply. |
| | VCL | Input | Connect this pin to VSS via a 0.1-μF capacitor. The capacitor should be placed close to the pin. |
| | VSS | Input | Ground pin. Connect it to the system power supply (0 V). |
| | PLLVCC | Input | Power supply pin for the PLL circuit. Connect it to the system power supply. |
| | PLLVSS | Input | Ground pin for the PLL circuit. |
| Clock | XTAL | Output | Pins for a crystal resonator. An external clock signal can be input through the EXTAL pin. |
| | EXTAL | Input | |
| | BCLK | Output | Outputs the external bus clock for external devices. |
| | SDCLK | Output | Outputs the clock dedicated for the SDRAM. |
| | XCOUT | Output | Input/output pins for the subclock generation circuit. Connect a crystal resonator between XCOUT and XCIN. |
| | XCIN | Input | |
| Operating mode control | MD0, MD1, MDE | Input | Pins for setting the operating mode. The signal levels on these pins must not be changed during operation. |
| System control | RES# | Input | Reset signal input pin. This LSI enters the reset state when this signal goes low. |
| | EMLE | Input | Input pin to enable the connection of the on-chip emulator signal. When the on-chip emulator is used, this pin should be driven high. When not used, it should be driven low. |
| | BSCANP | Input | Boundary scan pin. Boundary scan is enabled when this pin goes high. When not used, it should be driven low. |
| CNVSS | CNVSS | Input | Connect this pin to VSS via pull-down resister. |
| On-chip emulator | TRST# | Input | On-chip emulator pins or boundary scan pins. When the EMLE pin is driven high, these pins are dedicated for the on-chip emulator. |
| | TMS | Input | |
| | TDI | Input | |
| | TCK | Input | |
| | TDO | Output | |
| | TRCLK | Output | This pin outputs the clock for synchronization with the trace data. |
| | TRSYNC | Output | This pin indicates that output from the TRDATA0 to TRDATA3 pins is valid. |
| | TRDATA0-A/TRDATA3-B | Output | These pins output the trace information. |
| Address bus | A0 to A15<br>A16-A/A16-B to<br>A23-A/A23-B | Output | Output pins for the address. |
| Data bus | D0 to D31 | I/O | Input and output pins for the bidirectional data bus. |

**Table 1.9 Pin Functions (2 / 7)**

| Classifications | Pin Name | I/O | Description |
|---|---|---|---|
| Bus control | RD# | Output | Strobe signal which indicates that reading from the external bus interface space is in progress. |
| | WR# | Output | Strobe signal which indicates that writing to the external bus interface space is in progress, in 1-write strobe mode. |
| | WR0# to WR3# | Output | Strobe signals which indicate that any group of data bus pins (D7 to D0, D15 to D8, D23 to D16, and D31 to D24) is valid in writing to the external bus interface space, in byte strobe mode. |
| | BC0# to BC3# | Output | Strobe signals which indicate that any group of data bus pins (D7 to D0, D15 to D8, D23 to D16, and D31 to D24) is valid in access to the external bus interface space, in 1-write strobe mode. |
| | WE# | Output | Output pin for SDRAM write enable signals. |
| | CAS# | Output | Output pin for SDRAM column address strobe signals. |
| | RAS# | Output | Output pin for SDRAM row address strobe signals. |
| | CKE | Output | Output pin for SDRAM clock enable signals. |
| | DQM0 to DQM34 | Output | Output pins for SDRAM I/O data mask enable signals. |
| | SDCS# | Output | Output pin for SDRAM chip select signals. |
| | CS0#-A/CS0#-B<br>CS1#-A/CS1#-B/CS1#-C<br>CS2#-A/CS2#-B/CS2#-C<br>CS3#-A/CS3#-B/CS3#-C<br>CS4#-A/CS4#-B/CS4#-C<br>CS5#-A/CS5#-B/CS5#-C<br>CS6#-A/CS6#-B/CS6#-C<br>CS7#-A/CS7#-B/CS7#-C | Output | Select signals for areas 0 to 7. |
| | WAIT#-A/WAIT#-B/<br>WAIT#-C/WAIT#-D | Input | Input pins for wait request signals in access to the external space. |
| EXDMA controller | EDREQ0-A/EDREQ0-B/<br>EDREQ0-C | Input | Input pins for external DMA transfer requests of channel 0. |
| | EDREQ1-A/EDREQ1-B/<br>EDREQ1-C | Input | Input pins for external DMA transfer requests of channel 1. |
| | EDACK0-A/EDACK0-B/<br>EDACK0-C | Output | Output pins for single address transfer acknowledge signals of channel 0. |
| | EDACK1-A/EDACK1-B/<br>EDACK1-C | Output | Output pins for single address transfer acknowledge signals of channel 1. |
| Interrupt | NMI | Input | Non-maskable interrupt request signal. |
| | IRQ0-A/IRQ0-B<br>IRQ1-A/IRQ1-B<br>IRQ2-A/IRQ2-B<br>IRQ3-A/IRQ3-B<br>IRQ4-A/IRQ4-B<br>IRQ5-A/IRQ5-B<br>IRQ6-A/IRQ6-B<br>IRQ7-A/IRQ7-B<br>IRQ8-A/IRQ8-B<br>IRQ9-A/IRQ9-B<br>IRQ10-A/IRQ10-B<br>IRQ11-A/IRQ11-B<br>IRQ12<br>IRQ13-A/IRQ13-B<br>IRQ14<br>IRQ15-A/IRQ15-B | Input | Interrupt request signals. |

**Table 1.9 Pin Functions (3 / 7)**

| Classifications | Pin Name | I/O | Description |
|---|---|---|---|
| Multi-function timer pulse unit | MTIOC0A<br>MTIOC0B<br>MTIOC0C<br>MTIOC0D | I/O | The TGRA0 to TGRD0 input capture input/output compare output/PWM output pins. |
| | MTIOC1A<br>MTIOC1B | I/O | The TGRA1 and TGRB1 input capture input/output compare output/PWM output pins. |
| | MTIOC2A<br>MTIOC2B | I/O | The TGRA2 and TGRB2 input capture input/output compare output/PWM output pins. |
| | MTIOC3A<br>MTIOC3B-A/MTIOC3B-B<br>MTIOC3C-A/MTIOC3C-B<br>MTIOC3D-A/MTIOC3D-B | I/O | The TGRA3 to TGRD3 input capture input/output compare output/PWM output pins. |
| | MTIOC4A-A/MTIOC4A-B<br>MTIOC4B-A/MTIOC4B-B<br>MTIOC4C-A/MTIOC4C-B<br>MTIOC4D-A/MTIOC4D-B | I/O | The TGRA4 and TGRB4 input capture input/output compare output/PWM output pins. |
| | MTIC5U-A/MTIC5U-B<br>MTIC5V-A/MTIC5V-B<br>MTIC5W-A/MTIC5W-B | Input | The TGRU5, TGRV5, and TGRW5 input capture input/dead time compensation input pins. |
| | MTIOC6A<br>MTIOC6B<br>MTIOC6C<br>MTIOC6D | I/O | The TGRA6 to TGRD6 input capture input/output compare output/PWM output pins. |
| | MTIOC7A<br>MTIOC7B | I/O | The TGRA7 and TGRB7 input capture input/output compare output/PWM output pins. |
| | MTIOC8A<br>MTIOC8B | I/O | The TGRA8 and TGRB8 input capture input/output compare output/PWM output pins. |
| | MTIOC9A<br>MTIOC9B<br>MTIOC9C<br>MTIOC9D | I/O | The TGRA9 to TGRD9 input capture input/output compare output/PWM output pins. |
| | MTIOC10A<br>MTIOC10B<br>MTIOC10C<br>MTIOC10D | I/O | The TGRA10 to TGRB10 input capture input/output compare output/PWM output pins. |
| | MTIC11U-A/MTIC11U-B<br>MTIC11V-A/MTIC11V-B<br>MTIC11W-A/MTIC11W-B | Input | The TGRU11, TGRV11, and TGRW11 input capture input/dead time compensation input pins. |
| | MTCLKA-A/MTCLKA-B<br>MTCLKB-A/MTCLKB-B<br>MTCLKC-A/MTCLKC-B<br>MTCLKD-A/MTCLKD-B<br>MTCLKE-A/MTCLKE-B<br>MTCLKF-A/MTCLKF-B<br>MTCLKG-A/MTCLKG-B<br>MTCLKH-A/MTCLKH-B | Input | Input pins for external clock signals. |
| Port output enable | POE0# to POE9# | Input | Input pins for request signals to place the MTU large-current pin in the high impedance state. |
| Programmable pulse generator | PO0 to PO31 | Output | Output pins for the pulse signals. |

**Table 1.9 Pin Functions (4 / 7)**

| Classifications | Pin Name | I/O | Description |
|---|---|---|---|
| 8-bit timer | TMO0 to TMO3 | Output | Output pins for the compare match signals. |
| | TMCI0-A/TMCI0-B<br>TMCI1-A/TMCI1-B<br>TMCI2-A/TMCI2-B<br>TMCI3-A/TMCI3-B | Input | Input pins for the external clock signals that drive for the counters. |
| | TMRI0-A/TMRI0-B<br>TMRI1<br>TMRI2<br>TMRI3-A/TMRI3-B | Input | Input pins for the counter-reset signals. |
| Watchdog timer | WDTOVF# | Output | Output pin for the counter-overflow signal in watchdog-timer mode. |
| Serial communications interface | TxD0<br>TxD1-A/TxD1-B<br>TxD2-A/TxD2-B<br>TxD3-A/TxD3-B<br>TxD5<br>TxD6-A/TxD6-B | Output | Output pins for data transmission. |
| | RxD0<br>RxD1-A/RxD1-B<br>RxD2-A/RxD2-B<br>RxD3-A/RxD3-B<br>RxD5<br>RxD6-A/RxD6-B | Input | Input pins for data reception. |
| | SCK0<br>SCK1-A/SCK1-B<br>SCK2-A/SCK2-B<br>SCK3-A/SCK3-B<br>SCK5<br>SCK6-A/SCK6-B | I/O | Input/output pins for clock signals. |
| $I^2C$ bus interface | SCL0, SCL1 | I/O | Input/output pins for $I^2C$ bus interface clocks. Bus can be directly driven by the NMOS open drain output. |
| | SDA0, SDA1 | I/O | Input/output pins for $I^2C$ bus interface data. Bus can be directly driven by the NMOS open drain output. |

**Table 1.9 Pin Functions (5 / 7)**

| Classifications | Pin Name | I/O | Description |
|---|---|---|---|
| Ethernet controller | REF50CK | Input | 50-MHz reference clock. This pin inputs reference signals for transmission/reception timings in RMII mode. |
| | RMII_CRS_DV | Input | Indicates that there are carrier detection signals and valid receive data on RMII_RXD1 and RMII_RXD0 in RMII mode. |
| | RMII_TXD0, RMII_TXD1 | Output | 2-bit transmit data in RMII mode. |
| | RMII_RXD0, RMII_RXD1 | Input | 2-bit receive data in RMII mode. |
| | RMII_TXD_EN | Output | Output pin for data transmit enable signals in RMII mode. |
| | RMII_RX_ER | Input | Indicates an error has occurred during reception of data in RMII mode. |
| | ET_CRS | Input | Carrier detection/data reception enable pin. |
| | ET_RX_DV | Input | Indicates that there are valid receive data on ET_ERXD3 to ET_ERXD0. |
| | ET_EXOUT | Output | General-purpose external output pin. |
| | ET_LINKSTA | Input | Inputs link status from the PHY-LSI. |
| | ET_ETXD0 to ET_ETXD3 | Output | 4 bits of MII transmit data. |
| | ET_ERXD0 to ET_ERXD3 | Input | 4 bits of MII receive data. |
| | ET_TX_EN | Output | Transmit enable pin. Indicates that transmit data is ready on ET_ETXD3 to ET_ETXD0. |
| | ET_TX_ER | Output | Transmit error pin. Notifies the PHY_LSI of an error during transmission. |
| | ET_RX_ER | Input | Receive error pin. Recognizes an error during reception. |
| | ET_TX_CLK | Input | Transmit clock pin. This pin inputs reference signals for output timings from ET_TX_EN, ET_ETXD3 to ET_ETXD0, and ET_TX_ER. |
| | ET_RX_CLK | Input | Receive clock pin. This pin inputs reference signals for input timings to ET_RX_DV, ET_ERXD3 to ET_ERXD0, and ET_RX_ER. |
| | ET_COL | Input | Inputs collision detection signals. |
| | ET_WOL | Output | Receives Magic Packets™ |
| | ET_MDC | Output | Outputs reference clock signals for information transfer via ET_MDIO. |
| | ET_MDIO | I/O | These pins carry bidirectional signals for the exchange of management information between the RX62N Group and the PHY-LSI. |

**Table 1.9 Pin Functions (6 / 7)**

| Classifications | Pin Name | I/O | Description |
|---|---|---|---|
| USB 2.0 host/function module | VCC_USB | Input | Power-supply pin for the USB. Connect this pin to the system power supply even when the USB is not to be used. |
| | VSS_USB | Input | Ground pin for the USB. Connect this pin to the system power supply (0 V) even when the USB is not to be used. |
| | USB0_DP<br>USB1_DP | I/O | Inputs or outputs D+ data for the USB bus. |
| | USB0_DM<br>USB1_DM | I/O | Inputs or outputs D- data for the USB bus. |
| | USB0_DPRPD<br>USB1_DPRPD | Output | Enable D+ pull-down. |
| | USB0_DRPD<br>USB1_DRPD | Output | Enable D- pull-down. |
| | USB0_EXICEN<br>USB1_EXICEN | Output | Connect these pins to the OTG power supply IC. |
| | USB0_ID<br>USB1_ID | Input | Connect these pins to the OTG power supply IC. |
| | USB0_VBUSEN-A/<br>USB0_VBUSEN-B<br>USB1_VBUSEN-A/<br>USB1_VBUSEN-B | Output | VBUS power enable pins for the USB. |
| | USB0_DPUPE-A/<br>USB0_DPUPE-B<br>USB1_DPUPE-A/<br>USB1_DPUPE-B | Output | Pull-up pins for the USB. |
| | USB0_OVRCURA/<br>USB0_OVRCURB<br>USB1_OVRCURA/<br>USB1_OVRCURB | Input | Over current pins for the USB. |
| | USB0_VBUS<br>USB1_VBUS | Input | Input pins for detection of connection and disconnection of the USB cable. |
| CAN module | CRX0 | Input | Input pins for the CAN. |
| | CTX0 | Output | Output pins for the CAN. |
| Serial peripheral interfaces | RSPCKA-A/<br>RSPCKA-B | I/O | Clock input/output pins for the RSPI. |
| | RSPCKB-A/<br>RSPCKB-B | I/O | Clock input/output pins for the RSPI |
| | MOSIA-A/MOSIA-B<br>MOSIB-A/MOSIB-B | I/O | Input or output data output from the master for the RSPI. |
| | MISOA-A/MISOA-B<br>MISOB-A/MISOB-B | I/O | Input or output data output from the slave for the RSPI. |
| | SSLA0-A/SSLA0-B | I/O | Select the slave for the RSPI. |
| | SSLA1-A/SSLA1-B<br>SSLA2-A/SSLA2-B<br>SSLA3-A/SSLA3-B | Output | |
| | SSLB0-A/SSLB0-B | I/O | |
| | SSLB1-A/SSLB1-B<br>SSLB2-A/SSLB2-B<br>SSLB3-A/SSLB3-B | Output | |
| Realtime clock | RTCOUT | Output | Output pin for 1-Hz clock. |
| A/D converter | AN0 to AN7 | Input | Input pins for the analog signals to be processed by the A/D converter. |
| | ADTRG0#-A/ADTRG0#-B<br>ADTRG1# | Input | Input pins for the external trigger signals that start the A/D conversion. |
| D/A converter | DA0, DA1 | Output | Output pins for the analog signals from the D/A converter. |

**Table 1.9 Pin Functions (7 / 7)**

| Classifications | Pin Name | I/O | Description |
|---|---|---|---|
| Analog power supply | AVCC | Input | Analog power supply pin for the A/D and D/A converters. When the A/D and D/A converters are not in use, connect this pin to the system power supply. |
| | AVSS | Input | Ground pin for the A/D and D/A converters. Connect this pin to the system power supply (0 V). |
| | VREFH | Input | Reference power supply pin for the A/D and D/A converters. When the A/D and D/A converters are not in use, connect this pin to the system power supply. |
| | VREFL | Input | Reference ground pin for the A/D and D/A converters. Make sure to connect this pin to the analog reference power supply (0 V). When the A/D and D/A converters are not in use, connect this pin to the system power supply (0 V). |
| I/O ports | P00 to P03, P05, P07 | I/O | 6-bit input/output pins. |
| | P10 to P17 | I/O | 8-bit input/output pins. |
| | P20 to P27 | I/O | 8-bit input/output pins. |
| | P30 to P34 | I/O | 5-bit input/output pins. |
| | P35 | Input | 1-bit input pin. |
| | P40 to P47 | I/O | 8-bit input/output pins. |
| | P50 to P52, P54 to P57 | I/O | 7-bit input/output pins. |
| | P53 | Input | 1-bit input pin. |
| | P60 to P67 | I/O | 8-bit input/output pins. |
| | P70 to P77 | I/O | 8-bit input/output pins. |
| | P80 to P85 | I/O | 6-bit input/output pins. |
| | P90 to P97 | I/O | 8-bit input/output pins. |
| | PA0 to PA7 | I/O | 8-bit input/output pins. |
| | PB0 to PB7 | I/O | 8-bit input/output pins. |
| | PC0 to PC7 | I/O | 8-bit input/output pins. |
| | PD0 to PD7 | I/O | 8-bit input/output pins. |
| | PE0 to PE7 | I/O | 8-bit input/output pins. |
| | PF0 to PF4 | I/O | 5-bit input/output pins. |
| | PG0 to PG7 | I/O | 8-bit input/output pins. |

# 2. CPU

The RX CPU has sixteen general-purpose registers, nine control registers, and one accumulator used for DSP instructions.

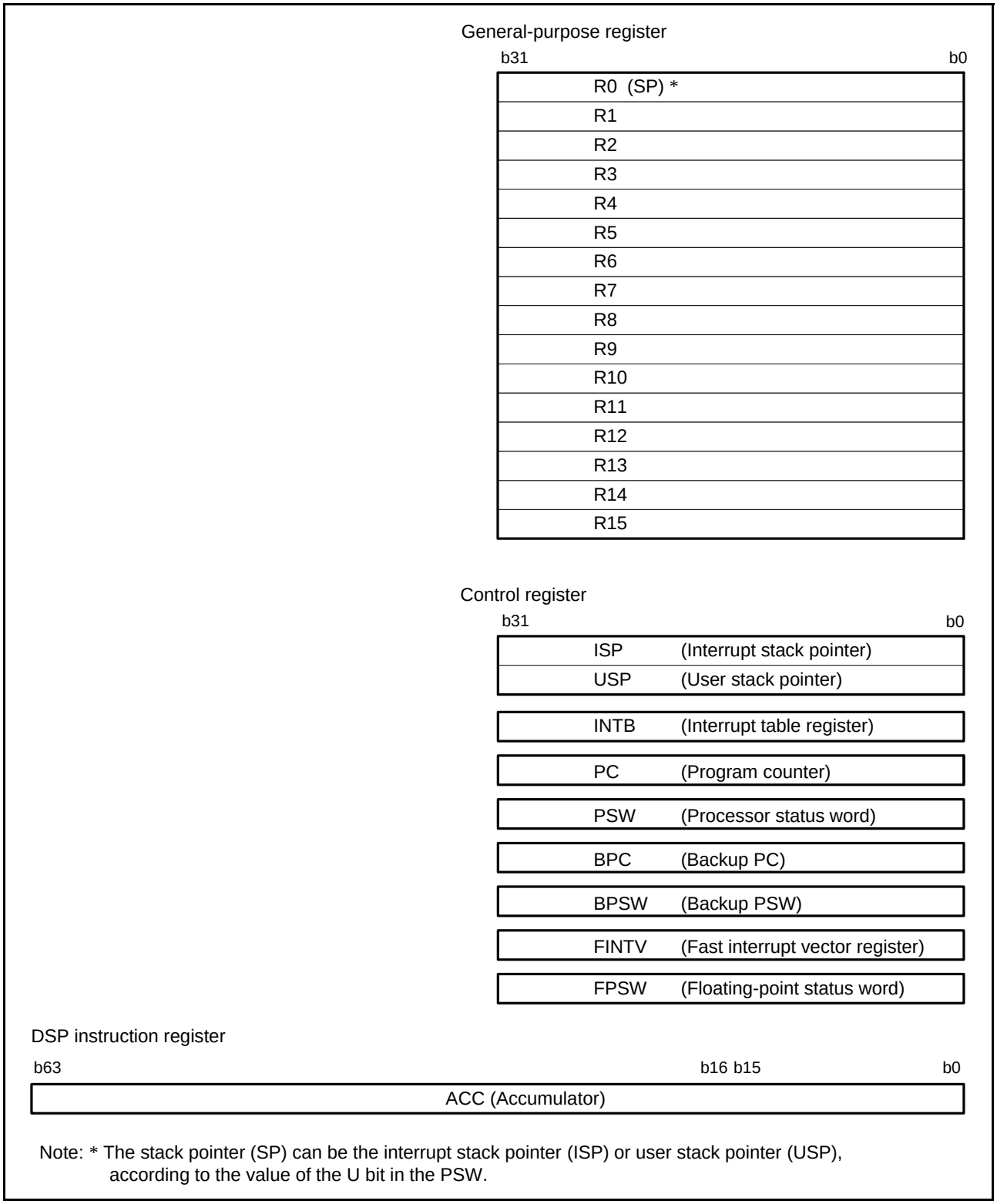



**Figure 2.1 Register Set of the CPU**

## 2.1 General-Purpose Registers (R0 to R15)

This CPU has sixteen general-purpose registers (R0 to R15). R1 to R15 can be used as data registers or address registers.

R0, a general-purpose register, also functions as the stack pointer (SP). The stack pointer is switched to operate as the interrupt stack pointer (ISP) or user stack pointer (USP) by the value of the stack pointer select bit (U) in the processor status word (PSW).

## 2.2 Control Registers

### (1) Interrupt Stack Pointer (ISP)/User Stack Pointer (USP)

The stack pointer (SP) can be either of two types, the interrupt stack pointer (ISP) or the user stack pointer (USP). Whether the stack pointer operates as the ISP or USP depends on the value of the stack pointer select bit (U) in the processor status word (PSW).

Set the ISP or USP to a multiple of four, as this reduces the numbers of cycles required to execute interrupt sequences and instructions entailing stack manipulation.

### (2) Interrupt Table Register (INTB)

The interrupt table register (INTB) specifies the address where the relocatable vector table starts.

Set INTB to a multiple of four.

### (3) Program Counter (PC)

The program counter (PC) indicates the address of the instruction being executed.

### (4) Processor Status Word (PSW)

The processor status word (PSW) indicates results of instruction execution or the state of the CPU.

### (5) Backup PC (BPC)

The backup PC (BPC) is provided to speed up response to interrupts.

After a fast interrupt has been generated, the contents of the program counter (PC) are saved in the BPC.

### (6) Backup PSW (BPSW)

The backup PSW (BPSW) is provided to speed up response to interrupts.

After a fast interrupt has been generated, the contents of the processor status word (PSW) are saved in the BPSW. The allocation of bits in the BPSW corresponds to that in the PSW.

### (7) Fast Interrupt Vector Register (FINTV)

The fast interrupt vector register (FINTV) is provided to speed up response to interrupts.

The FINTV register specifies a branch destination address when a fast interrupt has been generated.

### (8) Floating-Point Status Word (FPSW)

The floating-point status word (FPSW) indicates the results of floating-point operations.

When an exception handling enable bit (Ej) enables the exception handling (Ej = 1), the exception cause can be identified by checking the corresponding Cj flag in the exception handling routine. If the exception handling is masked (Ej = 0), the occurrence of exception can be checked by reading the Fj flag at the end of a series of processing. Once the Fj flag has been set to 1, this value is retained until it is cleared to 0 by software (j = X, U, Z, O, or V).

### (9) Accumulator (ACC)

The accumulator (ACC) is a 64-bit register used for DSP instructions. The accumulator is also used for the multiply and multiply-and-accumulate instructions; EMUL, EMULU, FMUL, MUL, and RMPA, in which case the prior value in the accumulator is modified by execution of the instruction.

Use the MVTACHI and MVTACLO instructions for writing to the accumulator. The MVTACHI and MVTACLO instructions write data to the higher-order 32 bits (bits 63 to 32) and the lower-order 32 bits (bits 31 to 0), respectively.

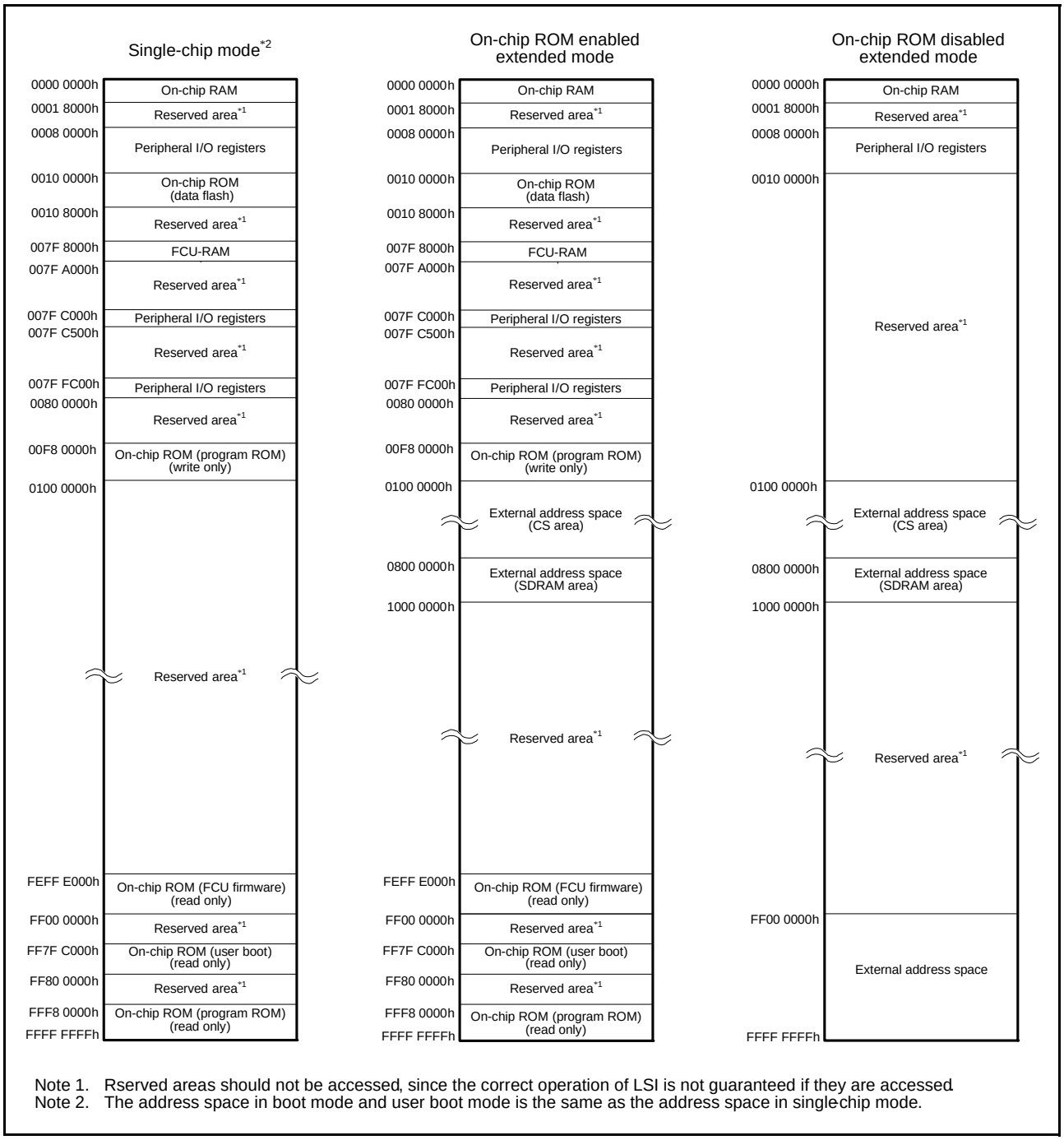
Use the MVFACHI and MVFACMI instructions for reading data from the accumulator. The MVFACHI and MVFACMI instructions read data from the higher-order 32 bits (bits 63 to 32) and the middle 32 bits (bits 47 to 16), respectively.

# 3. Address Space

## 3.1 Address Space

This LSI has a 4-Gbyte address space, consisting of the range of addresses from 0000 0000h to FFFF FFFFh. That is, linear access to an address space of up to 4 Gbytes is possible, and this contains both program and data areas.

Figure 3.1 shows the memory maps in the respective operating modes. Accessible areas will differ according to the operating mode and states of control bits.




Note 1. Rserved areas should not be accessed, since the correct operation of LSI is not guaranteed if they are accessed.
Note 2. The address space in boot mode and user boot mode is the same as the address space in single-chip mode.

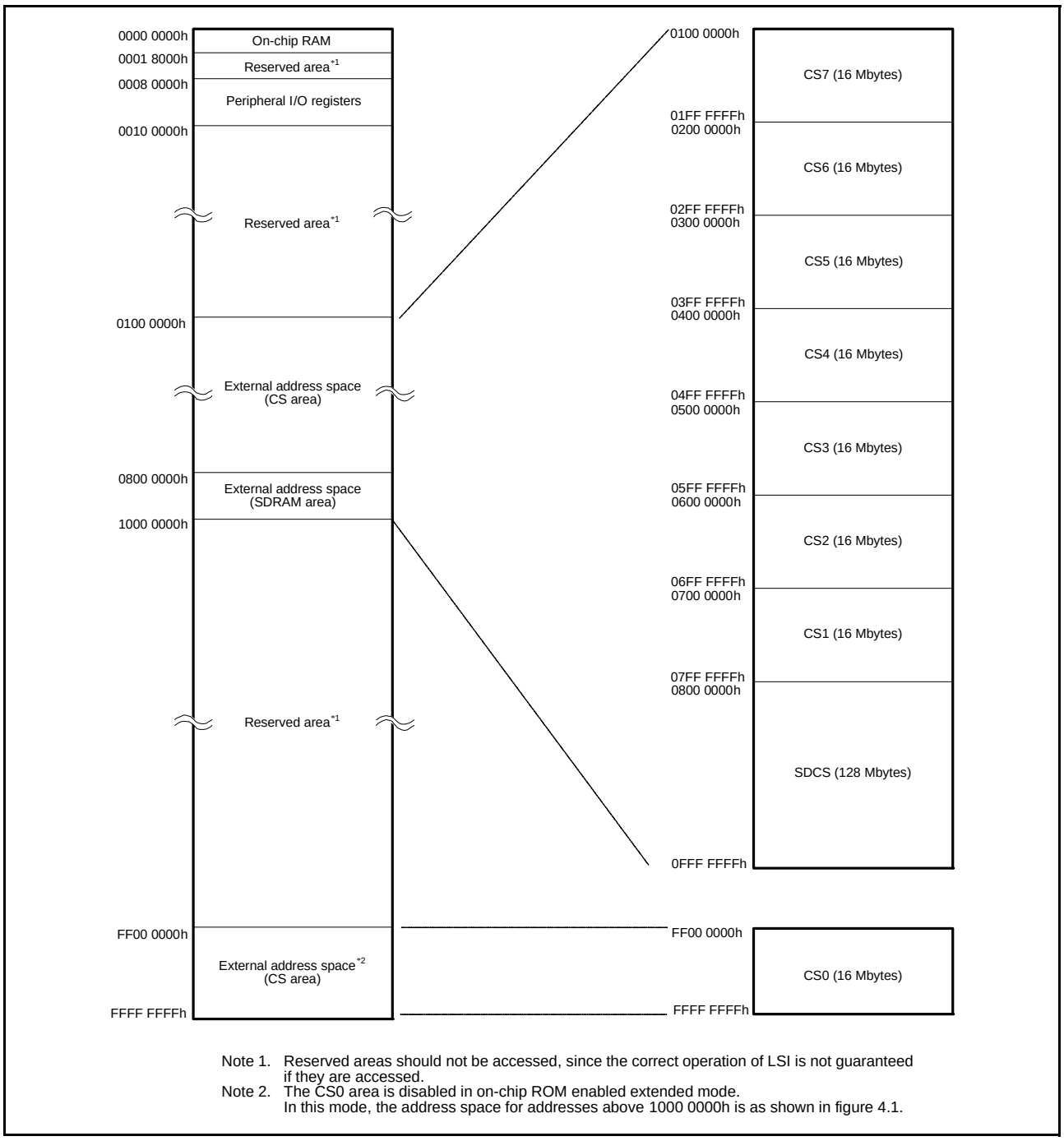
**Figure 3.1 Memory Map in Each Operating Mode**

## 3.2 External Address Space

The external address space is classified into CS areas (CS0 to CS7) and SDRAM area (SDCS).

The CS area is divided into up to 8 areas (CS0 to CS7), each corresponding to the CSi# signal output from a CSi# (i = 0 to 7) pin.

Figure 3.2 shows the address ranges corresponding to the individual CS areas (CS0 to CS7) and SDRAM area (SDCS) in on-chip ROM disabled extended mode.




Note 1. Reserved areas should not be accessed, since the correct operation of LSI is not guaranteed if they are accessed.
Note 2. The CS0 area is disabled in on-chip ROM enabled extended mode.
In this mode, the address space for addresses above 1000 0000h is as shown in figure 4.1.

**Figure 3.2 Correspondence between External Address Spaces, CS Areas (CS0 to CS7), and SDRAM area (SDCS) (In On-Chip ROM Disabled Extended Mode)**

# 4. I/O Registers

**Table 4.1 List of I/O Registers (Address Order) (1 / 36)**

| Address | Module Abbreviation | Register Name | Register Abbreviation | Number of Bits | Access Size | Number of Access Cycles |
|---|---|---|---|---|---|---|
| 0008 0000h | SYSTEM | Mode monitor register | MDMONR | 16 | 16 | 3 ICLK |
| 0008 0002h | SYSTEM | Mode status register | MDSR | 16 | 16 | 3 ICLK |
| 0008 0006h | SYSTEM | System control register 0 | SYSCR0 | 16 | 16 | 3 ICLK |
| 0008 0008h | SYSTEM | System control register 1 | SYSCR1 | 16 | 16 | 3 ICLK |
| 0008 000Ch | SYSTEM | Standby control register | SBYCR | 16 | 16 | 3 ICLK |
| 0008 0010h | SYSTEM | Module stop control register A | MSTPCRA | 32 | 32 | 3 ICLK |
| 0008 0014h | SYSTEM | Module stop control register B | MSTPCRB | 32 | 32 | 3 ICLK |
| 0008 0018h | SYSTEM | Module stop control register C | MSTPCRC | 32 | 32 | 3 ICLK |
| 0008 0020h | SYSTEM | System clock control register | SCKCR | 32 | 32 | 3 ICLK |
| 0008 0030h | SYSTEM | External bus clock control register | BCKCR | 8 | 8 | 3 ICLK |
| 0008 0040h | SYSTEM | Oscillation stop detection control register | OSTDCR | 16 | 16 | 3 ICLK |
| 0008 1300h | BSC | Bus error status clear register | BERCLR | 8 | 8 | 2 ICLK |
| 0008 1304h | BSC | Bus error monitoring enable register | BEREN | 8 | 8 | 2 ICLK |
| 0008 1308h | BSC | Bus error status register 1 | BERSR1 | 8 | 8 | 2 ICLK |
| 0008 130Ah | BSC | Bus error status register 2 | BERSR2 | 16 | 16 | 2 ICLK |
| 0008 2000h | DMAC0 | DMA source address register | DMSAR | 32 | 32 | 2 ICLK |
| 0008 2004h | DMAC0 | DMA destination address register | DMDAR | 32 | 32 | 2 ICLK |
| 0008 2008h | DMAC0 | DMA transfer count register | DMCRA | 32 | 32 | 2 ICLK |
| 0008 200Ch | DMAC0 | DMA block transfer count register | DMCRB | 16 | 16 | 2 ICLK |
| 0008 2010h | DMAC0 | DMA transfer mode register | DMTMD | 16 | 16 | 2 ICLK |
| 0008 2013h | DMAC0 | DMA interrupt setting register | DMINT | 8 | 8 | 2 ICLK |
| 0008 2014h | DMAC0 | DMA address mode register | DMAMD | 16 | 16 | 2 ICLK |
| 0008 2018h | DMAC0 | DMA offset register | DMOFR | 32 | 32 | 2 ICLK |
| 0008 201Ch | DMAC0 | MA transfer enable register | DMCNT | 8 | 8 | 2 ICLK |
| 0008 201Dh | DMAC0 | DMA software start register | DMREQ | 8 | 8 | 2 ICLK |
| 0008 201Eh | DMAC0 | DMA status register | DMSTS | 8 | 8 | 2 ICLK |
| 0008 201Fh | DMAC0 | DMA activation source flag control register | DMCSL | 8 | 8 | 2 ICLK |
| 0008 2040h | DMAC1 | DMA source address register | DMSAR | 32 | 32 | 2 ICLK |
| 0008 2044h | DMAC1 | DMA destination address register | DMDAR | 32 | 32 | 2 ICLK |
| 0008 2048h | DMAC1 | DMA transfer count register | DMCRA | 32 | 32 | 2 ICLK |
| 0008 204Ch | DMAC1 | DMA block transfer count register | DMCRB | 16 | 16 | 2 ICLK |
| 0008 2050h | DMAC1 | DMA transfer mode register | DMTMD | 16 | 16 | 2 ICLK |
| 0008 2053h | DMAC1 | DMA interrupt setting register | DMINT | 8 | 8 | 2 ICLK |
| 0008 2054h | DMAC1 | DMA address mode register | DMAMD | 16 | 16 | 2 ICLK |
| 0008 205Ch | DMAC1 | MA transfer enable register | DMCNT | 8 | 8 | 2 ICLK |
| 0008 205Dh | DMAC1 | DMA software start register | DMREQ | 8 | 8 | 2 ICLK |
| 0008 205Eh | DMAC1 | DMA status register | DMSTS | 8 | 8 | 2 ICLK |
| 0008 205Fh | DMAC1 | DMA activation source flag control register | DMCSL | 8 | 8 | 2 ICLK |
| 0008 2080h | DMAC2 | DMA source address register | DMSAR | 32 | 32 | 2 ICLK |
| 0008 2084h | DMAC2 | DMA destination address register | DMDAR | 32 | 32 | 2 ICLK |
| 0008 2088h | DMAC2 | DMA transfer count register | DMCRA | 32 | 32 | 2 ICLK |

**Table 4.1 List of I/O Registers (Address Order) (2 / 36)**

| Address | Module Abbreviation | Register Name | Register Abbreviation | Number of Bits | Access Size | Number of Access Cycles |
|---|---|---|---|---|---|---|
| 0008 208Ch | DMAC2 | DMA block transfer count register | DMCRB | 16 | 16 | 2 ICLK |
| 0008 2090h | DMAC2 | DMA transfer mode register | DMTMD | 16 | 16 | 2 ICLK |
| 0008 2093h | DMAC2 | DMA interrupt setting register | DMINT | 8 | 8 | 2 ICLK |
| 0008 2094h | DMAC2 | DMA address mode register | DMAMD | 16 | 16 | 2 ICLK |
| 0008 209Ch | DMAC2 | DMA transfer enable register | DMCNT | 8 | 8 | 2 ICLK |
| 0008 209Dh | DMAC2 | DMA software start register | DMREQ | 8 | 8 | 2 ICLK |
| 0008 209Eh | DMAC2 | DMA status register | DMSTS | 8 | 8 | 2 ICLK |
| 0008 209Fh | DMAC2 | DMA activation source flag control register | DMCSL | 8 | 8 | 2 ICLK |
| 0008 20C0h | DMAC3 | DMA source address register | DMSAR | 32 | 32 | 2 ICLK |
| 0008 20C4h | DMAC3 | DMA destination address register | DMDAR | 32 | 32 | 2 ICLK |
| 0008 20C8h | DMAC3 | DMA transfer count register | DMCRA | 32 | 32 | 2 ICLK |
| 0008 20CCh | DMAC3 | DMA block transfer count register | DMCRB | 16 | 16 | 2 ICLK |
| 0008 20D0h | DMAC3 | DMA transfer mode register | DMTMD | 16 | 16 | 2 ICLK |
| 0008 20D3h | DMAC3 | DMA interrupt setting register | DMINT | 8 | 8 | 2 ICLK |
| 0008 20D4h | DMAC3 | DMA address mode register | DMAMD | 16 | 16 | 2 ICLK |
| 0008 20DCh | DMAC3 | DMA transfer enable register | DMCNT | 8 | 8 | 2 ICLK |
| 0008 20DDh | DMAC3 | DMA software start register | DMREQ | 8 | 8 | 2 ICLK |
| 0008 20DEh | DMAC3 | DMA status register | DMSTS | 8 | 8 | 2 ICLK |
| 0008 20DFh | DMAC3 | DMA activation source flag control register | DMCSL | 8 | 8 | 2 ICLK |
| 0008 2200h | DMAC | DMACA start register | DMAST | 8 | 8 | 2 ICLK |
| 0008 2400h | DTC | DTC control register | DTCCR | 8 | 8 | 2 ICLK |
| 0008 2404h | DTC | DTC vector base register | DTCVBR | 32 | 32 | 2 ICLK |
| 0008 2408h | DTC | DTC address mode register | DTCADMOD | 8 | 8 | 2 ICLK |
| 0008 240Ch | DTC | DTC module start register | DTCST | 8 | 8 | 2 ICLK |
| 0008 240Eh | DTC | DTC status register | DTCSTS | 16 | 16 | 2 ICLK |
| 0008 2800h | EXDMAC0 | EXDMA source address register | EDMSAR | 32 | 32 | 1 to 2 BCLK*8 |
| 0008 2804h | EXDMAC0 | EXDMA destination address register | EDMDAR | 32 | 32 | 1 to 2 BCLK*8 |
| 0008 2808h | EXDMAC0 | EXDMA transfer count register | EDMCRA | 32 | 32 | 1 to 2 BCLK*8 |
| 0008 280Ch | EXDMAC0 | EXDMA block transfer count register | EDMCRB | 16 | 16 | 1 to 2 BCLK*8 |
| 0008 2810h | EXDMAC0 | EXDMA transfer mode register | EDMTMD | 16 | 16 | 1 to 2 BCLK*8 |
| 0008 2812h | EXDMAC0 | EXDMA output setting register | EDMOMD | 8 | 8 | 1 to 2 BCLK*8 |
| 0008 2813h | EXDMAC0 | EXDMA interrupt setting register | EDMINT | 8 | 8 | 1 to 2 BCLK*8 |
| 0008 2814h | EXDMAC0 | EXDMA address mode register | EDMAMD | 32 | 32 | 1 to 2 BCLK*8 |
| 0008 2818h | EXDMAC0 | EXDMA output setting register | EDMOFR | 32 | 32 | 1 to 2 BCLK*8 |
| 0008 281Ch | EXDMAC0 | EXDMA transfer enable register | EDMCNT | 8 | 8 | 1 to 2 BCLK*8 |
| 0008 281Dh | EXDMAC0 | EXDMA software start register | EDMREQ | 8 | 8 | 1 to 2 BCLK*8 |
| 0008 281Eh | EXDMAC0 | EXDMA status register | EDMSTS | 8 | 8 | 1 to 2 BCLK*8 |
| 0008 2820h | EXDMAC0 | EXDMA external request sense mode register | EDMRMD | 8 | 8 | 1 to 2 BCLK*8 |
| 0008 2821h | EXDMAC0 | EXDMA external request flag register | EDMERF | 8 | 8 | 1 to 2 BCLK*8 |
| 0008 2822h | EXDMAC0 | EXDMA peripheral request flag register | EDMPRF | 8 | 8 | 1 to 2 BCLK*8 |
| 0008 2840h | EXDMAC1 | EXDMA source address register | EDMSAR | 32 | 32 | 1 to 2 BCLK*8 |
| 0008 2844h | EXDMAC1 | EXDMA destination address register | EDMDAR | 32 | 32 | 1 to 2 BCLK*8 |
| 0008 2848h | EXDMAC1 | EXDMA transfer count register | EDMCRA | 32 | 32 | 1 to 2 BCLK*8 |

**Table 4.1 List of I/O Registers (Address Order) (3 / 36)**

| Address | Module Abbreviation | Register Name | Register Abbreviation | Number of Bits | Access Size | Number of Access Cycles |
|---|---|---|---|---|---|---|
| 0008 284Ch | EXDMAC1 | EXDMA block transfer count register | EDMCRB | 16 | 16 | 1 to 2 BCLK*8 |
| 0008 2850h | EXDMAC1 | EXDMA transfer mode register | EDMTMD | 16 | 16 | 1 to 2 BCLK*8 |
| 0008 2852h | EXDMAC1 | EXDMA output setting register | EDMOMD | 8 | 8 | 1 to 2 BCLK*8 |
| 0008 2853h | EXDMAC1 | EXDMA interrupt setting register | EDMINT | 8 | 8 | 1 to 2 BCLK*8 |
| 0008 2854h | EXDMAC1 | EXDMA address mode register | EDMAMD | 32 | 32 | 1 to 2 BCLK*8 |
| 0008 285Ch | EXDMAC1 | EXDMA transfer enable register | EDMCNT | 8 | 8 | 1 to 2 BCLK*8 |
| 0008 285Dh | EXDMAC1 | EXDMA software start register | EDMREQ | 8 | 8 | 1 to 2 BCLK*8 |
| 0008 285Eh | EXDMAC1 | EXDMA status register | EDMSTS | 8 | 8 | 1 to 2 BCLK*8 |
| 0008 2860h | EXDMAC1 | EXDMA external request sense mode register | EDMRMD | 8 | 8 | 1 to 2 BCLK*8 |
| 0008 2861h | EXDMAC1 | EXDMA external request flag register | EDMERF | 8 | 8 | 1 to 2 BCLK*8 |
| 0008 2862h | EXDMAC1 | EXDMA peripheral request flag register | EDMPRF | 8 | 8 | 1 to 2 BCLK*8 |
| 0008 2A00h | EXDMAC | EXDMA module start register | EDMAST | 8 | 8 | 1 to 2 BCLK*8 |
| 0008 2BE0h | EXDMAC | Cluster buffer register 0 | CLSBR0 | 32 | 32 | 1 to 2 BCLK*8 |
| 0008 2BE4h | EXDMAC | Cluster buffer register 1 | CLSBR1 | 32 | 32 | 1 to 2 BCLK*8 |
| 0008 2BE8h | EXDMAC | Cluster buffer register 2 | CLSBR2 | 32 | 32 | 1 to 2 BCLK*8 |
| 0008 2BECh | EXDMAC | Cluster buffer register 3 | CLSBR3 | 32 | 32 | 1 to 2 BCLK*8 |
| 0008 2BF0h | EXDMAC | Cluster buffer register 4 | CLSBR4 | 32 | 32 | 1 to 2 BCLK*8 |
| 0008 2BF4h | EXDMAC | Cluster buffer register 5 | CLSBR5 | 32 | 32 | 1 to 2 BCLK*8 |
| 0008 2BF8h | EXDMAC | Cluster buffer register 6 | CLSBR6 | 32 | 32 | 1 to 2 BCLK*8 |
| 0008 3002h | BSC | CS0 mode register | CS0MOD | 16 | 16 | 1 to 2 BCLK*8 |
| 0008 3004h | BSC | CS0 wait control register 1 | CS0WCR1 | 32 | 32 | 1 to 2 BCLK*8 |
| 0008 3008h | BSC | CS0 wait control register 2 | CS0WCR2 | 32 | 32 | 1 to 2 BCLK*8 |
| 0008 3012h | BSC | CS1 mode register | CS1MOD | 16 | 16 | 1 to 2 BCLK*8 |
| 0008 3014h | BSC | CS1 wait control register 1 | CS1WCR1 | 32 | 32 | 1 to 2 BCLK*8 |
| 0008 3018h | BSC | CS1 wait control register 2 | CS1WCR2 | 32 | 32 | 1 to 2 BCLK*8 |
| 0008 3022h | BSC | CS2 mode register | CS2MOD | 16 | 16 | 1 to 2 BCLK*8 |
| 0008 3024h | BSC | CS2 wait control register 1 | CS2WCR1 | 32 | 32 | 1 to 2 BCLK*8 |
| 0008 3028h | BSC | CS2 wait control register 2 | CS2WCR2 | 32 | 32 | 1 to 2 BCLK*8 |
| 0008 3032h | BSC | CS3 mode register | CS3MOD | 16 | 16 | 1 to 2 BCLK*8 |
| 0008 3034h | BSC | CS3 wait control register 1 | CS3WCR1 | 32 | 32 | 1 to 2 BCLK*8 |
| 0008 3038h | BSC | CS3 wait control register 2 | CS3WCR2 | 32 | 32 | 1 to 2 BCLK*8 |
| 0008 3042h | BSC | CS4 mode register | CS4MOD | 16 | 16 | 1 to 2 BCLK*8 |
| 0008 3044h | BSC | CS4 wait control register 1 | CS4WCR1 | 32 | 32 | 1 to 2 BCLK*8 |
| 0008 3048h | BSC | CS4 wait control register 2 | CS4WCR2 | 32 | 32 | 1 to 2 BCLK*8 |
| 0008 3052h | BSC | CS5 mode register | CS5MOD | 16 | 16 | 1 to 2 BCLK*8 |
| 0008 3054h | BSC | CS5 wait control register 1 | CS5WCR1 | 32 | 32 | 1 to 2 BCLK*8 |
| 0008 3058h | BSC | CS5 wait control register 2 | CS5WCR2 | 32 | 32 | 1 to 2 BCLK*8 |
| 0008 3062h | BSC | CS6 mode register | CS6MOD | 16 | 16 | 1 to 2 BCLK*8 |
| 0008 3064h | BSC | CS6 wait control register 1 | CS6WCR1 | 32 | 32 | 1 to 2 BCLK*8 |
| 0008 3068h | BSC | CS6 wait control register 2 | CS6WCR2 | 32 | 32 | 1 to 2 BCLK*8 |
| 0008 3072h | BSC | CS7 mode register | CS7MOD | 16 | 16 | 1 to 2 BCLK*8 |
| 0008 3074h | BSC | CS7 wait control register 1 | CS7WCR1 | 32 | 32 | 1 to 2 BCLK*8 |
| 0008 3078h | BSC | CS7 wait control register 2 | CS7WCR2 | 32 | 32 | 1 to 2 BCLK*8 |
| 0008 3802h | BSC | CS0 control register | CS0CR | 16 | 16 | 1 to 2 BCLK*8 |

**Table 4.1 List of I/O Registers (Address Order) (4 / 36)**

| Address | Module Abbreviation | Register Name | Register Abbreviation | Number of Bits | Access Size | Number of Access Cycles |
|---|---|---|---|---|---|---|
| 0008 380Ah | BSC | CS0 recovery cycle register | CS0REC | 16 | 16 | 1 to 2 BCLK*8 |
| 0008 3812h | BSC | CS1 control register | CS1CR | 16 | 16 | 1 to 2 BCLK*8 |
| 0008 381Ah | BSC | CS1 recovery cycle register | CS1REC | 16 | 16 | 1 to 2 BCLK*8 |
| 0008 3822h | BSC | CS2 control register | CS2CR | 16 | 16 | 1 to 2 BCLK*8 |
| 0008 382Ah | BSC | CS2 recovery cycle register | CS2REC | 16 | 16 | 1 to 2 BCLK*8 |
| 0008 3832h | BSC | CS3 control register | CS3CR | 16 | 16 | 1 to 2 BCLK*8 |
| 0008 383Ah | BSC | CS3 recovery cycle register | CS3REC | 16 | 16 | 1 to 2 BCLK*8 |
| 0008 3842h | BSC | CS4 control register | CS4CR | 16 | 16 | 1 to 2 BCLK*8 |
| 0008 384Ah | BSC | CS4 recovery cycle register | CS4REC | 16 | 16 | 1 to 2 BCLK*8 |
| 0008 3852h | BSC | CS5 control register | CS5CR | 16 | 16 | 1 to 2 BCLK*8 |
| 0008 385Ah | BSC | CS5 recovery cycle register | CS5REC | 16 | 16 | 1 to 2 BCLK*8 |
| 0008 3862h | BSC | CS6 control register | CS6CR | 16 | 16 | 1 to 2 BCLK*8 |
| 0008 386Ah | BSC | CS6 recovery cycle register | CS6REC | 16 | 16 | 1 to 2 BCLK*8 |
| 0008 3872h | BSC | CS7 control register | CS7CR | 16 | 16 | 1 to 2 BCLK*8 |
| 0008 387Ah | BSC | CS7 recovery cycle register | CS7REC | 16 | 16 | 1 to 2 BCLK*8 |
| 0008 3C00h | BSC | SDC control register | SDCCR | 8 | 8 | 1 to 2 BCLK*8 |
| 0008 3C01h | BSC | SDC mode register | SDCMOD | 8 | 8 | 1 to 2 BCLK*8 |
| 0008 3C02h | BSC | SDRAM access mode register | SDAMOD | 8 | 8 | 1 to 2 BCLK*8 |
| 0008 3C10h | BSC | SDRAM self-refresh control register | SDSELF | 8 | 8 | 1 to 2 BCLK*8 |
| 0008 3C14h | BSC | SDRAM refresh control register | SDRFCR | 16 | 16 | 1 to 2 BCLK*8 |
| 0008 3C16h | BSC | SDRAM auto-refresh control register | SDRFEN | 8 | 8 | 1 to 2 BCLK*8 |
| 0008 3C20h | BSC | SDRAM initialization sequence control register | SDICR | 8 | 8 | 1 to 2 BCLK*8 |
| 0008 3C24h | BSC | SDRAM initialization register | SDIR | 16 | 16 | 1 to 2 BCLK*8 |
| 0008 3C40h | BSC | SDRAM address register | SDADR | 8 | 8 | 1 to 2 BCLK*8 |
| 0008 3C44h | BSC | SDRAM timing register | SDTR | 32 | 32 | 1 to 2 BCLK*8 |
| 0008 3C48h | BSC | SDRAM mode register | SDMOD | 16 | 16 | 1 to 2 BCLK*8 |
| 0008 3C50h | BSC | SDRAM status register | SDSR | 8 | 8 | 1 to 2 BCLK*8 |
| 0008 6400h | MPU | Region 0 start page-number register | RSPAGE0 | 32 | 32 | 1 ICLK |
| 0008 6404h | MPU | Region 0 end page-number register | REPAGE0 | 32 | 32 | 1 ICLK |
| 0008 6408h | MPU | Region 1 start page-number register | RSPAGE1 | 32 | 32 | 1 ICLK |
| 0008 640Ch | MPU | Region 1 end page-number register | REPAGE1 | 32 | 32 | 1 ICLK |
| 0008 6410h | MPU | Region 2 start page-number register | RSPAGE2 | 32 | 32 | 1 ICLK |
| 0008 6414h | MPU | Region 2 end page-number register | REPAGE2 | 32 | 32 | 1 ICLK |
| 0008 6418h | MPU | Region 3 start page-number register | RSPAGE3 | 32 | 32 | 1 ICLK |
| 0008 641Ch | MPU | Region 3 end page-number register | REPAGE3 | 32 | 32 | 1 ICLK |
| 0008 6420h | MPU | Region 4 start page-number register | RSPAGE4 | 32 | 32 | 1 ICLK |
| 0008 6424h | MPU | Region 4 end page-number register | REPAGE4 | 32 | 32 | 1 ICLK |
| 0008 6428h | MPU | Region 5 start page-number register | RSPAGE5 | 32 | 32 | 1 ICLK |
| 0008 642Ch | MPU | Region 5 end page-number register | REPAGE5 | 32 | 32 | 1 ICLK |
| 0008 6430h | MPU | Region 6 start page-number register | RSPAGE6 | 32 | 32 | 1 ICLK |
| 0008 6434h | MPU | Region 6 end page-number register | REPAGE6 | 32 | 32 | 1 ICLK |
| 0008 6438h | MPU | Region 7 start page-number register | RSPAGE7 | 32 | 32 | 1 ICLK |
| 0008 643Ch | MPU | Region 7 end page-number register | REPAGE7 | 32 | 32 | 1 ICLK |
| 0008 6500h | MPU | Memory-protection enable register | MPEN | 32 | 32 | 1 ICLK |

**Table 4.1 List of I/O Registers (Address Order) (5 / 36)**

| Address | Module Abbreviation | Register Name | Register Abbreviation | Number of Bits | Access Size | Number of Access Cycles |
|---|---|---|---|---|---|---|
| 0008 6504h | MPU | Background access control register | MPBAC | 32 | 32 | 1 ICLK |
| 0008 6508h | MPU | Memory-protection error status-clearing register | MPECLR | 32 | 32 | 1 ICLK |
| 0008 650Ch | MPU | Memory-protection error status register | MPESTS | 32 | 32 | 1 ICLK |
| 0008 6514h | MPU | Data memory-protection error address register | MPDEA | 32 | 32 | 1 ICLK |
| 0008 6520h | MPU | Region search address register | MPSA | 32 | 32 | 1 ICLK |
| 0008 6524h | MPU | Region search operation register | MPOPS | 16 | 16 | 1 ICLK |
| 0008 6526h | MPU | Region invalidation operation register | MPOPI | 16 | 16 | 1 ICLK |
| 0008 6528h | MPU | Instruction-hit region register | MHITI | 32 | 32 | 1 ICLK |
| 0008 652Ch | MPU | Data-hit region register | MHITD | 32 | 32 | 1 ICLK |
| 0008 7010h | ICU | Interrupt request register 016 | IR016 | 8 | 8 | 2 ICLK |
| 0008 7015h | ICU | Interrupt request register 021 | IR021 | 8 | 8 | 2 ICLK |
| 0008 7017h | ICU | Interrupt request register 023 | IR023 | 8 | 8 | 2 ICLK |
| 0008 701Bh | ICU | Interrupt request register 027 | IR027 | 8 | 8 | 2 ICLK |
| 0008 701Ch | ICU | Interrupt request register 028 | IR028 | 8 | 8 | 2 ICLK |
| 0008 701Dh | ICU | Interrupt request register 029 | IR029 | 8 | 8 | 2 ICLK |
| 0008 701Eh | ICU | Interrupt request register 030 | IR030 | 8 | 8 | 2 ICLK |
| 0008 701Fh | ICU | Interrupt request register 031 | IR031 | 8 | 8 | 2 ICLK |
| 0008 7020h | ICU | Interrupt request register 032 | IR032 | 8 | 8 | 2 ICLK |
| 0008 7024h | ICU | Interrupt request register 036 | IR036 | 8 | 8 | 2 ICLK |
| 0008 7025h | ICU | Interrupt request register 037 | IR037 | 8 | 8 | 2 ICLK |
| 0008 7026h | ICU | Interrupt request register 038 | IR038 | 8 | 8 | 2 ICLK |
| 0008 7028h | ICU | Interrupt request register 040 | IR040 | 8 | 8 | 2 ICLK |
| 0008 7029h | ICU | Interrupt request register 041 | IR041 | 8 | 8 | 2 ICLK |
| 0008 702Ah | ICU | Interrupt request register 042 | IR042 | 8 | 8 | 2 ICLK |
| 0008 702Ch | ICU | Interrupt request register 044 | IR044 | 8 | 8 | 2 ICLK |
| 0008 702Dh | ICU | Interrupt request register 045 | IR045 | 8 | 8 | 2 ICLK |
| 0008 702Eh | ICU | Interrupt request register 046 | IR046 | 8 | 8 | 2 ICLK |
| 0008 702Fh | ICU | Interrupt request register 047 | IR047 | 8 | 8 | 2 ICLK |
| 0008 7030h | ICU | Interrupt request register 048 | IR048 | 8 | 8 | 2 ICLK |
| 0008 7031h | ICU | Interrupt request register 049 | IR049 | 8 | 8 | 2 ICLK |
| 0008 7032h | ICU | Interrupt request register 050 | IR050 | 8 | 8 | 2 ICLK |
| 0008 7033h | ICU | Interrupt request register 051 | IR051 | 8 | 8 | 2 ICLK |
| 0008 7038h | ICU | Interrupt request register 056 | IR056 | 8 | 8 | 2 ICLK |
| 0008 7039h | ICU | Interrupt request register 057 | IR057 | 8 | 8 | 2 ICLK |
| 0008 703Ah | ICU | Interrupt request register 058 | IR058 | 8 | 8 | 2 ICLK |
| 0008 703Bh | ICU | Interrupt request register 059 | IR059 | 8 | 8 | 2 ICLK |
| 0008 703Ch | ICU | Interrupt request register 060 | IR060 | 8 | 8 | 2 ICLK |
| 0008 703Eh | ICU | Interrupt request register 062 | IR062 | 8 | 8 | 2 ICLK |
| 0008 703Fh | ICU | Interrupt request register 063 | IR063 | 8 | 8 | 2 ICLK |
| 0008 7040h | ICU | Interrupt request register 064 | IR064 | 8 | 8 | 2 ICLK |
| 0008 7041h | ICU | Interrupt request register 065 | IR065 | 8 | 8 | 2 ICLK |
| 0008 7042h | ICU | Interrupt request register 066 | IR066 | 8 | 8 | 2 ICLK |
| 0008 7043h | ICU | Interrupt request register 067 | IR067 | 8 | 8 | 2 ICLK |

**Table 4.1 List of I/O Registers (Address Order) (6 / 36)**

| Address | Module Abbreviation | Register Name | Register Abbreviation | Number of Bits | Access Size | Number of Access Cycles |
|---|---|---|---|---|---|---|
| 0008 7044h | ICU | Interrupt request register 068 | IR068 | 8 | 8 | 2 ICLK |
| 0008 7045h | ICU | Interrupt request register 069 | IR069 | 8 | 8 | 2 ICLK |
| 0008 7046h | ICU | Interrupt request register 070 | IR070 | 8 | 8 | 2 ICLK |
| 0008 7047h | ICU | Interrupt request register 071 | IR071 | 8 | 8 | 2 ICLK |
| 0008 7048h | ICU | Interrupt request register 072 | IR072 | 8 | 8 | 2 ICLK |
| 0008 7049h | ICU | Interrupt request register 073 | IR073 | 8 | 8 | 2 ICLK |
| 0008 704Ah | ICU | Interrupt request register 074 | IR074 | 8 | 8 | 2 ICLK |
| 0008 704Bh | ICU | Interrupt request register 075 | IR075 | 8 | 8 | 2 ICLK |
| 0008 704Ch | ICU | Interrupt request register 076 | IR076 | 8 | 8 | 2 ICLK |
| 0008 704Dh | ICU | Interrupt request register 077 | IR077 | 8 | 8 | 2 ICLK |
| 0008 704Eh | ICU | Interrupt request register 078 | IR078 | 8 | 8 | 2 ICLK |
| 0008 704Fh | ICU | Interrupt request register 079 | IR079 | 8 | 8 | 2 ICLK |
| 0008 705Ah | ICU | Interrupt request register 090 | IR090 | 8 | 8 | 2 ICLK |
| 0008 705Bh | ICU | Interrupt request register 091 | IR091 | 8 | 8 | 2 ICLK |
| 0008 705Ch | ICU | Interrupt request register 092 | IR092 | 8 | 8 | 2 ICLK |
| 0008 7060h | ICU | Interrupt request register 096 | IR096 | 8 | 8 | 2 ICLK |
| 0008 7062h | ICU | Interrupt request register 098 | IR098 | 8 | 8 | 2 ICLK |
| 0008 7063h | ICU | Interrupt request register 099 | IR099 | 8 | 8 | 2 ICLK |
| 0008 7066h | ICU | Interrupt request register 102 | IR102 | 8 | 8 | 2 ICLK |
| 0008 7072h | ICU | Interrupt request register 114 | IR114 | 8 | 8 | 2 ICLK |
| 0008 7073h | ICU | Interrupt request register 115 | IR115 | 8 | 8 | 2 ICLK |
| 0008 7074h | ICU | Interrupt request register 116 | IR116 | 8 | 8 | 2 ICLK |
| 0008 7075h | ICU | Interrupt request register 117 | IR117 | 8 | 8 | 2 ICLK |
| 0008 7076h | ICU | Interrupt request register 118 | IR118 | 8 | 8 | 2 ICLK |
| 0008 7077h | ICU | Interrupt request register 119 | IR119 | 8 | 8 | 2 ICLK |
| 0008 7078h | ICU | Interrupt request register 120 | IR120 | 8 | 8 | 2 ICLK |
| 0008 7079h | ICU | Interrupt request register 121 | IR121 | 8 | 8 | 2 ICLK |
| 0008 707Ah | ICU | Interrupt request register 122 | IR122 | 8 | 8 | 2 ICLK |
| 0008 707Bh | ICU | Interrupt request register 123 | IR123 | 8 | 8 | 2 ICLK |
| 0008 707Ch | ICU | Interrupt request register 124 | IR124 | 8 | 8 | 2 ICLK |
| 0008 707Dh | ICU | Interrupt request register 125 | IR125 | 8 | 8 | 2 ICLK |
| 0008 707Eh | ICU | Interrupt request register 126 | IR126 | 8 | 8 | 2 ICLK |
| 0008 707Fh | ICU | Interrupt request register 127 | IR127 | 8 | 8 | 2 ICLK |
| 0008 7080h | ICU | Interrupt request register 128 | IR128 | 8 | 8 | 2 ICLK |
| 0008 7081h | ICU | Interrupt request register 129 | IR129 | 8 | 8 | 2 ICLK |
| 0008 7082h | ICU | Interrupt request register 130 | IR130 | 8 | 8 | 2 ICLK |
| 0008 7083h | ICU | Interrupt request register 131 | IR131 | 8 | 8 | 2 ICLK |
| 0008 7084h | ICU | Interrupt request register 132 | IR132 | 8 | 8 | 2 ICLK |
| 0008 7085h | ICU | Interrupt request register 133 | IR133 | 8 | 8 | 2 ICLK |
| 0008 7086h | ICU | Interrupt request register 134 | IR134 | 8 | 8 | 2 ICLK |
| 0008 7087h | ICU | Interrupt request register 135 | IR135 | 8 | 8 | 2 ICLK |
| 0008 7088h | ICU | Interrupt request register 136 | IR136 | 8 | 8 | 2 ICLK |
| 0008 7089h | ICU | Interrupt request register 137 | IR137 | 8 | 8 | 2 ICLK |
| 0008 708Ah | ICU | Interrupt request register 138 | IR138 | 8 | 8 | 2 ICLK |
| 0008 708Bh | ICU | Interrupt request register 139 | IR139 | 8 | 8 | 2 ICLK |

**Table 4.1 List of I/O Registers (Address Order) (7 / 36)**

| Address | Module Abbreviation | Register Name | Register Abbreviation | Number of Bits | Access Size | Number of Access Cycles |
|---|---|---|---|---|---|---|
| 0008 708Ch | ICU | Interrupt request register 140 | IR140 | 8 | 8 | 2 ICLK |
| 0008 708Dh | ICU | Interrupt request register 141 | IR141 | 8 | 8 | 2 ICLK |
| 0008 708Eh | ICU | Interrupt request register 142 | IR142 | 8 | 8 | 2 ICLK |
| 0008 708Fh | ICU | Interrupt request register 143 | IR143 | 8 | 8 | 2 ICLK |
| 0008 7090h | ICU | Interrupt request register 144 | IR144 | 8 | 8 | 2 ICLK |
| 0008 7091h | ICU | Interrupt request register 145 | IR145 | 8 | 8 | 2 ICLK |
| 0008 7092h | ICU | Interrupt request register 146 | IR146 | 8 | 8 | 2 ICLK |
| 0008 7093h | ICU | Interrupt request register 147 | IR147 | 8 | 8 | 2 ICLK |
| 0008 7094h | ICU | Interrupt request register 148 | IR148 | 8 | 8 | 2 ICLK |
| 0008 7095h | ICU | Interrupt request register 149 | IR149 | 8 | 8 | 2 ICLK |
| 0008 7096h | ICU | Interrupt request register 150 | IR150 | 8 | 8 | 2 ICLK |
| 0008 7097h | ICU | Interrupt request register 151 | IR151 | 8 | 8 | 2 ICLK |
| 0008 7098h | ICU | Interrupt request register 152 | IR152 | 8 | 8 | 2 ICLK |
| 0008 7099h | ICU | Interrupt request register 153 | IR153 | 8 | 8 | 2 ICLK |
| 0008 709Ah | ICU | Interrupt request register 154 | IR154 | 8 | 8 | 2 ICLK |
| 0008 709Bh | ICU | Interrupt request register 155 | IR155 | 8 | 8 | 2 ICLK |
| 0008 709Ch | ICU | Interrupt request register 156 | IR156 | 8 | 8 | 2 ICLK |
| 0008 709Dh | ICU | Interrupt request register 157 | IR157 | 8 | 8 | 2 ICLK |
| 0008 709Eh | ICU | Interrupt request register 158 | IR158 | 8 | 8 | 2 ICLK |
| 0008 709Fh | ICU | Interrupt request register 159 | IR159 | 8 | 8 | 2 ICLK |
| 0008 70A0h | ICU | Interrupt request register 160 | IR160 | 8 | 8 | 2 ICLK |
| 0008 70A1h | ICU | Interrupt request register 161 | IR161 | 8 | 8 | 2 ICLK |
| 0008 70A2h | ICU | Interrupt request register 162 | IR162 | 8 | 8 | 2 ICLK |
| 0008 70A3h | ICU | Interrupt request register 163 | IR163 | 8 | 8 | 2 ICLK |
| 0008 70A4h | ICU | Interrupt request register 164 | IR164 | 8 | 8 | 2 ICLK |
| 0008 70A5h | ICU | Interrupt request register 165 | IR165 | 8 | 8 | 2 ICLK |
| 0008 70A6h | ICU | Interrupt request register 166 | IR166 | 8 | 8 | 2 ICLK |
| 0008 70A7h | ICU | Interrupt request register 167 | IR167 | 8 | 8 | 2 ICLK |
| 0008 70A8h | ICU | Interrupt request register 168 | IR168 | 8 | 8 | 2 ICLK |
| 0008 70A9h | ICU | Interrupt request register 169 | IR169 | 8 | 8 | 2 ICLK |
| 0008 70AAh | ICU | Interrupt request register 170 | IR170 | 8 | 8 | 2 ICLK |
| 0008 70ABh | ICU | Interrupt request register 171 | IR171 | 8 | 8 | 2 ICLK |
| 0008 70ACh | ICU | Interrupt request register 172 | IR172 | 8 | 8 | 2 ICLK |
| 0008 70ADh | ICU | Interrupt request register 173 | IR173 | 8 | 8 | 2 ICLK |
| 0008 70AEh | ICU | Interrupt request register 174 | IR174 | 8 | 8 | 2 ICLK |
| 0008 70AFh | ICU | Interrupt request register 175 | IR175 | 8 | 8 | 2 ICLK |
| 0008 70B0h | ICU | Interrupt request register 176 | IR176 | 8 | 8 | 2 ICLK |
| 0008 70B1h | ICU | Interrupt request register 177 | IR177 | 8 | 8 | 2 ICLK |
| 0008 70B2h | ICU | Interrupt request register 178 | IR178 | 8 | 8 | 2 ICLK |
| 0008 70B3h | ICU | Interrupt request register 179 | IR179 | 8 | 8 | 2 ICLK |
| 0008 70B4h | ICU | Interrupt request register 180 | IR180 | 8 | 8 | 2 ICLK |
| 0008 70B5h | ICU | Interrupt request register 181 | IR181 | 8 | 8 | 2 ICLK |
| 0008 70B6h | ICU | Interrupt request register 182 | IR182 | 8 | 8 | 2 ICLK |
| 0008 70B7h | ICU | Interrupt request register 183 | IR183 | 8 | 8 | 2 ICLK |
| 0008 70B8h | ICU | Interrupt request register 184 | IR184 | 8 | 8 | 2 ICLK |

**Table 4.1 List of I/O Registers (Address Order) (8 / 36)**

| Address | Module Abbreviation | Register Name | Register Abbreviation | Number of Bits | Access Size | Number of Access Cycles |
|---|---|---|---|---|---|---|
| 0008 70B9h | ICU | Interrupt request register 185 | IR185 | 8 | 8 | 2 ICLK |
| 0008 70C6h | ICU | Interrupt request register 198 | IR198 | 8 | 8 | 2 ICLK |
| 0008 70C7h | ICU | Interrupt request register 199 | IR199 | 8 | 8 | 2 ICLK |
| 0008 70C8h | ICU | Interrupt request register 200 | IR200 | 8 | 8 | 2 ICLK |
| 0008 70C9h | ICU | Interrupt request register 201 | IR201 | 8 | 8 | 2 ICLK |
| 0008 70CAh | ICU | Interrupt request register 202 | IR202 | 8 | 8 | 2 ICLK |
| 0008 70CBh | ICU | Interrupt request register 203 | IR203 | 8 | 8 | 2 ICLK |
| 0008 70D6h | ICU | Interrupt request register 214 | IR214 | 8 | 8 | 2 ICLK |
| 0008 70D7h | ICU | Interrupt request register 215 | IR215 | 8 | 8 | 2 ICLK |
| 0008 70D8h | ICU | Interrupt request register 216 | IR216 | 8 | 8 | 2 ICLK |
| 0008 70D9h | ICU | Interrupt request register 217 | IR217 | 8 | 8 | 2 ICLK |
| 0008 70DAh | ICU | Interrupt request register 218 | IR218 | 8 | 8 | 2 ICLK |
| 0008 70DBh | ICU | Interrupt request register 219 | IR219 | 8 | 8 | 2 ICLK |
| 0008 70DCh | ICU | Interrupt request register 220 | IR220 | 8 | 8 | 2 ICLK |
| 0008 70DDh | ICU | Interrupt request register 221 | IR221 | 8 | 8 | 2 ICLK |
| 0008 70DEh | ICU | Interrupt request register 222 | IR222 | 8 | 8 | 2 ICLK |
| 0008 70DFh | ICU | Interrupt request register 223 | IR223 | 8 | 8 | 2 ICLK |
| 0008 70E0h | ICU | Interrupt request register 224 | IR224 | 8 | 8 | 2 ICLK |
| 0008 70E1h | ICU | Interrupt request register 225 | IR225 | 8 | 8 | 2 ICLK |
| 0008 70E2h | ICU | Interrupt request register 226 | IR226 | 8 | 8 | 2 ICLK |
| 0008 70E3h | ICU | Interrupt request register 227 | IR227 | 8 | 8 | 2 ICLK |
| 0008 70E4h | ICU | Interrupt request register 228 | IR228 | 8 | 8 | 2 ICLK |
| 0008 70E5h | ICU | Interrupt request register 229 | IR229 | 8 | 8 | 2 ICLK |
| 0008 70EAh | ICU | Interrupt request register 234 | IR234 | 8 | 8 | 2 ICLK |
| 0008 70EBh | ICU | Interrupt request register 235 | IR235 | 8 | 8 | 2 ICLK |
| 0008 70ECh | ICU | Interrupt request register 236 | IR236 | 8 | 8 | 2 ICLK |
| 0008 70EDh | ICU | Interrupt request register 237 | IR237 | 8 | 8 | 2 ICLK |
| 0008 70EEh | ICU | Interrupt request register 238 | IR238 | 8 | 8 | 2 ICLK |
| 0008 70EFh | ICU | Interrupt request register 239 | IR239 | 8 | 8 | 2 ICLK |
| 0008 70F0h | ICU | Interrupt request register 240 | IR240 | 8 | 8 | 2 ICLK |
| 0008 70F1h | ICU | Interrupt request register 241 | IR241 | 8 | 8 | 2 ICLK |
| 0008 70F6h | ICU | Interrupt request register 246 | IR246 | 8 | 8 | 2 ICLK |
| 0008 70F7h | ICU | Interrupt request register 247 | IR247 | 8 | 8 | 2 ICLK |
| 0008 70F8h | ICU | Interrupt request register 248 | IR248 | 8 | 8 | 2 ICLK |
| 0008 70F9h | ICU | Interrupt request register 249 | IR249 | 8 | 8 | 2 ICLK |
| 0008 70FAh | ICU | Interrupt request register 250 | IR250 | 8 | 8 | 2 ICLK |
| 0008 70FBh | ICU | Interrupt request register 251 | IR251 | 8 | 8 | 2 ICLK |
| 0008 70FCh | ICU | Interrupt request register 252 | IR252 | 8 | 8 | 2 ICLK |
| 0008 70FDh | ICU | Interrupt request register 253 | IR253 | 8 | 8 | 2 ICLK |
| 0008 711Bh | ICU | DTC activation enable register 027 | DTCER027 | 8 | 8 | 2 ICLK |
| 0008 711Ch | ICU | DTC activation enable register 028 | DTCER028 | 8 | 8 | 2 ICLK |
| 0008 711Dh | ICU | DTC activation enable register 029 | DTCER029 | 8 | 8 | 2 ICLK |
| 0008 711Eh | ICU | DTC activation enable register 030 | DTCER030 | 8 | 8 | 2 ICLK |
| 0008 711Fh | ICU | DTC activation enable register 031 | DTCER031 | 8 | 8 | 2 ICLK |
| 0008 7124h | ICU | DTC activation enable register 036 | DTCER036 | 8 | 8 | 2 ICLK |

**Table 4.1 List of I/O Registers (Address Order) (9 / 36)**

| Address | Module Abbreviation | Register Name | Register Abbreviation | Number of Bits | Access Size | Number of Access Cycles |
|---|---|---|---|---|---|---|
| 0008 7125h | ICU | DTC activation enable register 037 | DTCER037 | 8 | 8 | 2 ICLK |
| 0008 7128h | ICU | DTC activation enable register 040 | DTCER040 | 8 | 8 | 2 ICLK |
| 0008 7129h | ICU | DTC activation enable register 041 | DTCER041 | 8 | 8 | 2 ICLK |
| 0008 712Dh | ICU | DTC activation enable register 045 | DTCER045 | 8 | 8 | 2 ICLK |
| 0008 712Eh | ICU | DTC activation enable register 046 | DTCER046 | 8 | 8 | 2 ICLK |
| 0008 7131h | ICU | DTC activation enable register 049 | DTCER049 | 8 | 8 | 2 ICLK |
| 0008 7132h | ICU | DTC activation enable register 050 | DTCER050 | 8 | 8 | 2 ICLK |
| 0008 7140h | ICU | DTC activation enable register 064 | DTCER064 | 8 | 8 | 2 ICLK |
| 0008 7141h | ICU | DTC activation enable register 065 | DTCER065 | 8 | 8 | 2 ICLK |
| 0008 7142h | ICU | DTC activation enable register 066 | DTCER066 | 8 | 8 | 2 ICLK |
| 0008 7143h | ICU | DTC activation enable register 067 | DTCER067 | 8 | 8 | 2 ICLK |
| 0008 7144h | ICU | DTC activation enable register 068 | DTCER068 | 8 | 8 | 2 ICLK |
| 0008 7145h | ICU | DTC activation enable register 069 | DTCER069 | 8 | 8 | 2 ICLK |
| 0008 7146h | ICU | DTC activation enable register 070 | DTCER070 | 8 | 8 | 2 ICLK |
| 0008 7147h | ICU | DTC activation enable register 071 | DTCER071 | 8 | 8 | 2 ICLK |
| 0008 7148h | ICU | DTC activation enable register 072 | DTCER072 | 8 | 8 | 2 ICLK |
| 0008 7149h | ICU | DTC activation enable register 073 | DTCER073 | 8 | 8 | 2 ICLK |
| 0008 714Ah | ICU | DTC activation enable register 074 | DTCER074 | 8 | 8 | 2 ICLK |
| 0008 714Bh | ICU | DTC activation enable register 075 | DTCER075 | 8 | 8 | 2 ICLK |
| 0008 714Ch | ICU | DTC activation enable register 076 | DTCER076 | 8 | 8 | 2 ICLK |
| 0008 714Dh | ICU | DTC activation enable register 077 | DTCER077 | 8 | 8 | 2 ICLK |
| 0008 714Eh | ICU | DTC activation enable register 078 | DTCER078 | 8 | 8 | 2 ICLK |
| 0008 714Fh | ICU | DTC activation enable register 079 | DTCER079 | 8 | 8 | 2 ICLK |
| 0008 7162h | ICU | DTC activation enable register 098 | DTCER098 | 8 | 8 | 2 ICLK |
| 0008 7163h | ICU | DTC activation enable register 099 | DTCER099 | 8 | 8 | 2 ICLK |
| 0008 7166h | ICU | DTC activation enable register 102 | DTCER102 | 8 | 8 | 2 ICLK |
| 0008 7172h | ICU | DTC activation enable register 114 | DTCER114 | 8 | 8 | 2 ICLK |
| 0008 7173h | ICU | DTC activation enable register 115 | DTCER115 | 8 | 8 | 2 ICLK |
| 0008 7174h | ICU | DTC activation enable register 116 | DTCER116 | 8 | 8 | 2 ICLK |
| 0008 7175h | ICU | DTC activation enable register 117 | DTCER117 | 8 | 8 | 2 ICLK |
| 0008 7179h | ICU | DTC activation enable register 121 | DTCER121 | 8 | 8 | 2 ICLK |
| 0008 717Ah | ICU | DTC activation enable register 122 | DTCER122 | 8 | 8 | 2 ICLK |
| 0008 717Dh | ICU | DTC activation enable register 125 | DTCER125 | 8 | 8 | 2 ICLK |
| 0008 717Eh | ICU | DTC activation enable register 126 | DTCER126 | 8 | 8 | 2 ICLK |
| 0008 7181h | ICU | DTC activation enable register 129 | DTCER129 | 8 | 8 | 2 ICLK |
| 0008 7182h | ICU | DTC activation enable register 130 | DTCER130 | 8 | 8 | 2 ICLK |
| 0008 7183h | ICU | DTC activation enable register 131 | DTCER131 | 8 | 8 | 2 ICLK |
| 0008 7184h | ICU | DTC activation enable register 132 | DTCER132 | 8 | 8 | 2 ICLK |
| 0008 7186h | ICU | DTC activation enable register 134 | DTCER134 | 8 | 8 | 2 ICLK |
| 0008 7187h | ICU | DTC activation enable register 135 | DTCER135 | 8 | 8 | 2 ICLK |
| 0008 7188h | ICU | DTC activation enable register 136 | DTCER136 | 8 | 8 | 2 ICLK |
| 0008 7189h | ICU | DTC activation enable register 137 | DTCER137 | 8 | 8 | 2 ICLK |
| 0008 718Ah | ICU | DTC activation enable register 138 | DTCER138 | 8 | 8 | 2 ICLK |
| 0008 718Bh | ICU | DTC activation enable register 139 | DTCER139 | 8 | 8 | 2 ICLK |
| 0008 718Ch | ICU | DTC activation enable register 140 | DTCER140 | 8 | 8 | 2 ICLK |

**Table 4.1 List of I/O Registers (Address Order) (10 / 36)**

| Address | Module Abbreviation | Register Name | Register Abbreviation | Number of Bits | Access Size | Number of Access Cycles |
|---|---|---|---|---|---|---|
| 0008 718Dh | ICU | DTC activation enable register 141 | DTCER141 | 8 | 8 | 2 ICLK |
| 0008 718Eh | ICU | DTC activation enable register 142 | DTCER142 | 8 | 8 | 2 ICLK |
| 0008 718Fh | ICU | DTC activation enable register 143 | DTCER143 | 8 | 8 | 2 ICLK |
| 0008 7190h | ICU | DTC activation enable register 144 | DTCER144 | 8 | 8 | 2 ICLK |
| 0008 7191h | ICU | DTC activation enable register 145 | DTCER145 | 8 | 8 | 2 ICLK |
| 0008 7195h | ICU | DTC activation enable register 149 | DTCER149 | 8 | 8 | 2 ICLK |
| 0008 7196h | ICU | DTC activation enable register 150 | DTCER150 | 8 | 8 | 2 ICLK |
| 0008 7199h | ICU | DTC activation enable register 153 | DTCER153 | 8 | 8 | 2 ICLK |
| 0008 719Ah | ICU | DTC activation enable register 154 | DTCER154 | 8 | 8 | 2 ICLK |
| 0008 719Dh | ICU | DTC activation enable register 157 | DTCER157 | 8 | 8 | 2 ICLK |
| 0008 719Eh | ICU | DTC activation enable register 158 | DTCER158 | 8 | 8 | 2 ICLK |
| 0008 719Fh | ICU | DTC activation enable register 159 | DTCER159 | 8 | 8 | 2 ICLK |
| 0008 71A0h | ICU | DTC activation enable register 160 | DTCER160 | 8 | 8 | 2 ICLK |
| 0008 71A2h | ICU | DTC activation enable register 162 | DTCER162 | 8 | 8 | 2 ICLK |
| 0008 71A3h | ICU | DTC activation enable register 163 | DTCER163 | 8 | 8 | 2 ICLK |
| 0008 71A4h | ICU | DTC activation enable register 164 | DTCER164 | 8 | 8 | 2 ICLK |
| 0008 71A5h | ICU | DTC activation enable register 165 | DTCER165 | 8 | 8 | 2 ICLK |
| 0008 71A6h | ICU | DTC activation enable register 166 | DTCER166 | 8 | 8 | 2 ICLK |
| 0008 71A7h | ICU | DTC activation enable register 167 | DTCER167 | 8 | 8 | 2 ICLK |
| 0008 71A8h | ICU | DTC activation enable register 168 | DTCER168 | 8 | 8 | 2 ICLK |
| 0008 71A9h | ICU | DTC activation enable register 169 | DTCER169 | 8 | 8 | 2 ICLK |
| 0008 71AEh | ICU | DTC activation enable register 174 | DTCER174 | 8 | 8 | 2 ICLK |
| 0008 71AFh | ICU | DTC activation enable register 175 | DTCER175 | 8 | 8 | 2 ICLK |
| 0008 71B1h | ICU | DTC activation enable register 177 | DTCER177 | 8 | 8 | 2 ICLK |
| 0008 71B2h | ICU | DTC activation enable register 178 | DTCER178 | 8 | 8 | 2 ICLK |
| 0008 71B4h | ICU | DTC activation enable register 180 | DTCER180 | 8 | 8 | 2 ICLK |
| 0008 71B5h | ICU | DTC activation enable register 181 | DTCER181 | 8 | 8 | 2 ICLK |
| 0008 71B7h | ICU | DTC activation enable register 183 | DTCER183 | 8 | 8 | 2 ICLK |
| 0008 71B8h | ICU | DTC activation enable register 184 | DTCER184 | 8 | 8 | 2 ICLK |
| 0008 71C6h | ICU | DTC activation enable register 198 | DTCER198 | 8 | 8 | 2 ICLK |
| 0008 71C7h | ICU | DTC activation enable register 199 | DTCER199 | 8 | 8 | 2 ICLK |
| 0008 71C8h | ICU | DTC activation enable register 200 | DTCER200 | 8 | 8 | 2 ICLK |
| 0008 71C9h | ICU | DTC activation enable register 201 | DTCER201 | 8 | 8 | 2 ICLK |
| 0008 71CAh | ICU | DTC activation enable register 202 | DTCER202 | 8 | 8 | 2 ICLK |
| 0008 71CBh | ICU | DTC activation enable register 203 | DTCER203 | 8 | 8 | 2 ICLK |
| 0008 71D7h | ICU | DTC activation enable register 215 | DTCER215 | 8 | 8 | 2 ICLK |
| 0008 71D8h | ICU | DTC activation enable register 216 | DTCER216 | 8 | 8 | 2 ICLK |
| 0008 71DBh | ICU | DTC activation enable register 219 | DTCER219 | 8 | 8 | 2 ICLK |
| 0008 71DCh | ICU | DTC activation enable register 220 | DTCER220 | 8 | 8 | 2 ICLK |
| 0008 71DFh | ICU | DTC activation enable register 223 | DTCER223 | 8 | 8 | 2 ICLK |
| 0008 71E0h | ICU | DTC activation enable register 224 | DTCER224 | 8 | 8 | 2 ICLK |
| 0008 71E3h | ICU | DTC activation enable register 227 | DTCER227 | 8 | 8 | 2 ICLK |
| 0008 71E4h | ICU | DTC activation enable register 228 | DTCER228 | 8 | 8 | 2 ICLK |
| 0008 71EBh | ICU | DTC activation enable register 235 | DTCER235 | 8 | 8 | 2 ICLK |
| 0008 71ECh | ICU | DTC activation enable register 236 | DTCER236 | 8 | 8 | 2 ICLK |

**Table 4.1 List of I/O Registers (Address Order) (11 / 36)**

| Address | Module Abbreviation | Register Name | Register Abbreviation | Number of Bits | Access Size | Number of Access Cycles |
|---|---|---|---|---|---|---|
| 0008 71EFh | ICU | DTC activation enable register 239 | DTCER239 | 8 | 8 | 2 ICLK |
| 0008 71F0h | ICU | DTC activation enable register 240 | DTCER240 | 8 | 8 | 2 ICLK |
| 0008 71F7h | ICU | DTC activation enable register 247 | DTCER247 | 8 | 8 | 2 ICLK |
| 0008 71F8h | ICU | DTC activation enable register 248 | DTCER248 | 8 | 8 | 2 ICLK |
| 0008 71FBh | ICU | DTC activation enable register 251 | DTCER251 | 8 | 8 | 2 ICLK |
| 0008 71FCh | ICU | DTC activation enable register 252 | DTCER252 | 8 | 8 | 2 ICLK |
| 0008 7202h | ICU | Interrupt request enable register 02 | IER02 | 8 | 8 | 2 ICLK |
| 0008 7203h | ICU | Interrupt request enable register 03 | IER03 | 8 | 8 | 2 ICLK |
| 0008 7204h | ICU | Interrupt request enable register 04 | IER04 | 8 | 8 | 2 ICLK |
| 0008 7205h | ICU | Interrupt request enable register 05 | IER05 | 8 | 8 | 2 ICLK |
| 0008 7206h | ICU | Interrupt request enable register 06 | IER06 | 8 | 8 | 2 ICLK |
| 0008 7207h | ICU | Interrupt request enable register 07 | IER07 | 8 | 8 | 2 ICLK |
| 0008 7208h | ICU | Interrupt request enable register 08 | IER08 | 8 | 8 | 2 ICLK |
| 0008 7209h | ICU | Interrupt request enable register 09 | IER09 | 8 | 8 | 2 ICLK |
| 0008 720Bh | ICU | Interrupt request enable register 0B | IER0B | 8 | 8 | 2 ICLK |
| 0008 720Ch | ICU | Interrupt request enable register 0C | IER0C | 8 | 8 | 2 ICLK |
| 0008 720Eh | ICU | Interrupt request enable register 0E | IER0E | 8 | 8 | 2 ICLK |
| 0008 720Fh | ICU | Interrupt request enable register 0F | IER0F | 8 | 8 | 2 ICLK |
| 0008 7210h | ICU | Interrupt request enable register 10 | IER10 | 8 | 8 | 2 ICLK |
| 0008 7211h | ICU | Interrupt request enable register 11 | IER11 | 8 | 8 | 2 ICLK |
| 0008 7212h | ICU | Interrupt request enable register 12 | IER12 | 8 | 8 | 2 ICLK |
| 0008 7213h | ICU | Interrupt request enable register 13 | IER13 | 8 | 8 | 2 ICLK |
| 0008 7214h | ICU | Interrupt request enable register 14 | IER14 | 8 | 8 | 2 ICLK |
| 0008 7215h | ICU | Interrupt request enable register 15 | IER15 | 8 | 8 | 2 ICLK |
| 0008 7216h | ICU | Interrupt request enable register 16 | IER16 | 8 | 8 | 2 ICLK |
| 0008 7217h | ICU | Interrupt request enable register 17 | IER17 | 8 | 8 | 2 ICLK |
| 0008 7218h | ICU | Interrupt request enable register 18 | IER18 | 8 | 8 | 2 ICLK |
| 0008 7219h | ICU | Interrupt request enable register 19 | IER19 | 8 | 8 | 2 ICLK |
| 0008 721Ah | ICU | Interrupt request enable register 1A | IER1A | 8 | 8 | 2 ICLK |
| 0008 721Bh | ICU | Interrupt request enable register 1B | IER1B | 8 | 8 | 2 ICLK |
| 0008 721Ch | ICU | Interrupt request enable register 1C | IER1C | 8 | 8 | 2 ICLK |
| 0008 721Dh | ICU | Interrupt request enable register 1D | IER1D | 8 | 8 | 2 ICLK |
| 0008 721Eh | ICU | Interrupt request enable register 1E | IER1E | 8 | 8 | 2 ICLK |
| 0008 721Fh | ICU | Interrupt request enable register 1F | IER1F | 8 | 8 | 2 ICLK |
| 0008 72E0h | ICU | Software interrupt activation register | SWINTR | 8 | 8 | 2 ICLK |
| 0008 72F0h | ICU | Fast interrupt set register | FIR | 16 | 16 | 2 ICLK |
| 0008 7300h | ICU | Interrupt source priority register 00 | IPR00 | 8 | 8 | 2 ICLK |
| 0008 7301h | ICU | Interrupt source priority register 01 | IPR01 | 8 | 8 | 2 ICLK |
| 0008 7302h | ICU | Interrupt source priority register 02 | IPR02 | 8 | 8 | 2 ICLK |
| 0008 7303h | ICU | Interrupt source priority register 03 | IPR03 | 8 | 8 | 2 ICLK |
| 0008 7304h | ICU | Interrupt source priority register 04 | IPR04 | 8 | 8 | 2 ICLK |
| 0008 7305h | ICU | Interrupt source priority register 05 | IPR05 | 8 | 8 | 2 ICLK |
| 0008 7306h | ICU | Interrupt source priority register 06 | IPR06 | 8 | 8 | 2 ICLK |
| 0008 7307h | ICU | Interrupt source priority register 07 | IPR07 | 8 | 8 | 2 ICLK |
| 0008 7308h | ICU | Interrupt source priority register 08 | IPR08 | 8 | 8 | 2 ICLK |

**Table 4.1 List of I/O Registers (Address Order) (12 / 36)**

| Address | Module Abbreviation | Register Name | Register Abbreviation | Number of Bits | Access Size | Number of Access Cycles |
|---|---|---|---|---|---|---|
| 0008 730Ch | ICU | Interrupt source priority register 0C | IPR0C | 8 | 8 | 2 ICLK |
| 0008 730Dh | ICU | Interrupt source priority register 0D | IPR0D | 8 | 8 | 2 ICLK |
| 0008 730Eh | ICU | Interrupt source priority register 0E | IPR0E | 8 | 8 | 2 ICLK |
| 0008 7310h | ICU | Interrupt source priority register 10 | IPR10 | 8 | 8 | 2 ICLK |
| 0008 7311h | ICU | Interrupt source priority register 11 | IPR11 | 8 | 8 | 2 ICLK |
| 0008 7312h | ICU | Interrupt source priority register 12 | IPR12 | 8 | 8 | 2 ICLK |
| 0008 7314h | ICU | Interrupt source priority register 14 | IPR14 | 8 | 8 | 2 ICLK |
| 0008 7315h | ICU | Interrupt source priority register 15 | IPR15 | 8 | 8 | 2 ICLK |
| 0008 7318h | ICU | Interrupt source priority register 18 | IPR18 | 8 | 8 | 2 ICLK |
| 0008 731Eh | ICU | Interrupt source priority register 1E | IPR1E | 8 | 8 | 2 ICLK |
| 0008 731Fh | ICU | Interrupt source priority register 1F | IPR1F | 8 | 8 | 2 ICLK |
| 0008 7320h | ICU | Interrupt source priority register 20 | IPR20 | 8 | 8 | 2 ICLK |
| 0008 7321h | ICU | Interrupt source priority register 21 | IPR21 | 8 | 8 | 2 ICLK |
| 0008 7322h | ICU | Interrupt source priority register 22 | IPR22 | 8 | 8 | 2 ICLK |
| 0008 7323h | ICU | Interrupt source priority register 23 | IPR23 | 8 | 8 | 2 ICLK |
| 0008 7324h | ICU | Interrupt source priority register 24 | IPR24 | 8 | 8 | 2 ICLK |
| 0008 7325h | ICU | Interrupt source priority register 25 | IPR25 | 8 | 8 | 2 ICLK |
| 0008 7326h | ICU | Interrupt source priority register 26 | IPR26 | 8 | 8 | 2 ICLK |
| 0008 7327h | ICU | Interrupt source priority register 27 | IPR27 | 8 | 8 | 2 ICLK |
| 0008 7328h | ICU | Interrupt source priority register 28 | IPR28 | 8 | 8 | 2 ICLK |
| 0008 7329h | ICU | Interrupt source priority register 29 | IPR29 | 8 | 8 | 2 ICLK |
| 0008 732Ah | ICU | Interrupt source priority register 2A | IPR2A | 8 | 8 | 2 ICLK |
| 0008 732Bh | ICU | Interrupt source priority register 2B | IPR2B | 8 | 8 | 2 ICLK |
| 0008 732Ch | ICU | Interrupt source priority register 2C | IPR2C | 8 | 8 | 2 ICLK |
| 0008 732Dh | ICU | Interrupt source priority register 2D | IPR2D | 8 | 8 | 2 ICLK |
| 0008 732Eh | ICU | Interrupt source priority register 2E | IPR2E | 8 | 8 | 2 ICLK |
| 0008 732Fh | ICU | Interrupt source priority register 2F | IPR2F | 8 | 8 | 2 ICLK |
| 0008 733Ah | ICU | Interrupt source priority register 3A | IPR3A | 8 | 8 | 2 ICLK |
| 0008 733Bh | ICU | Interrupt source priority register 3B | IPR3B | 8 | 8 | 2 ICLK |
| 0008 733Ch | ICU | Interrupt source priority register 3C | IPR3C | 8 | 8 | 2 ICLK |
| 0008 7340h | ICU | Interrupt source priority register 40 | IPR40 | 8 | 8 | 2 ICLK |
| 0008 7344h | ICU | Interrupt source priority register 44 | IPR44 | 8 | 8 | 2 ICLK |
| 0008 7345h | ICU | Interrupt source priority register 45 | IPR45 | 8 | 8 | 2 ICLK |
| 0008 7348h | ICU | Interrupt source priority register 48 | IPR48 | 8 | 8 | 2 ICLK |
| 0008 7351h | ICU | Interrupt source priority register 51 | IPR51 | 8 | 8 | 2 ICLK |
| 0008 7352h | ICU | Interrupt source priority register 52 | IPR52 | 8 | 8 | 2 ICLK |
| 0008 7353h | ICU | Interrupt source priority register 53 | IPR53 | 8 | 8 | 2 ICLK |
| 0008 7354h | ICU | Interrupt source priority register 54 | IPR54 | 8 | 8 | 2 ICLK |
| 0008 7355h | ICU | Interrupt source priority register 55 | IPR55 | 8 | 8 | 2 ICLK |
| 0008 7356h | ICU | Interrupt source priority register 56 | IPR56 | 8 | 8 | 2 ICLK |
| 0008 7357h | ICU | Interrupt source priority register 57 | IPR57 | 8 | 8 | 2 ICLK |
| 0008 7358h | ICU | Interrupt source priority register 58 | IPR58 | 8 | 8 | 2 ICLK |
| 0008 7359h | ICU | Interrupt source priority register 59 | IPR59 | 8 | 8 | 2 ICLK |
| 0008 735Ah | ICU | Interrupt source priority register 5A | IPR5A | 8 | 8 | 2 ICLK |
| 0008 735Bh | ICU | Interrupt source priority register 5B | IPR5B | 8 | 8 | 2 ICLK |

**Table 4.1 List of I/O Registers (Address Order) (13 / 36)**

| Address | Module Abbreviation | Register Name | Register Abbreviation | Number of Bits | Access Size | Number of Access Cycles |
|---|---|---|---|---|---|---|
| 0008 735Ch | ICU | Interrupt source priority register 5C | IPR5C | 8 | 8 | 2 ICLK |
| 0008 735Dh | ICU | Interrupt source priority register 5D | IPR5D | 8 | 8 | 2 ICLK |
| 0008 735Eh | ICU | Interrupt source priority register 5E | IPR5E | 8 | 8 | 2 ICLK |
| 0008 735Fh | ICU | Interrupt source priority register 5F | IPR5F | 8 | 8 | 2 ICLK |
| 0008 7360h | ICU | Interrupt source priority register 60 | IPR60 | 8 | 8 | 2 ICLK |
| 0008 7361h | ICU | Interrupt source priority register 61 | IPR61 | 8 | 8 | 2 ICLK |
| 0008 7362h | ICU | Interrupt source priority register 62 | IPR62 | 8 | 8 | 2 ICLK |
| 0008 7363h | ICU | Interrupt source priority register 63 | IPR63 | 8 | 8 | 2 ICLK |
| 0008 7364h | ICU | Interrupt source priority register 64 | IPR64 | 8 | 8 | 2 ICLK |
| 0008 7365h | ICU | Interrupt source priority register 65 | IPR65 | 8 | 8 | 2 ICLK |
| 0008 7366h | ICU | Interrupt source priority register 66 | IPR66 | 8 | 8 | 2 ICLK |
| 0008 7367h | ICU | Interrupt source priority register 67 | IPR67 | 8 | 8 | 2 ICLK |
| 0008 7368h | ICU | Interrupt source priority register 68 | IPR68 | 8 | 8 | 2 ICLK |
| 0008 7369h | ICU | Interrupt source priority register 69 | IPR69 | 8 | 8 | 2 ICLK |
| 0008 736Ah | ICU | Interrupt source priority register 6A | IPR6A | 8 | 8 | 2 ICLK |
| 0008 736Bh | ICU | Interrupt source priority register 6B | IPR6B | 8 | 8 | 2 ICLK |
| 0008 7370h | ICU | Interrupt source priority register 70 | IPR70 | 8 | 8 | 2 ICLK |
| 0008 7371h | ICU | Interrupt source priority register 71 | IPR71 | 8 | 8 | 2 ICLK |
| 0008 7372h | ICU | Interrupt source priority register 72 | IPR72 | 8 | 8 | 2 ICLK |
| 0008 7373h | ICU | Interrupt source priority register 73 | IPR73 | 8 | 8 | 2 ICLK |
| 0008 7374h | ICU | Interrupt source priority register 74 | IPR74 | 8 | 8 | 2 ICLK |
| 0008 7375h | ICU | Interrupt source priority register 75 | IPR75 | 8 | 8 | 2 ICLK |
| 0008 7380h | ICU | Interrupt source priority register 80 | IPR80 | 8 | 8 | 2 ICLK |
| 0008 7381h | ICU | Interrupt source priority register 81 | IPR81 | 8 | 8 | 2 ICLK |
| 0008 7382h | ICU | Interrupt source priority register 82 | IPR82 | 8 | 8 | 2 ICLK |
| 0008 7383h | ICU | Interrupt source priority register 83 | IPR83 | 8 | 8 | 2 ICLK |
| 0008 7385h | ICU | Interrupt source priority register 85 | IPR85 | 8 | 8 | 2 ICLK |
| 0008 7386h | ICU | Interrupt source priority register 86 | IPR86 | 8 | 8 | 2 ICLK |
| 0008 7388h | ICU | Interrupt source priority register 88 | IPR88 | 8 | 8 | 2 ICLK |
| 0008 7389h | ICU | Interrupt source priority register 89 | IPR89 | 8 | 8 | 2 ICLK |
| 0008 738Ah | ICU | Interrupt source priority register 8A | IPR8A | 8 | 8 | 2 ICLK |
| 0008 738Bh | ICU | Interrupt source priority register 8B | IPR8B | 8 | 8 | 2 ICLK |
| 0008 738Ch | ICU | Interrupt source priority register 8C | IPR8C | 8 | 8 | 2 ICLK |
| 0008 738Dh | ICU | Interrupt source priority register 8D | IPR8D | 8 | 8 | 2 ICLK |
| 0008 738Eh | ICU | Interrupt source priority register 8E | IPR8E | 8 | 8 | 2 ICLK |
| 0008 738Fh | ICU | Interrupt source priority register 8F | IPR8F | 8 | 8 | 2 ICLK |
| 0008 7400h | ICU | DMACA activation source select register 0 | DMRSR0 | 8 | 8 | 2 ICLK |
| 0008 7404h | ICU | DMACA activation source select register 1 | DMRSR1 | 8 | 8 | 2 ICLK |
| 0008 7408h | ICU | DMACA activation source select register 2 | DMRSR2 | 8 | 8 | 2 ICLK |
| 0008 740Ch | ICU | DMACA activation source select register 3 | DMRSR3 | 8 | 8 | 2 ICLK |
| 0008 7500h | ICU | IRQ control register 0 | IRQCR0 | 8 | 8 | 2 ICLK |
| 0008 7501h | ICU | IRQ control register 1 | IRQCR1 | 8 | 8 | 2 ICLK |
| 0008 7502h | ICU | IRQ control register 2 | IRQCR2 | 8 | 8 | 2 ICLK |
| 0008 7503h | ICU | IRQ control register 3 | IRQCR3 | 8 | 8 | 2 ICLK |
| 0008 7504h | ICU | IRQ control register 4 | IRQCR4 | 8 | 8 | 2 ICLK |

**Table 4.1 List of I/O Registers (Address Order) (14 / 36)**

| Address | Module Abbreviation | Register Name | Register Abbreviation | Number of Bits | Access Size | Number of Access Cycles |
|---|---|---|---|---|---|---|
| 0008 7505h | ICU | IRQ control register 5 | IRQCR5 | 8 | 8 | 2 ICLK |
| 0008 7506h | ICU | IRQ control register 6 | IRQCR6 | 8 | 8 | 2 ICLK |
| 0008 7507h | ICU | IRQ control register 7 | IRQCR7 | 8 | 8 | 2 ICLK |
| 0008 7508h | ICU | IRQ control register 8 | IRQCR8 | 8 | 8 | 2 ICLK |
| 0008 7509h | ICU | IRQ control register 9 | IRQCR9 | 8 | 8 | 2 ICLK |
| 0008 750Ah | ICU | IRQ control register 10 | IRQCR10 | 8 | 8 | 2 ICLK |
| 0008 750Bh | ICU | IRQ control register 11 | IRQCR11 | 8 | 8 | 2 ICLK |
| 0008 750Ch | ICU | IRQ control register 12 | IRQCR12 | 8 | 8 | 2 ICLK |
| 0008 750Dh | ICU | IRQ control register 13 | IRQCR13 | 8 | 8 | 2 ICLK |
| 0008 750Eh | ICU | IRQ control register 14 | IRQCR14 | 8 | 8 | 2 ICLK |
| 0008 750Fh | ICU | IRQ control register 15 | IRQCR15 | 8 | 8 | 2 ICLK |
| 0008 7580h | ICU | Non-maskable interrupt status register | NMISR | 8 | 8 | 2 ICLK |
| 0008 7581h | ICU | Non-maskable interrupt enable register | NMIER | 8 | 8 | 2 ICLK |
| 0008 7582h | ICU | Non-maskable interrupt clear register | NMICLR | 8 | 8 | 2 ICLK |
| 0008 7583h | ICU | NMI pin interrupt control register | NMICR | 8 | 8 | 2 ICLK |
| 0008 8000h | CMT | Compare match timer start register 0 | CMSTR0 | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 8002h | CMT0 | Compare match timer control register | CMCR | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 8004h | CMT0 | Compare match timer counter | CMCNT | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 8006h | CMT0 | Compare match timer constant register | CMCOR | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 8008h | CMT1 | Compare match timer control register | CMCR | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 800Ah | CMT1 | Compare match timer counter | CMCNT | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 800Ch | CMT1 | Compare match timer constant register | CMCOR | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 8010h | CMT | Compare match timer start register 1 | CMSTR1 | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 8012h | CMT2 | Compare match timer control register | CMCR | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 8014h | CMT2 | Compare match timer counter | CMCNT | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 8016h | CMT2 | Compare match timer constant register | CMCOR | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 8018h | CMT3 | Compare match timer control register | CMCR | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 801Ah | CMT3 | Compare match timer counter | CMCNT | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 801Ch | CMT3 | Compare match timer constant register | CMCOR | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 8028h | WDT | Timer control/status register | READ.TCSR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8028h | WDT | Write window A register | WRITE.WINA | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 8029h | WDT | Timer counter | READ.TCNT | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 802Ah | WDT | Write window B register | WRITE.WINB | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 802Bh | WDT | Reset control/status register | READ.RSTCSR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8030h | IWDT | IWDT refresh register | IWDTRR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8032h | IWDT | IWDT control register | IWDTCR | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 8034h | IWDT | IWDT status register | IWDTSR | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 8040h | AD0 | A/D data register A | ADDRA | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 8042h | AD0 | A/D data register B | ADDRB | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 8044h | AD0 | A/D data register C | ADDRC | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 8046h | AD0 | A/D data register D | ADDRD | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 8050h | AD0 | A/D control/status register | ADCSR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8051h | AD0 | A/D control register | ADCR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8052h | AD0 | ADDRn format select register | ADDPR | 8 | 8 | 2 to 3 PCLK*8 |

**Table 4.1 List of I/O Registers (Address Order) (15 / 36)**

| Address | Module Abbreviation | Register Name | Register Abbreviation | Number of Bits | Access Size | Number of Access Cycles |
|---|---|---|---|---|---|---|
| 0008 8053h | AD0 | A/D sampling state register | ADSSTR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 805Fh | AD0 | A/D self-diagnostic register | ADDIAGR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8060h | AD1 | A/D data register A | ADDRA | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 8062h | AD1 | A/D data register B | ADDRB | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 8064h | AD1 | A/D data register C | ADDRC | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 8066h | AD1 | A/D data register D | ADDRD | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 8070h | AD1 | A/D control/status register | ADCSR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8071h | AD1 | A/D control register | ADCR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8072h | AD1 | ADDRn format select register | ADDPR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8073h | AD1 | A/D sampling state register | ADSSTR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 807Fh | AD1 | A/D self-diagnostic register | ADDIAGR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 80C0h | DA | D/A data register 0 | DADR0 | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 80C2h | DA | D/A data register 1 | DADR1 | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 80C4h | DA | D/A control register | DACR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 80C5h | DA | DADRm format select register | DADPR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 81E6h | PPG0 | PPG output control register | PCR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 81E7h | PPG0 | PPG output mode register | PMR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 81E8h | PPG0 | Next data enable register H | NDERH | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 81E9h | PPG0 | Next data enable register L | NDERL | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 81EAh | PPG0 | Output data register H | PODRH | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 81EBh | PPG0 | Output data register L | PODRL | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 81ECh*1 | PPG0 | Next data register H | NDRH | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 81EDh*2 | PPG0 | Next data register L | NDRL | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 81EEh*1 | PPG0 | Next data register H2 | NDRH2 | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 81EFh*2 | PPG0 | Next data register L2 | NDRL2 | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 81F0h | PPG1 | PPG trigger select register | PTRSLR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 81F6h | PPG1 | PPG output control register | PCR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 81F7h | PPG1 | PPG output mode register | PMR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 81F8h | PPG1 | Next data enable register H | NDERH | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 81F9h | PPG1 | Next data enable register L | NDERL | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 81FAh | PPG1 | Output data register H | PODRH | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 81FBh | PPG1 | Output data register L | PODRL | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 81FCh*3 | PPG1 | Next data register H | NDRH | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 81FDh*4 | PPG1 | Next data register L | NDRL | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 81FEh*3 | PPG1 | Next data register H2 | NDRH2 | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 81FFh*4 | PPG1 | Next data register L2 | NDRL2 | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8200h | TMR0 | Timer control register | TCR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8201h | TMR1 | Timer control register | TCR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8202h | TMR0 | Timer control/status register | TCSR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8203h | TMR1 | Timer control/status register | TCSR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8204h | TMR0 | Time constant register A | TCORA | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8205h | TMR1 | Time constant register A | TCORA | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8206h | TMR0 | Time constant register B | TCORB | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8207h | TMR1 | Time constant register B | TCORB | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8208h | TMR0 | Timer counter | TCNT | 8 | 8 | 2 to 3 PCLK*8 |

**Table 4.1 List of I/O Registers (Address Order) (16 / 36)**

| Address | Module Abbreviation | Register Name | Register Abbreviation | Number of Bits | Access Size | Number of Access Cycles |
|---|---|---|---|---|---|---|
| 0008 8209h | TMR1 | Timer counter | TCNT | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 820Ah | TMR0 | Timer counter control register | TCCR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 820Bh | TMR1 | Timer counter control register | TCCR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8204h | TMR01 | Time constant register A | TCORA | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 8206h | TMR01 | Time constant register B | TCORB | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 8208h | TMR01 | Timer counter | TCNT | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 820Ah | TMR01 | Timer counter control register | TCCR | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 8210h | TMR2 | Timer control register | TCR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8211h | TMR3 | Timer control register | TCR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8212h | TMR2 | Timer control/status register | TCSR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8213h | TMR3 | Timer control/status register | TCSR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8214h | TMR2 | Time constant register A | TCORA | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8215h | TMR3 | Time constant register A | TCORA | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8216h | TMR2 | Time constant register B | TCORB | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8217h | TMR3 | Time constant register B | TCORB | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8218h | TMR2 | Timer counter | TCNT | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8219h | TMR3 | Timer counter | TCNT | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 821Ah | TMR2 | Timer counter control register | TCCR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 821Bh | TMR3 | Timer counter control register | TCCR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8214h | TMR23 | Time constant register A | TCORA | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 8216h | TMR23 | Time constant register B | TCORB | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 8218h | TMR23 | Timer counter | TCNT | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 821Ah | TMR23 | Timer counter control register | TCCR | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 8240h | SCI0 | Serial mode register | SMR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8241h | SCI0 | Bit rate register | BRR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8242h | SCI0 | Serial control register | SCR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8243h | SCI0 | Transmit data register | TDR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8244h | SCI0 | Serial status register | SSR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8245h | SCI0 | Receive data register | RDR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8246h | SCI0 | Smart card mode register | SCMR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8247h | SCI0 | Serial extended mode register | SEMR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8240h | SMCI0 | Serial mode register | SMR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8241h | SMCI0 | Bit rate register | BRR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8242h | SMCI0 | Serial control register | SCR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8243h | SMCI0 | Transmit data register | TDR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8244h | SMCI0 | Serial status register | SSR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8245h | SMCI0 | Receive data register | RDR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8246h | SMCI0 | Smart card mode register | SCMR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8248h | SCI1 | Serial mode register | SMR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8249h | SCI1 | Bit rate register | BRR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 824Ah | SCI1 | Serial control register | SCR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 824Bh | SCI1 | Transmit data register | TDR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 824Ch | SCI1 | Serial status register | SSR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 824Dh | SCI1 | Receive data register | RDR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 824Eh | SCI1 | Smart card mode register | SCMR | 8 | 8 | 2 to 3 PCLK*8 |

**Table 4.1 List of I/O Registers (Address Order) (17 / 36)**

| Address | Module Abbreviation | Register Name | Register Abbreviation | Number of Bits | Access Size | Number of Access Cycles |
|---|---|---|---|---|---|---|
| 0008 824Fh | SCI1 | Serial extended mode register | SEMR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8248h | SMCI1 | Serial mode register | SMR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8249h | SMCI1 | Bit rate register | BRR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 824Ah | SMCI1 | Serial control register | SCR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 824Bh | SMCI1 | Transmit data register | TDR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 824Ch | SMCI1 | Serial status register | SSR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 824Dh | SMCI1 | Receive data register | RDR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 824Eh | SMCI1 | Smart card mode register | SCMR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8250h | SCI2 | Serial mode register | SMR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8251h | SCI2 | Bit rate register | BRR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8252h | SCI2 | Serial control register | SCR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8253h | SCI2 | Transmit data register | TDR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8254h | SCI2 | Serial status register | SSR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8255h | SCI2 | Receive data register | RDR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8256h | SCI2 | Smart card mode register | SCMR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8257h | SCI2 | Serial extended mode register | SEMR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8250h | SMCI2 | Serial mode register | SMR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8251h | SMCI2 | Bit rate register | BRR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8252h | SMCI2 | Serial control register | SCR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8253h | SMCI2 | Transmit data register | TDR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8254h | SMCI2 | Serial status register | SSR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8255h | SMCI2 | Receive data register | RDR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8256h | SMCI2 | Smart card mode register | SCMR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8258h | SCI3 | Serial mode register | SMR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8259h | SCI3 | Bit rate register | BRR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 825Ah | SCI3 | Serial control register | SCR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 825Bh | SCI3 | Transmit data register | TDR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 825Ch | SCI3 | Serial status register | SSR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 825Dh | SCI3 | Receive data register | RDR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 825Eh | SCI3 | Smart card mode register | SCMR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 825Fh | SCI3 | Serial extended mode register | SEMR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8258h | SMCI3 | Serial mode register | SMR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8259h | SMCI3 | Bit rate register | BRR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 825Ah | SMCI3 | Serial control register | SCR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 825Bh | SMCI3 | Transmit data register | TDR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 825Ch | SMCI3 | Serial status register | SSR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 825Dh | SMCI3 | SMCI3 Receive data register | RDR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 825Eh | SMCI3 | SMCI3 Smart card mode register | SCMR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8268h | SCI5 | Serial mode register | SMR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8269h | SCI5 | Bit rate register | BRR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 826Ah | SCI5 | Serial control register | SCR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 826Bh | SCI5 | Transmit data register | TDR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 826Ch | SCI5 | Serial status register | SSR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 826Dh | SCI5 | Receive data register | RDR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 826Eh | SCI5 | Smart card mode register | SCMR | 8 | 8 | 2 to 3 PCLK*8 |

**Table 4.1 List of I/O Registers (Address Order) (18 / 36)**

| Address | Module Abbreviation | Register Name | Register Abbreviation | Number of Bits | Access Size | Number of Access Cycles |
|---|---|---|---|---|---|---|
| 0008 826Fh | SCI5 | Serial extended mode register | SEMR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8268h | SMCI5 | Serial mode register | SMR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8269h | SMCI5 | Bit rate register | BRR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 826Ah | SMCI5 | Serial control register | SCR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 826Bh | SMCI5 | Transmit data register | TDR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 826Ch | SMCI5 | Serial status register | SSR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 826Dh | SMCI5 | Receive data register | RDR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 826Eh | SMCI5 | Smart card mode register | SCMR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8270h | SCI6 | Serial mode register | SMR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8271h | SCI6 | Bit rate register | BRR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8272h | SCI6 | Serial control register | SCR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8273h | SCI6 | Transmit data register | TDR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8274h | SCI6 | Serial status register | SSR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8275h | SCI6 | Receive data register | RDR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8276h | SCI6 | Smart card mode register | SCMR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8277h | SCI6 | Serial extended mode register | SEMR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8270h | SMCI6 | Serial mode register | SMR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8271h | SMCI6 | Bit rate register | BRR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8272h | SMCI6 | Serial control register | SCR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8273h | SMCI6 | Transmit data register | TDR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8274h | SMCI6 | Serial status register | SSR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8275h | SMCI6 | Receive data register | RDR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8276h | SMCI6 | Smart card mode register | SCMR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8280h | CRC | CRC control register | CRCCR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8281h | CRC | CRC data input register | CRCDIR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8282h | CRC | CRC data output register | CRCDOR | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 8300h | RIIC0 | I2C bus control register 1 | ICCR1 | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8301h | RIIC0 | I2C bus control register 2 | ICCR2 | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8302h | RIIC0 | I2C bus mode register 1 | ICMR1 | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8303h | RIIC0 | I2C bus mode register 2 | ICMR2 | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8304h | RIIC0 | I2C bus mode register 3 | ICMR3 | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8305h | RIIC0 | I2C bus function enable register | ICFER | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8306h | RIIC0 | I2C bus status enable register | ICSER | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8307h | RIIC0 | I2C bus interrupt enable register | ICIER | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8308h | RIIC0 | I2C bus status register 1 | ICSR1 | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8309h | RIIC0 | I2C bus status register 2 | ICSR2 | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 830Ah | RIIC0 | Slave address register L0 | SARL0 | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 830Ah | RIIC0 | Timeout internal counter | TMOCNT | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 830Ah | RIIC0 | Timeout internal counter L | TMOCNTL | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 830Bh | RIIC0 | Slave address register U0 | SARU0 | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 830Bh | RIIC0 | Timeout internal counter U | TMOCNTU | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 830Ch | RIIC0 | Slave address register L1 | SARL1 | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 830Dh | RIIC0 | Slave address register U1 | SARU1 | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 830Eh | RIIC0 | Slave address register L2 | SARL2 | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 830Fh | RIIC0 | Slave address register U2 | SARU2 | 8 | 8 | 2 to 3 PCLK*8 |

**Table 4.1 List of I/O Registers (Address Order) (19 / 36)**

| Address | Module Abbreviation | Register Name | Register Abbreviation | Number of Bits | Access Size | Number of Access Cycles |
|---|---|---|---|---|---|---|
| 0008 8310h | RIIC0 | I²C bus bit rate low-level register | ICBRL | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8311h | RIIC0 | I²C bus bit rate high-level register | ICBRH | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8312h | RIIC0 | I²C bus transmit data register | ICDRT | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8313h | RIIC0 | I²C bus receive data register | ICDRR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8320h | RIIC1 | I²C bus control register 1 | ICCR1 | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8321h | RIIC1 | I²C bus control register 2 | ICCR2 | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8322h | RIIC1 | I²C bus mode register 1 | ICMR1 | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8323h | RIIC1 | I²C bus mode register 2 | ICMR2 | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8324h | RIIC1 | I²C bus mode register 3 | ICMR3 | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8325h | RIIC1 | I²C bus function enable register | ICFER | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8326h | RIIC1 | I²C bus status enable register | ICSER | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8327h | RIIC1 | I²C bus interrupt enable register | ICIER | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8328h | RIIC1 | I²C bus status register 1 | ICSR1 | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8329h | RIIC1 | I²C bus status register 2 | ICSR2 | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 832Ah | RIIC1 | Slave address register L0 | SARL0 | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 832Ah | RIIC1 | Timeout internal counter | TMOCNT | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 832Ah | RIIC1 | Timeout internal counter L | TMOCNTL | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 832Bh | RIIC1 | Slave address register U0 | SARU0 | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 832Bh | RIIC1 | Timeout internal counter U | TMOCNTU | | 8 | 2 to 3 PCLK*8 |
| 0008 832Ch | RIIC1 | Slave address register L1 | SARL1 | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 832Dh | RIIC1 | Slave address register U1 | SARU1 | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 832Eh | RIIC1 | Slave address register L2 | SARL2 | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 832Fh | RIIC1 | Slave address register U2 | SARU2 | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8330h | RIIC1 | I²C bus bit rate low-level register | ICBRL | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8331h | RIIC1 | I²C bus bit rate high-level register | ICBRH | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8332h | RIIC1 | I²C bus transmit data register | ICDRT | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8333h | RIIC1 | I²C bus receive data register | ICDRR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8380h | RSPI0 | RSPI control register | SPCR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8381h | RSPI0 | RSPI slave select polarity register | SSLP | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8382h | RSPI0 | RSPI pin control register | SPPCR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8383h | RSPI0 | RSPI status register | SPSR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8384h | RSPI0 | RSPI data register | SPDR | 32 | 16, 32 | 2 to 3 PCLK*8 |
| 0008 8388h | RSPI0 | RSPI sequence control register | SPSCR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8389h | RSPI0 | RSPI sequence status register | SPSSR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 838Ah | RSPI0 | RSPI bit rate register | SPBR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 838Bh | RSPI0 | RSPI data control register | SPDCR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 838Ch | RSPI0 | RSPI clock delay register | SPCKD | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 838Dh | RSPI0 | RSPI slave select negation delay register | SSLND | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 838Eh | RSPI0 | RSPI next-access delay register | SPND | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 838Fh | RSPI0 | RSPI control register 2 | SPCR2 | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8390h | RSPI0 | RSPI command register 0 | SPCMD0 | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 8392h | RSPI0 | RSPI command register 1 | SPCMD1 | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 8394h | RSPI0 | RSPI command register 2 | SPCMD2 | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 8396h | RSPI0 | RSPI command register 3 | SPCMD3 | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 8398h | RSPI0 | RSPI command register 4 | SPCMD4 | 16 | 16 | 2 to 3 PCLK*8 |

**Table 4.1 List of I/O Registers (Address Order) (20 / 36)**

| Address | Module Abbreviation | Register Name | Register Abbreviation | Number of Bits | Access Size | Number of Access Cycles |
|---|---|---|---|---|---|---|
| 0008 839Ah | RSPI0 | RSPI command register 5 | SPCMD5 | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 839Ch | RSPI0 | RSPI command register 6 | SPCMD6 | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 839Eh | RSPI0 | RSPI command register 7 | SPCMD7 | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 83A0h | RSPI1 | RSPI control register | SPCR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 83A1h | RSPI1 | RSPI slave select polarity register | SSLP | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 83A2h | RSPI1 | RSPI pin control register | SPPCR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 83A3h | RSPI1 | RSPI status register | SPSR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 83A4h | RSPI1 | RSPI data register | SPDR | 32 | 16, 32 | 2 to 3 PCLK*8 |
| 0008 83A8h | RSPI1 | RSPI sequence control register | SPSCR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 83A9h | RSPI1 | RSPI sequence status register | SPSSR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 83AAh | RSPI1 | RSPI bit rate register | SPBR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 83ABh | RSPI1 | RSPI data control register | SPDCR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 83ACh | RSPI1 | RSPI clock delay register | SPCKD | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 83ADh | RSPI1 | RSPI slave select negation delay register | SSLND | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 83AEh | RSPI1 | RSPI next-access delay register | SPND | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 83AFh | RSPI1 | RSPI control register 2 | SPCR2 | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 83B0h | RSPI1 | RSPI command register 0 | SPCMD0 | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 83B2h | RSPI1 | RSPI command register 1 | SPCMD1 | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 83B4h | RSPI1 | RSPI command register 2 | SPCMD2 | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 83B6h | RSPI1 | RSPI command register 3 | SPCMD3 | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 83B8h | RSPI1 | RSPI command register 4 | SPCMD4 | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 83BAh | RSPI1 | RSPI command register 5 | SPCMD5 | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 83BCh | RSPI1 | RSPI command register 6 | SPCMD6 | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 83BEh | RSPI1 | RSPI command register 7 | SPCMD7 | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 8600h | MTU3 | Timer control register | TCR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8601h | MTU4 | Timer control register | TCR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8602h | MTU3 | Timer mode register | TMDR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8603h | MTU4 | Timer mode register | TMDR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8604h | MTU3 | Timer I/O control register H | TIORH | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8605h | MTU3 | Timer I/O control register L | TIORL | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8606h | MTU4 | Timer I/O control register H | TIORH | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8607h | MTU4 | Timer I/O control register L | TIORL | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8608h | MTU3 | Timer interrupt enable register | TIER | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8609h | MTU4 | Timer interrupt enable register | TIER | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 860Ah | MTUA | Timer output master enable register | TOER | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 860Dh | MTUA | Timer gate control register | TGCR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 860Eh | MTUA | Timer output control register 1 | TOCR1 | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 860Fh | MTUA | Timer output control register 2 | TOCR2 | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8610h | MTU3 | Timer counter | TCNT | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 8612h | MTU4 | Timer counter | TCNT | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 8614h | MTUA | Timer cycle data register | TCDR | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 8616h | MTUA | Timer dead time data register | TDDR | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 8618h | MTU3 | Timer general register A | TGRA | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 861Ah | MTU3 | Timer general register B | TGRB | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 861Ch | MTU4 | Timer general register A | TGRA | 16 | 16 | 2 to 3 PCLK*8 |

**Table 4.1 List of I/O Registers (Address Order) (21 / 36)**

| Address | Module Abbreviation | Register Name | Register Abbreviation | Number of Bits | Access Size | Number of Access Cycles |
|---|---|---|---|---|---|---|
| 0008 861Eh | MTU4 | Timer general register B | TGRB | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 8620h | MTUA | Timer subcounter | TCNTS | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 8622h | MTUA | Timer cycle buffer register | TCBR | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 8624h | MTU3 | Timer general register C | TGRC | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 8626h | MTU3 | Timer general register D | TGRD | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 8628h | MTU4 | Timer general register C | TGRC | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 862Ah | MTU4 | Timer general register D | TGRD | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 862Ch | MTU3 | Timer status register | TSR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 862Dh | MTU4 | Timer status register | TSR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8630h | MTUA | Timer interrupt skipping set register | TITCR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8631h | MTUA | Timer interrupt skipping counter | TITCNT | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8632h | MTUA | Timer buffer transfer set register | TBTER | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8634h | MTUA | Timer dead time enable register | TDER | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8636h | MTUA | Timer output level buffer register | TOLBR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8638h | MTU3 | Timer buffer operation transfer mode register | TBTM | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8639h | MTU4 | Timer buffer operation transfer mode register | TBTM | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8640h | MTU4 | Timer A/D converter start request control register | TADCR | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 8644h | MTU4 | Timer A/D converter start request cycle set register A | TADCORA | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 8646h | MTU4 | Timer A/D converter start request cycle set register B | TADCORB | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 8648h | MTU4 | Timer A/D converter start request cycle set buffer register A | TADCOBRA | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 864Ah | MTU4 | Timer A/D converter start request cycle set buffer register B | TADCOBRB | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 8660h | MTUA | Timer waveform control register | TWCR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8680h | MTUA | Timer start register | TSTR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8681h | MTUA | Timer synchronous register | TSYR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8684h | MTUA | Timer read/write enable register | TRWER | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8700h | MTU0 | Timer control register | TCR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8701h | MTU0 | Timer mode register | TMDR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8702h | MTU0 | Timer I/O control register H | TIORH | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8703h | MTU0 | Timer I/O control register L | TIORL | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8704h | MTU0 | Timer interrupt enable register | TIER | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8705h | MTU0 | Timer status register | TSR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8706h | MTU0 | Timer counter | TCNT | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 8708h | MTU0 | Timer general register A | TGRA | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 870Ah | MTU0 | Timer general register B | TGRB | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 870Ch | MTU0 | Timer general register C | TGRC | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 870Eh | MTU0 | Timer general register D | TGRD | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 8720h | MTU0 | Timer general register E | TGRE | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 8722h | MTU0 | Timer general register F | TGRF | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 8724h | MTU0 | Timer interrupt enable register 2 | TIER2 | 8 | 8 | 2 to 3 PCLK*8 |

**Table 4.1 List of I/O Registers (Address Order) (22 / 36)**

| Address | Module Abbreviation | Register Name | Register Abbreviation | Number of Bits | Access Size | Number of Access Cycles |
|---|---|---|---|---|---|---|
| 0008 8726h | MTU0 | Timer buffer operation transfer mode register | TBTM | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8780h | MTU1 | Timer control register | TCR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8781h | MTU1 | Timer mode register | TMDR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8782h | MTU1 | Timer I/O control register | TIOR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8784h | MTU1 | Timer interrupt enable register | TIER | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8785h | MTU1 | Timer status register | TSR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8786h | MTU1 | Timer counter | TCNT | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 8788h | MTU1 | Timer general register A | TGRA | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 878Ah | MTU1 | Timer general register B | TGRB | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 8790h | MTU1 | Timer input capture control register | TICCR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8800h | MTU2 | Timer control register | TCR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8801h | MTU2 | Timer mode register | TMDR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8802h | MTU2 | Timer I/O control register | TIOR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8804h | MTU2 | Timer interrupt enable register | TIER | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8805h | MTU2 | Timer status register | TSR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8806h | MTU2 | Timer counter | TCNT | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 8808h | MTU2 | Timer general register A | TGRA | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 880Ah | MTU2 | Timer general register B | TGRB | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 8880h | MTU5 | Timer counter U | TCNTU | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 8882h | MTU5 | Timer general register U | TGRU | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 8884h | MTU5 | Timer control register U | TCRU | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8886h | MTU5 | Timer I/O control register U | TIORU | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8890h | MTU5 | Timer counter V | TCNTV | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 8892h | MTU5 | Timer general register V | TGRV | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 8894h | MTU5 | Timer control register V | TCRV | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8896h | MTU5 | Timer I/O control register V | TIORV | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 88A0h | MTU5 | Timer counter W | TCNTW | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 88A2h | MTU5 | Timer general register W | TGRW | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 88A4h | MTU5 | Timer control register W | TCRW | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 88A6h | MTU5 | Timer I/O control register W | TIORW | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 88B2h | MTU5 | Timer interrupt enable register | TIER | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 88B4h | MTU5 | Timer start register | TSTR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 88B6h | MTU5 | Timer compare match clear register | TCNTCMPCLR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8900h | POE | Input level control/status register 1 | ICSR1 | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 8902h | POE | Output level control/status register 1 | OCSR1 | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 8904h | POE | Input level control/status register 2 | ICSR2 | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 8906h | POE | Output level control/status register 2 | OCSR2 | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 8908h | POE | Input level control/status register 3 | ICSR3 | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 890Ah | POE | Software port output enable register | SPOER | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 890Bh | POE | Port output enable control register 1 | POECR1 | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 890Ch | POE | Port output enable control register 2 | POECR2 | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 890Eh | POE | Input level control/status register 4 | ICSR4 | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 8A00h | MTU9 | Timer control register | TCR | 8 | 8 | 2 to 3 PCLK*8 |

**Table 4.1 List of I/O Registers (Address Order) (23 / 36)**

| Address | Module Abbreviation | Register Name | Register Abbreviation | Number of Bits | Access Size | Number of Access Cycles |
|---|---|---|---|---|---|---|
| 0008 8A01h | MTU10 | Timer control register | TCR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8A02h | MTU9 | Timer mode register | TMDR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8A03h | MTU10 | Timer mode register | TMDR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8A04h | MTU9 | Timer I/O control register H | TIORH | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8A05h | MTU9 | Timer I/O control register L | TIORL | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8A06h | MTU10 | Timer I/O control register H | TIORH | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8A07h | MTU10 | Timer I/O control register L | TIORL | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8A08h | MTU9 | Timer interrupt enable register | TIER | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8A09h | MTU10 | Timer interrupt enable register | TIER | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8A0Ah | MTUB | Timer output master enable register | TOER | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8A0Dh | MTUB | Timer gate control register | TGCR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8A0Eh | MTUB | Timer output control register 1 | TOCR1 | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8A0Fh | MTUB | Timer output control register 2 | TOCR2 | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8A10h | MTU9 | Timer counter | TCNT | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 8A12h | MTU10 | Timer counter | TCNT | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 8A14h | MTUB | Timer cycle data register | TCDR | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 8A16h | MTUB | Timer dead time data register | TDDR | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 8A18h | MTU9 | Timer general register A | TGRA | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 8A1Ah | MTU9 | Timer general register B | TGRB | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 8A1Ch | MTU10 | Timer general register A | TGRA | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 8A1Eh | MTU10 | Timer general register B | TGRB | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 8A20h | MTUB | Timer subcounter | TCNTS | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 8A22h | MTUB | MTUB Timer cycle buffer register | TCBR | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 8A24h | MTU9 | Timer general register C | TGRC | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 8A26h | MTU9 | Timer general register D | TGRD | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 8A28h | MTU10 | Timer general register C | TGRC | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 8A2Ah | MTU10 | Timer general register D | TGRD | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 8A2Ch | MTU9 | Timer status register | TSR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8A2Dh | MTU10 | Timer status register | TSR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8A30h | MTUB | Timer interrupt skipping set register | TITCR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8A31h | MTUB | Timer interrupt skipping counter | TITCNT | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8A32h | MTUB | TUB Timer dead time enable register | TBTER | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8A34h | MTUB | Timer dead time enable register | TDER | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8A36h | MTUB | Timer output level buffer register | TOLBR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8A38h | MTU9 | Timer buffer operation transfer mode register | TBTM | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8A39h | MTU10 | Timer buffer operation transfer mode register | TBTM | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8A40h | MTU10 | Timer A/D converter start request control register | TADCR | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 8A44h | MTU10 | Timer A/D converter start request cycle set register A | TADCORA | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 8A46h | MTU10 | Timer A/D converter start request cycle set register B | TADCORB | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 8A48h | MTU10 | Timer A/D converter start request cycle set buffer register A | TADCOBRA | 16 | 16 | 2 to 3 PCLK*8 |

**Table 4.1 List of I/O Registers (Address Order) (24 / 36)**

| Address | Module Abbreviation | Register Name | Register Abbreviation | Number of Bits | Access Size | Number of Access Cycles |
|---|---|---|---|---|---|---|
| 0008 8A4Ah | MTU10 | Timer A/D converter start request cycle set buffer register B | TADCOBRB | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 8A60h | MTUB | Timer waveform control register | TWCR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8A80h | MTUB | Timer start register | TSTR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8A81h | MTUB | MTUB Timer synchronous register | TSYR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8A84h | MTUB | MTUB Timer read/write enable register | TRWER | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8B00h | MTU6 | Timer control register | TCR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8B01h | MTU6 | Timer mode register | TMDR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8B02h | MTU6 | Timer I/O control register H | TIORH | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8B03h | MTU6 | Timer I/O control register L | TIORL | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8B04h | MTU6 | Timer interrupt enable register | TIER | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8B05h | MTU6 | Timer status register | TSR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8B06h | MTU6 | Timer counter | TCNT | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 8B08h | MTU6 | Timer general register A | TGRA | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 8B0Ah | MTU6 | Timer general register B | TGRB | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 8B0Ch | MTU6 | Timer general register C | TGRC | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 8B0Eh | MTU6 | Timer general register D | TGRD | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 8B20h | MTU6 | Timer general register E | TGRE | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 8B22h | MTU6 | Timer general register F | TGRF | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 8B24h | MTU6 | Timer interrupt enable register 2 | TIER2 | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8B26h | MTU6 | Timer buffer operation transfer mode register | TBTM | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8B80h | MTU7 | Timer control register | TCR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8B81h | MTU7 | Timer mode register | TMDR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8B82h | MTU7 | Timer I/O control register | TIOR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8B84h | MTU7 | Timer interrupt enable register | TIER | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8B85h | MTU7 | Timer status register | TSR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8B86h | MTU7 | Timer counter | TCNT | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 8B88h | MTU7 | Timer general register A | TGRA | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 8B8Ah | MTU7 | Timer general register B | TGRB | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 8B90h | MTU7 | Timer input capture control register | TICCR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8C00h | MTU8 | Timer control register | TCR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8C01h | MTU8 | Timer mode register | TMDR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8C02h | MTU8 | Timer I/O control register | TIOR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8C04h | MTU8 | Timer interrupt enable register | TIER | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8C05h | MTU8 | Timer status register | TSR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8C06h | MTU8 | Timer counter | TCNT | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 8C08h | MTU8 | Timer general register A | TGRA | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 8C0Ah | MTU8 | Timer general register B | TGRB | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 8C80h | MTU11 | Timer counter U | TCNTU | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 8C82h | MTU11 | Timer general register U | TGRU | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 8C84h | MTU11 | Timer control register U | TCRU | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8C86h | MTU11 | Timer I/O control register U | TIORU | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8C90h | MTU11 | Timer counter V | TCNTV | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 8C92h | MTU11 | Timer general register V | TGRV | 16 | 16 | 2 to 3 PCLK*8 |

**Table 4.1 List of I/O Registers (Address Order) (25 / 36)**

| Address | Module Abbreviation | Register Name | Register Abbreviation | Number of Bits | Access Size | Number of Access Cycles |
|---|---|---|---|---|---|---|
| 0008 8C94h | MTU11 | Timer control register V | TCRV | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8C96h | MTU11 | Timer I/O control register V | TIORV | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8CA0h | MTU11 | Timer counter W | TCNTW | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 8CA2h | MTU11 | Timer general register W | TGRW | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 8CA4h | MTU11 | Timer control register W | TCRW | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8CA6h | MTU11 | Timer I/O control register W | TIORW | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8CB2h | MTU11 | Timer interrupt enable register | TIER | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8CB4h | MTU11 | Timer start register | TSTR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 8CB6h | MTU11 | Timer compare match clear register | TCNTCMPCLR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 9000h | S12AD | A/D control register | ADCSR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 9004h | S12AD | A/D channel select register | ADANS | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 9008h | S12AD | A/D-converted value addition mode select register | ADADS | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 900Ch | S12AD | A/D-converted value addition count select register | ADADC | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 900Eh | S12AD | A/D control extended register | ADCER | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 9010h | S12AD | A/D start trigger select register | ADSTRGR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 9020h | S12AD | A/D data register 0 | ADDR0 | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 9022h | S12AD | A/D data register 1 | ADDR1 | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 9024h | S12AD | A/D data register 2 | ADDR2 | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 9026h | S12AD | A/D data register 3 | ADDR3 | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 9028h | S12AD | A/D data register 4 | ADDR4 | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 902Ah | S12AD | A/D data register 5 | ADDR5 | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 902Ch | S12AD | A/D data register 6 | ADDR6 | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 902Eh | S12AD | A/D data register 7 | ADDR7 | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 C000h | PORT0 | Data direction register | DDR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 C001h | PORT1 | Data direction register | DDR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 C002h | PORT2 | Data direction register | DDR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 C003h | PORT3 | Data direction register | DDR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 C004h | PORT4 | Data direction register | DDR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 C005h | PORT5 | Data direction register | DDR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 C006h | PORT6 | Data direction register | DDR*6*7 | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 C007h | PORT7 | Data direction register | DDR*6*7 | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 C008h | PORT8 | Data direction register | DDR*6*7 | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 C009h | PORT9 | Data direction register | DDR*6*7 | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 C00Ah | PORTA | Data direction register | DDR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 C00Bh | PORTB | Data direction register | DDR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 C00Ch | PORTC | Data direction register | DDR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 C00Dh | PORTD | Data direction register | DDR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 C00Eh | PORTE | Data direction register | DDR*7 | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 C00Fh | PORTF | Data direction register | DDR*5*6*7 | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 C010h | PORTG | Data direction register | DDR*5*6*7 | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 C020h | PORT0 | Data register | DR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 C021h | PORT1 | Data register | DR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 C022h | PORT2 | Data register | DR | 8 | 8 | 2 to 3 PCLK*8 |

**Table 4.1 List of I/O Registers (Address Order) (26 / 36)**

| Address | Module Abbreviation | Register Name | Register Abbreviation | Number of Bits | Access Size | Number of Access Cycles |
|---|---|---|---|---|---|---|
| 0008 C023h | PORT3 | Data register | DR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 C024h | PORT4 | Data register | DR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 C025h | PORT5 | Data register | DR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 C026h | PORT6 | Data register | DR*6*7 | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 C027h | PORT7 | Data register | DR*6*7 | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 C028h | PORT8 | Data register | DR*6*7 | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 C029h | PORT9 | Data register | DR*6*7 | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 C02Ah | PORTA | Data register | DR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 C02Bh | PORTB | Data register | DR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 C02Ch | PORTC | Data register | DR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 C02Dh | PORTD | Data register | DR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 C02Eh | PORTE | Data register | DR*7 | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 C02Fh | PORTF | Data register | DR*5*6*7 | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 C030h | PORTG | Data register | DR**5*6*7 | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 C040h | PORT0 | Port register | PORT | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 C041h | PORT1 | Port register | PORT | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 C042h | PORT2 | Port register | PORT | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 C043h | PORT3 | Port register | PORT | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 C044h | PORT4 | Port register | PORT | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 C045h | PORT5 | Port register | PORT | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 C046h | PORT6 | Port register | PORT*6*7 | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 C047h | PORT7 | Port register | PORT*6*7 | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 C048h | PORT8 | Port register | PORT*6*7 | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 C049h | PORT9 | Port register | PORT*6*7 | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 C04Ah | PORTA | Port register | PORT | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 C04Bh | PORTB | Port register | PORT | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 C04Ch | PORTC | Port register | PORT | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 C04Dh | PORTD | Port register | PORT | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 C04Eh | PORTE | Port register | PORT*7 | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 C04Fh | PORTF | Port register | PORT*5*6*7 | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 C050h | PORTG | Port register | PORT*5*6*7 | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 C060h | PORT0 | Input buffer control register | ICR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 C061h | PORT1 | Input buffer control register | ICR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 C062h | PORT2 | Input buffer control register | ICR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 C063h | PORT3 | Input buffer control register | ICR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 C064h | PORT4 | Input buffer control register | ICR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 C065h | PORT5 | Input buffer control register | ICR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 C066h | PORT6 | Input buffer control register | ICR*6*7 | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 C067h | PORT7 | Input buffer control register | ICR*6*7 | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 C068h | PORT8 | Input buffer control register | ICR*6*7 | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 C069h | PORT9 | Input buffer control register | ICR*6*7 | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 C06Ah | PORTA | Input buffer control register | ICR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 C06Bh | PORTB | Input buffer control register | ICR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 C06Ch | PORTC | Input buffer control register | ICR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 C06Dh | PORTD | Input buffer control register | ICR | 8 | 8 | 2 to 3 PCLK*8 |

**Table 4.1 List of I/O Registers (Address Order) (27 / 36)**

| Address | Module Abbreviation | Register Name | Register Abbreviation | Number of Bits | Access Size | Number of Access Cycles |
|---|---|---|---|---|---|---|
| 0008 C06Eh | PORTE | Input buffer control register | ICR*7 | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 C06Fh | PORTF | Input buffer control register | ICR*5*6*7 | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 C070h | PORTG | Input buffer control register | ICR*5*6*7 | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 C080h | PORT0 | Open drain control register | ODR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 C081h | PORT1 | Open drain control register | ODR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 C082h | PORT2 | Open drain control register | ODR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 C083h | PORT3 | Open drain control register | ODR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 C08Ch | PORTC | Open drain control register | ODR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 C0C9h | PORT9 | Pull-up resistor control register | PCR*6*7 | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 C0CAh | PORTA | Pull-up resistor control register | PCR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 C0CBh | PORTB | Pull-up resistor control register | PCR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 C0CCh | PORTC | Pull-up resistor control register | PCR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 C0CDh | PORTD | Pull-up resistor control register | PCR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 C0CEh | PORTE | Pull-up resistor control register | PCR*7 | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 C0D0h | PORTG | Pull-up resistor control register | PCR*5*6*7 | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 C100h | IOPORT | Port function register 0 | PF0CSE | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 C101h | IOPORT | Port function register 1 | PF1CSS*6*7 | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 C102h | IOPORT | Port function register 2 | PF2CSS*6*7 | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 C103h | IOPORT | Port function register 3 | PF3BUS | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 C104h | IOPORT | Port function register 4 | PF4BUS | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 C105h | IOPORT | Port function register 5 | PF5BUS | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 C106h | IOPORT | Port function register 6 | PF6BUS | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 C107h | IOPORT | Port function register 7 | PF7DMA | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 C108h | IOPORT | Port function register 8 | PF8IRQ | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 C109h | IOPORT | Port function register 9 | PF9IRQ | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 C10Ah | IOPORT | Port function register A | PFAADC | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 C10Bh | IOPORT | Port function register B | PFBTMR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 C10Ch | IOPORT | Port function register C | PFCMTU | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 C10Dh | IOPORT | Port function register D | PFDMTU | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 C10Eh | IOPORT | Port function register E | PFENET | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 C10Fh | IOPORT | Port function register F | PFFSCI | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 C110h | IOPORT | Port function register G | PFGSPI | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 C111h | IOPORT | Port function register H | PFHSPI | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 C113h | IOPORT | Port function register J | PFJCAN | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 C114h | IOPORT | Port function register K | PFKUSB | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 C115h | IOPORT | Port function register L | PFLUSB*6*7 | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 C116h | IOPORT | Port function register M | PFMPOE*7 | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 C117h | IOPORT | Port function register N | PFNPOE*7 | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 C280h | SYSTEM | Deep standby control register | DPSBYCR | 8 | 8 | 4 to 5 PCLK*8 |
| 0008 C281h | SYSTEM | Deep standby wait control register | DPSWCR | 8 | 8 | 4 to 5 PCLK*8 |
| 0008 C282h | SYSTEM | Deep standby interrupt enable register | DPSIER | 8 | 8 | 4 to 5 PCLK*8 |
| 0008 C283h | SYSTEM | Deep standby interrupt flag register | DPSIFR | 8 | 8 | 4 to 5 PCLK*8 |
| 0008 C284h | SYSTEM | Deep standby interrupt edge register | DPSIEGR | 8 | 8 | 4 to 5 PCLK*8 |
| 0008 C285h | SYSTEM | Reset status register | RSTSR | 8 | 8 | 4 to 5 PCLK*8 |
| 0008 C289h | FLASH | Flash write erase protection register | FWEPROR | 8 | 8 | 4 to 5 PCLK*8 |

**Table 4.1 List of I/O Registers (Address Order) (28 / 36)**

| Address | Module Abbreviation | Register Name | Register Abbreviation | Number of Bits | Access Size | Number of Access Cycles |
|---|---|---|---|---|---|---|
| 0008 C28Ah | SYSTEM | Sub-clock oscillator control register | SUBOSCCR | 8 | 8 | 4 to 5 PCLK*8 |
| 0008 C28Ch | SYSTEM | Key code register for voltage detection control register | LVDKEYR | 8 | 8 | 4 to 5 PCLK*8 |
| 0008 C28Dh | SYSTEM | Voltage detection control register | LVDCR | 8 | 8 | 4 to 5 PCLK*8 |
| 0008 C290h | SYSTEM | Deep standby backup register 0 | DPSBKR0 | 8 | 8 | 4 to 5 PCLK*8 |
| 0008 C291h | SYSTEM | Deep standby backup register 1 | DPSBKR1 | 8 | 8 | 4 to 5 PCLK*8 |
| 0008 C292h | SYSTEM | Deep standby backup register 2 | DPSBKR2 | 8 | 8 | 4 to 5 PCLK*8 |
| 0008 C293h | SYSTEM | Deep standby backup register 3 | DPSBKR3 | 8 | 8 | 4 to 5 PCLK*8 |
| 0008 C294h | SYSTEM | Deep standby backup register 4 | DPSBKR4 | 8 | 8 | 4 to 5 PCLK*8 |
| 0008 C295h | SYSTEM | Deep standby backup register 5 | DPSBKR5 | 8 | 8 | 4 to 5 PCLK*8 |
| 0008 C296h | SYSTEM | Deep standby backup register 6 | DPSBKR6 | 8 | 8 | 4 to 5 PCLK*8 |
| 0008 C297h | SYSTEM | Deep standby backup register 7 | DPSBKR7 | 8 | 8 | 4 to 5 PCLK*8 |
| 0008 C298h | SYSTEM | Deep standby backup register 8 | DPSBKR8 | 8 | 8 | 4 to 5 PCLK*8 |
| 0008 C299h | SYSTEM | Deep standby backup register 9 | DPSBKR9 | 8 | 8 | 4 to 5 PCLK*8 |
| 0008 C29Ah | SYSTEM | Deep standby backup register 10 | DPSBKR10 | 8 | 8 | 4 to 5 PCLK*8 |
| 0008 C29Bh | SYSTEM | Deep standby backup register 11 | DPSBKR11 | 8 | 8 | 4 to 5 PCLK*8 |
| 0008 C29Ch | SYSTEM | Deep standby backup register 12 | DPSBKR12 | 8 | 8 | 4 to 5 PCLK*8 |
| 0008 C29Dh | SYSTEM | Deep standby backup register 13 | DPSBKR13 | 8 | 8 | 4 to 5 PCLK*8 |
| 0008 C29Eh | SYSTEM | Deep standby backup register 14 | DPSBKR14 | 8 | 8 | 4 to 5 PCLK*8 |
| 0008 C29Fh | SYSTEM | Deep standby backup register 15 | DPSBKR15 | 8 | 8 | 4 to 5 PCLK*8 |
| 0008 C2A0h | SYSTEM | Deep standby backup register 16 | DPSBKR16 | 8 | 8 | 4 to 5 PCLK*8 |
| 0008 C2A1h | SYSTEM | Deep standby backup register 17 | DPSBKR17 | 8 | 8 | 4 to 5 PCLK*8 |
| 0008 C2A2h | SYSTEM | Deep standby backup register 18 | DPSBKR18 | 8 | 8 | 4 to 5 PCLK*8 |
| 0008 C2A3h | SYSTEM | Deep standby backup register 19 | DPSBKR19 | 8 | 8 | 4 to 5 PCLK*8 |
| 0008 C2A4h | SYSTEM | Deep standby backup register 20 | DPSBKR20 | 8 | 8 | 4 to 5 PCLK*8 |
| 0008 C2A5h | SYSTEM | Deep standby backup register 21 | DPSBKR21 | 8 | 8 | 4 to 5 PCLK*8 |
| 0008 C2A6h | SYSTEM | Deep standby backup register 22 | DPSBKR22 | 8 | 8 | 4 to 5 PCLK*8 |
| 0008 C2A7h | SYSTEM | Deep standby backup register 23 | DPSBKR23 | 8 | 8 | 4 to 5 PCLK*8 |
| 0008 C2A8h | SYSTEM | Deep standby backup register 24 | DPSBKR24 | 8 | 8 | 4 to 5 PCLK*8 |
| 0008 C2A9h | SYSTEM | Deep standby backup register 25 | DPSBKR25 | 8 | 8 | 4 to 5 PCLK*8 |
| 0008 C2AAh | SYSTEM | Deep standby backup register 26 | DPSBKR26 | 8 | 8 | 4 to 5 PCLK*8 |
| 0008 C2ABh | SYSTEM | Deep standby backup register 27 | DPSBKR27 | 8 | 8 | 4 to 5 PCLK*8 |
| 0008 C2ACh | SYSTEM | Deep standby backup register 28 | DPSBKR28 | 8 | 8 | 4 to 5 PCLK*8 |
| 0008 C2ADh | SYSTEM | Deep standby backup register 29 | DPSBKR29 | 8 | 8 | 4 to 5 PCLK*8 |
| 0008 C2AEh | SYSTEM | Deep standby backup register 30 | DPSBKR30 | 8 | 8 | 4 to 5 PCLK*8 |
| 0008 C2AFh | SYSTEM | Deep standby backup register 31 | DPSBKR31 | 8 | 8 | 4 to 5 PCLK*8 |
| 0008 C400h | RTC | 64-Hz counter | R64CNT | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 C402h | RTC | Second counter | RSECCNT | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 C404h | RTC | Minute counter | RMINCNT | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 C406h | RTC | Hour counter | RHRCNT | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 C408h | RTC | Day-of-week counter | RWKCNT | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 C40Ah | RTC | Date counter | RDAYCNT | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 C40Ch | RTC | Month counter | RMONCNT | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 C40Eh | RTC | Year counter | RYRCNT | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 C410h | RTC | Second alarm register | RSECAR | 8 | 8 | 2 to 3 PCLK*8 |

**Table 4.1 List of I/O Registers (Address Order) (29 / 36)**

| Address | Module Abbreviation | Register Name | Register Abbreviation | Number of Bits | Access Size | Number of Access Cycles |
|---|---|---|---|---|---|---|
| 0008 C412h | RTC | Minute alarm register | RMINAR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 C414h | RTC | Hour alarm register | RHRAR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 C416h | RTC | Day-of-week alarm register | RWKAR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 C418h | RTC | Date alarm register | RDAYAR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 C41Ah | RTC | Month alarm register | RMONAR | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 C41Ch | RTC | Year alarm register | RYRAR | 16 | 16 | 2 to 3 PCLK*8 |
| 0008 C41Eh | RTC | Year alarm enable register | RYRAREN | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 C422h | RTC | RTC control register 1 | RCR1 | 8 | 8 | 2 to 3 PCLK*8 |
| 0008 C424h | RTC | RTC control register 2 | RCR2 | 8 | 8 | 2 to 3 PCLK*8 |
| 0009 0200h to 0009 03FFh | CAN0 | Mailbox registers 0 to 31 | MB0 to MB31 | 128 | 8, 16, 32 | 2 to 3 PCLK*8 |
| 0009 0400h | CAN0 | Mask register 0 | MKR0 | 32 | 8, 16, 32 | 2 to 3 PCLK*8 |
| 0009 0404h | CAN0 | Mask register 1 | MKR1 | 32 | 8, 16, 32 | 2 to 3 PCLK*8 |
| 0009 0408h | CAN0 | Mask register 2 | MKR2 | 32 | 8, 16, 32 | 2 to 3 PCLK*8 |
| 0009 040Ch | CAN0 | Mask register 3 | MKR3 | 32 | 8, 16, 32 | 2 to 3 PCLK*8 |
| 0009 0410h | CAN0 | Mask register 4 | MKR4 | 32 | 8, 16, 32 | 2 to 3 PCLK*8 |
| 0009 0414h | CAN0 | Mask register 5 | MKR5 | 32 | 8, 16, 32 | 2 to 3 PCLK*8 |
| 0009 0418h | CAN0 | Mask register 6 | MKR6 | 32 | 8, 16, 32 | 2 to 3 PCLK*8 |
| 0009 041Ch | CAN0 | Mask register 7 | MKR7 | 32 | 8, 16, 32 | 2 to 3 PCLK*8 |
| 0009 0420h | CAN0 | FIFO received ID compare register 0 | FIDCR0 | 32 | 8, 16, 32 | 2 to 3 PCLK*8 |
| 0009 0424h | CAN0 | FIFO received ID compare register 1 | FIDCR1 | 32 | 8, 16, 32 | 2 to 3 PCLK*8 |
| 0009 0428h | CAN0 | Mask invalid register | MKIVLR | 32 | 8, 16, 32 | 2 to 3 PCLK*8 |
| 0009 042Ch | CAN0 | Mailbox interrupt enable register | MIER | 32 | 8, 16, 32 | 2 to 3 PCLK*8 |
| 0009 0820h to 0009 083Fh | CAN0 | Message control registers 0 to 31 | MCTL0 to MCTL31 | 8 | 8 | 2 to 3 PCLK*8 |
| 0009 0840h | CAN0 | Control register | CTLR | 16 | 8, 16 | 2 to 3 PCLK*8 |
| 0009 0842h | CAN0 | Status register | STR | 16 | 8, 16 | 2 to 3 PCLK*8 |
| 0009 0844h | CAN0 | Bit configuration register | BCR | 32 | 8, 16, 32 | 2 to 3 PCLK*8 |
| 0009 0848h | CAN0 | Receive FIFO control register | RFCR | 8 | 8 | 2 to 3 PCLK*8 |
| 0009 0849h | CAN0 | Receive FIFO pointer control register | RFPCR | 8 | 8 | 2 to 3 PCLK*8 |
| 0009 084Ah | CAN0 | Transmit FIFO control register | TFCR | 8 | 8 | 2 to 3 PCLK*8 |
| 0009 084Bh | CAN0 | Transmit FIFO pointer control register | TFPCR | 8 | 8 | 2 to 3 PCLK*8 |
| 0009 084Ch | CAN0 | Error interrupt enable register | EIER | 8 | 8 | 2 to 3 PCLK*8 |
| 0009 084Dh | CAN0 | Error interrupt factor judge register | EIFR | 8 | 8 | 2 to 3 PCLK*8 |
| 0009 084Eh | CAN0 | Receive error count register | RECR | 8 | 8 | 2 to 3 PCLK*8 |
| 0009 084Fh | CAN0 | Transmit error count register | TECR | 8 | 8 | 2 to 3 PCLK*8 |
| 0009 0850h | CAN0 | Error code store register | ECSR | 8 | 8 | 2 to 3 PCLK*8 |
| 0009 0851h | CAN0 | Channel search support register | CSSR | 8 | 8 | 2 to 3 PCLK*8 |
| 0009 0852h | CAN0 | Mailbox search status register | MSSR | 8 | 8 | 2 to 3 PCLK*8 |
| 0009 0853h | CAN0 | Mailbox search mode register | MSMR | 8 | 8 | 2 to 3 PCLK*8 |
| 0009 0854h | CAN0 | Time stamp register | TSR | 16 | 8, 16 | 2 to 3 PCLK*8 |
| 0009 0856h | CAN0 | Acceptance filter support register | AFSR | 16 | 8, 16 | 2 to 3 PCLK*8 |
| 0009 0858h | CAN0 | Test control register | TCR | 8 | 8 | 2 to 3 PCLK*8 |
| 000A 0000h | USB0 | System configuration control register | SYSCFG | 16 | 16 | 3 to 4 PCLK*8 |
| 000A 0004h | USB0 | System configuration status register 0 | SYSSTS0 | 16 | 16 | at least 9 PCLK*9 |

**Table 4.1 List of I/O Registers (Address Order) (30 / 36)**

| Address | Module Abbreviation | Register Name | Register Abbreviation | Number of Bits | Access Size | Number of Access Cycles |
|---|---|---|---|---|---|---|
| 000A 0008h | USB0 | Device state control register 0 | DVSTCTR0 | 16 | 16 | at least 9 PCLK*9 |
| 000A 0014h | USB0 | CFIFO port register | CFIFO | 16 | 8, 16 | 3 to 4 PCLK*8 |
| 000A 0018h | USB0 | D0FIFO port register | D0FIFO | 16 | 8, 16 | 3 to 4 PCLK*8 |
| 000A 001Ch | USB0 | D1FIFO port register | D1FIFO | 16 | 8, 16 | 3 to 4 PCLK*8 |
| 000A 0020h | USB0 | CFIFO port select register | CFIFOSEL | 16 | 16 | 3 to 4 PCLK*8 |
| 000A 0022h | USB0 | CFIFO port control register | CFIFOCTR | 16 | 16 | 3 to 4 PCLK*8 |
| 000A 0028h | USB0 | D0FIFO port select register | D0FIFOSEL | 16 | 16 | 3 to 4 PCLK*8 |
| 000A 002Ah | USB0 | D0FIFO port control register | D0FIFOCTR | 16 | 16 | 3 to 4 PCLK*8 |
| 000A 002Ch | USB0 | D1FIFO port select register | D1FIFOSEL | 16 | 16 | 3 to 4 PCLK*8 |
| 000A 002Eh | USB0 | D1FIFO port control register | D1FIFOCTR | 16 | 16 | 3 to 4 PCLK*8 |
| 000A 0030h | USB0 | Interrupt enable register 0 | INTENB0 | 16 | 16 | at least 9 PCLK*9 |
| 000A 0032h | USB0 | Interrupt enable register 1 | INTENB1 | 16 | 16 | at least 9 PCLK*9 |
| 000A 0036h | USB0 | BRDY interrupt enable register | BRDYENB | 16 | 16 | at least 9 PCLK*9 |
| 000A 0038h | USB0 | NRDY interrupt enable register | NRDYENB | 16 | 16 | at least 9 PCLK*9 |
| 000A 003Ah | USB0 | BEMP interrupt enable register | BEMPENB | 16 | 16 | at least 9 PCLK*9 |
| 000A 003Ch | USB0 | SOF output configuration register | SOFCFG | 16 | 16 | at least 9 PCLK*9 |
| 000A 0040h | USB0 | Interrupt status register 0 | INTSTS0 | 16 | 16 | at least 9 PCLK*9 |
| 000A 0042h | USB0 | Interrupt status register 1 | INTSTS1 | 16 | 16 | at least 9 PCLK*9 |
| 000A 0046h | USB0 | BRDY interrupt enable register | BRDYSTS | 16 | 16 | at least 9 PCLK*9 |
| 000A 0048h | USB0 | NRDY interrupt status register | NRDYSTS | 16 | 16 | at least 9 PCLK*9 |
| 000A 004Ah | USB0 | BEMP interrupt status register | BEMPSTS | 16 | 16 | at least 9 PCLK*9 |
| 000A 004Ch | USB0 | Frame number register | FRMNUM | 16 | 16 | at least 9 PCLK*9 |
| 000A 004Eh | USB0 | Device state change register | DVCHGR | 16 | 16 | at least 9 PCLK*9 |
| 000A 0050h | USB0 | USB address register | USBADDR | 16 | 16 | at least 9 PCLK*9 |
| 000A 0054h | USB0 | USB request type register | USBREQ | 16 | 16 | at least 9 PCLK*9 |
| 000A 0056h | USB0 | USB request value register | USBVAL | 16 | 16 | at least 9 PCLK*9 |
| 000A 0058h | USB0 | USB request index register | USBINDX | 16 | 16 | at least 9 PCLK*9 |
| 000A 005Ah | USB0 | USB request length register | USBLENG | 16 | 16 | at least 9 PCLK*9 |
| 000A 005Ch | USB0 | DCP configuration register | DCPCFG | 16 | 16 | at least 9 PCLK*9 |
| 000A 005Eh | USB0 | DCP maximum packet size register | DCPMAXP | 16 | 16 | at least 9 PCLK*9 |

**Table 4.1 List of I/O Registers (Address Order) (31 / 36)**

| Address | Module Abbreviation | Register Name | Register Abbreviation | Number of Bits | Access Size | Number of Access Cycles |
|---|---|---|---|---|---|---|
| 000A 0060h | USB0 | DCP control register | DCPCTR | 16 | 16 | at least 9 PCLK*9 |
| 000A 0064h | USB0 | Pipe window select register | PIPESEL | 16 | 16 | at least 9 PCLK*9 |
| 000A 0068h | USB0 | Pipe configuration register | PIPECFG | 16 | 16 | at least 9 PCLK*9 |
| 000A 006Ch | USB0 | Pipe maximum packet size register | PIPEMAXP | 16 | 16 | at least 9 PCLK*9 |
| 000A 006Eh | USB0 | Pipe cycle control register | PIPEPERI | 16 | 16 | at least 9 PCLK*9 |
| 000A 0070h | USB0 | Pipe 1 control register | PIPE1CTR | 16 | 16 | at least 9 PCLK*9 |
| 000A 0072h | USB0 | Pipe 2 control register | PIPE2CTR | 16 | 16 | at least 9 PCLK*9 |
| 000A 0074h | USB0 | Pipe 3 control register | PIPE3CTR | 16 | 16 | at least 9 PCLK*9 |
| 000A 0076h | USB0 | Pipe 4 control register | PIPE4CTR | 16 | 16 | at least 9 PCLK*9 |
| 000A 0078h | USB0 | Pipe 5 control register | PIPE5CTR | 16 | 16 | at least 9 PCLK*9 |
| 000A 007Ah | USB0 | Pipe 6 control register | PIPE6CTR | 16 | 16 | at least 9 PCLK*9 |
| 000A 007Ch | USB0 | Pipe 7 control register | PIPE7CTR | 16 | 16 | at least 9 PCLK*9 |
| 000A 007Eh | USB0 | Pipe 8 control register | PIPE8CTR | 16 | 16 | at least 9 PCLK*9 |
| 000A 0080h | USB0 | Pipe 9 control register | PIPE9CTR | 16 | 16 | at least 9 PCLK*9 |
| 000A 0090h | USB0 | Pipe 1 transaction counter enable register | PIPE1TRE | 16 | 16 | at least 9 PCLK*9 |
| 000A 0092h | USB0 | Pipe 1 transaction counter register | PIPE1TRN | 16 | 16 | at least 9 PCLK*9 |
| 000A 0094h | USB0 | Pipe 2 transaction counter enable register | PIPE2TRE | 16 | 16 | at least 9 PCLK*9 |
| 000A 0096h | USB0 | Pipe 2 transaction counter register | PIPE2TRN | 16 | 16 | at least 9 PCLK*9 |
| 000A 0098h | USB0 | Pipe 3 transaction counter enable register | PIPE3TRE | 16 | 16 | at least 9 PCLK*9 |
| 000A 009Ah | USB0 | Pipe 3 transaction counter register | PIPE3TRN | 16 | 16 | at least 9 PCLK*9 |
| 000A 009Ch | USB0 | Pipe 4 transaction counter enable register | PIPE4TRE | 16 | 16 | at least 9 PCLK*9 |
| 000A 009Eh | USB0 | Pipe 4 transaction counter register | PIPE4TRN | 16 | 16 | at least 9 PCLK*9 |
| 000A 00A0h | USB0 | Pipe 5 transaction counter enable register | PIPE5TRE | 16 | 16 | at least 9 PCLK*9 |
| 000A 00A2h | USB0 | Pipe 5 transaction counter register | PIPE5TRN | 16 | 16 | at least 9 PCLK*9 |
| 000A 00D0h | USB0 | Device address 0 configuration register | DEVADD0 | 16 | 16 | at least 9 PCLK*9 |
| 000A 00D2h | USB0 | Device address 1 configuration register | DEVADD1 | 16 | 16 | at least 9 PCLK*9 |

**Table 4.1 List of I/O Registers (Address Order) (32 / 36)**

| Address | Module Abbreviation | Register Name | Register Abbreviation | Number of Bits | Access Size | Number of Access Cycles |
|---|---|---|---|---|---|---|
| 000A 00D4h | USB0 | Device address 2 configuration register | DEVADD2 | 16 | 16 | at least 9 PCLK*9 |
| 000A 00D6h | USB0 | Device address 3 configuration register | DEVADD3 | 16 | 16 | at least 9 PCLK*9 |
| 000A 00D8h | USB0 | Device address 4 configuration register | DEVADD4 | 16 | 16 | at least 9 PCLK*9 |
| 000A 00DAh | USB0 | Device address 5 configuration register | DEVADD5 | 16 | 16 | at least 9 PCLK*9 |
| 000A 0200h | USB1 | System configuration control register | SYSCFG | 16 | 16 | 3 to 4 PCLK*8 |
| 000A 0204h | USB1 | System configuration status register 0 | SYSSTS0 | 16 | 16 | at least 9 PCLK*9 |
| 000A 0208h | USB1 | Device state control register 0 | DVSTCTR0 | 16 | 16 | at least 9 PCLK*9 |
| 000A 0214h | USB1 | CFIFO port register | CFIFO | 16 | 8, 16 | 3 to 4 PCLK*8 |
| 000A 0218h | USB1 | D0FIFO port register | D0FIFO | 16 | 8, 16 | 3 to 4 PCLK*8 |
| 000A 021Ch | USB1 | D1FIFO port register | D1FIFO | 16 | 8, 16 | 3 to 4 PCLK*8 |
| 000A 0220h | USB1 | CFIFO port select register | CFIFOSEL | 16 | 16 | 3 to 4 PCLK*8 |
| 000A 0222h | USB1 | CFIFO port control register | CFIFOCTR | 16 | 16 | 3 to 4 PCLK*8 |
| 000A 0228h | USB1 | D0FIFO port select register | D0FIFOSEL | 16 | 16 | 3 to 4 PCLK*8 |
| 000A 022Ah | USB1 | D0FIFO port control register | D0FIFOCTR | 16 | 16 | 3 to 4 PCLK*8 |
| 000A 022Ch | USB1 | D1FIFO port select register | D1FIFOSEL | 16 | 16 | 3 to 4 PCLK*8 |
| 000A 022Eh | USB1 | D1FIFO port control register | D1FIFOCTR | 16 | 16 | 3 to 4 PCLK*8 |
| 000A 0230h | USB1 | Interrupt enable register 0 | INTENB0 | 16 | 16 | at least 9 PCLK*9 |
| 000A 0232h | USB1 | Interrupt enable register 1 | INTENB1 | 16 | 16 | at least 9 PCLK*9 |
| 000A 0236h | USB1 | BRDY interrupt enable register | BRDYENB | 16 | 16 | at least 9 PCLK*9 |
| 000A 0238h | USB1 | NRDY interrupt enable register | NRDYENB | 16 | 16 | at least 9 PCLK*9 |
| 000A 023Ah | USB1 | BEMP interrupt enable register | BEMPENB | 16 | 16 | at least 9 PCLK*9 |
| 000A 023Ch | USB1 | SOF output configuration register | SOFCFG | 16 | 16 | at least 9 PCLK*9 |
| 000A 0240h | USB1 | Interrupt status register 0 | INTSTS0 | 16 | 16 | at least 9 PCLK*9 |
| 000A 0242h | USB1 | Interrupt status register 1 | INTSTS1 | 16 | 16 | at least 9 PCLK*9 |
| 000A 0246h | USB1 | BRDY interrupt status register | BRDYSTS | 16 | 16 | at least 9 PCLK*9 |
| 000A 0248h | USB1 | NRDY interrupt status register | NRDYSTS | 16 | 16 | at least 9 PCLK*9 |
| 000A 024Ah | USB1 | BEMP interrupt status register | BEMPSTS | 16 | 16 | at least 9 PCLK*9 |
| 000A 024Ch | USB1 | Frame number register | FRMNUM | 16 | 16 | at least 9 PCLK*9 |
| 000A 024Eh | USB1 | Device state change register | DVCHGR | 16 | 16 | at least 9 PCLK*9 |
| 000A 0250h | USB1 | USB address register | USBADDR | 16 | 16 | at least 9 PCLK*9 |

**Table 4.1 List of I/O Registers (Address Order) (33 / 36)**

| Address | Module Abbreviation | Register Name | Register Abbreviation | Number of Bits | Access Size | Number of Access Cycles |
|---|---|---|---|---|---|---|
| 000A 0254h | USB1 | USB request type register | USBREQ | 16 | 16 | at least 9 PCLK*9 |
| 000A 0256h | USB1 | USB request value register | USBVAL | 16 | 16 | at least 9 PCLK*9 |
| 000A 0258h | USB1 | USB request index register | USBINDX | 16 | 16 | at least 9 PCLK*9 |
| 000A 025Ah | USB1 | USB request length register | USBLENG | 16 | 16 | at least 9 PCLK*9 |
| 000A 025Ch | USB1 | DCP configuration register | DCPCFG | 16 | 16 | at least 9 PCLK*9 |
| 000A 025Eh | USB1 | DCP maximum packet size register | DCPMAXP | 16 | 16 | at least 9 PCLK*9 |
| 000A 0260h | USB1 | DCP control register | DCPCTR | 16 | 16 | at least 9 PCLK*9 |
| 000A 0264h | USB1 | Pipe window select register | PIPESEL | 16 | 16 | at least 9 PCLK*9 |
| 000A 0268h | USB1 | Pipe configuration register | PIPECFG | 16 | 16 | at least 9 PCLK*9 |
| 000A 026Ch | USB1 | Pipe maximum packet size register | PIPEMAXP | 16 | 16 | at least 9 PCLK*9 |
| 000A 026Eh | USB1 | Pipe cycle control register | PIPEPERI | 16 | 16 | at least 9 PCLK*9 |
| 000A 0270h | USB1 | Pipe 1 control register | PIPE1CTR | 16 | 16 | at least 9 PCLK*9 |
| 000A 0272h | USB1 | Pipe 2 control register | PIPE2CTR | 16 | 16 | at least 9 PCLK*9 |
| 000A 0274h | USB1 | Pipe 3 control register | PIPE3CTR | 16 | 16 | at least 9 PCLK*9 |
| 000A 0276h | USB1 | Pipe 4 control register | PIPE4CTR | 16 | 16 | at least 9 PCLK*9 |
| 000A 0278h | USB1 | Pipe 5 control register | PIPE5CTR | 16 | 16 | at least 9 PCLK*9 |
| 000A 027Ah | USB1 | Pipe 6 control register | PIPE6CTR | 16 | 16 | at least 9 PCLK*9 |
| 000A 027Ch | USB1 | Pipe 7 control register | PIPE7CTR | 16 | 16 | at least 9 PCLK*9 |
| 000A 027Eh | USB1 | Pipe 8 control register | PIPE8CTR | 16 | 16 | at least 9 PCLK*9 |
| 000A 0280h | USB1 | Pipe 9 control register | PIPE9CTR | 16 | 16 | at least 9 PCLK*9 |
| 000A 0290h | USB1 | Pipe 1 transaction counter enable register | PIPE1TRE | 16 | 16 | at least 9 PCLK*9 |
| 000A 0292h | USB1 | Pipe 1 transaction counter register | PIPE1TRN | 16 | 16 | at least 9 PCLK*9 |
| 000A 0294h | USB1 | Pipe 2 transaction counter enable register | PIPE2TRE | 16 | 16 | at least 9 PCLK*9 |
| 000A 0296h | USB1 | Pipe 2 transaction counter register | PIPE2TRN | 16 | 16 | at least 9 PCLK*9 |
| 000A 0298h | USB1 | Pipe 3 transaction counter enable register | PIPE3TRE | 16 | 16 | at least 9 PCLK*9 |
| 000A 029Ah | USB1 | Pipe 3 transaction counter register | PIPE3TRN | 16 | 16 | at least 9 PCLK*9 |

**Table 4.1 List of I/O Registers (Address Order) (34 / 36)**

| Address | Module Abbreviation | Register Name | Register Abbreviation | Number of Bits | Access Size | Number of Access Cycles |
|---|---|---|---|---|---|---|
| 000A 029Ch | USB1 | Pipe 4 transaction counter enable register | PIPE4TRE | 16 | 16 | at least 9 PCLK*9 |
| 000A 029Eh | USB1 | Pipe 4 transaction counter register | PIPE4TRN | 16 | 16 | at least 9 PCLK*9 |
| 000A 02A0h | USB1 | Pipe 5 transaction counter enable register | PIPE5TRE | 16 | 16 | at least 9 PCLK*9 |
| 000A 02A2h | USB1 | Pipe 5 transaction counter register | PIPE5TRN | 16 | 16 | at least 9 PCLK*9 |
| 000A 02D0h | USB1 | Device address 0 configuration register | DEVADD0 | 16 | 16 | at least 9 PCLK*9 |
| 000A 02D2h | USB1 | Device address 1 configuration register | DEVADD1 | 16 | 16 | at least 9 PCLK*9 |
| 000A 02D4h | USB1 | Device address 2 configuration register | DEVADD2 | 16 | 16 | at least 9 PCLK*9 |
| 000A 02D6h | USB1 | Device address 3 configuration register | DEVADD3 | 16 | 16 | at least 9 PCLK*9 |
| 000A 02D8h | USB1 | Device address 4 configuration register | DEVADD4 | 16 | 16 | at least 9 PCLK*9 |
| 000A 02DAh | USB1 | Device address 5 configuration register | DEVADD5 | 16 | 16 | at least 9 PCLK*9 |
| 000A 0400h | USB | Deep standby USB transceiver control/ pin monitor register | DPUSR0R | 32 | 32 | 1 to 2PCLK*8 |
| 000A 0404h | USB | Deep standby USB suspend/resume interrupt register | DPUSR1R | 32 | 32 | 1 to 2PCLK*8 |
| 000C 0000h | EDMAC | EDMAC mode register | EDMR | 32 | 32 | 4 to 5 ICLK |
| 000C 0008h | EDMAC | EDMAC transmit request register | EDTRR | 32 | 32 | 4 to 5 ICLK |
| 000C 0010h | EDMAC | EDMAC receive request register | EDRRR | 32 | 32 | 4 to 5 ICLK |
| 000C 0018h | EDMAC | Transmit descriptor list start address register | TDLAR | 32 | 32 | 4 to 5 ICLK |
| 000C 0020h | EDMAC | Receive descriptor list start address register | RDLAR | 32 | 32 | 4 to 5 ICLK |
| 000C 0028h | EDMAC | ETHERC/EDMAC status register | EESR | 32 | 32 | 4 to 5 ICLK |
| 000C 0030h | EDMAC | ETHERC/EDMAC status interrupt permission register | EESIPR | 32 | 32 | 4 to 5 ICLK |
| 000C 0038h | EDMAC | Transmit/receive status copy enable register | TRSCER | 32 | 32 | 4 to 5 ICLK |
| 000C 0040h | EDMAC | Receive missed-frame counter register | RMFCR | 32 | 32 | 4 to 5 ICLK |
| 000C 0048h | EDMAC | Transmit FIFO threshold register | TFTR | 32 | 32 | 4 to 5 ICLK |
| 000C 0050h | EDMAC | FIFO depth register | FDR | 32 | 32 | 4 to 5 ICLK |
| 000C 0058h | EDMAC | Receiving method control register | RMCR | 32 | 32 | 4 to 5 ICLK |
| 000C 0064h | EDMAC | Transmit FIFO underrun counter | TFUCR | 32 | 32 | 4 to 5 ICLK |
| 000C 0068h | EDMAC | Receive FIFO overflow counter | RFOCR | 32 | 32 | 4 to 5 ICLK |
| 000C 006Ch | EDMAC | Independent output signal setting register | IOSR | 32 | 32 | 4 to 5 ICLK |
| 000C 0070h | EDMAC | Flow control start FIFO threshold setting register | FCFTR | 32 | 32 | 4 to 5 ICLK |
| 000C 0078h | EDMAC | Receive data padding insert register | RPADIR | 32 | 32 | 4 to 5 ICLK |
| 000C 007Ch | EDMAC | Transmit interrupt setting register | TRIMD | 32 | 32 | 4 to 5 ICLK |
| 000C 00C8h | EDMAC | Receive buffer write address register | RBWAR | 32 | 32 | 4 to 5 ICLK |
| 000C 00CCh | EDMAC | Receive descriptor fetch address register | RDFAR | 32 | 32 | 4 to 5 ICLK |

**Table 4.1 List of I/O Registers (Address Order) (35 / 36)**

| Address | Module Abbreviation | Register Name | Register Abbreviation | Number of Bits | Access Size | Number of Access Cycles |
|---|---|---|---|---|---|---|
| 000C 00D4h | EDMAC | Transmit buffer read address register | TBRAR | 32 | 32 | 4 to 5 ICLK |
| 000C 00D8h | EDMAC | Transmit descriptor fetch address register | TDFAR | 32 | 32 | 4 to 5 ICLK |
| 000C 0100h | ETHERC | ETHERC mode register | ECMR | 32 | 32 | 4 to 5 ICLK |
| 000C 0108h | ETHERC | Receive frame length register | RFLR | 32 | 32 | 4 to 5 ICLK |
| 000C 0110h | ETHERC | ETHERC status register | ECSR | 32 | 32 | 4 to 5 ICLK |
| 000C 0118h | ETHERC | ETHERC interrupt enable register | ECSIPR | 32 | 32 | 4 to 5 ICLK |
| 000C 0120h | ETHERC | PHY interface register | PIR | 32 | 32 | 4 to 5 ICLK |
| 000C 0128h | ETHERC | PHY status register | PSR | 32 | 32 | 4 to 5 ICLK |
| 000C 0140h | ETHERC | Random number generation counter upper limit setting register | RDMLR | 32 | 32 | 4 to 5 ICLK |
| 000C 0150h | ETHERC | IPG register | IPGR | 32 | 32 | 4 to 5 ICLK |
| 000C 0154h | ETHERC | Automatic PAUSE frame register | APR | 32 | 32 | 4 to 5 ICLK |
| 000C 0158h | ETHERC | Manual PAUSE frame register | MPR | 32 | 32 | 4 to 5 ICLK |
| 000C 0160h | ETHERC | PAUSE frame receive counter register | RFCF | 32 | 32 | 4 to 5 ICLK |
| 000C 0164h | ETHERC | Automatic PAUSE frame retransmit count register | TPAUSER | 32 | 32 | 4 to 5 ICLK |
| 000C 0168h | ETHERC | PAUSE frame retransmit counter register | TPAUSECR | 32 | 32 | 4 to 5 ICLK |
| 000C 016Ch | ETHERC | Broadcast frame receive count setting register | BCFRR | 32 | 32 | 4 to 5 ICLK |
| 000C 01C0h | ETHERC | MAC address high register | MAHR | 32 | 32 | 4 to 5 ICLK |
| 000C 01C8h | ETHERC | MAC address low register | MALR | 32 | 32 | 4 to 5 ICLK |
| 000C 01D0h | ETHERC | Transmit retry over counter register | TROCR | 32 | 32 | 4 to 5 ICLK |
| 000C 01D4h | ETHERC | Delayed collision detect counter register | CDCR | 32 | 32 | 4 to 5 ICLK |
| 000C 01D8h | ETHERC | Lost carrier counter register | LCCR | 32 | 32 | 4 to 5 ICLK |
| 000C 01DCh | ETHERC | Carrier not detect counter register | CNDCR | 32 | 32 | 4 to 5 ICLK |
| 000C 01E4h | ETHERC | CRC error frame receive counter register | CEFCR | 32 | 32 | 4 to 5 ICLK |
| 000C 01E8h | ETHERC | Frame receive error counter register | FRECR | 32 | 32 | 4 to 5 ICLK |
| 000C 01ECh | ETHERC | Too-short frame receive counter register | TSFRCR | 32 | 32 | 4 to 5 ICLK |
| 000C 01F0h | ETHERC | Too-long frame receive counter register | TLFRCR | 32 | 32 | 4 to 5 ICLK |
| 000C 01F4h | ETHERC | Residual-bit frame receive counter register | RFCR | 32 | 32 | 4 to 5 ICLK |
| 000C 01F8h | ETHERC | Multicast address frame receive counter register | MAFCR | 32 | 32 | 4 to 5 ICLK |
| 007F C402h | FLASH | Flash mode register | FMODR | 8 | 8 | 2 to 3 PCLK*8 |
| 007F C410h | FLASH | Flash access status register | FASTAT | 8 | 8 | 2 to 3 PCLK*8 |
| 007F C411h | FLASH | Flash access error interrupt enable register | FAEINT | 8 | 8 | 2 to 3 PCLK*8 |
| 007F C412h | FLASH | Flash ready interrupt enable register | FRDYIE | 8 | 8 | 2 to 3 PCLK*8 |
| 007F C440h | FLASH | Data flash read enable register0 | DFLRE0 | 16 | 16 | 2 to 3 PCLK*8 |
| 007F C442h | FLASH | Data flash read enable register1 | DFLRE1 | 16 | 16 | 2 to 3 PCLK*8 |
| 007F C450h | FLASH | Data flash programming/erasure enable register0 | DFLWE0 | 16 | 16 | 2 to 3 PCLK*8 |
| 007F C452h | FLASH | Data flash programming/erasure enable register1 | DFLWE1 | 16 | 16 | 2 to 3 PCLK*8 |
| 007F C454h | FLASH | FCU RAM enable register | FCURAME | 16 | 16 | 2 to 3 PCLK*8 |
| 007F FFB0h | FLASH | Flash status register 0 | FSTATR0 | 8 | 8 | 2 to 3 PCLK*8 |

**Table 4.1 List of I/O Registers (Address Order) (36 / 36)**

| Address | Module Abbreviation | Register Name | Register Abbreviation | Number of Bits | Access Size | Number of Access Cycles |
|---|---|---|---|---|---|---|
| 007F FFB1h | FLASH | Flash status register 1 | FSTATR1 | 8 | 8 | 2 to 3 PCLK*8 |
| 007F FFB2h | FLASH | Flash P/E mode entry register | FENTRYR | 16 | 16 | 2 to 3 PCLK*8 |
| 007F FFB4h | FLASH | Flash protect register | FPROTR | 16 | 16 | 2 to 3 PCLK*8 |
| 007F FFB6h | FLASH | Flash reset register | FRESETR | 16 | 16 | 2 to 3 PCLK*8 |
| 007F FFBAh | FLASH | FCU command register | FCMDR | 16 | 16 | 2 to 3 PCLK*8 |
| 007F FFC8h | FLASH | FCU processing switching register | FCPSR | 16 | 16 | 2 to 3 PCLK*8 |
| 007F FFCAh | FLASH | Data flash blank check control register | DFLBCCNT | 16 | 16 | 2 to 3 PCLK*8 |
| 007F FFCCh | FLASH | Flash P/E status register | FPESTAT | 16 | 16 | 2 to 3 PCLK*8 |
| 007F FFCEh | FLASH | Data flash blank check status register | DFLBCSTAT | 16 | 16 | 2 to 3 PCLK*8 |
| 007F FFE8h | FLASH | Peripheral clock notification register | PCKAR | 16 | 16 | 2 to 3 PCLK*8 |

Note 1. When the same output trigger is specified for pulse output groups 2 and 3 by the PPG0.PCR setting, the PPG0.NDRH address is 000881ECh. When different output triggers are specified, the PPG0.NDRH2 addresses for pulse output groups 2 and 3 are 000881EEh and 000881ECh, respectively.
Note 2. When the same output trigger is specified for pulse output groups 0 and 1 by the PPG0.PCR setting, the PPG0.NDRL address is 000881EDh. When different output triggers are specified, the PPG0.NDRL2 addresses for pulse output groups 0 and 1 are 000881EFh and 000881EDh, respectively.
Note 3. When the same output trigger is specified for pulse output groups 6 and 7 by the PPG1.PCR setting, the PPG1.NDRH address is 000881FCh. When different output triggers are specified, the PPG1.NDRH2 addresses for pulse output groups 6 and 7 are 000881FEh and 000881FCh, respectively.
Note 4. When the same output trigger is specified for pulse output groups 4 and 5 by the PPG1.PCR setting, the PPG1.NDRL address is 000881FDh. When different output triggers are specified, the PPG1.NDRL2 addresses for pulse output groups 4 and 5 are 000881FFh and 000881FDh, respectively.
Note 5. This register is not supported by the 145-pin TFLGA or 144-pin LQFP version.
Note 6. This register is not supported by the 100-pin LQFP version.
Note 7. This register is not supported by the 85-pin TFLGA version.
Note 8. The number of access states depends on the number of divided cycles for clock synchronization (0 to 1 PCLK, 0 to 1 BCLK).
Note 9. Access may be disabled if a register is accessed during the USB operation.

# 5. Electrical Characteristics

## 5.1 Absolute Maximum Ratings

**Table 5.1 Absolute Maximum Ratings**

| Item | Symbol | Value | Unit |
|---|---|---|---|
| Power supply voltage | VCC<br>PLLVCC<br>VCC_USB | -0.3 to +4.6 | V |
| Input voltage<br>(except for ports 00 to 02, 07, ports 12, 13, 16, 17,<br>ports 20, 21, port 33) | $V_{IN}$ | -0.3 to VCC+0.3 | V |
| Input voltage<br>(ports 00 to 02, 07, ports 12, 13, 16, 17,<br>ports 20, 21, port 33*1) | $V_{IN}$ | -0.3 to +5.8 | V |
| Reference power supply voltage | $V_{REF}$ | -0.3 to VCC+0.3 | V |
| Analog power supply voltage | AVCC*2 | -0.3 to +4.6 | V |
| Analog input voltage | $V_{AN}$ | -0.3 to VCC+0.3 | V |
| Operating temperature | $T_{opr}$ | -40 to +85 | °C |
| Storage temperature | $T_{stg}$ | -55 to +125 | °C |

Caution: Permanent damage to the LSI may result if absolute maximum ratings are exceeded.

Note 1. Ports 00 to 02, 07, ports 12, 13, 16, 17, ports 20, 21, and port 33 are 5 V tolerant.

Note 2. Connect AVCC to VCC. When neither the A/D converter nor the D/A converter is in use, do not leave the AVCC, VREFH, AVSS, and VREFL pins open. Connect the AVCC and VREFH pins to VCC, and the AVSS and VREFL pins to VSS, respectively.

## 5.2 DC Characteristics

**Table 5.2 DC Characteristics (1)**

Conditions: VCC = PLLVCC = AVCC = VCC_USB = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC
VSS = PLLVSS = AVSS = VREFL = VSS_USB = 0 V
$T_a$ = -40 to +85°C

| Item | | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| Schmitt trigger input voltage | IRQ input pin*1<br>MTU input pin*1<br>TMR input pin*1<br>SCI input pin*1<br>ADTRG input pin*1<br>RES#, NMI | $V_{IH}$ | VCC × 0.8 | — | VCC+0.3 | V | |
| | | $V_{IL}$ | -0.3 | — | VCC × 0.2 | | |
| | | $\Delta V_T$ | VCC × 0.06 | — | — | | |
| | RIIC input pin<br>(except for SMBus) | $V_{IH}$ | VCC × 0.7 | — | 5.8 | | |
| | | $V_{IL}$ | -0.3 | — | VCC × 0.3 | | |
| | | $\Delta V_T$ | VCC × 0.05 | — | — | | |
| | Ports 00 to 02, 07<br>ports 12, 13, 16, 17<br>ports 20, 21<br>port 33 | $V_{IH}$ | VCC × 0.8 | — | 5.8 | | |
| | | $V_{IL}$ | -0.3 | — | VCC × 0.2 | | |
| | Ports 03, 05, 10, 11, 14, 15<br>ports 22 to 27<br>ports 30 to 32, 34, 35<br>ports 4 to G<br>Other input pins | $V_{IH}$ | VCC × 0.8 | — | VCC+0.3 | | |
| | | $V_{IL}$ | -0.3 | — | VCC × 0.2 | | |
| Input high voltage (except Schmitt trigger input pin) | MD pin, EMLE | $V_{IH}$ | VCC × 0.9 | — | VCC+0.3 | V | |
| | EXTAL, RSPI, ETHERC<br>EXDMAC, WAIT#, TCK | | VCC × 0.8 | — | VCC+0.3 | | |
| | XCIN | | VCC × 0.8 | — | VCC+0.3 | | |
| | D0 to D31 | | VCC × 0.7 | — | VCC+0.3 | | |
| | RIIC (SMBus) | | 2.1 | — | VCC+0.3 | | |
| Input low voltage (except Schmitt trigger input pin) | MD pin, EMLE | $V_{IL}$ | -0.3 | — | VCC × 0.1 | V | |
| | EXTAL, RSPI, ETHERC<br>EXDMAC, WAIT#, TCK | | -0.3 | — | VCC × 0.2 | | |
| | XCIN | | -0.3 | — | VCC×0.2 | | |
| | D0 to D31 | | -0.3 | — | VCC×0.3 | | |
| | RIIC (SMBus) | | -0.3 | — | 0.8 | | |

**Table 5.3 DC Characteristics (2)**

Conditions: VCC = PLLVCC = AVCC = VCC_USB = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC
VSS = PLLVSS = AVSS = VREFL = VSS_USB = 0 V
$T_a$ = -40 to +85°C

| Item | | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| Output high voltage | All output pins | $V_{OH}$ | VCC-0.5 | — | — | V | $I_{OH}$ = -1 mA |
| Output low voltage | All output pins (except for RIIC pins) | $V_{OL}$ | — | — | 0.5 | V | $I_{OL}$ = 1.0 mA |
| | RIIC pins | | — | — | 0.4 | V | $I_{OL}$ = 3.0 mA |
| | | | — | — | 0.6 | | $I_{OL}$ = 6.0 mA |
| | RIIC pins (only P12 and P13 in channel 0) | $V_{OL}$ | — | — | 0.4 | V | $I_{OL}$ = 15.0 mA (ICFER.FMPE = 1) |
| | | | — | 0.4 | — | | $I_{OL}$ = 20.0 mA (ICFER.FMPE = 1) |
| Input leakage current | RES#, MD pin, EMLE, NMI | $\lvert I_{in} \rvert$ | — | — | 1.0 | µA | $V_{in}$ = 0 V<br>$V_{in}$ = VCC |
| Three-state leakage current (off state) | Ports 03, 05, 10, 11, 14, 15<br>ports 22 to 27<br>ports 30 to 32, 34, 35<br>ports 4 to G | $\lvert I_{TSI} \rvert$ | — | — | 1.0 | µA | $V_{in}$ = 0 V<br>$V_{in}$ = VCC |
| | Ports 00 to 02, 07, 12, 13<br>Ports 16, 17, 20, 21, 33 | | — | — | 5.0 | | |
| Input pull-up MOS current | Ports 9 to E, G | $-I_p$ | 10 | — | 300 | µA | VCC = 2.7 to 3.6 V<br>$V_{in}$ = 0 V |
| Input capacitance | All input pins (except for ports 12, 13, 20, 21 ports 40 to 47, and EMLE) | $C_{in}$ | — | — | 15 | pF | $V_{in}$ = 0 V<br>f = 1 MHz<br>$T_a$ = 25°C |
| | Ports 12, 13, 20, 21,<br>Ports 40 to 47, EMLE | | — | — | 30 | | |

**Table 5.4 DC Characteristics (3)**

Conditions: VCC = PLLVCC = AVCC = VCC_USB = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC
VSS = PLLVSS = AVSS = VREFL = VSS_USB = 0 V
$T_a$ = -40 to +85°C

| Item | | | | | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|---|---|---|
| Supply current*2 | In operation | Max.*3 | | | $I_{CC}$*4 | — | — | 100 | mA | ICLK = 100 MHz<br>PCLK = 50 MHz<br>BCLK = 50 MHz |
| | | Normal operation | Peripheral function: Clocks supplied*5 | | | — | 48 | — | | |
| | | | Peripheral function: Clocks not supplied*5 | | | — | 35 | — | | |
| | | Increased by BGO operation*6 | | | | — | 15 | — | | |
| | Sleep | | | | | — | 20 | 60 | | |
| | All-module-clock-stop mode*7 | | | | | — | 14 | 28 | | |
| | Standby mode | Software standby mode | | | | — | 0.12 | 3.0 | mA | |
| | | Deep software standby mode | RTC in operation | RAM, USB retained | | — | 30 | 206 | µA | |
| | | | | RAM, USB power supply halted | | — | 26 | 66 | µA | |
| | | | RTC halted | RAM, USB retained | | — | 25 | 200 | µA | |
| | | | | RAM, USB power supply halted | | — | 21 | 60 | µA | |
| Analog power supply current | During 12-bit A/D conversion (per unit) | | | | $AI_{CC}$ | — | 2.5 | 3.0 | mA | |
| | During 10-bit A/D conversion (per unit) | | | | | — | 0.8 | 1.2 | mA | |
| | During D/A conversion (per channel) | | | | | — | 0.3 | 2.0 | µA | |
| | Idle (all units) | | | | | — | 30 | 35 | µA | |
| | During A/D or D/A standby (all units) | | | | | — | 0.1 | 4.0 | µA | |
| Reference power supply current | During 12-bit A/D conversion (per unit) | | | | $AI_{CC}$ | — | 0.5 | 0.7 | mA | |
| | During 10-bit A/D conversion (per unit) | | | | | — | 0.06 | 0.1 | mA | |
| | During D/A conversion (per channel) | | | | | — | 0.6 | 1.0 | mA | |
| | Idle (all units) | | | | | — | 0.4 | 0.6 | mA | |
| | During A/D or D/A standby (all units) | | | | | — | 0.1 | 2.0 | µA | |
| RAM standby voltage | | | | | $V_{RAM}$ | 2.48 | — | — | V | |
| VCC rising gradient | | | | | SVCC | — | — | 20 | ms/V | |

Note 1. The $V_{IH}$ characteristic of the pins multiplexed with 5-V tolerant ports 00 to 02, 07, 12, 13, 16, 17, 20, 21, and 33 is the same as the $V_{IH}$ characteristic of 5-V tolerant ports.
Note 2. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.
Note 3. Measured with clocks supplied to the peripheral functions. This does not include the BGO operation.
Note 4. ICC depends on f (ICLK) as follows. (ICLK: PCLK: BCLK: BCLK pin = 8 : 4: 8: 4)
ICC max. = 0.89 x f + 11 (max.)
ICC typ. = 0.43 x f + 5 (normal operation, peripheral function: clocks supplied)
ICC typ. = 0.30 x f + 5 (normal operation, peripheral function: clocks not supplied)
ICC max. = 0.48 x f + 12 (sleep mode)
Note 5. This does not include the BGO operation.
Note 6. Incremented if data is written to or erased from the ROM or data flash for data storage during the program execution.
Note 7. The values are for reference.

**Table 5.5 Permissible Output Currents**

Conditions: VCC = PLLVCC = AVCC = VCC_USB = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC
VSS = PLLVSS = AVSS = VREFL = VSS_USB = 0 V
$T_a$ = -40 to +85°C

| Item | | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Permissible output low current (average value per pin) | All output pins except for RIIC pins | $I_{OL}$ | — | — | 2.0 | mA |
| | RIIC pins (ICFER.FMPE = 0) | $I_{OL}$ | — | — | 6.0 | mA |
| | RIIC pins (ICFER.FMPE = 1) | $I_{OL}$ | — | — | 20.0 | mA |
| Permissible output low current (max. value per pin) | All output pins except for RIIC pins | $I_{OL}$ | — | — | 4.0 | mA |
| | RIIC pins (ICFER.FMPE = 0) | $I_{OL}$ | — | — | 6.0 | mA |
| | RIIC pins (ICFER.FMPE = 1) | $I_{OL}$ | — | — | 20.0 | mA |
| Permissible output low current (total) | Total of all output pins | $\Sigma I_{OL}$ | — | — | 80 | mA |
| Permissible output high current (average value per pin) | All output pins (except for USB_DPUPE pin) | $-I_{OH}$ | — | — | 2.0 | mA |
| | USB_DPUPE pin | $-I_{OH}$ | — | — | 3.0 | mA |
| Permissible output high current (max. value per pin) | All output pins | $-I_{OH}$ | — | — | 4.0 | mA |
| Permissible output high current (total) | Total of all output pins | $\Sigma-I_{OH}$ | — | — | 80 | mA |

Caution: To protect the LSI's reliability, the output current values should not exceed the permissible output current.

## 5.3 AC Characteristics

**Table 5.6 Operation Frequency Value [176-pin LFBGA/145-pin TFLGA/144-pin LQFP]**

Conditions: VCC = PLLVCC = AVCC = VCC_USB = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC
VSS = PLLVSS = AVSS = VREFL = VSS_USB = 0 V
ICLK = 8 to 100 MHz, PCLK = 8 to 50 MHz, BCLK = 8 to 100 MHz, SDCLK = 8 to 50 MHz
$T_a$ = -40 to +85°C

| Item | | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Operation frequency | System clock (ICLK) | f | 8*1 | — | 100 | MHz |
| | Peripheral module clock (PCLK) | | 8*2 | — | 50 | |
| | External bus clock (BCLK) | | 8 | — | 100 | |
| | BCLK pin output | | 8 | — | 50 | |
| | SDRAM clock (SDCLK) | | 8 | — | 50 | |
| | SDCLK pin output | | 8 | — | 50 | |

Note 1. The ICLK must run at a frequency of at least 12.5 MHz if the Ethernet controller is in use.
Note 2. The PCLK must run at a frequency of at least 24 MHz if the USB is in use.

**Table 5.7 Operation Frequency Value [100-pin LQFP/85-pin TFLGA]**

Conditions: VCC = PLLVCC = AVCC = VCC_USB = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC
VSS = PLLVSS = AVSS = VREFL = VSS_USB = 0 V
ICLK = 8 to 100 MHz, PCLK = 8 to 50 MHz, BCLK = 8 to 50 MHz
$T_a$ = -40 to +85°C

| Item | | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Operation frequency | System clock (ICLK) | f | 8*1 | — | 100 | MHz |
| | Peripheral module clock (PCLK) | | 8*2 | — | 50 | |
| | External bus clock (BCLK) | | 8 | — | 50 | |
| | BCLK pin output | | 8 | — | 25 | |

Note 1. The ICLK must run at a frequency of at least 12.5 MHz if the Ethernet controller is in use.
Note 2. The PCLK must run at a frequency of at least 24 MHz if the USB is in use.

### 5.3.1 Clock Timing

**Table 5.8 Clock Timing**

Conditions: VCC = PLLVCC = AVCC = VCC_USB = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC
VSS = PLLVSS = AVSS = VREFL = VSS_USB = 0 V
$T_a$ = -40 to +85°C

| Item | Symbol | Min. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|
| BCLK pin output cycle time [176-pin LFBGA/145-pin TFLGA/144-pin LQFP] | $t_{Bcyc}$ | 20 | 125 | ns | Figure 5.1 |
| BCLK pin output cycle time [100-pin LQFP/85-pin TFLGA] | $t_{Bcyc}$ | 40 | 125 | ns | |
| BCLK pin output high pulse width | $t_{CH}$ | 5 | — | ns | |
| BCLK pin output low pulse width | $t_{CL}$ | 5 | — | ns | |
| BCLK pin output rising time | $t_{Cr}$ | — | 5 | ns | |
| BCLK pin output falling time | $t_{Cf}$ | — | 5 | ns | |
| SDCLK pin output cycle time | $t_{SDcyc}$ | 20 | 125 | ns | |
| SDCLK pin output high pulse width | $t_{CH}$ | 5 | — | ns | |
| SDCLK pin output low pulse width | $t_{CL}$ | 5 | — | ns | |
| SDCLK pin output rising time | $t_{Cr}$ | — | 5 | ns | |
| SDCLK pin output falling time | $t_{Cf}$ | — | 5 | ns | |
| Oscillation settling time after reset (crystal) | $t_{OSC1}$ | 10 | — | ms | Figure 5.2 |
| Oscillation settling time after leaving software standby mode (crystal) | $t_{OSC2}$ | 10 | — | ms | Figure 5.3 |
| Oscillation settling time after leaving deep software standby mode (crystal) | $t_{OSC3}$ | 10 | — | ms | Figure 5.4 |
| EXTAL external clock output delay settling time | $t_{DEXT}$ | 1 | — | ms | Figure 5.2 |
| EXTAL external clock input low pulse width | $t_{EXL}$ | 30.71 | — | ns | Figure 5.5 |
| EXTAL external clock input high pulse width | $t_{EXH}$ | 30.71 | — | ns | |
| EXTAL external clock rising time | $t_{EXr}$ | — | 5 | ns | |
| EXTAL external clock falling time | $t_{EXf}$ | — | 5 | ns | |
| XCIN sub-clock oscillation settling time | $t_{SUBOSC}$ | 2 | — | s | Figure 5.6 |
| XCIN sub-clock oscillation frequency | $f_{SUB}$ | 32.768 | — | kHz | |
| On-chip oscillator (IWDTCLK) oscillation frequency | $f_{IWDTCLK}$ | 62.5 | 187.5 | kHz | |

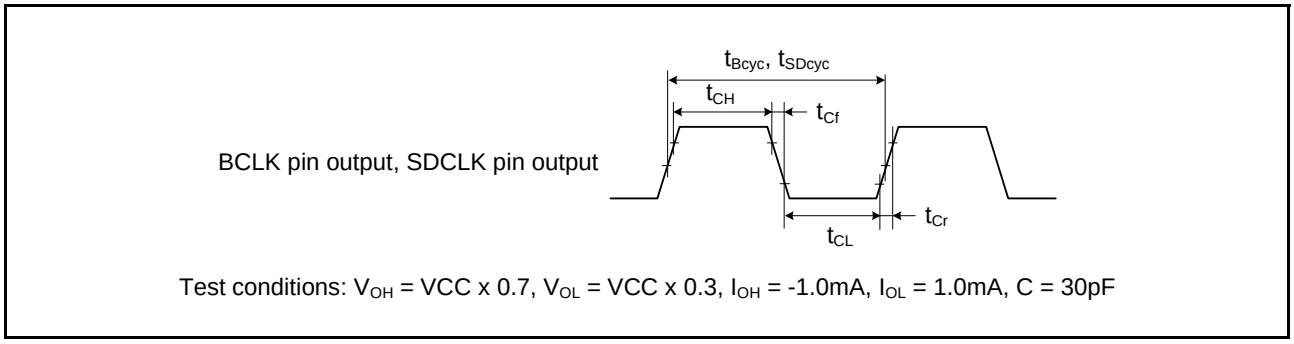



**Figure 5.1 BCLK Pin Output, SDCLK Pin Output Timing**

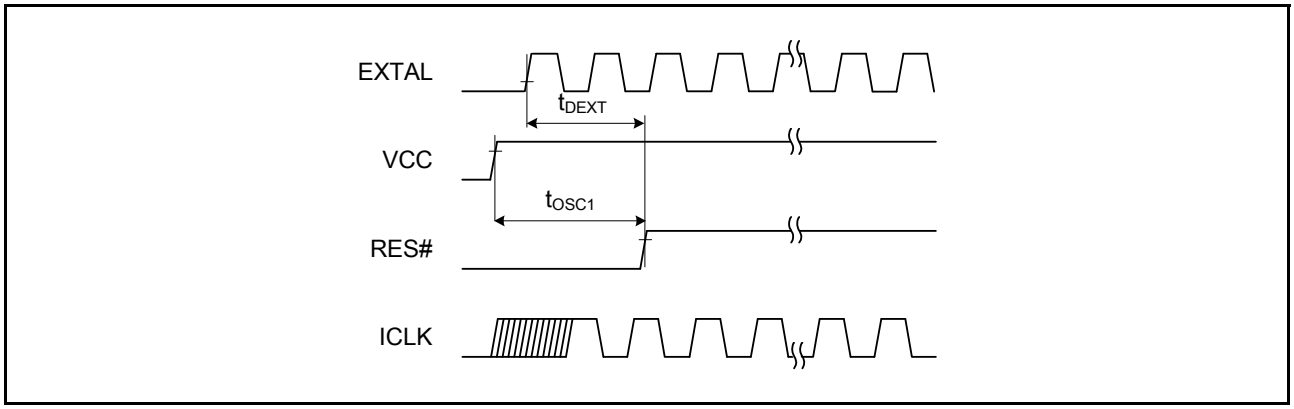



**Figure 5.2 Oscillation Settling Timing**

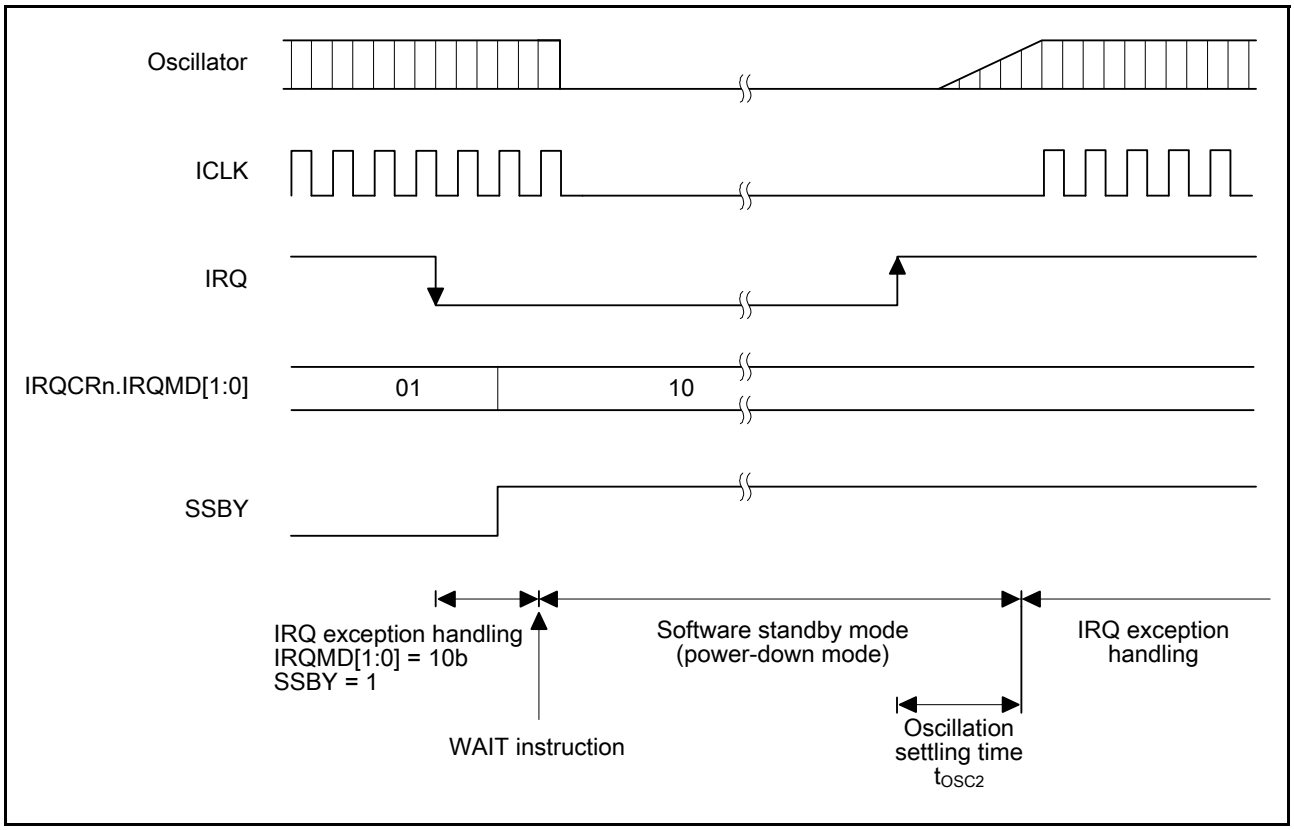



**Figure 5.3 Oscillation Settling Timing after Software Standby Mode**

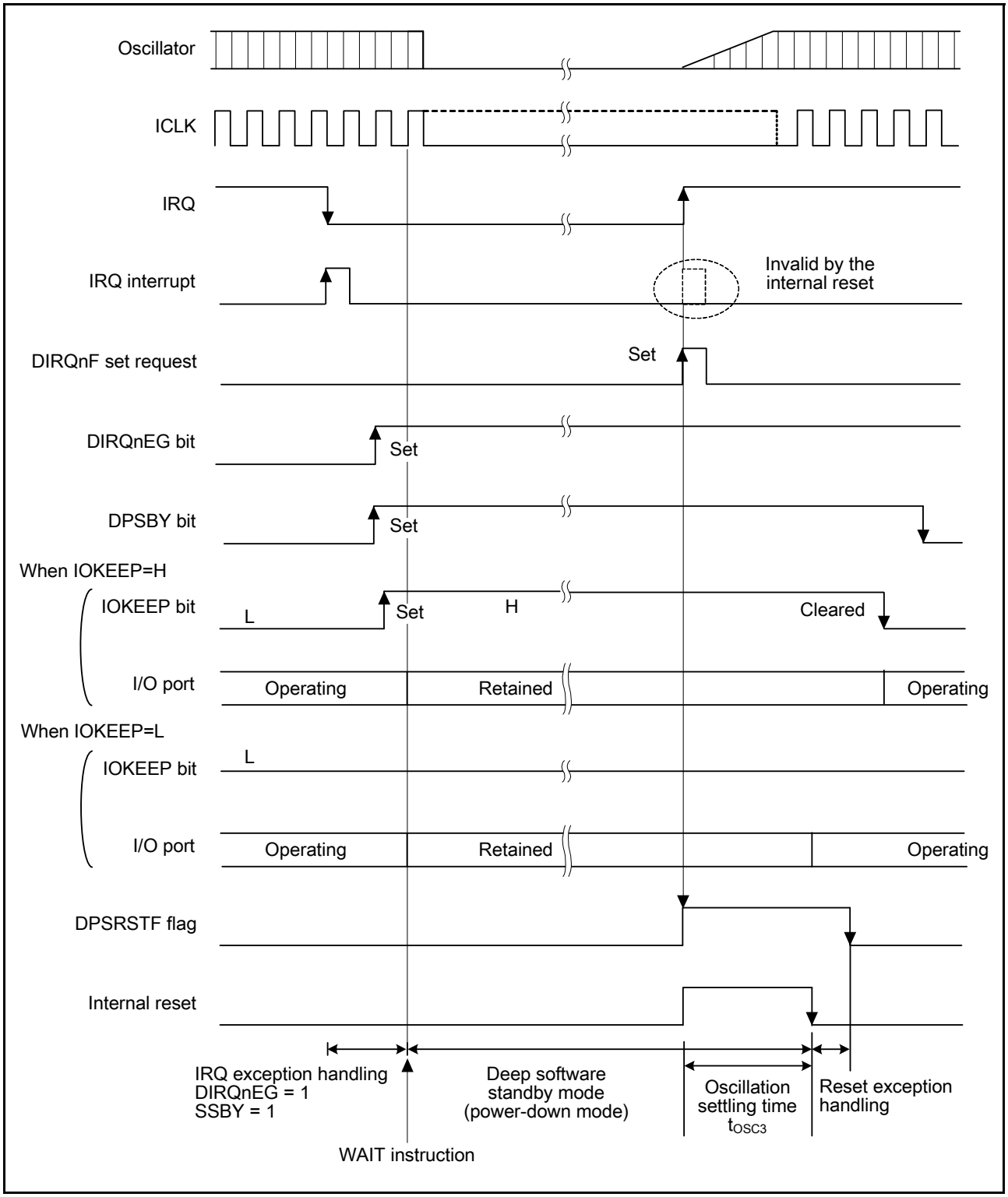



**Figure 5.4 Oscillation Settling Timing after Deep Software Standby Mode**

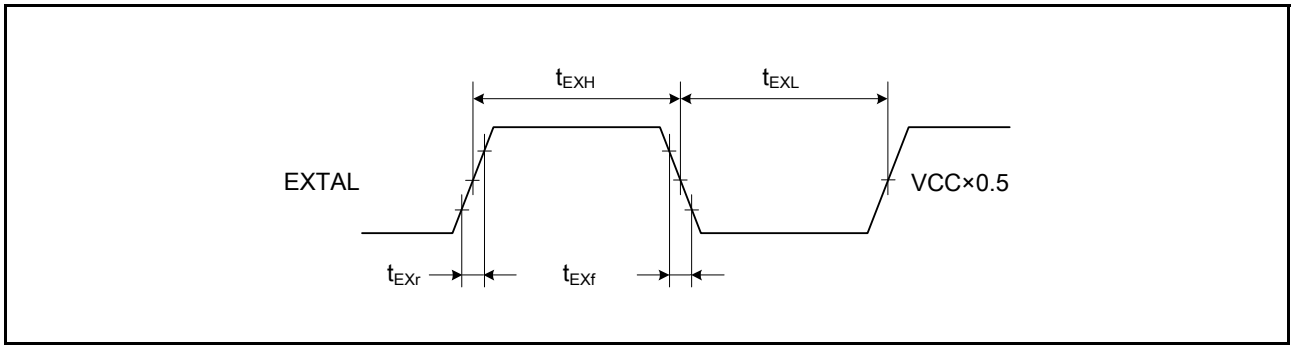



**Figure 5.5 EXTAL External Input Clock Timing**

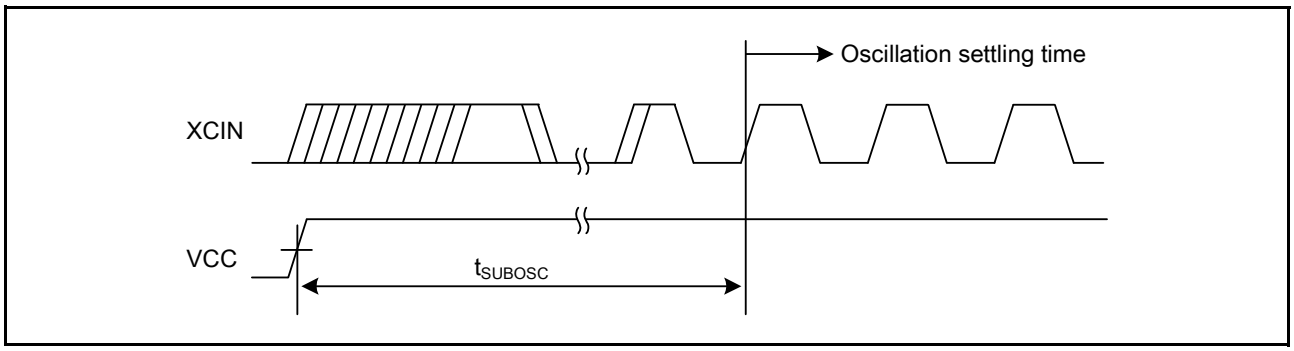



**Figure 5.6 XCIN Sub-Clock Oscillation Settling Time**

### 5.3.2 Control Signal Timing

**Table 5.9 Control Signal Timing**

Conditions: VCC = PLLVCC = AVCC = VCC_USB = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC
VSS = PLLVSS = AVSS = VREFL = VSS_USB = 0 V
$T_a$ = -40 to +85°C

| Item | Symbol | Min. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|
| RES# pulse width (except for programming or erasure of the ROM or data-flash memory or blank checking of the data-flash memory) | $t_{RESW}$*1 | 20 | — | $t_{Icyc}$*3 | Figure 5.7 |
| | | 1.5 | — | µs | |
| Internal reset time*2 | $t_{RESW2}$ | 35 | — | µs | |
| NMI pulse width | $t_{NMIW}$ | 200 | — | ns | Figure 5.8 |
| IRQ pulse width | $t_{IRQW}$ | 200 | — | ns | Figure 5.9 |

Note 1. Both the time and the number of cycles should satisfy the specifications.
Note 2. This is to specify the FCU reset.
Note 3. $t_{Icyc}$: ICLK cycles

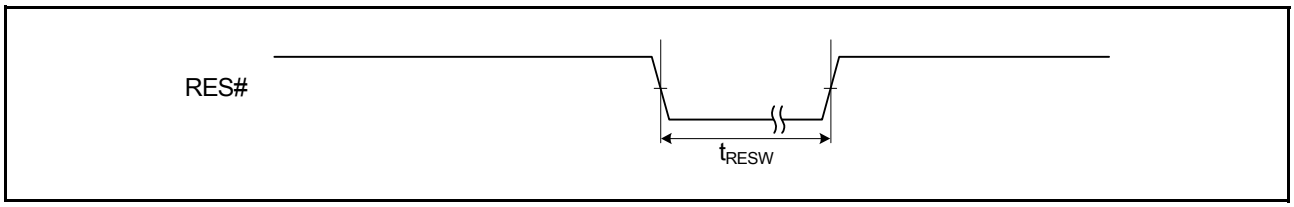



**Figure 5.7 Reset Input Timing**

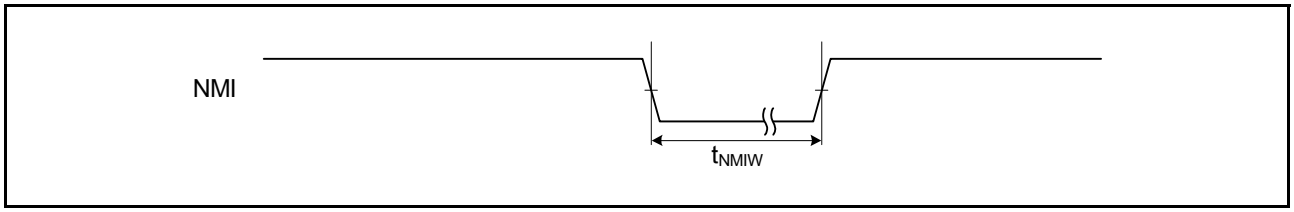



**Figure 5.8 NMI Interrupt Input Timing**

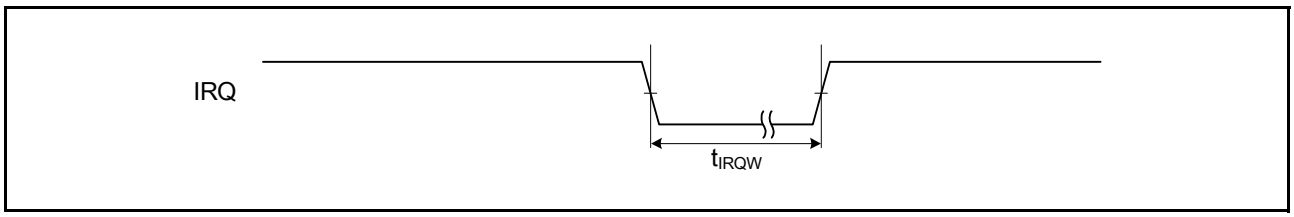



**Figure 5.9 IRQ Interrupt Input Timing**

### 5.3.3 Bus Timing

**Table 5.10 Bus Timing [176-pin LFBGA/145-pin TFLGA/144-pin LQFP]**

Conditions: VCC = PLLVCC = AVCC = VCC_USB = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC
VSS = PLLVSS = AVSS = VREFL = VSS_USB = 0 V
ICLK = 8 to 100 MHz, BCLK = 8 to 100 MHz, SDCLK = 8 to 50 MHz
$T_a$ = -40 to +85°C
Output load conditions: $V_{OH}$ = VCC×0.5, $V_{OL}$ = VCC×0.5, $I_{OH}$ = -1.0 mA, $I_{OL}$ = 1.0 mA, C = 30 pF

| Item | Symbol | Min. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|
| Address delay time | $t_{AD}$ | — | 15 | ns | Figure 5.10 to Figure 5.13 |
| Byte control delay time | $t_{BCD}$ | — | 15 | ns | |
| CS# delay time | $t_{CSD}$ | — | 15 | ns | |
| RD# delay time | $t_{RSD}$ | — | 15 | ns | |
| Read data setup time | $t_{RDS}$ | 15 | — | ns | |
| Read data hold time | $t_{RDH}$ | 0.0 | — | ns | |
| WR# delay time | $t_{WRD}$ | — | 15 | ns | |
| Write data delay time | $t_{WDD}$ | — | 15 | ns | |
| Write data hold time | $t_{WDH}$ | 0 | — | ns | |
| WAIT# setup time | $t_{WTS}$ | 15 | — | ns | Figure 5.14 |
| WAIT# hold time | $t_{WTH}$ | 0.0 | — | ns | |
| Address delay time 2 (SDRAM) | $t_{AD2}$ | 1 | 15 | ns | Figure 5.22 to Figure 5.28 |
| CS# delay time 2 (SDRAM) | $t_{CSD2}$ | 1 | 15 | ns | |
| DQM delay time (SDRAM) | $t_{DQMD}$ | 1 | 15 | ns | |
| CKE delay time (SDRAM) | $t_{CKED}$ | 1 | 15 | ns | |
| Read data setup time 2 (SDRAM) | $t_{RDS2}$ | 12 | — | ns | |
| Read data hold time 2 (SDRAM) | $t_{RDH2}$ | 0 | — | ns | |
| Write data delay time 2 (SDRAM) | $t_{WDD2}$ | — | 15 | ns | |
| Write data hold time 2 (SDRAM) | $t_{WDH2}$ | 1 | — | ns | |
| WE# delay time (SDRAM) | $t_{WED}$ | 1 | 15 | ns | |
| RAS# delay time (SDRAM) | $t_{RASD}$ | 1 | 15 | ns | |
| CAS# delay time (SDRAM) | $t_{CASD}$ | 1 | 15 | ns | |

**Table 5.11 Bus Timing [100-pin LQFP/85-pin TFLGA]**

Conditions: VCC = PLLVCC = AVCC = VCC_USB = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC
VSS = PLLVSS = AVSS = VREFL = VSS_USB = 0 V
ICLK = 8 to 100 MHz, PCLK = 8 to 50 MHz, BCLK = 8 to 50 MHz
$T_a$ = -40 to +85°C
Output load conditions: $V_{OH}$ = VCC × 0.5, $V_{OL}$ = VCC × 0.5, $I_{OH}$ = -1.0 mA, $I_{OL}$ = 1.0 mA, C = 30 pF

| Item | Symbol | Min. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|
| Address delay time | $t_{AD}$ | — | 30 | ns | Figure 5.10 to Figure 5.13 |
| Byte control delay time | $t_{BCD}$ | — | 30 | ns | |
| CS# delay time | $t_{CSD}$ | — | 30 | ns | |
| RD# delay time | $t_{RSD}$ | — | 30 | ns | |
| Read data setup time | $t_{RDS}$ | 15 | — | ns | |
| Read data hold time | $t_{RDH}$ | 0.0 | — | ns | |
| WR# delay time | $t_{WRD}$ | — | 30 | ns | |
| Write data delay time | $t_{WDD}$ | — | 35 | ns | |
| Write data hold time | $t_{WDH}$ | 0 | — | ns | |
| WAIT# setup time | $t_{WTS}$ | 15 | — | ns | Figure 5.14 |
| WAIT# hold time | $t_{WTH}$ | 0.0 | — | ns | |

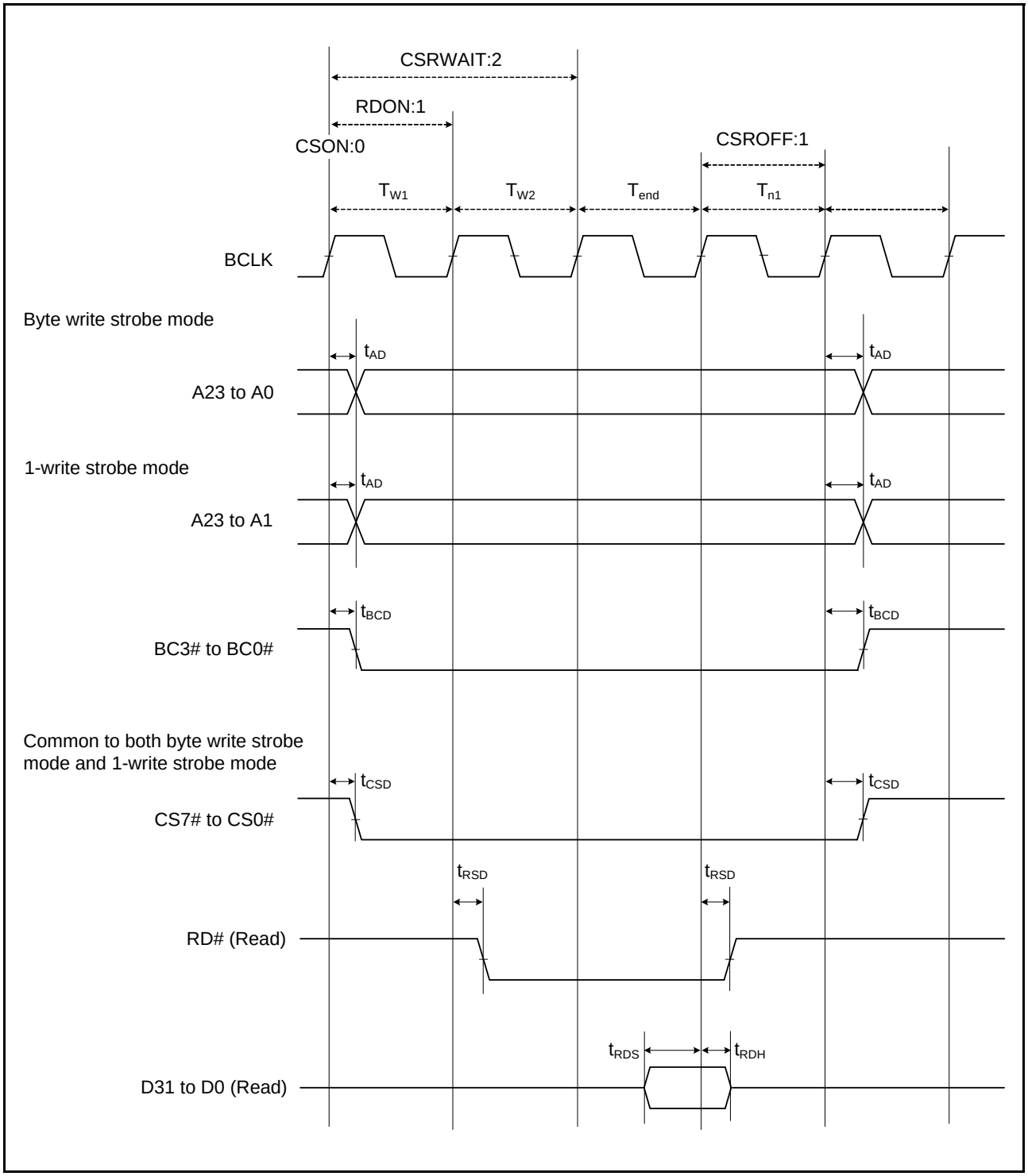
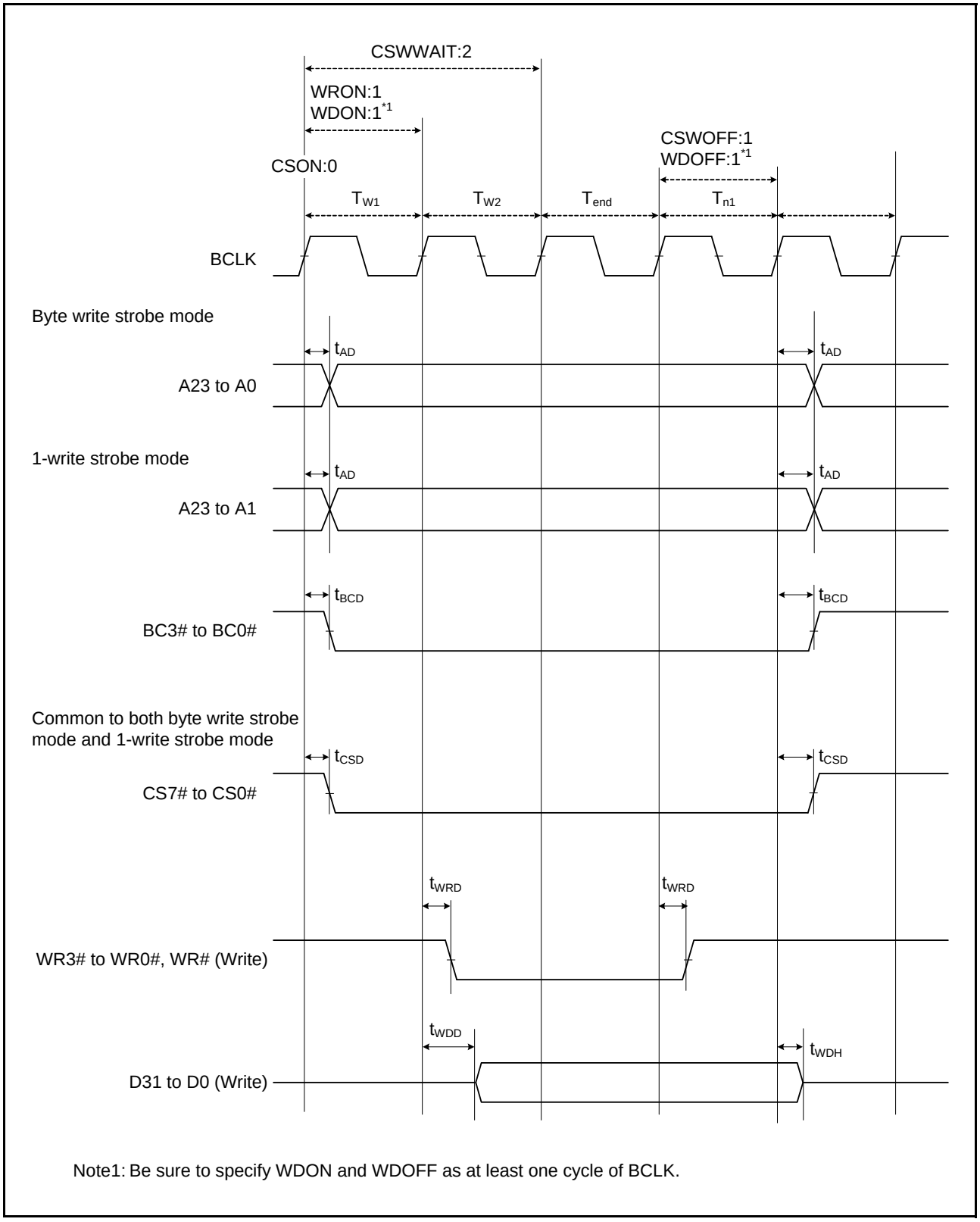



**Figure 5.10 External Bus Timing/Normal Read Cycle (Bus Clock Synchronized)**




Note1: Be sure to specify WDON and WDOFF as at least one cycle of BCLK.

**Figure 5.11 External Bus Timing/Normal Write Cycle (Bus Clock Synchronized)**

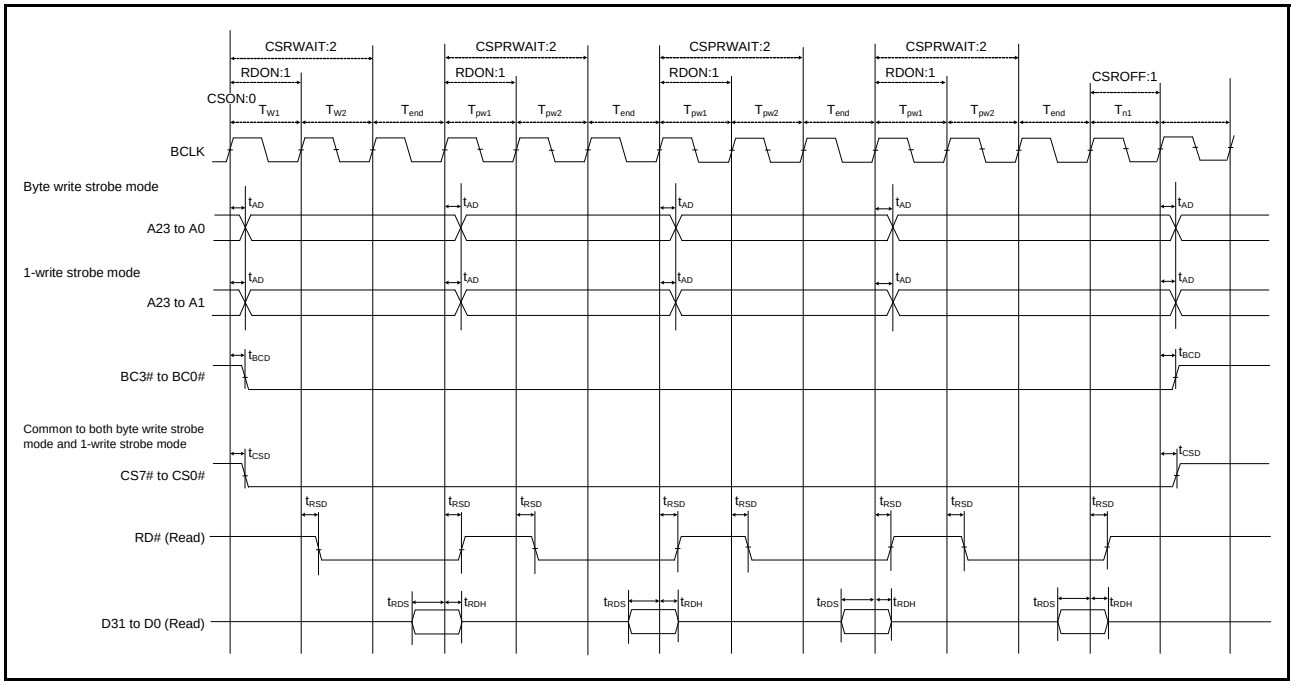



**Figure 5.12 External Bus Timing/Page Read Cycle (Bus Clock Synchronized)**

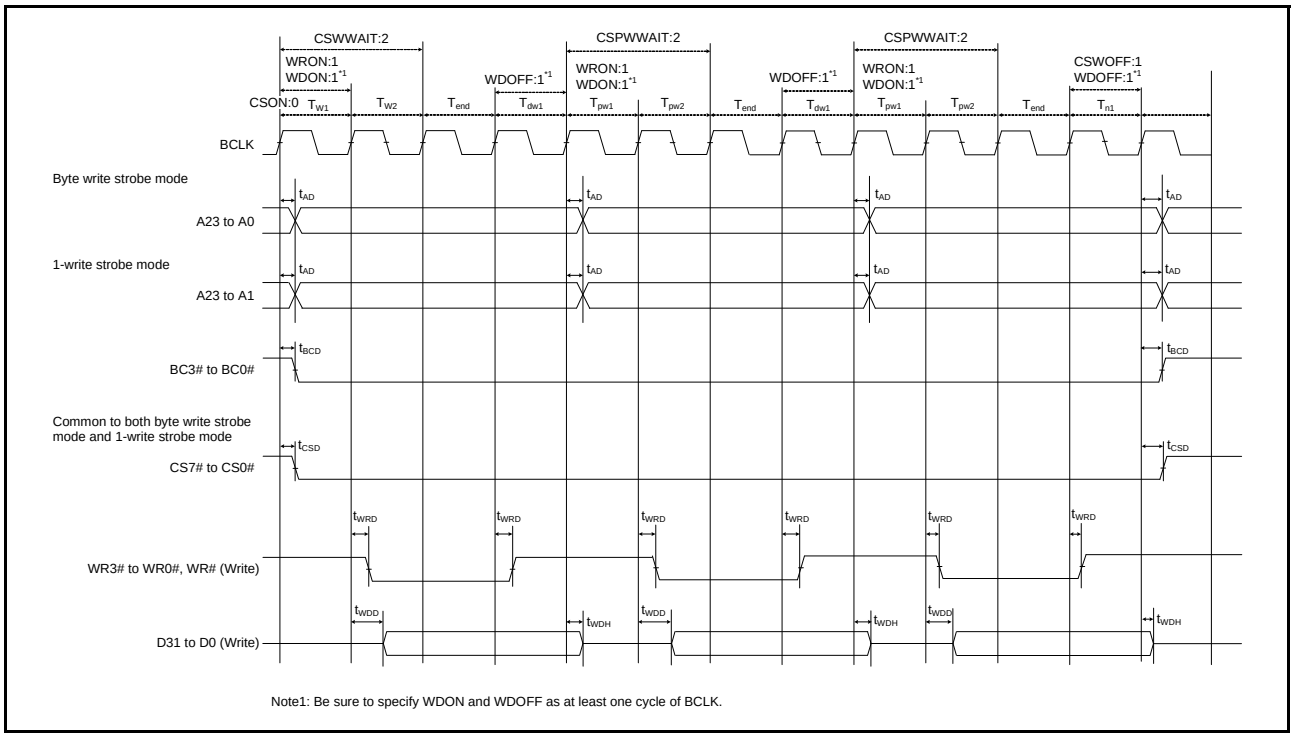



**Figure 5.13 External Bus Timing/Page Write Cycle (Bus Clock Synchronized)**

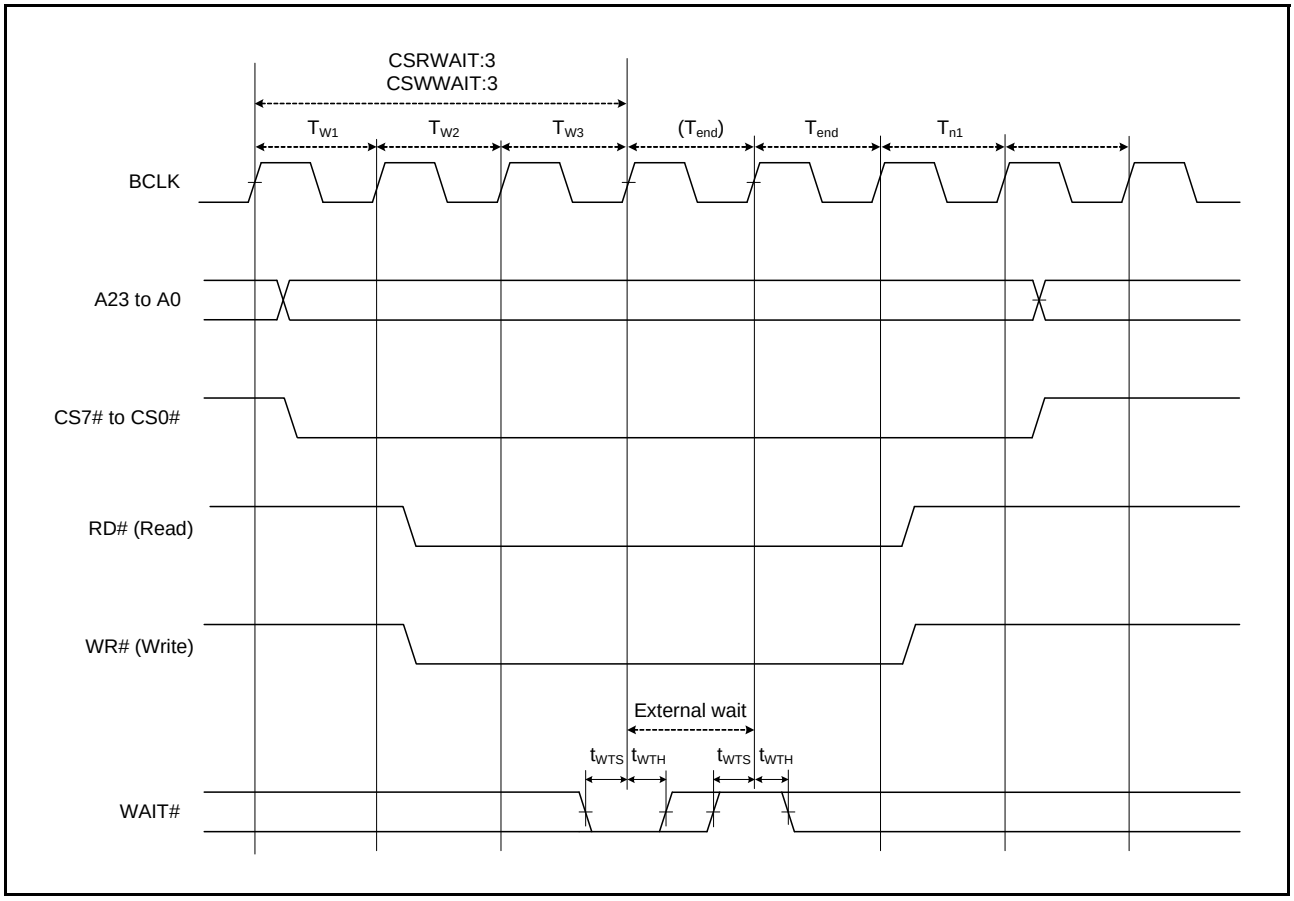



**Figure 5.14 External Bus Timing/External Wait Control**

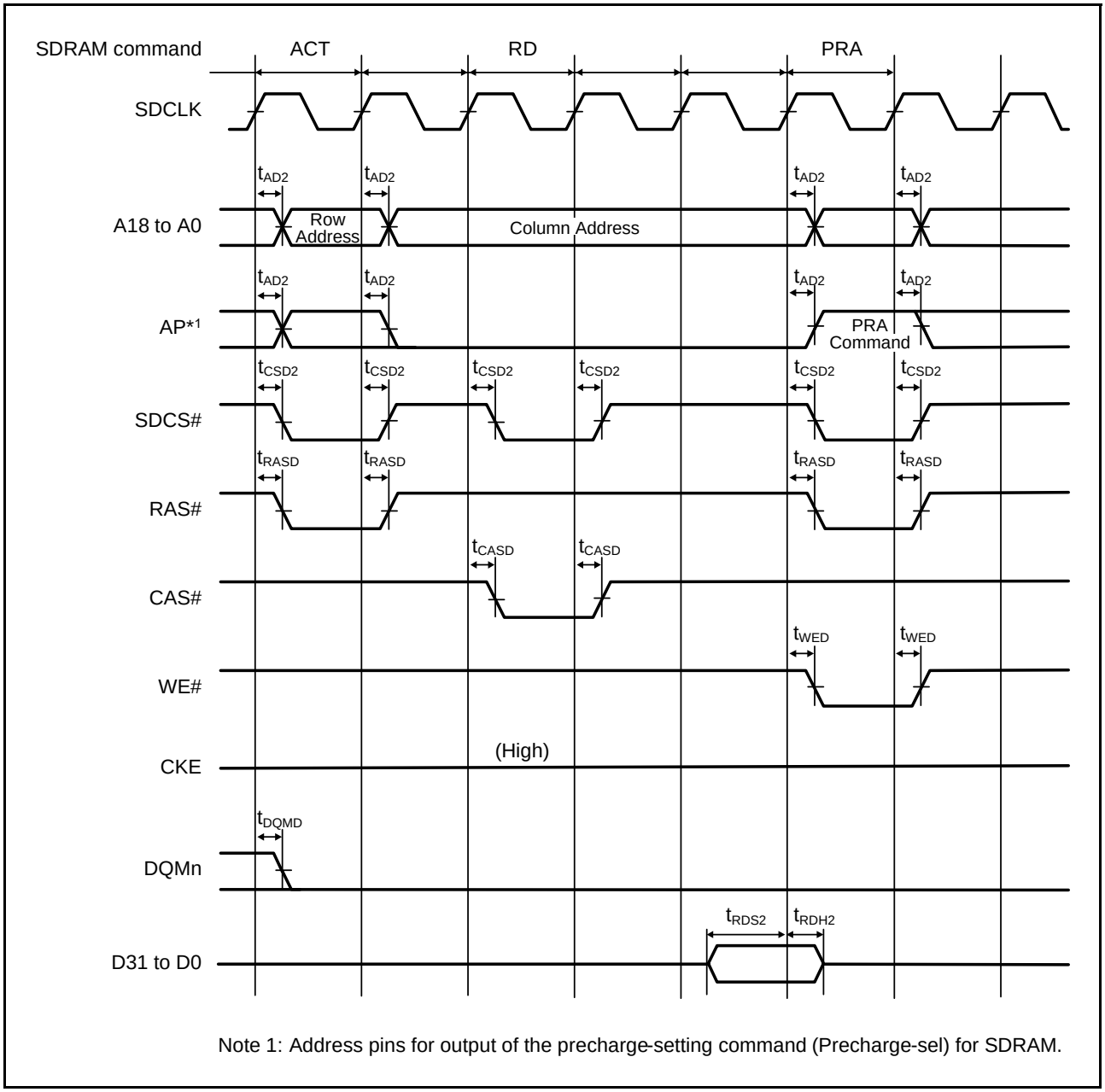



**Figure 5.15 SDRAM Space Single Read Bus Timing**

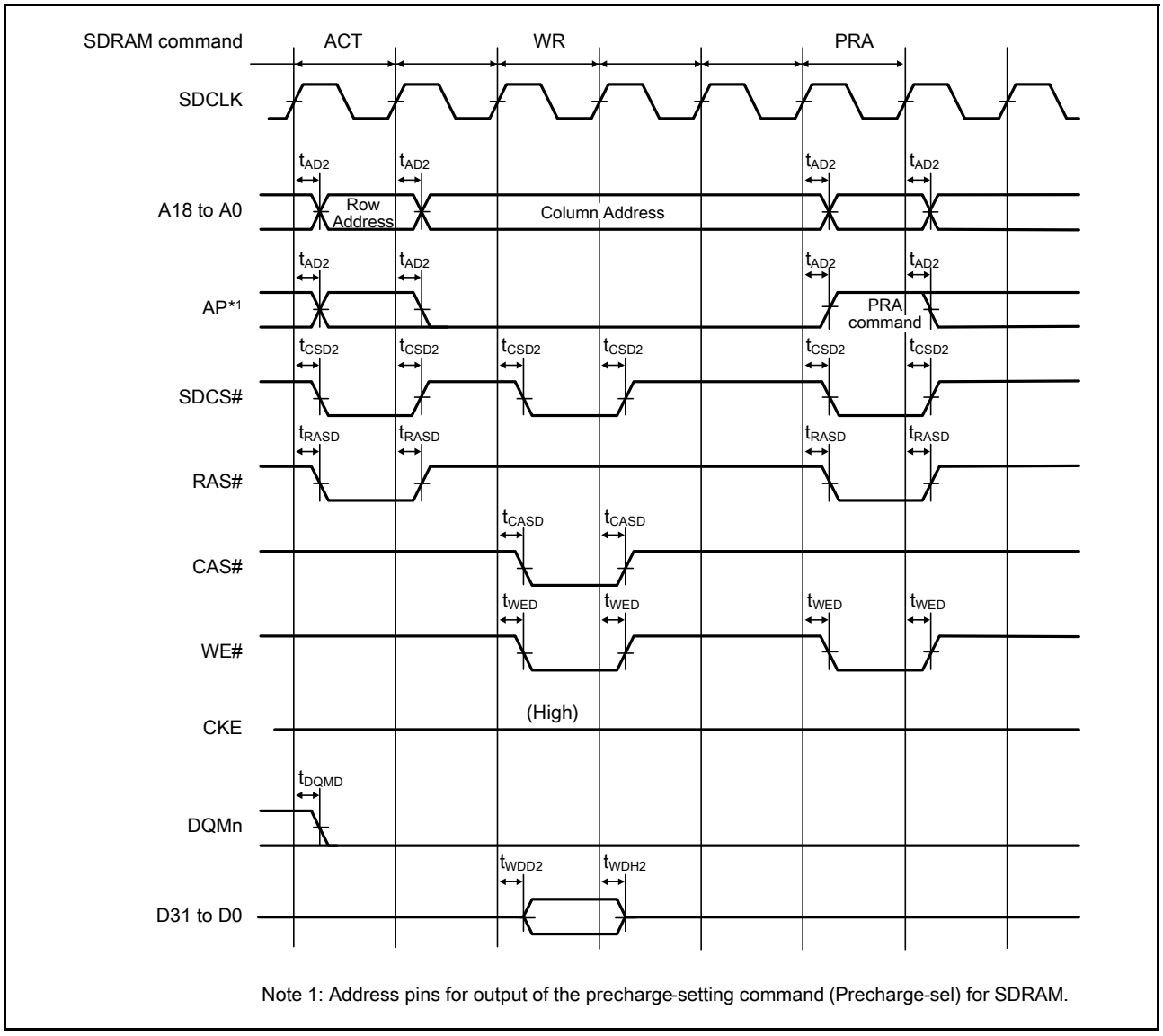
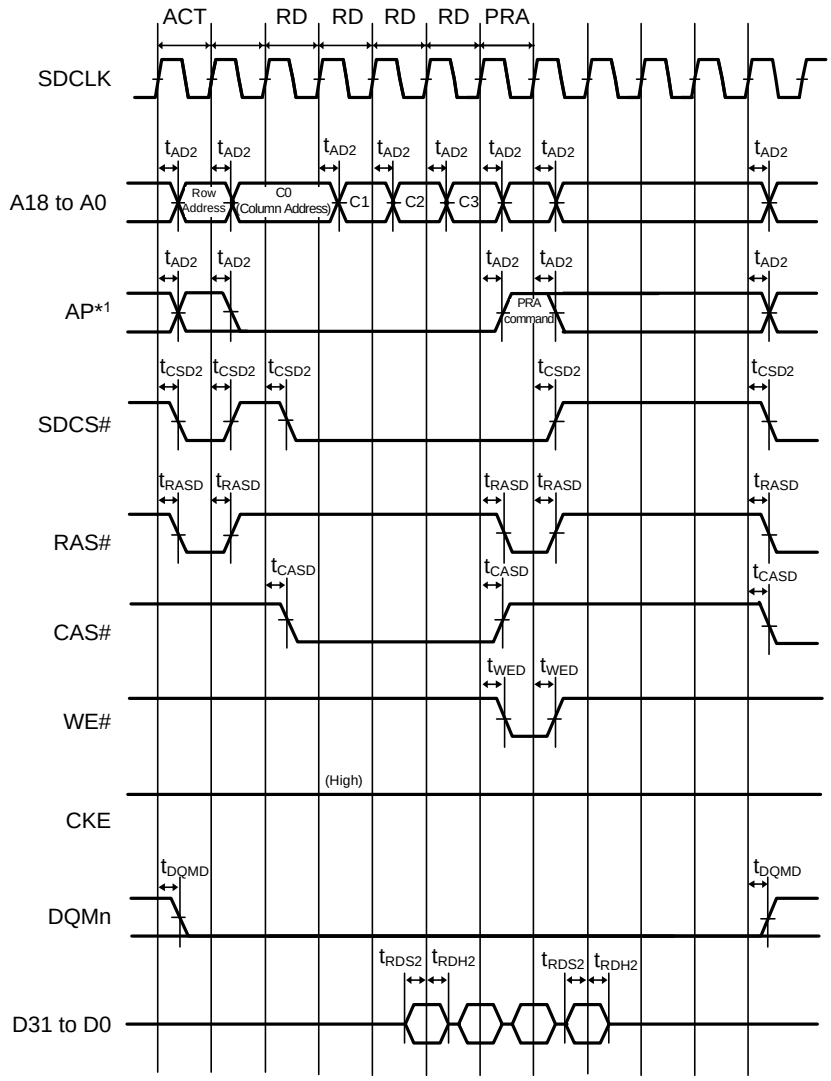
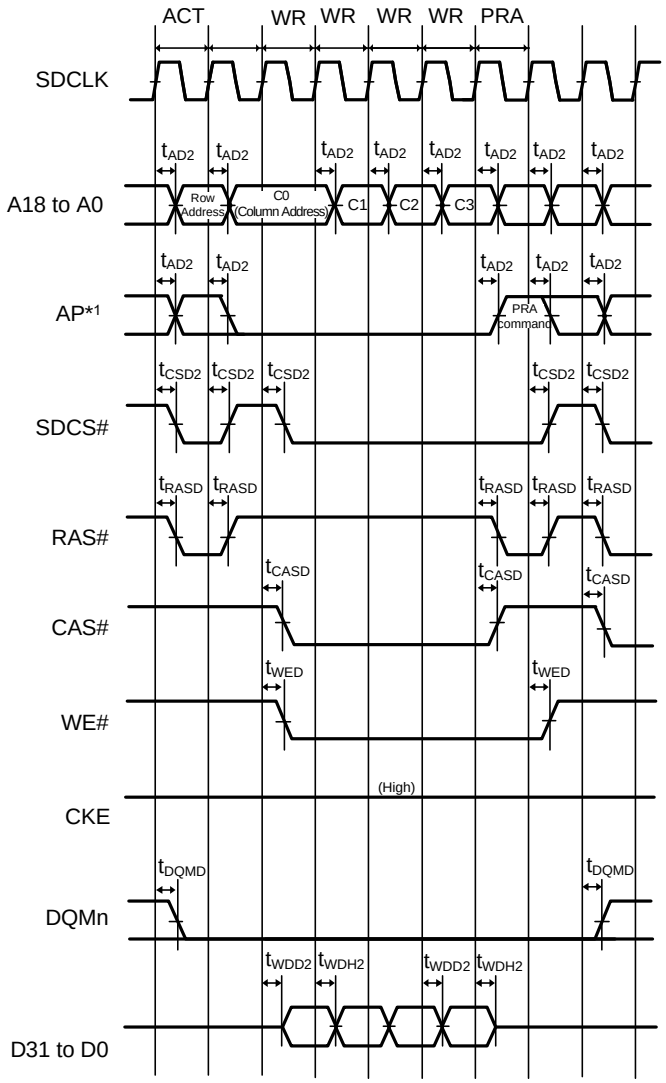



**Figure 5.16 SDRAM Space Single Write Bus Timing**



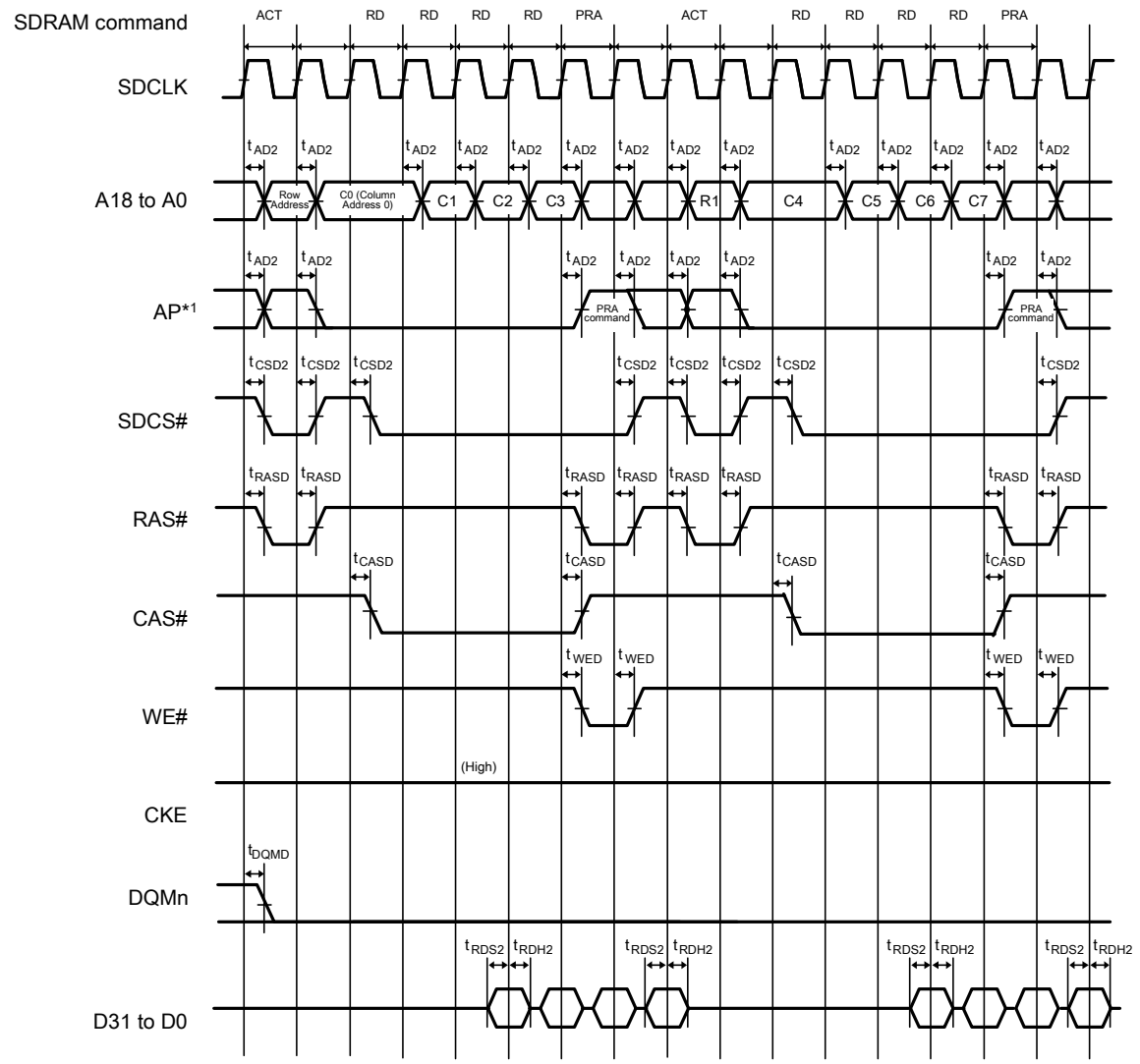

Note 1: Address pins for output of the precharge-setting command (Precharge-sel) for SDRAM.

**Figure 5.17 SDRAM Space Multiple Read Bus Timing**



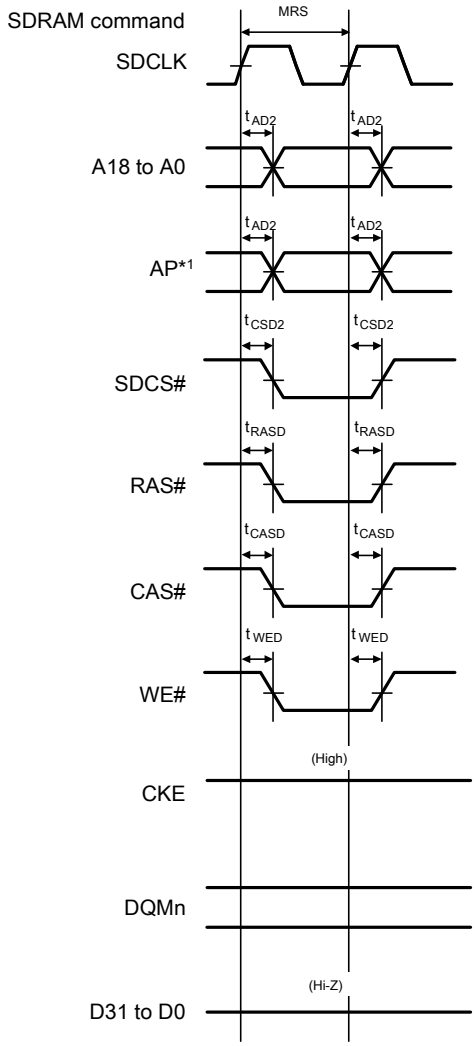

Note 1: Address pins for output of the precharge-setting command (Precharge-sel) for SDRAM.

**Figure 5.18 SDRAM Space Multiple Write Bus Timing**



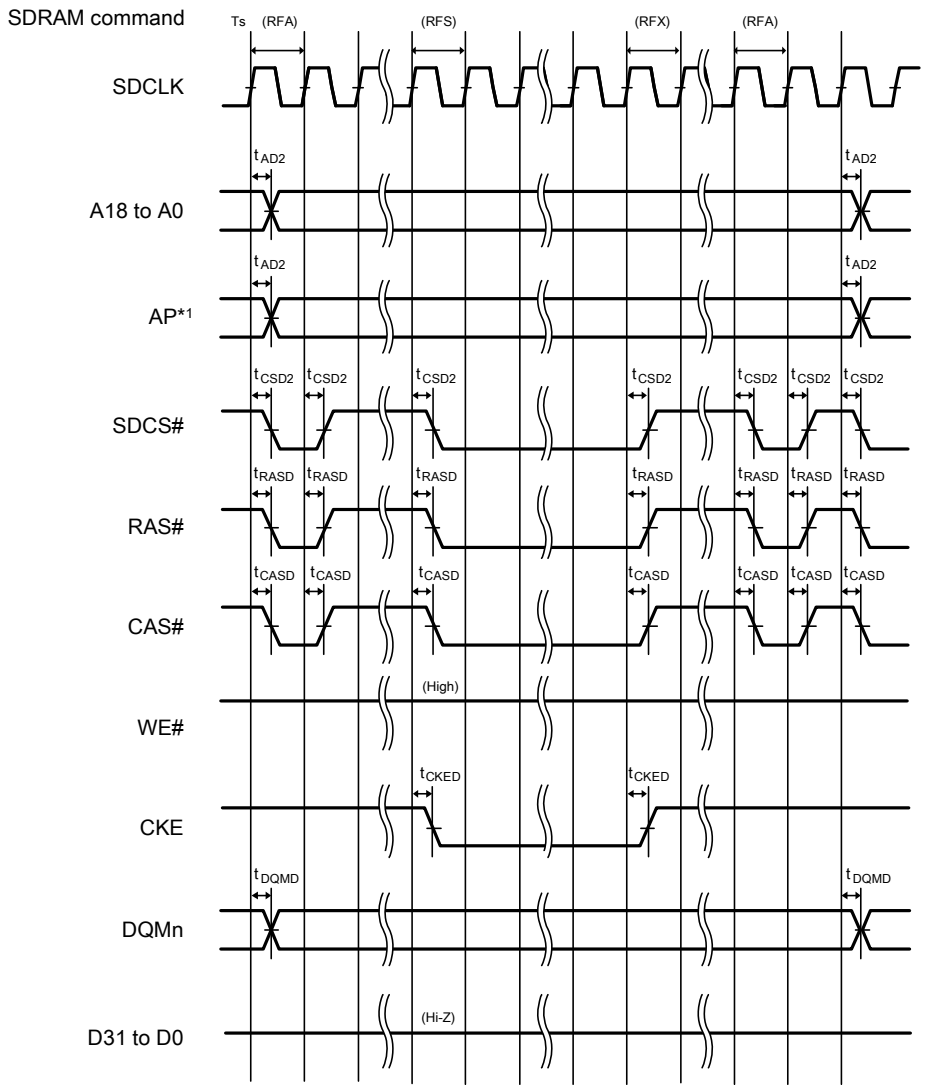

Note 1: Address pins for output of the precharge-setting command (Precharge-sel) for SDRAM.

**Figure 5.19 SDRAM Space Multiple Read Line Stride Bus Timing**




Note 1: Address pins for output of the precharge-setting command (Precharge-sel) for SDRAM.

**Figure 5.20 SDRAM Space Mode Register Set Bus Timing**




Note 1: Address pins for output of the precharge-setting command (Precharge-sel) for SDRAM.

**Figure 5.21 SDRAM Space Self-Refresh Bus Timing**

### 5.3.4 EXDMAC Timing

**Table 5.12 EXDMAC Timing**

Conditions: VCC = PLLVCC = AVCC = VCC_USB = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC
VSS = PLLVSS = AVSS = VREFL = VSS_USB = 0 V
ICLK = 8 to 100 MHz, PCLK = 8 to 50 MHz, BCLK = 8 to 100 MHz, SDCLK = 8 to 50 MHz
$T_a$ = -40 to +85°C

| Item | | Symbol | Min. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| EXDMAC | EDREQ setup time | $t_{EDRQS}$ | 20 | — | ns | Figure 5.22 |
| | EDREQ hold time | $t_{EDRQH}$ | 5 | — | ns | |
| | EDACK delay time | $t_{EDACD}$ | — | 15 | ns | Figure 5.23 and Figure 5.24 |

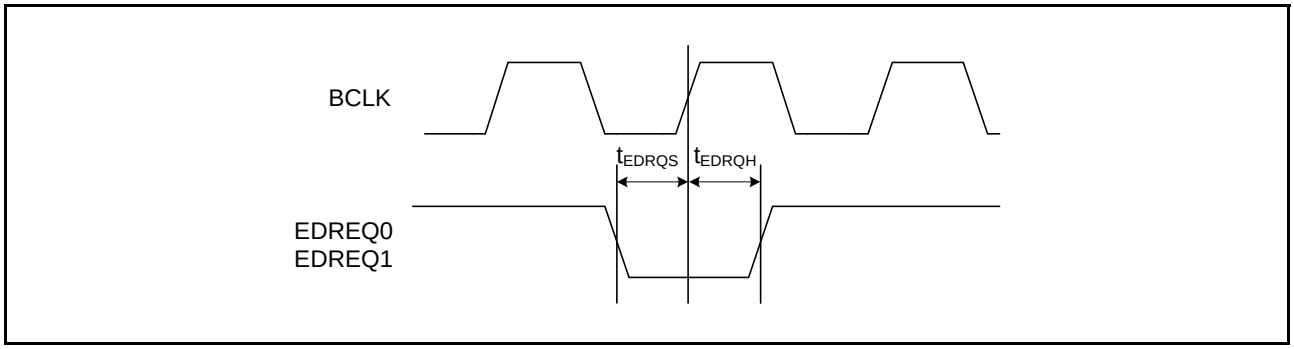



**Figure 5.22 EDREQ0 and EDREQ1 Input Timing**

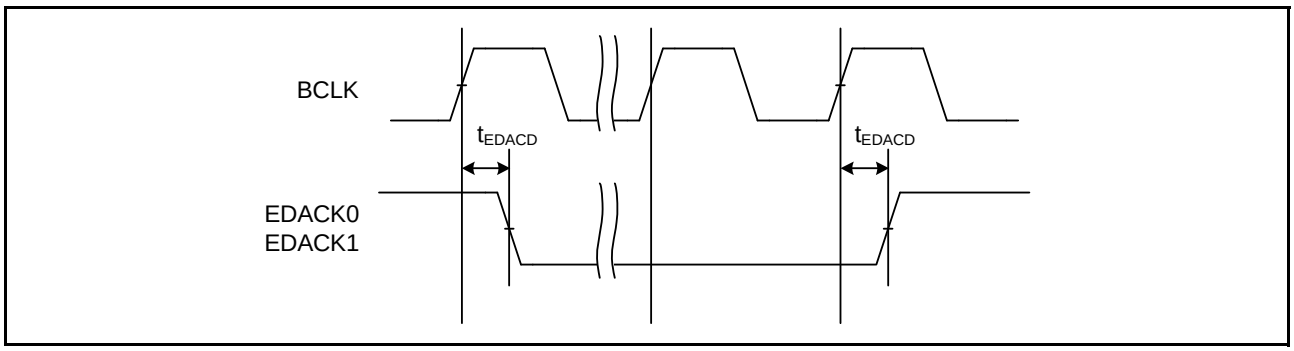



**Figure 5.23 EDACK0 and EDACK1 Single-Address Transfer Timing (for a CS Area)**

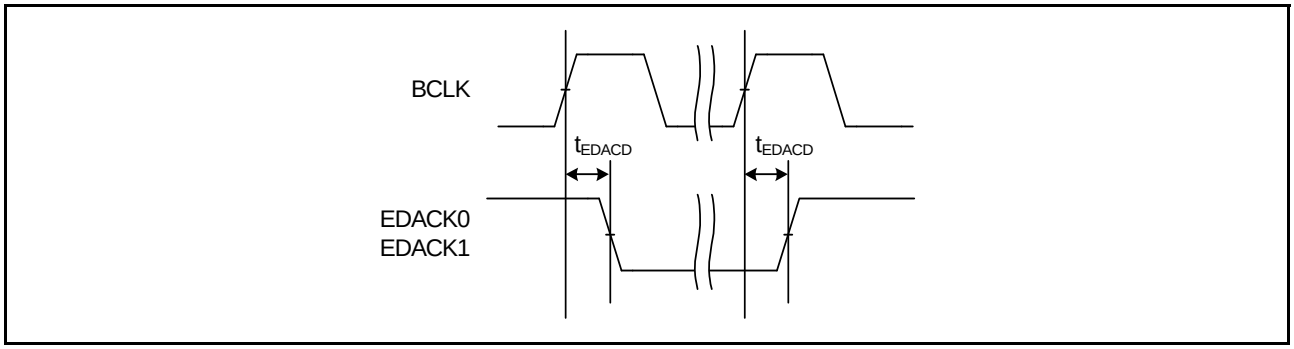



**Figure 5.24 EDACK0 and EDACK1 Single-Address Transfer Timing (for SDRAM)**

## 5.3.5 Timing of On-Chip Peripheral Modules

**Table 5.13 Timing of On-Chip Peripheral Modules (1)**

Conditions: VCC = PLLVCC = AVCC = VCC_USB = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC
VSS = PLLVSS = AVSS = VREFL = VSS_USB = 0 V
PCLK = 8 to 50 MHz
$T_a$ = -40 to +85°C

| Item | | | Symbol | Min. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| I/O ports | Output data delay time | | $t_{PWD}$ | — | 40 | ns | Figure 5.25 |
| | Input data setup time | | $t_{PRS}$ | 25 | — | ns | |
| | Input data hold time | | $t_{PRH}$ | 25 | — | ns | |
| MTU2 | Output compare output delay time | | $t_{TOCD}$ | — | 40 | ns | Figure 5.26 |
| | Input capture input setup time | | $t_{TICS}$ | 20 | — | ns | |
| | Input capture input pulse width (single-edge setting) | | $t_{TICW}$ | 1.5 × $t_{Pcyc}$ | — | ns | |
| | Input capture input pulse width (both-edge setting) | | $t_{TICW}$ | 2.5 × $t_{Pcyc}$ | — | ns | |
| | Timer input setup time | | $t_{TCKS}$ | 20 | — | ns | Figure 5.27 |
| | Timer clock pulse width (single-edge setting) | | $t_{TCKWH/L}$ | 1.5 × $t_{Pcyc}$ | — | ns | |
| | Timer clock pulse width (both-edge setting) | | $t_{TCKWH/L}$ | 2.5 × $t_{Pcyc}$ | — | ns | |
| | Timer clock pulse width (phase counting mode) | | $t_{TCKWH/L}$ | 2.5 × $t_{Pcyc}$ | — | ns | |
| POE2 | POE# input setup time | | $t_{POES}$ | 50 | — | ns | Figure 5.28 |
| | POE# input pulse width | | $t_{POEW}$ | 1.5 × $t_{Pcyc}$ | — | ns | |
| PPG | Pulse output delay time | | $t_{POD}$ | — | 40 | ns | Figure 5.29 |
| 8-bit timer | Timer output delay time | | $t_{TMOD}$ | — | 40 | ns | Figure 5.30 |
| | Timer reset input setup time | | $t_{TMRS}$ | 25 | — | ns | Figure 5.31 |
| | Timer clock input setup time | | $t_{TMCS}$ | 25 | — | ns | Figure 5.32 |
| | Timer clock pulse width | Single-edge setting | $t_{TMCWH}$ | 1.5 × $t_{Pcyc}$ | — | ns | |
| | | Both-edge setting | $t_{TMCWL}$ | 2.5 × $t_{Pcyc}$ | — | ns | |
| WDT | Overflow output delay time | | $t_{WOVD}$ | — | 40 | ns | Figure 5.33 |

**Table 5.13 Timing of On-Chip Peripheral Modules (2)**

Conditions: VCC = PLLVCC = AVCC = VCC_USB = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC
VSS = PLLVSS = AVSS = VREFL = VSS_USB = 0 V
PCLK = 8 to 50 MHz
$T_a$ = -40 to +85°C

| Item | | | Symbol | Min. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| SCI | Input clock cycle | Asynchronous | $t_{Scyc}$ | 4 × $t_{Pcyc}$ | — | ns | Figure 5.34 and Figure 5.35 |
| | | Clock synchronous | | 6 × $t_{Pcyc}$ | — | | |
| | Input clock pulse width | | $t_{SCKW}$ | 0.4 × $t_{Scyc}$ | 0.6 × $t_{Scyc}$ | ns | |
| | Input clock rise time | | $t_{SCKr}$ | — | 20 | ns | |
| | Input clock fall time | | $t_{SCKf}$ | — | 20 | ns | |
| | Output clock cycle | Asynchronous | $t_{Scyc}$ | 16 × $t_{Pcyc}$ | — | ns | |
| | | Clock synchronous | | 4 × $t_{Pcyc}$ | — | | |
| | Output clock pulse width | | $t_{SCKW}$ | 0.4 × $t_{Scyc}$ | 0.6 × $t_{Scyc}$ | ns | |
| | Output clock rise time | | $t_{SCKr}$ | — | 20 | ns | |
| | Output clock fall time | | $t_{SCKf}$ | — | 20 | ns | |
| | Transmit data delay time (clock synchronous) | | $t_{TXD}$ | — | 40 | ns | |
| | Receive data setup time (clock synchronous) | | $t_{RXS}$ | 40 | — | ns | |
| | Receive data hold time (clock synchronous) | | $t_{RXH}$ | 40 | — | ns | |
| A/D converter | 10-bit A/D converter trigger input setup time | | $t_{TRGS}$ | 25 | — | ns | Figure 5.36 |
| | 12-bit A/D converter trigger input setup time | | $t_{TRGS}$ | 25 | — | ns | |

**Table 5.14 Timing of On-Chip Peripheral Modules (3)**

Conditions: VCC = PLLVCC = AVCC = VCC_USB = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC
VSS = PLLVSS = AVSS = VREFL = VSS_USB = 0 V
PCLK = 8 to 50 MHz
$T_a$ = -40 to +85°C

| Item | | | Symbol | Min. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| CAN | Transmit data delay time | | $t_{CTXD}$ | — | 40.0 | ns | Figure 5.37 |
| | Receive data setup time | | $t_{CRXS}$ | 40.0 | — | ns | |
| | Receive data hold time | | $t_{CRXH}$ | 40.0 | — | ns | |
| RSPI | RSPCK clock cycle | Master | $t_{SPcyc}$ | 2 | 4096 | $t_{Pcyc}$ *1 | Figure 5.38 |
| | | Slave | | 8 | 4096 | | |
| | RSPCK clock high pulse width | Master | $t_{SPCKWH}$ | $(t_{SPcyc}-t_{SPCKR}-t_{SPCKF})$ / 2-3 | — | ns | |
| | | Slave | | $(t_{SPcyc}-t_{SPCKR}-t_{SPCKF})$ / 2 | — | | |
| | RSPCK clock low pulse width | Master | $t_{SPCKWL}$ | $(t_{SPcyc}-t_{SPCKR}-t_{SPCKF})$ / 2-3 | — | ns | |
| | | Slave | | $(t_{SPcyc}-t_{SPCKR}-t_{SPCKF})$ / 2 | — | | |
| | RSPCK clock rise/fall time | Output [176-pin LFBGA/ 145-pin TFLGA/ 144-pin LQFP] | $t_{SPCKr}$, $t_{SPCKf}$ | — | 5 | ns | |
| | | Output [100-pin LQFP/ 85-pin TFLGA] | | — | 10 | | |
| | | Input | | — | 1 | µs | |

Note 1. tPcyc: PCLK cycle

**Table 5.14 Timing of On-Chip Peripheral Modules (4)**

Conditions: VCC = PLLVCC = AVCC = VCC_USB = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC
VSS = PLLVSS = AVSS = VREFL = VSS_USB = 0 V
PCLK = 8 to 50 MHz
$T_a$ = -40 to +85°C

| Item | | | Symbol | Min. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| RSPI | Data input setup time | Master [176-pin LFBGA/ 145-pin TFLGA/ 144-pin LQFP] | $t_{SU}$ | 16 | — | ns | Figure 5.39 to Figure 5.42 |
| | | Master [100-pin LQFP/ 85-pin TFLGA] | | 30 | — | | |
| | | Slave | | 20-2 × $t_{Pcyc}$ | — | | |
| | Data input hold time | Master | $t_H$ | 0 | — | ns | |
| | | Slave | | 20+2 × $t_{Pcyc}$ | — | | |
| | SSL setup time | Master | $t_{LEAD}$ | 1 | 8 | $t_{SPcyc}$ | |
| | | Slave | | 4 | — | $t_{Pcyc}$ | |
| | SSL hold time | Master | $t_{LAG}$ | 1 | 8 | $t_{SPcyc}$ | |
| | | Slave | | 4 | — | $t_{Pcyc}$ | |
| | Data output delay time | Master [176-pin LFBGA/ 145-pin TFLGA/ 144-pin LQFP] | $t_{OD}$ | — | 20 | ns | |
| | | Master [100-pin LQFP/ 85-pin TFLGA] | | — | 30 | | |
| | | Slave [176-pin LFBGA/ 145-pin TFLGA/ 144-pin LQFP] | | — | 3 × $t_{Pcyc}$+40 | | |
| | | Slave [100-pin LQFP/ 85-pin TFLGA] | | — | 3 × $t_{Pcyc}$+50 | | |

Note 1. tPcyc: PCLK cycle

**Table 5.15 Timing of On-Chip Peripheral Modules (5)**

Conditions: VCC = PLLVCC = AVCC = VCC_USB = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC
VSS = PLLVSS = AVSS = VREFL = VSS_USB = 0 V
PCLK = 8 to 50 MHz
$T_a$ = -40 to +85°C

| Item | | | Symbol | Min. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| RSPI | Data output hold time | Master | $t_{OH}$ | 0 | — | ns | Figure 5.39 to Figure 5.42 |
| | | Slave | | 0 | — | | |
| | Successive transmission delay time | Master | $t_{TD}$ | $t_{SPcyc}+2 \times t_{Pcyc}$ | $8 \times t_{SPcyc}+2 \times t_{Pcyc}$ | ns | |
| | | Slave | | $4 \times t_{Pcyc}$ | — | | |
| | MOSI, MISO rise/fall time | Output [176-pin LFBGA/ 145-pin TFLGA/ 144-pin LQFP] | $t_{Dr}$, $t_{Df}$ | — | 5 | ns | |
| | | Output [100-pin LQFP/ 85-pin TFLGA] | | — | 10 | | |
| | | Input | | — | 1 | µs | |
| | SSL rise/fall time | Output [176-pin LFBGA 145-pin TFLGA 144-pin LQFP] | $t_{SSLr}$, $t_{SSLf}$ | — | 5 | ns | |
| | | Output [100-pin LQFP/ 85-pin TFLGA] | | — | 10 | | |
| | | Input | | — | 1 | µs | |
| | Slave access time | | $t_{SA}$ | — | 4 | $t_{Pcyc}$ | Figure 5.41 and Figure 5.42 |
| | Slave output release time | | $t_{REL}$ | — | 3 | $t_{Pcyc}$ | |

Note 1. tPcyc: PCLK cycle

**Table 5.16 Timing of On-Chip Peripheral Modules (6)**

Conditions: VCC = PLLVCC = AVCC = VCC_USB = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC
VSS = PLLVSS = AVSS = VREFL = VSS_USB = 0 V
PCLK = 8 to 50 MHz
$T_a$ = -40 to +85°C

| Item | | Symbol | Min.*1*2 | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| RIIC (Standard-mode, SMBus) ICFER.FMPE = 0 | SCL input cycle time | $t_{SCL}$ | 6(12) × $t_{IICcyc}$ + 1300 | — | ns | Figure 5.43 |
| | SCL input high pulse width | $t_{SCLH}$ | 3(6) × $t_{IICcyc}$ + 300 | — | ns | |
| | SCL input low pulse width | $t_{SCLL}$ | 3(6) × $t_{IICcyc}$ + 300 | — | ns | |
| | SCL, SDA input rising time | $t_{Sr}$ | — | 1000 | ns | |
| | SCL, SDA input falling time | $t_{Sf}$ | — | 300 | ns | |
| | SCL, SDA input spike pulse removal time | $t_{SP}$ | 0 | 1(4) × $t_{IICcyc}$ | ns | |
| | SDA input bus free time | $t_{BUF}$ | 3(6) × $t_{IICcyc}$ + 300 | — | ns | |
| | Start condition input hold time | $t_{STAH}$ | $t_{IICcyc}$ + 300 | — | ns | |
| | Re-start condition input setup time | $t_{STAS}$ | 1000 | — | ns | |
| | Stop condition input setup time | $t_{STOS}$ | 1000 | — | ns | |
| | Data input setup time | $t_{SDAS}$ | $t_{IICcyc}$ + 50 | — | ns | |
| | Data input hold time | $t_{SDAH}$ | 0 | — | ns | |
| | SCL, SDA capacitive load | $C_b$ | — | 400 | pF | |
| RIIC (Fast-mode) | SCL input cycle time | $t_{SCL}$ | 6(12) × $t_{IICcyc}$ + 600 | — | ns | |
| | SCL input high pulse width | $t_{SCLH}$ | 3(6) × $t_{IICcyc}$ + 300 | — | ns | |
| | SCL input low pulse width | $t_{SCLL}$ | 3(6) × $t_{IICcyc}$ + 300 | — | ns | |
| | SCL, SDA input rising time | $t_{Sr}$ | 20+0.1$C_b$ | 300 | ns | |
| | SCL, SDA input falling time | $t_{Sf}$ | 20+0.1$C_b$ | 300 | ns | |
| | SCL, SDA input spike pulse removal time | $t_{SP}$ | 0 | 1(4) × $t_{IICcyc}$ | ns | |
| | SDA input bus free time | $t_{BUF}$ | 3(6) × $t_{IICcyc}$ + 300 | — | ns | |
| | Start condition input hold time | $t_{STAH}$ | $t_{IICcyc}$ + 300 | — | ns | |
| | Re-start condition input setup time | $t_{STAS}$ | 300 | — | ns | |
| | Stop condition input setup time | $t_{STOS}$ | 300 | — | ns | |
| | Data input setup time | $t_{SDAS}$ | $t_{IICcyc}$ + 50 | — | ns | |
| | Data input hold time | $t_{SDAH}$ | 0 | — | ns | |
| | SCL, SDA capacitive load | $C_b$ | — | 400 | pF | |

Note: $t_{IICcyc}$: RIIC internal reference clock (IICφ) cycles
Note 1. The value in parentheses is used when ICMR3.NF[1:0] are set to 11b while a digital filter is enabled with ICFER.NFE = 1.
Note 2. $C_b$ indicates the total capacity of the bus line.

**Table 5.16 Timing of On-Chip Peripheral Modules (7)**

Conditions: VCC = PLLVCC = AVCC = VCC_USB = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC
VSS = PLLVSS = AVSS = VREFL = VSS_USB = 0 V
PCLK = 8 to 50 MHz
$T_a$ = -40 to +85°C

| Item | | Symbol | Min.*1*2 | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| RIIC (Fast-mode+) ICFER.FMPE = 1 | SCL input cycle time | $t_{SCL}$ | 6(12) × $t_{IICcyc}$ + 240 | — | ns | Figure 5.43 |
| | SCL input high pulse width | $t_{SCLH}$ | 3(6) × $t_{IICcyc}$ + 120 | — | ns | |
| | SCL input low pulse width | $t_{SCLL}$ | 3(6) × $t_{IICcyc}$ + 120 | — | ns | |
| | SCL, SDA input rising time | $t_{Sr}$ | — | 120 | ns | |
| | SCL, SDA input falling time | $t_{Sf}$ | — | 120 | ns | |
| | SCL, SDA input spike pulse removal time | $t_{SP}$ | 0 | 1(4) × $t_{IICcyc}$ | ns | |
| | SDA input bus free time | $t_{BUF}$ | 3(6) × $t_{IICcyc}$ + 120 | — | ns | |
| | Start condition input hold time | $t_{STAH}$ | $t_{IICcyc}$ + 120 | | ns | |
| | Re-start condition input setup time | $t_{STAS}$ | 120 | — | ns | |
| | Stop condition input setup time | $t_{STOS}$ | 120 | — | ns | |
| | Data input setup time | $t_{SDAS}$ | $t_{IICcyc}$ + 20 | — | ns | |
| | Data input hold time | $t_{SDAH}$ | 0 | — | ns | |
| | SCL, SDA capacitive load | $C_b$ | — | 550 | pF | |

Note: $t_{IICcyc}$: RIIC internal reference clock (IICφ) cycles
Note 1. The value in parentheses is used when ICMR3.NF[1:0] are set to 11b while a digital filter is enabled with ICFER.NFE = 1.
Note 2. $C_b$ indicates the total capacity of the bus line.

**Table 5.17 Timing of On-Chip Peripheral Modules (8)**

Conditions: VCC = PLLVCC = AVCC = VCC_USB = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC
VSS = PLLVSS = AVSS = VREFL = VSS_USB = 0 V
ICLK = 12.5 to 100 MHz
$T_a$ = -40 to +85°C

| Item | | Symbol | Min. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| ETHERC(RMII) | REF50CK cycle time | $T_{ck}$ | 20 | — | ns | Figure 5.44 to Figure 5.47 |
| | REF50CK frequency<br>Typ. 50 MHz | — | — | 50 + 100ppm | MHz | |
| | REF50CK duty | — | 35 | 65 | % | |
| | REF50CK rise/fall time | $T_{ckr/ckf}$ | 0.5 | 3.5 | ns | |
| | RMII_xxxx*1 output delay time | $T_{co}$ | 2.5 | 12.5 | ns | |
| | RMII_xxxx*2 setup time | $T_{su}$ | 3 | — | ns | |
| | RMII_xxxx*2 hold time | $T_{hd}$ | 1 | — | ns | |
| | RMII_xxxx*1*2 rise/fall time | Tr/Tf | 0.5 | 6 | ns | |
| | ET_MDIO setup time | $t_{MDIOs}$ | 10 | — | ns | Figure 5.48 |
| | ET_MDIO hold time | $t_{MDIOh}$ | 10 | — | ns | |
| | ET_MDIO output hold time*3 | $t_{MDIODh}$ | 5 | — | ns | Figure 5.49 |
| | ET_WOL output delay time | $t_{WOLd}$ | 1 | 20 | ns | Figure 5.50 |

Note 1. RMII_TXD_EN, RMII_TXD1, RMII_TXD0
Note 2. RMII_CRS_DV, RMII_RXD1, RMII_RXD0, RMII_RX_ER
Note 3. The user program must make settings so that this stipulation is satisfied.

**Table 5.17 Timing of On-Chip Peripheral Modules (9)**

Conditions: VCC = PLLVCC = AVCC = VCC_USB = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC
VSS = PLLVSS = AVSS = VREFL = VSS_USB = 0 V
ICLK = 12.5 to 100 MHz
$T_a$ = -40 to +85°C

| Item | | Symbol | Min. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| ETHERC(MII) | ET_TX_CLK cycle time | $t_{Tcyc}$ | 40 | — | ns | — |
| | ET_TX_EN output delay time | $t_{TENd}$ | 1 | 20 | ns | Figure 5.51 |
| | ET_ETXD0 to ET_ETXD3 output delay time | $t_{MTDd}$ | 1 | 20 | ns | |
| | ET_CRS setup time | $t_{CRSs}$ | 10 | — | ns | |
| | ET_CRS hold time | $t_{CRSh}$ | 10 | — | ns | |
| | ET_COL setup time | $t_{COLs}$ | 10 | — | ns | Figure 5.52 |
| | ET_COL hold time | $t_{COLh}$ | 10 | — | ns | |
| | ET_RX_CLK cycle time | $t_{TRcyc}$ | 40 | — | ns | — |
| | ET_RX_DV setup time | $t_{RDVs}$ | 10 | | ns | Figure 5.53 |
| | ET_RX_DV hold time | $t_{RDVh}$ | 10 | — | ns | |
| | ET_ERXD0 to ET_ERXD3 setup time | $t_{MRDs}$ | 10 | — | ns | |
| | ET_ERXD0 to ET_ERXD3 hold time | $t_{MRDh}$ | 10 | — | ns | |
| | ET_RX_ER setup time | $t_{RERs}$ | 10 | — | ns | Figure 5.54 |
| | ET_RX_ER hold time | $t_{RESh}$ | 10 | — | ns | |
| | ET_MDIO setup time | $t_{MDIOs}$ | 10 | — | ns | Figure 5.55 |
| | ET_MDIO hold time | $t_{MDIOh}$ | 10 | — | ns | |
| | ET_MDIO utput hold time | $t_{MDIOdh}$ | 5 | — | ns | Figure 5.56 |
| | ET_WOL output delay time | $t_{WOLd}$ | 1 | 20 | ns | Figure 5.57 |

Note 1. RMII_TXD_EN, RMII_TXD1, RMII_TXD0
Note 2. RMII_CRS_DV, RMII_RXD1, RMII_RXD0, RMII_RX_ER
Note 3. The user program must make settings so that this stipulation is satisfied.

**Table 5.18 Timing of On-Chip Peripheral Modules (10)**

Conditions: VCC = PLLVCC = AVCC = VCC_USB = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC
VSS = PLLVSS = AVSS = VREFL = VSS_USB = 0 V
PCLK = 8 to 50 MHz
$T_a$ = -40 to +85°C

| Item | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| TCK clock cycle time | $t_{TCKcyc}$ | 100 | — | — | ns | Figure 5.58 |
| TCK clock high pulse width | $t_{TCKH}$ | 45 | — | — | ns | |
| TCK clock low pulse width | $t_{TCKL}$ | 45 | — | — | ns | |
| TCK clock rising time | $t_{TCKr}$ | — | — | 5 | ns | |
| TCK clock falling time | $t_{TCKf}$ | — | — | 5 | ns | |
| TRST# pulse width | $t_{TRSTW}$ | 20 | — | — | $t_{TCKcyc}$ | Figure 5.59 |
| TMS setup time | $t_{TMSS}$ | 20 | — | — | ns | Figure 5.60 |
| TMS hold time | $t_{TMSH}$ | 20 | — | — | ns | |
| TDI setup time | $t_{TDIS}$ | 20 | — | — | ns | |
| TDI hold time | $t_{TDIH}$ | 20 | — | — | ns | |
| TDO data delay time | $t_{TDOD}$ | — | — | 40 | ns | |

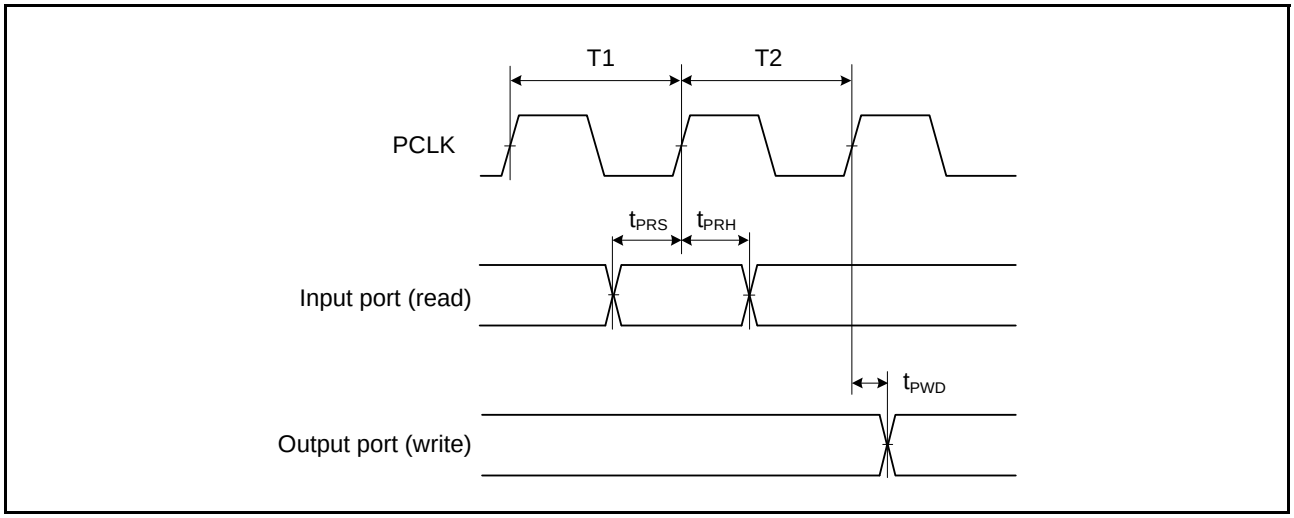



**Figure 5.25 I/O Port Input/Output Timing**

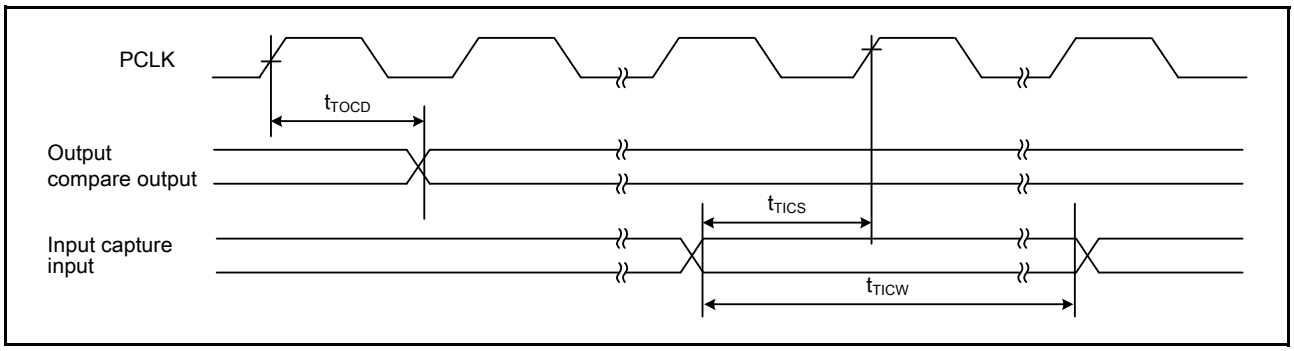



**Figure 5.26 MTU2 Input/Output Timing**

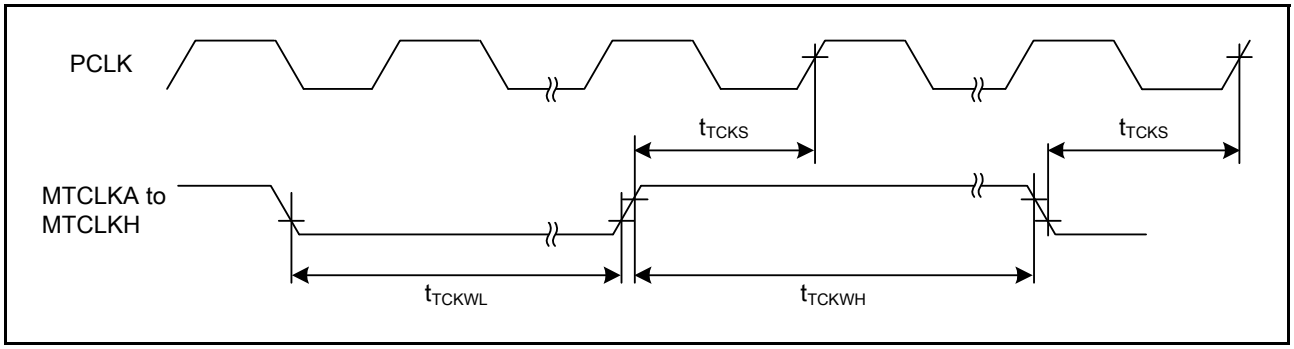



**Figure 5.27 MTU2 Clock Input Timing**

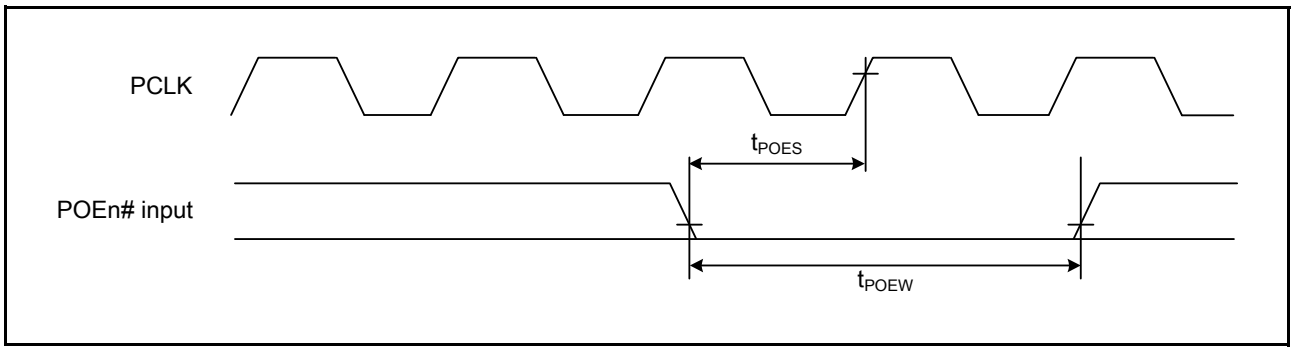



**Figure 5.28 POE# Input Timing**

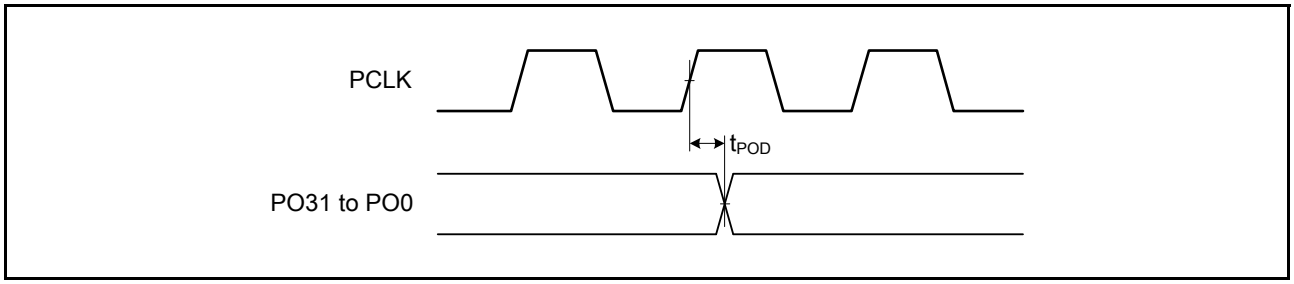



**Figure 5.29 PPG Output Timing**

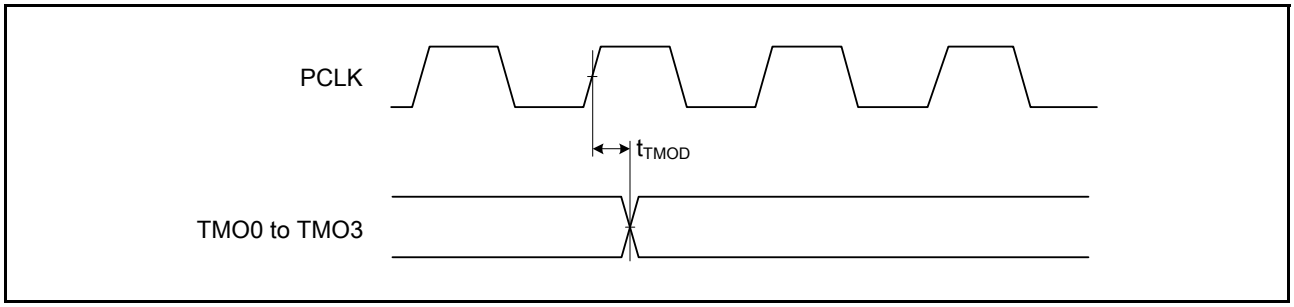



**Figure 5.30 8-Bit Timer Output Timing**

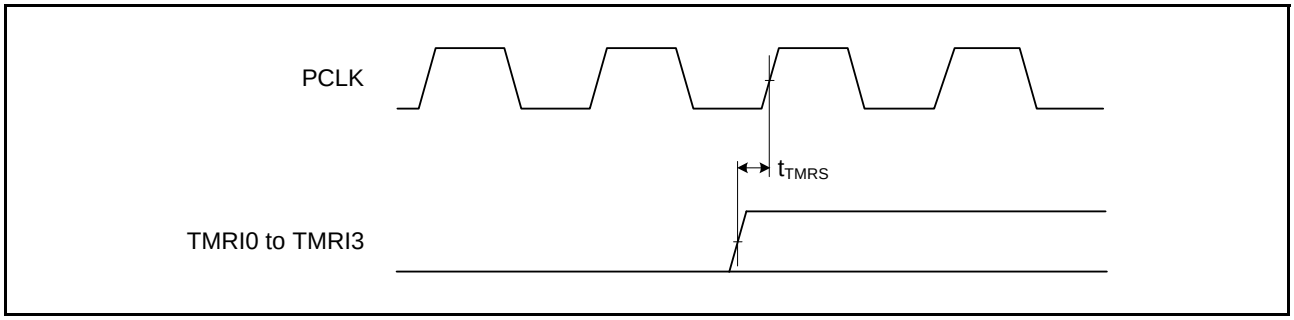



**Figure 5.31 8-Bit Timer Reset Input Timing**

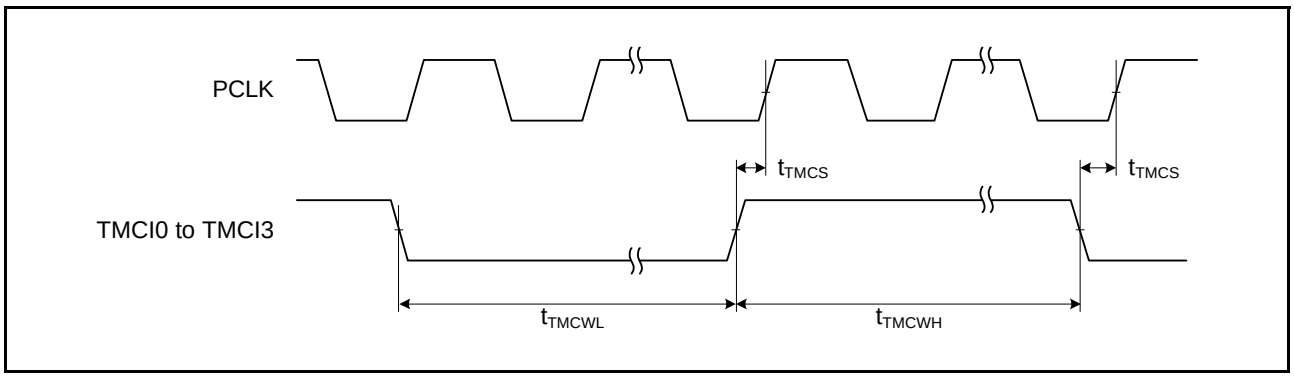



**Figure 5.32 8-Bit Timer Clock Input Timing**

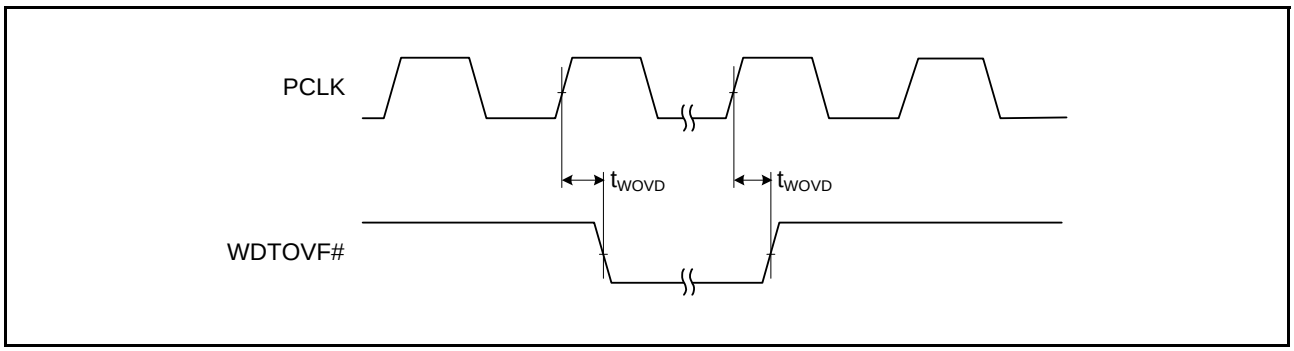



**Figure 5.33 WDT Output Timing**

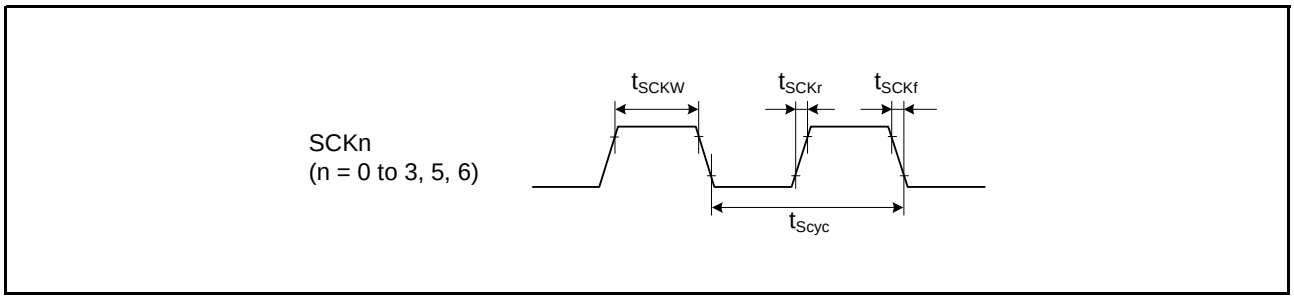



**Figure 5.34 SCK Clock Input Timing**

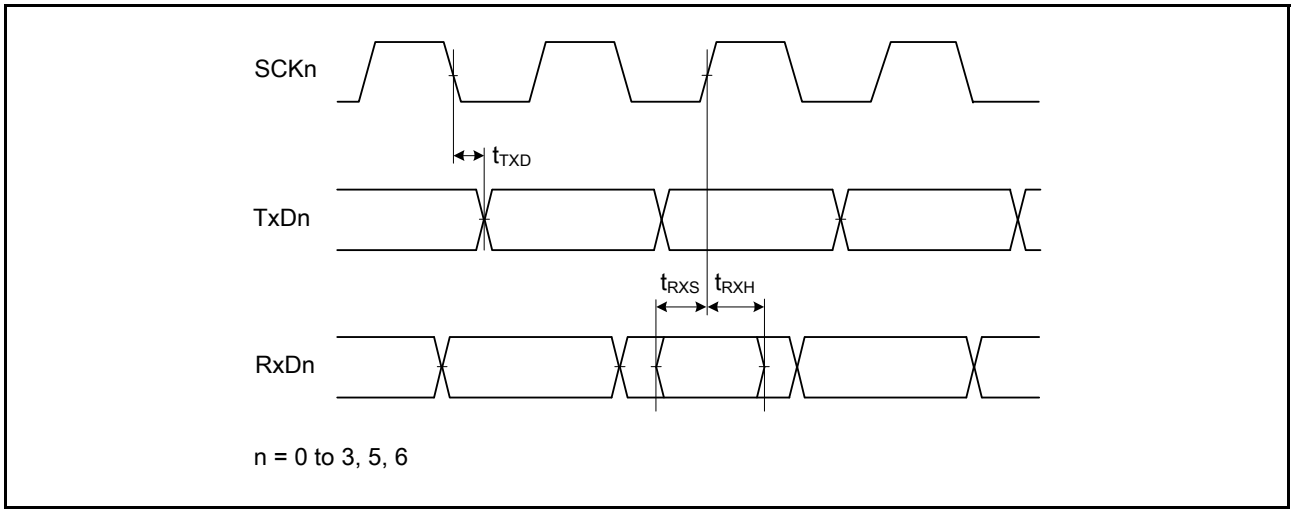



**Figure 5.35 SCI Input/Output Timing: Clock Synchronous Mode**

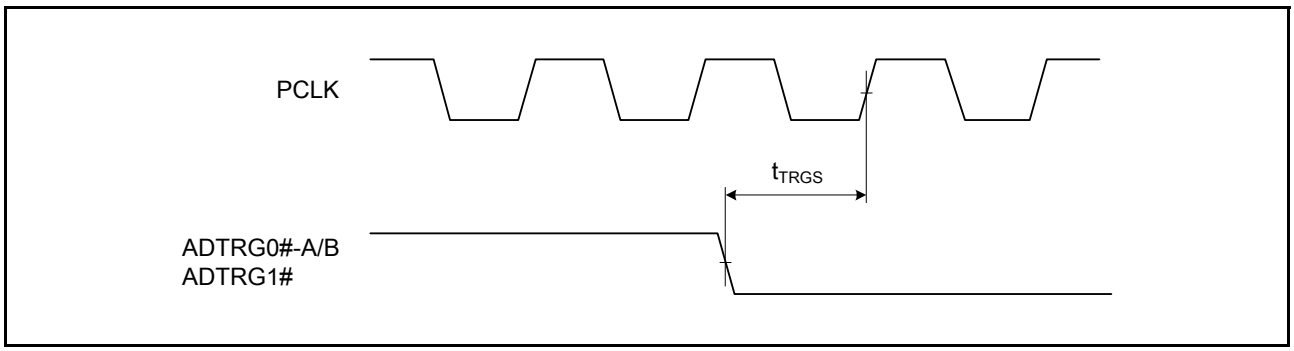



**Figure 5.36 A/D Converter External Trigger Input Timing**

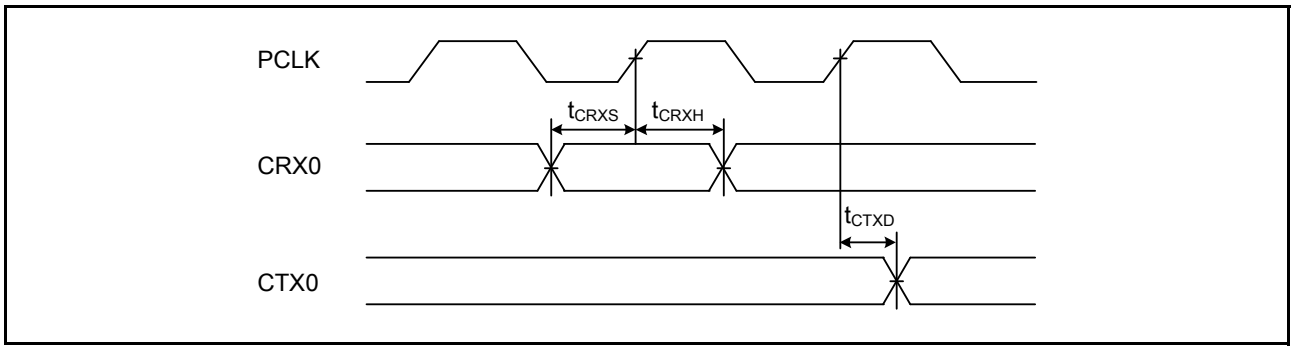



**Figure 5.37 CAN Input/Output Timing**

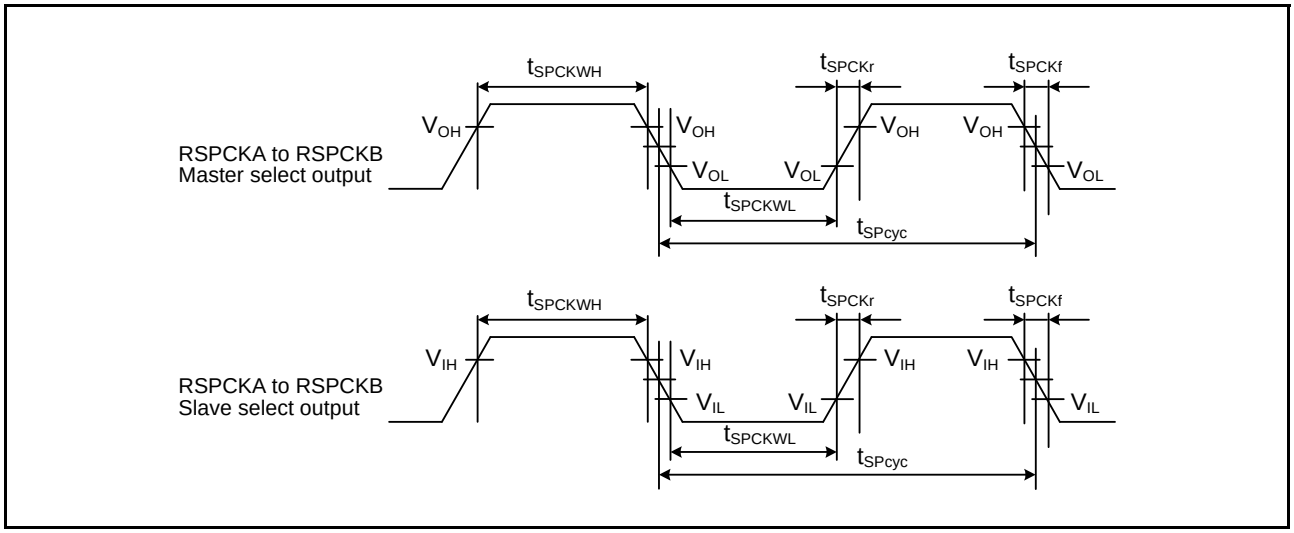



**Figure 5.38 RSPI Clock Timing**

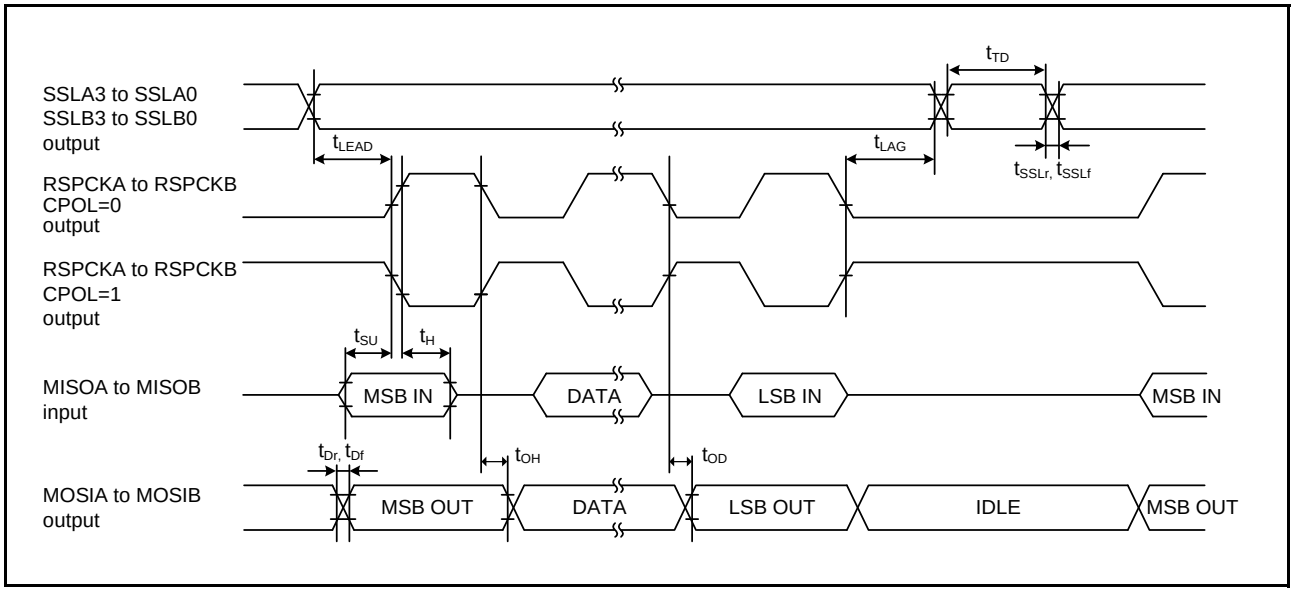



**Figure 5.39 RSPI Timing (Master, CPHA = 0)**

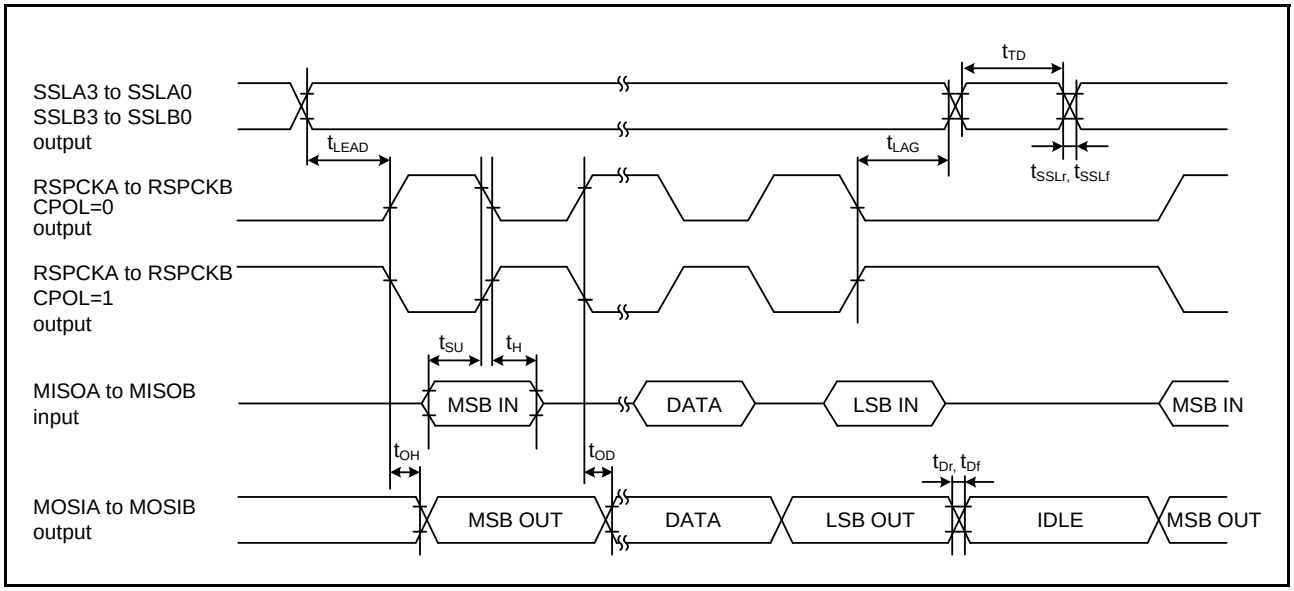



**Figure 5.40 RSPI Timing (Master, CPHA = 1)**

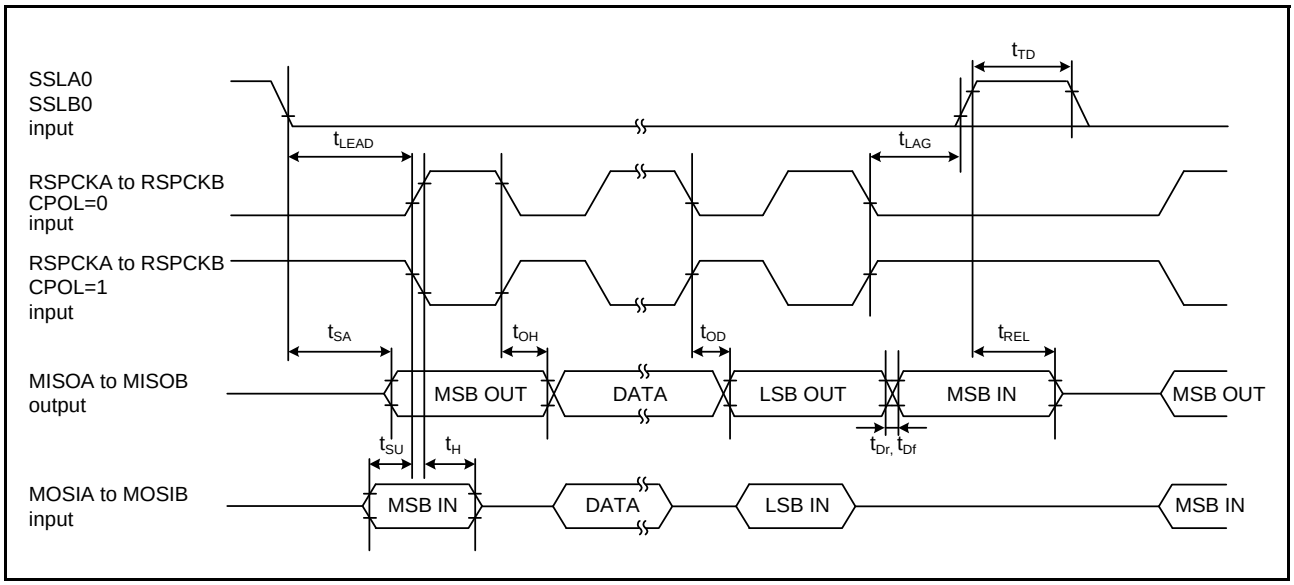



**Figure 5.41 RSPI Timing (Slave, CPHA = 0)**

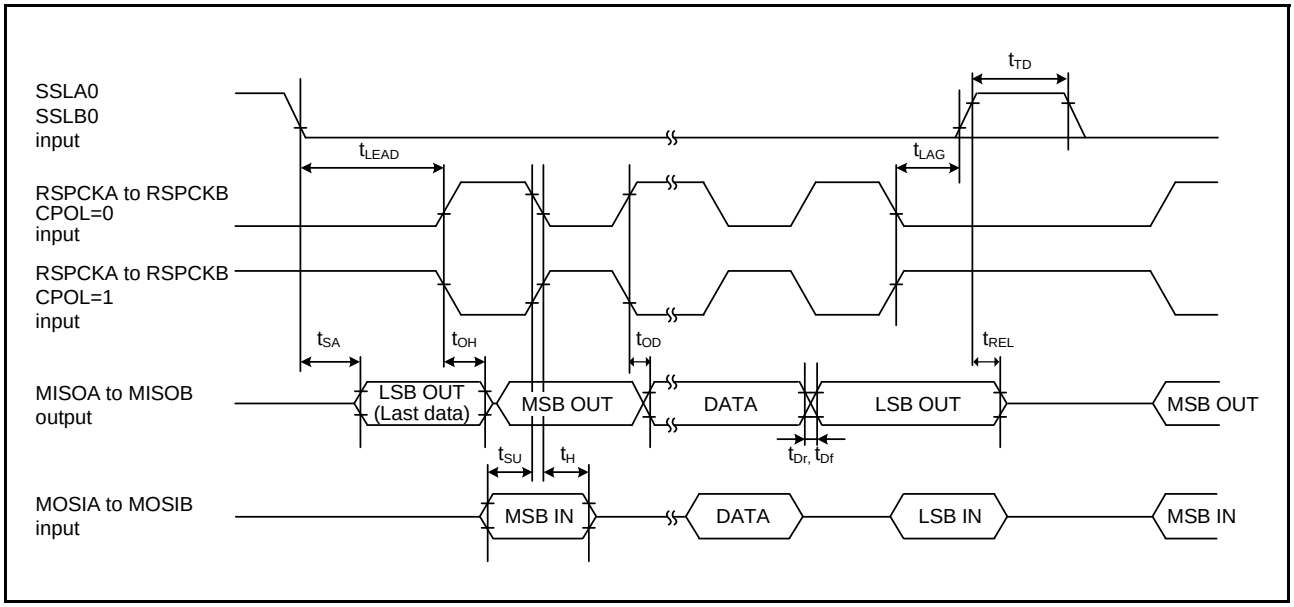



**Figure 5.42 RSPI Timing (Slave, CPHA = 1)**

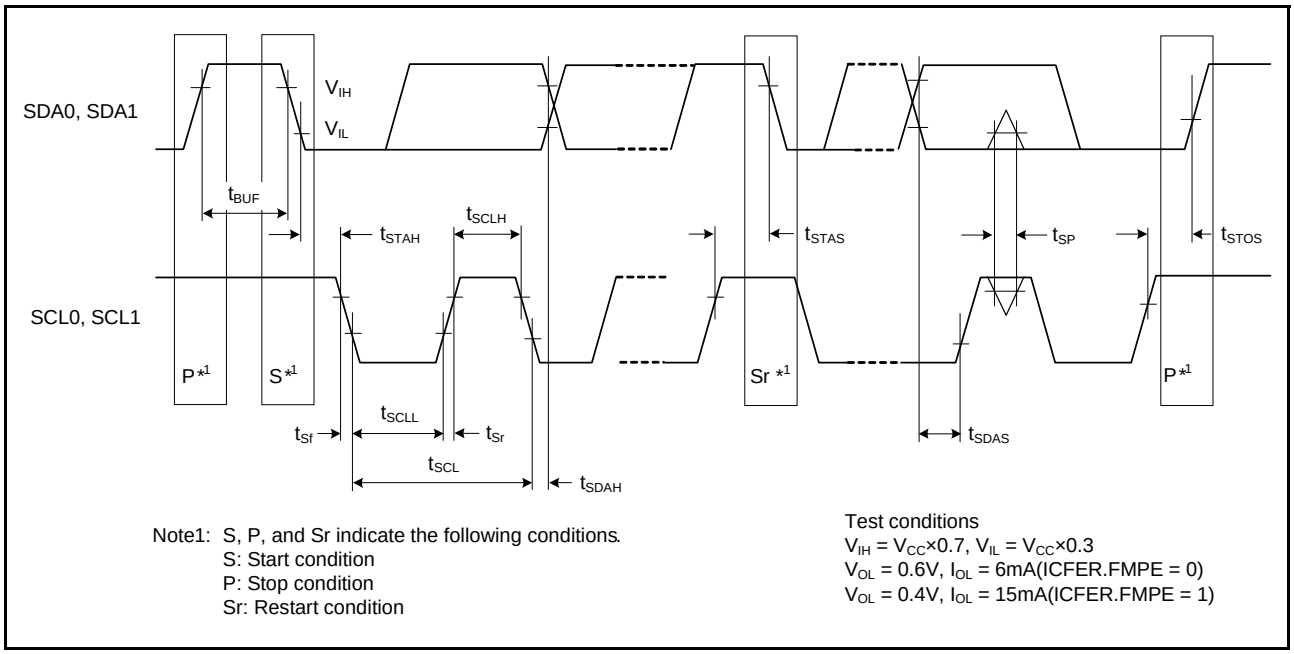



**Figure 5.43 I2C Bus Interface Input/Output Timing**

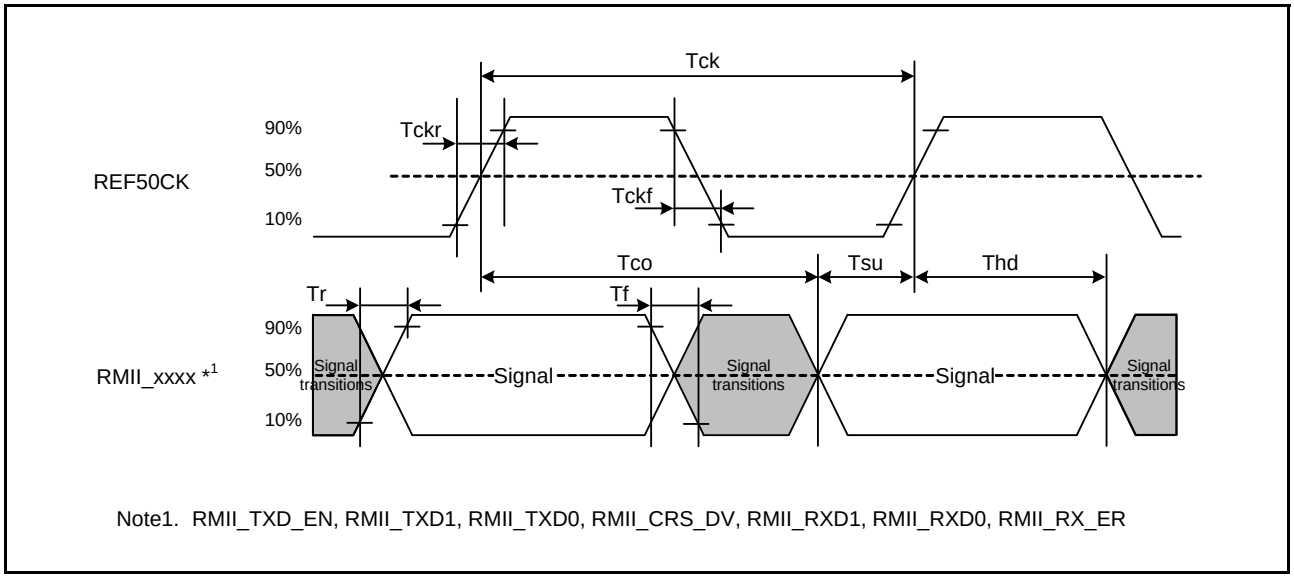



**Figure 5.44 REF50CK and RMII Signal Timing**

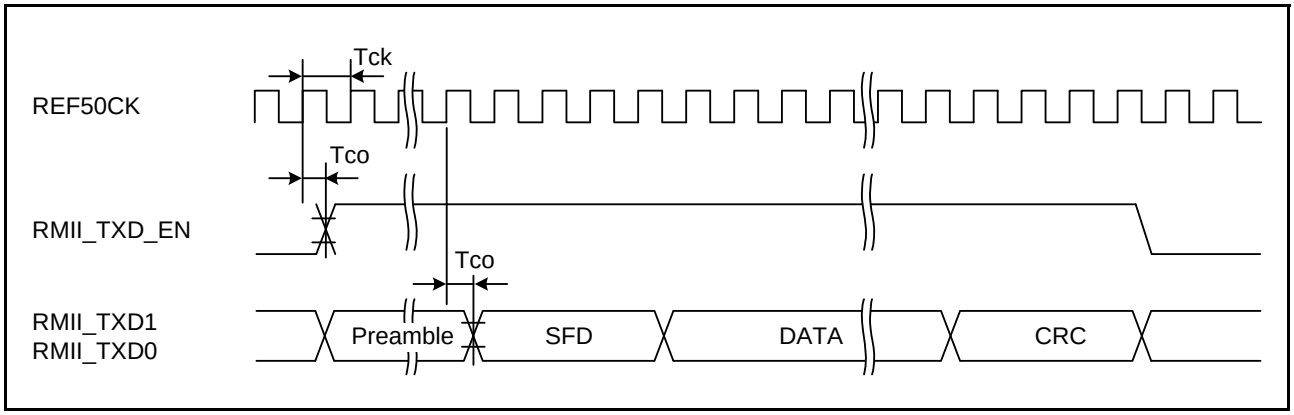



**Figure 5.45 RMII Transmission Timing**

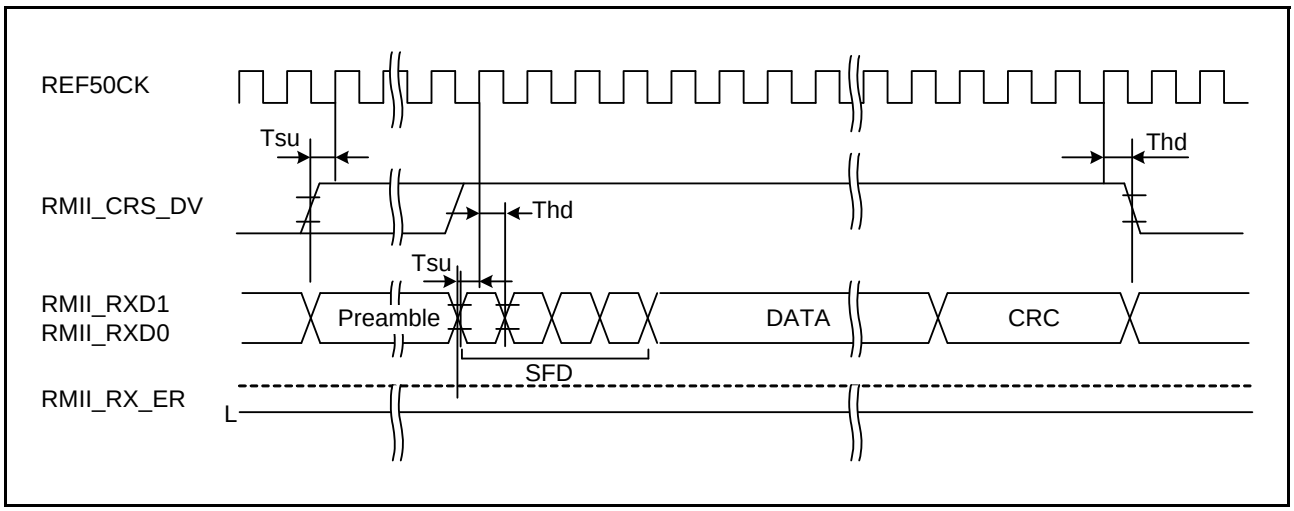



**Figure 5.46 RMII Reception Timing (Normal Operation)**

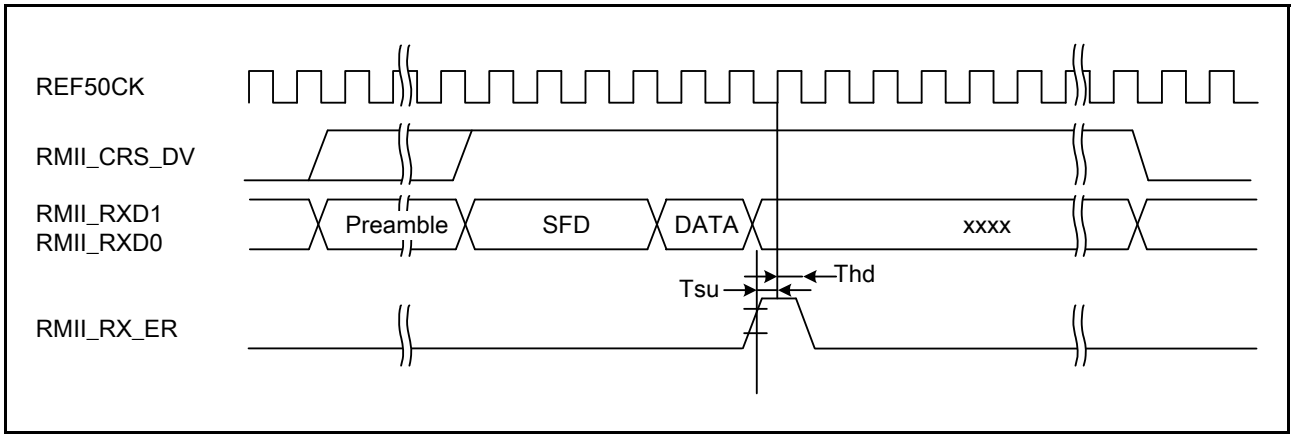



**Figure 5.47 RMII Reception Timing (Error Occurrence)**

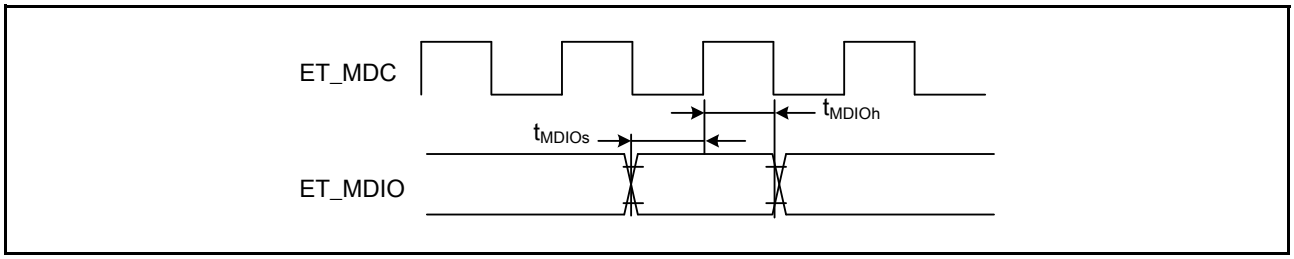



**Figure 5.48 MDIO Input Timing (RMII)**

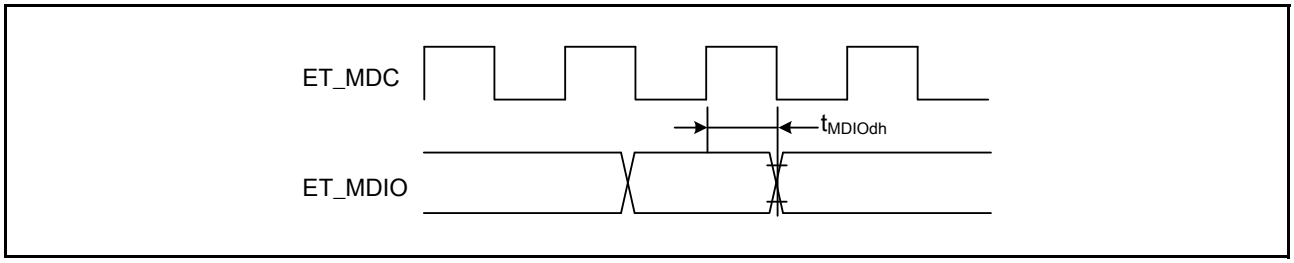



**Figure 5.49 MDIO Output Timing (RMII)**

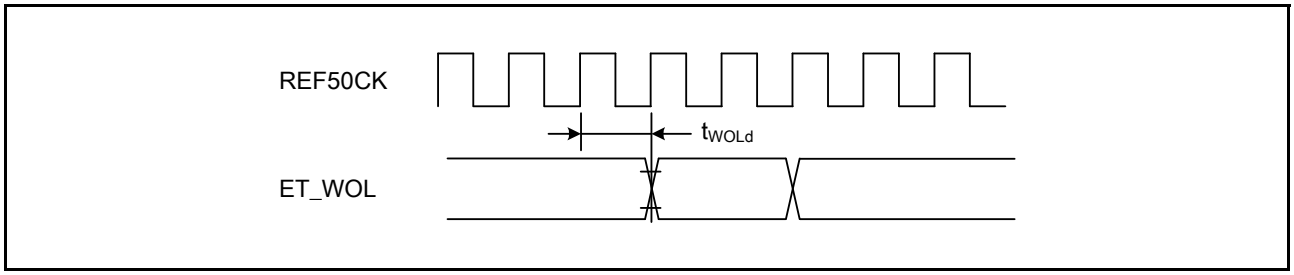



**Figure 5.50 WOL Output Timing (RMII)**

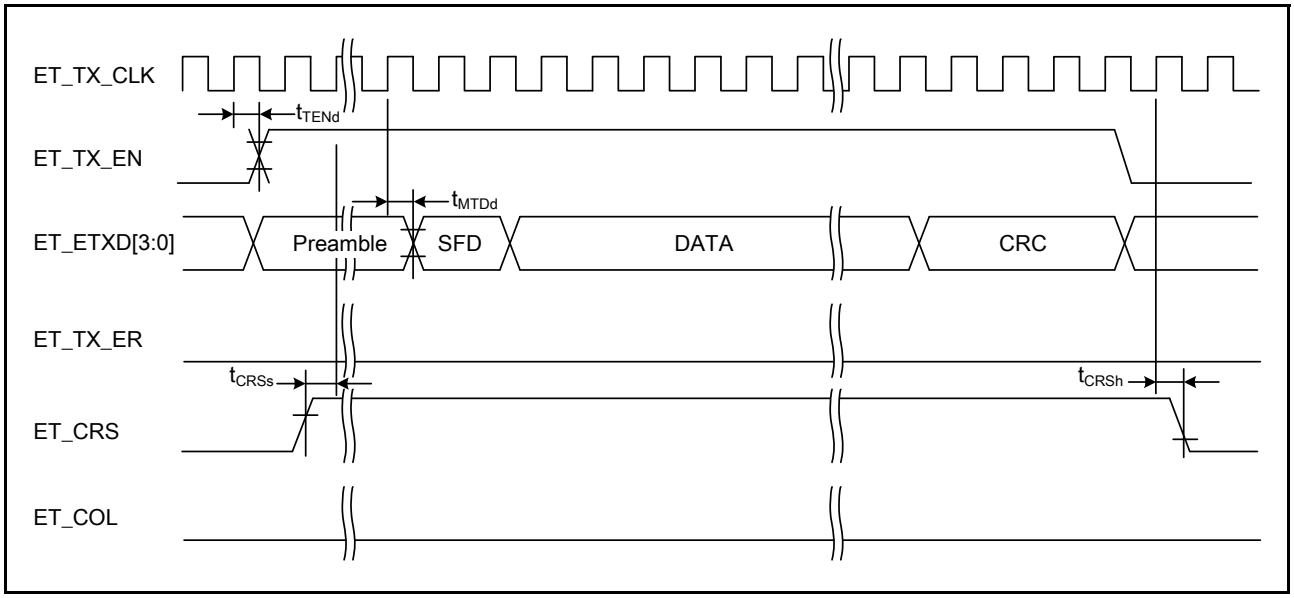



**Figure 5.51 MII Transmission Timing (Normal Operation)**

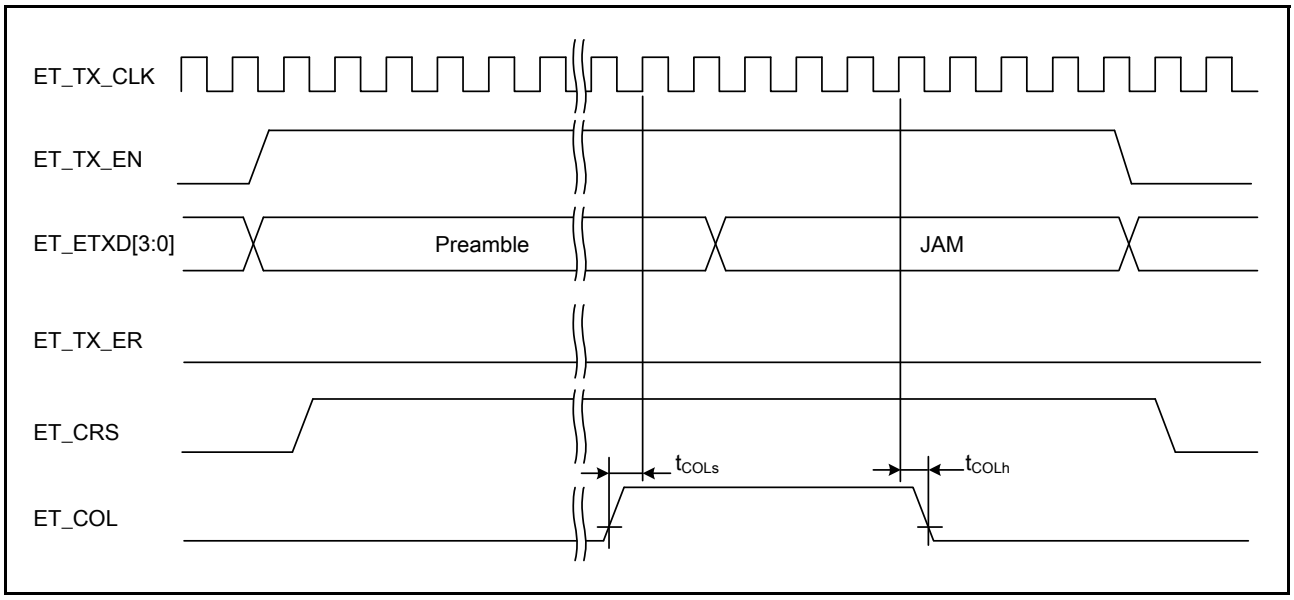



**Figure 5.52 MII Transmission Timing (Conflict Occurrence)**

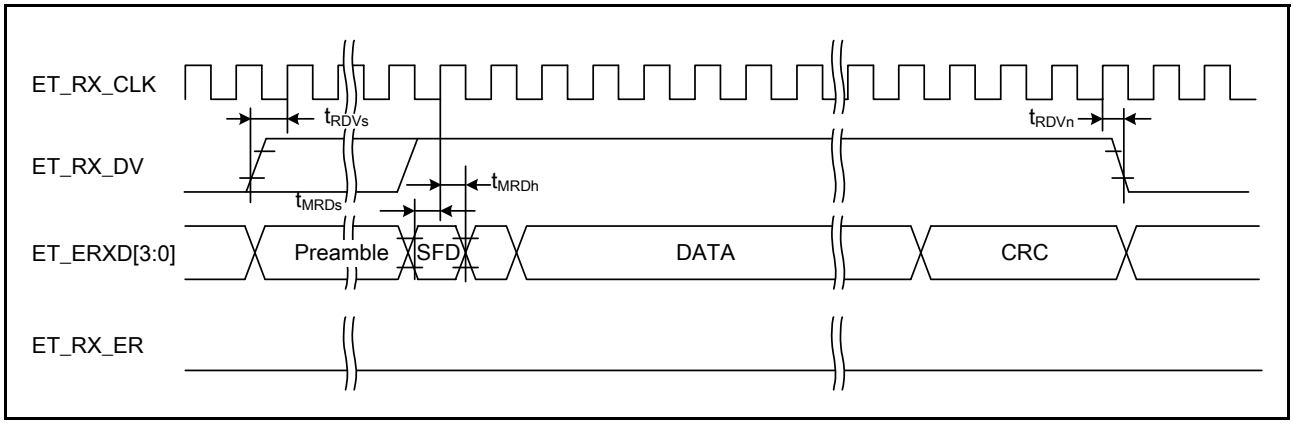



**Figure 5.53 MII Reception Timing (Normal Operation)**

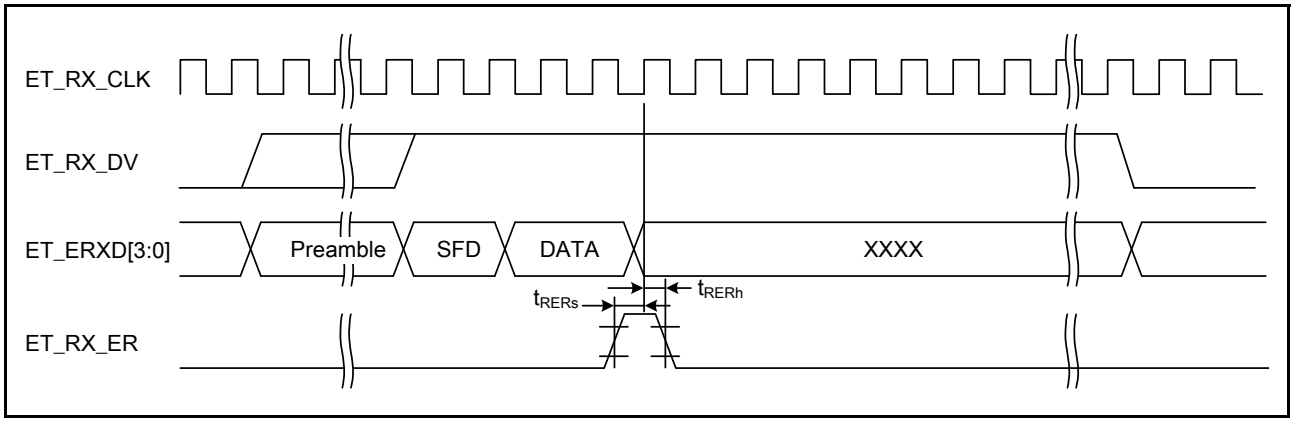



**Figure 5.54 MII Reception Timing (Error Occurrence)**

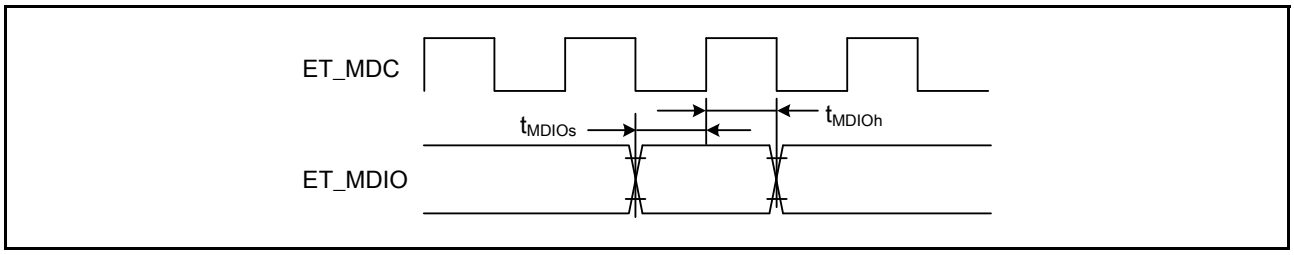



**Figure 5.55 MDIO Input Timing (MII)**

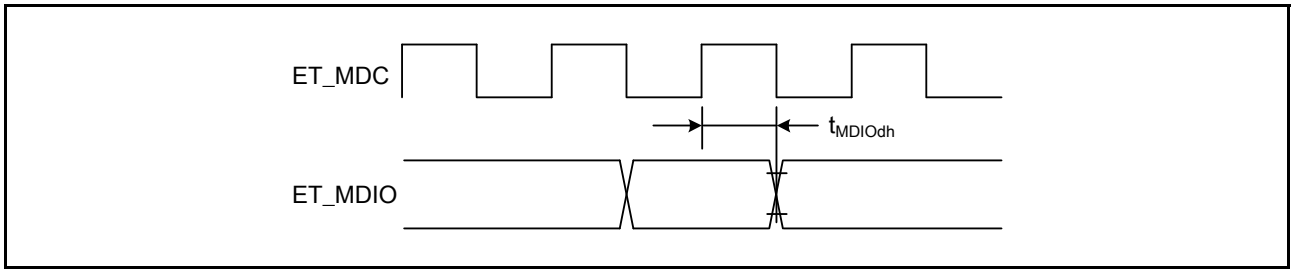



**Figure 5.56 MDIO Output Timing (MII)**

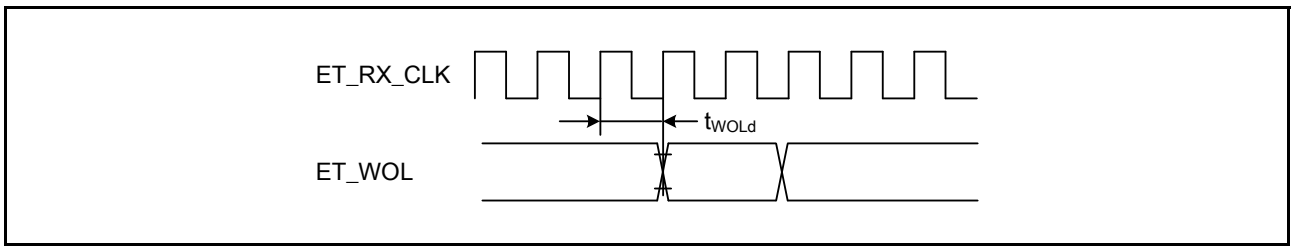



**Figure 5.57 WOL Output Timing (MII)**

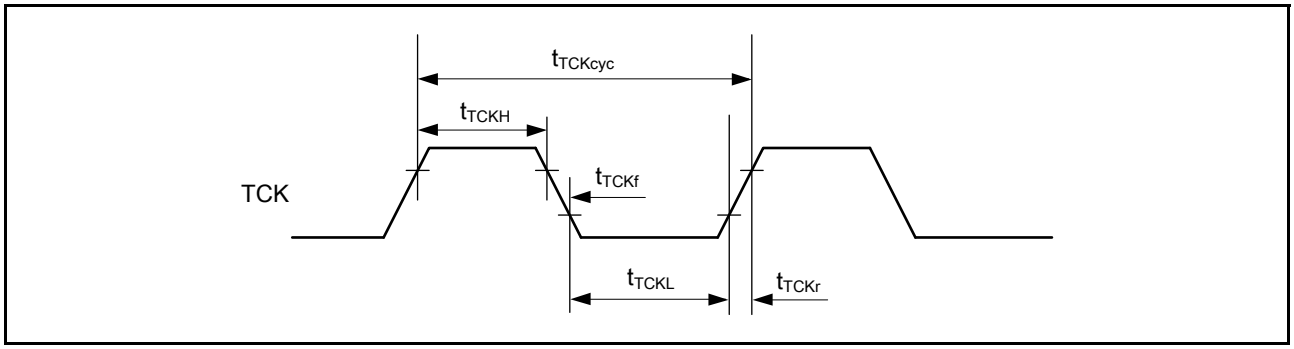



**Figure 5.58 Boundary Scan TCK Timing**

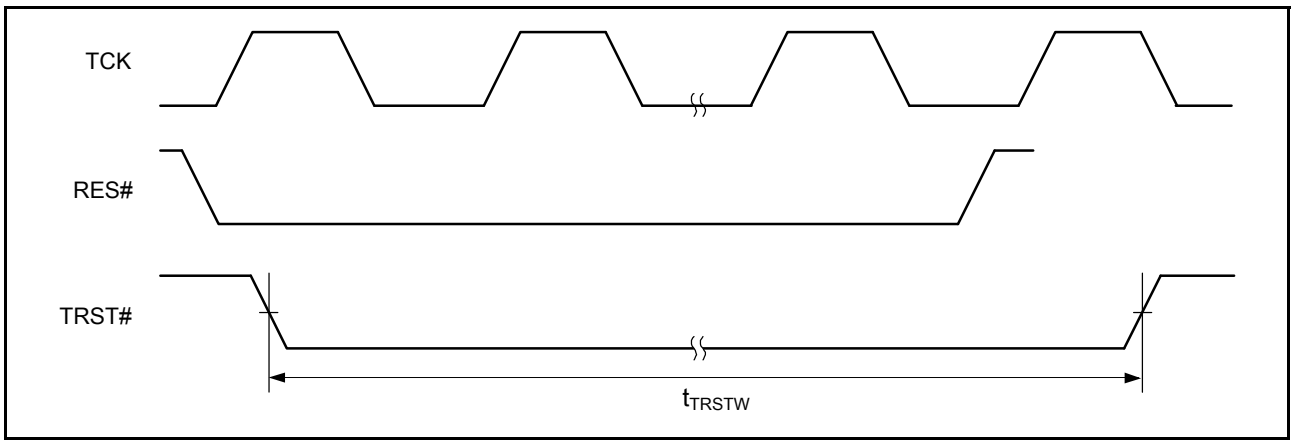



**Figure 5.59 Boundary Scan TRST# Timing**

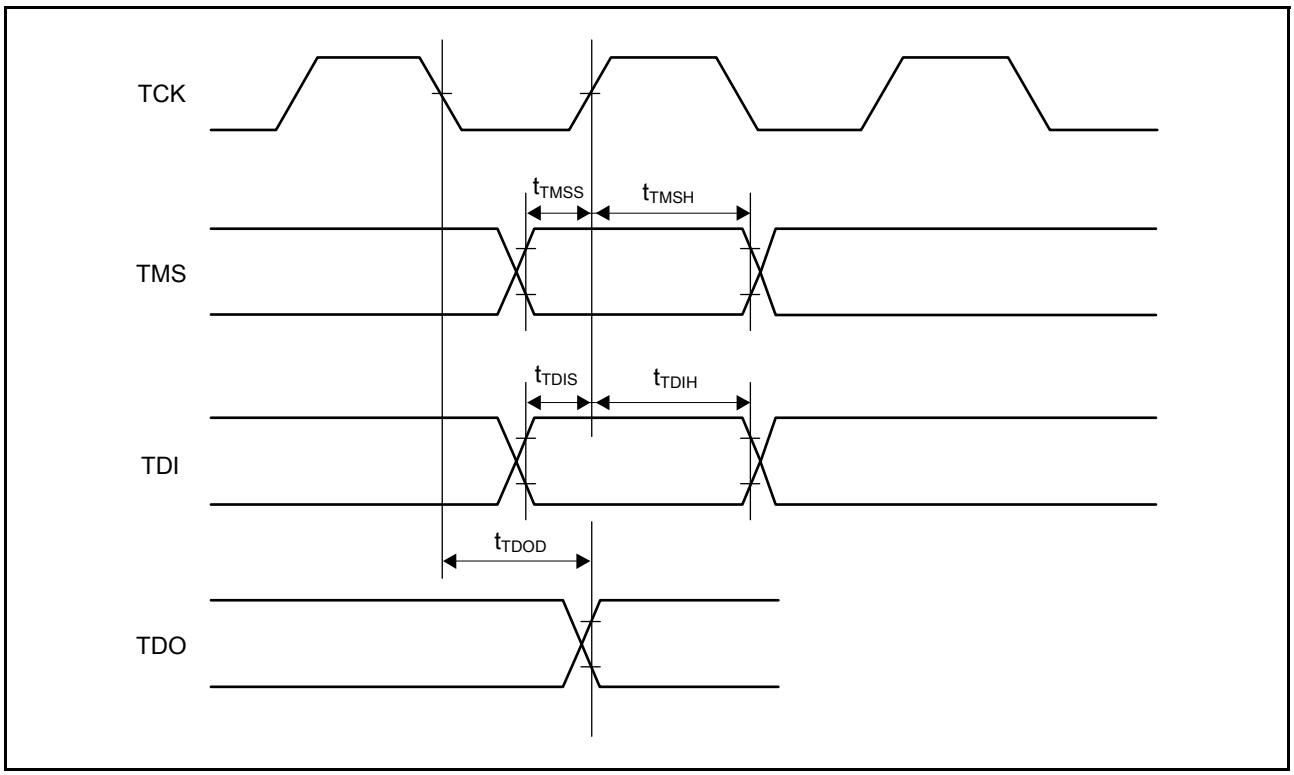



**Figure 5.60 Boundary Scan Input/Output Timing**

## 5.4 USB Characteristics

**Table 5.19 Internal USB Full-Speed Characteristics (DP, DM Pin Characteristics)**

Conditions: VCC = PLLVCC = AVCC = VCC_USB = 3.0 to 3.6 V, VREFH = 3.0 V to AVCC
VSS = PLLVSS = AVSS = VREFL = VSS_USB = 0 V
PCLK = 24 to 50 MHz
$T_a$ = -40 to +85°C

| Item | | Symbol | Min. | Max. | Unit | Test Conditions | |
|---|---|---|---|---|---|---|---|
| Input characteristics | Input high level voltage | $V_{IH}$ | 2.0 | — | V | | Figure 5.61 and Figure 5.62 |
| | Input low level voltage | $V_{IL}$ | — | 0.8 | V | | |
| | Differential input Sensitivity | $V_{DI}$ | 0.2 | — | V | \| DP — DM \| | |
| | Differential commom mode range | $V_{CM}$ | 0.8 | 2.5 | V | | |
| Output characteristics | Output high level voltage | $V_{OH}$ | 2.8 | 3.6 | V | $I_{OH}$ = -200µA | |
| | Output low level voltage | $V_{OL}$ | 0.0 | 0.3 | V | $I_{OL}$ = 2 mA | |
| | Cross over voltage | $V_{CRS}$ | 1.3 | 2.0 | V | | |
| | Rising time | $t_{Lr}$ | 4 | 20 | ns | | |
| | Falling time | $t_{Lf}$ | 4 | 20 | ns | | |
| | Rising/falling time ratio | $t_{Lr}$ / $t_{Lf}$ | 90 | 111.11 | % | $t_{Lr}$ / $t_{Lf}$ | |
| | Output resistance | $Z_{DRV}$ | 28 | 44 | Ω | Rs = 22Ω included | |

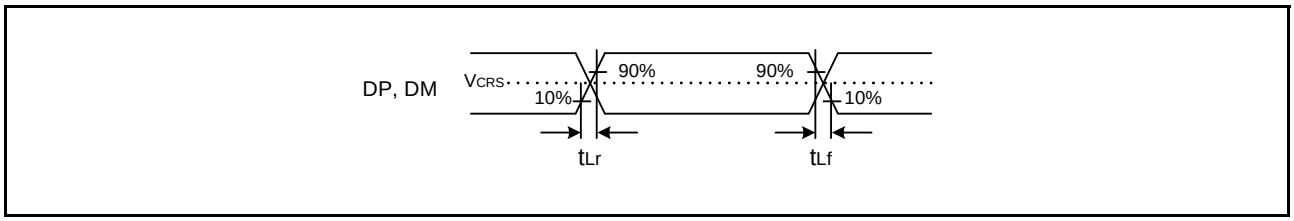



**Figure 5.61 DP, DM Output Timing (Full-Speed)**

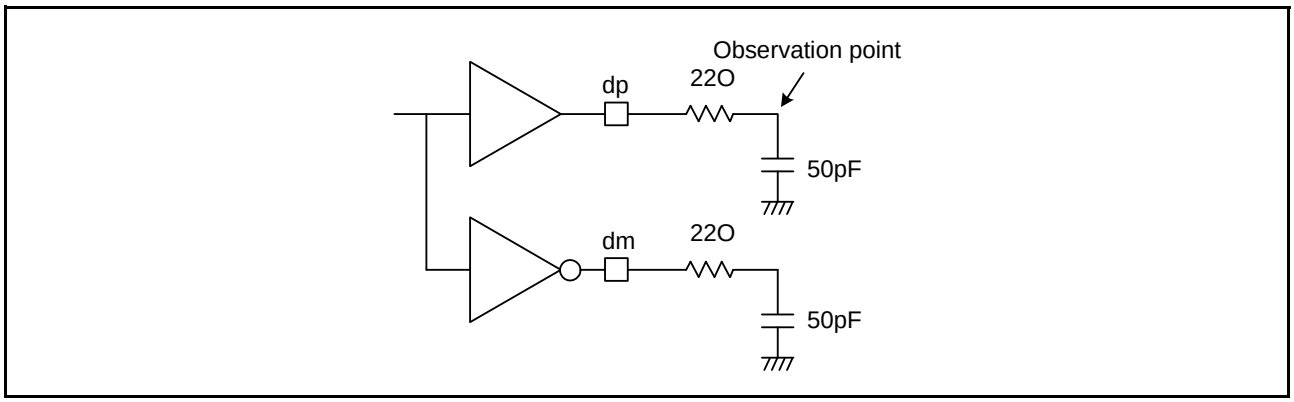



**Figure 5.62 Test Circuit (Full-Speed)**

## 5.5 A/D Conversion Characteristics

**Table 5.20 10-Bit A/D Conversion Characteristics**

Conditions: VCC = PLLVCC = AVCC = VCC_USB = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC
VSS = PLLVSS = AVSS = VREFL = VSS_USB = 0 V
PCLK = 8 to 50 MHz
$T_a$ = -40 to +85°C

| Item | | | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| Resolution | | | 10 | 10 | 10 | bits | |
| Conversion time*1 (PCLK = 50-MHz operation) | With 0.1-µF external capacitor | When the capacitor is charged enough*2 | 0.8 (0.3)*3 | — | — | µs | Sampling 15 states |
| | Without external capacitor | Permissible signal source impedance (max.) = 1.0 kΩ | 1.0 (0.5)*3 | — | — | | Sampling 25 states |
| | | Permissible signal source impedance (max.) = 5.0 kΩ | 2.6 (2.1)*3 | — | — | | Sampling 105 states |
| Analog input capacitance | | | — | — | 6.0 | pF | |
| INL integral nonlinearity error | | | — | ±1.5 | ±3.0 | LSB | |
| Offset error | | | — | ±1.5 | ±3.0 | LSB | |
| Full-scale error | | | — | ±1.5 | ±3.0 | LSB | |
| Quantization error | | | — | ±0.5 | — | LSB | |
| Absolute accuracy | | | — | ±1.5 | ±3.0 | LSB | |
| DNL differential nonlinearity error | | | — | ±0.5 | ±1.0 | LSB | |

Note 1. The conversion time includes the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.
Note 2. The scanning is not supported.
Note 3. The value in parentheses indicates the sampling time.

**Table 5.21 12-Bit A/D Conversion Characteristics**

Conditions: VCC = PLLVCC = AVCC = VCC_USB = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC
VSS = PLLVSS = AVSS = VREFL = VSS_USB = 0 V
PCLK = 8 to 50 MHz
$T_a$ = -40 to +85°C

| Item | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|
| Resolution | 12 | 12 | 12 | bits | |
| Conversion time*1 | 1.0 | — | — | µs | AVCC ≥ 3.0 |
| | 2.0 | — | — | µs | AVCC ≥ 2.7 |
| Analog input capacitance | — | — | 30 | pF | |
| Offset error | — | ±2.0 | ±7.5 | LSB | |
| Full-scale error | — | ±2.0 | ±7.5 | LSB | |
| Quantization error | — | ±0.5 | — | LSB | |
| Absolute accuracy | — | ±2.5 | ±8.0 | LSB | |
| Nonlinearity error | — | ±2.0 | ±4.0 | LSB | |

Note 1. The time conversion takes is the sum of the sampling interval and the time comparison takes (permissible signal-source impedance is up to 1.0 kΩ)

## 5.6 D/A Conversion Characteristics

**Table 5.22 D/A Conversion Characteristics**

Conditions: VCC = PLLVCC = AVCC = VCC_USB = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC
VSS = PLLVSS = AVSS = VREFL = VSS_USB = 0 V
$T_a$ = -40 to +85°C

| Item | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|
| Resolution | 10 | 10 | 10 | bits | |
| Conversion time | — | — | 3.0 | µs | 20-pF capacitive load |
| Absolute accuracy | — | ±2.0 | ±4.0 | LSB | 2-MΩ resistive load |
| | — | — | ±3.0 | LSB | 4-MΩ resistive load |
| | — | — | ±2.0 | LSB | 10-MΩ resistive load |
| RO output resistance | — | 3.6 | — | kΩ | |

## 5.7 Power-on Reset Circuit, Voltage Detection Circuit Characteristics

**Table 5.23 Power-on Reset Circuit, Voltage Detection Circuit Characteristics**

Conditions: VCC = PLLVCC = AVCC = VCC_USB = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC
VSS = PLLVSS = AVSS = VREFL = VSS_USB = 0 V
$T_a$ = -40 to +85°C

| Item | | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| Voltage detection level | Power-on reset (POR) | $V_{POR}$ | 2.48 | 2.58 | 2.68 | V | Figure 5.63 |
| | Voltage detection circuit (LVD) | Vdet1 | 2.75 | 2.85 | 2.95 | | Figure 5.64 and Figure 5.65 |
| | | Vdet2 | 3.05 | 3.15 | 3.25 | | |
| Internal reset time | | $t_{POR}$ | 20 | 35 | 50 | ms | |
| Min. VCC down time*1 | | $t_{VOFF}$ | 200 | — | — | µs | Figure 5.64 and Figure 5.65 |
| Reply delay time | | tdet | — | — | 200 | µs | |

Note 1. The power-off time indicates the time when VCC is below the minimum value of voltage detection levels $V_{POR}$, Vdet1, and Vdet2 for the POR/ LVD.

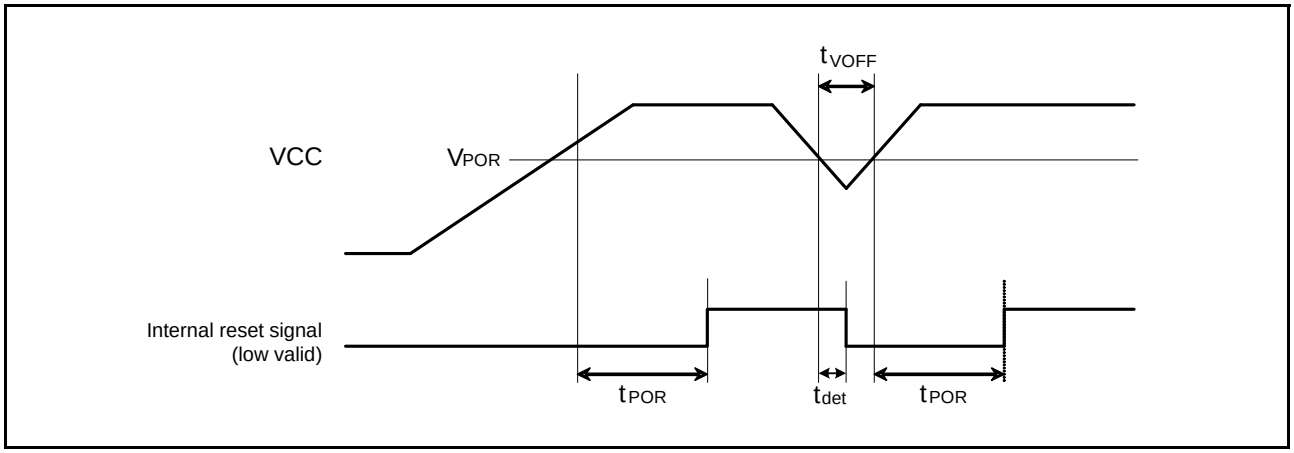



**Figure 5.63 Power-on Reset Timing**

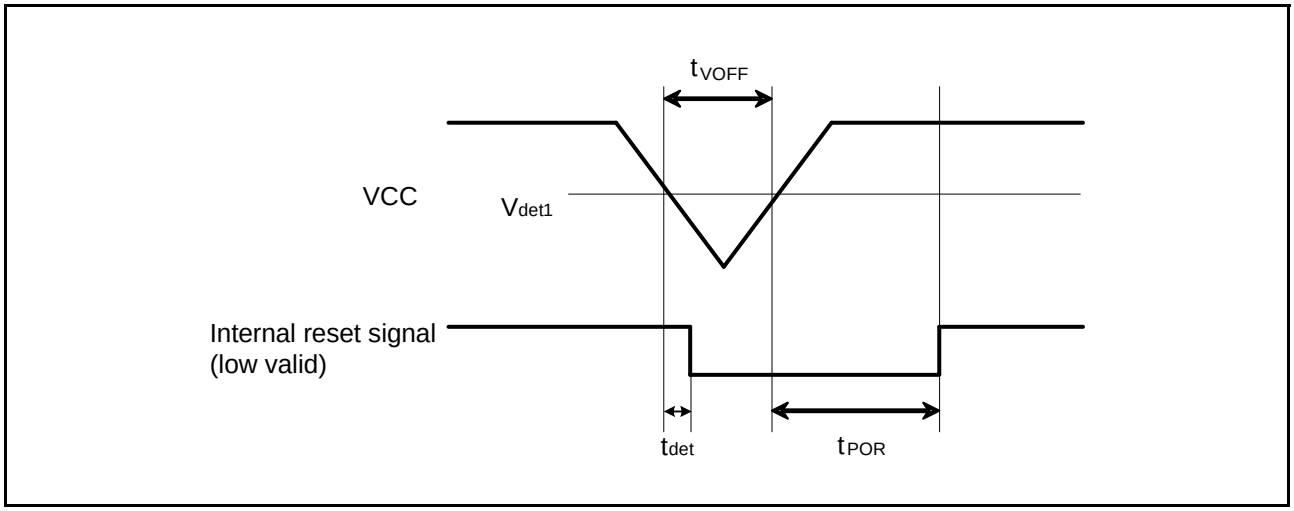



**Figure 5.64 Voltage Detection Circuit Timing (Vdet1)**

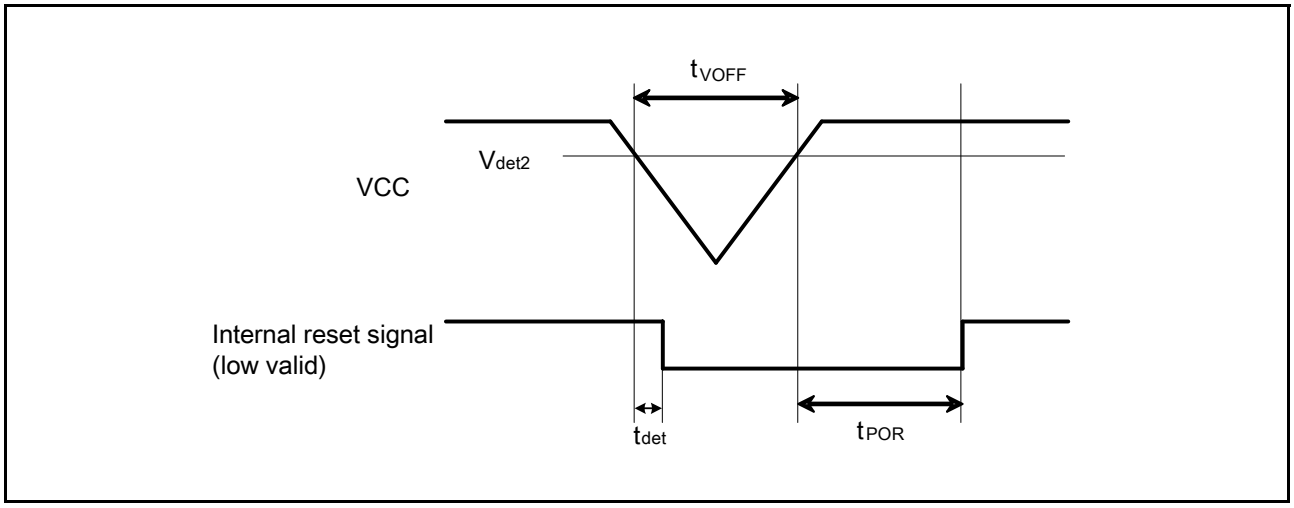



**Figure 5.65 Voltage Detection Circuit Timing (Vdet2)**

## 5.8 Oscillation Stop Detection Timing

**Table 5.24 Oscillation Stop Detection Circuit Characteristics**

Conditions: VCC = PLLVCC = AVCC = VCC_USB = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC
VSS = PLLVSS = AVSS = VREFL = VSS_USB = 0 V
$T_a$ = -40 to +85°C

| Item | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Detection time | tdr | — | — | 1.0 | ms | Figure 5.66 |
| Internal oscillation frequency when oscillation stop is detected | $f_{MAIN}$ | 0.5 | — | 7.0 | MHz | |

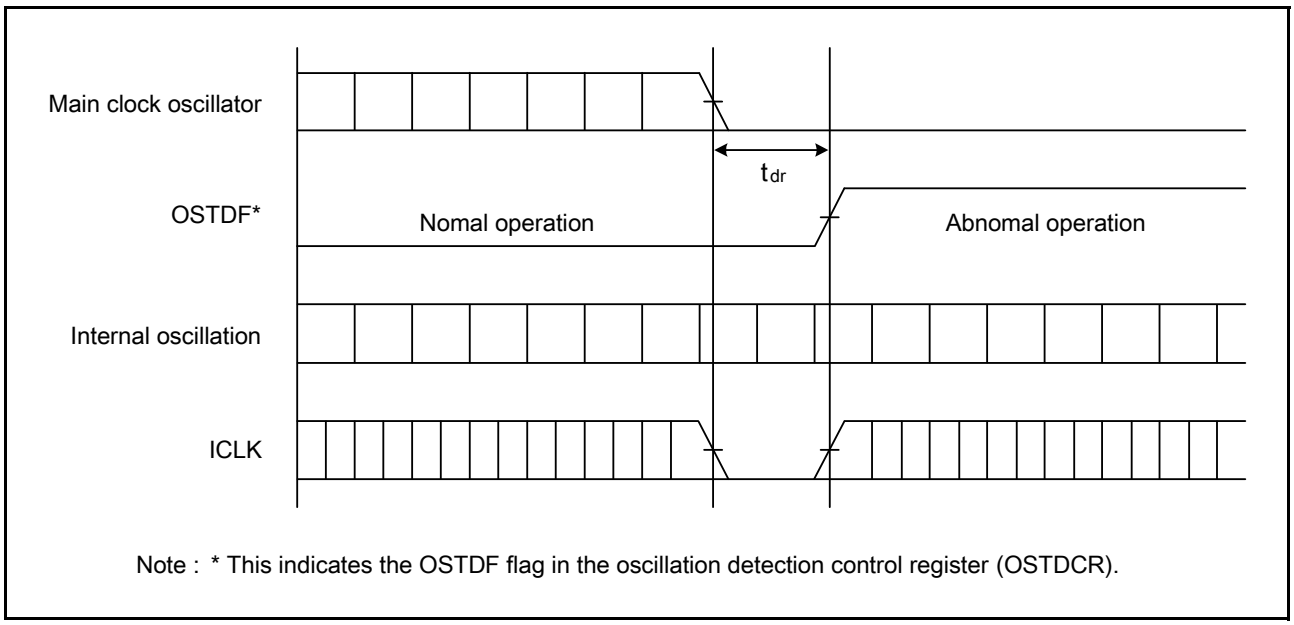



**Figure 5.66 Oscillation Stop Detection Timing**

## 5.9 ROM (Flash Memory for Code Storage) Characteristics

**Table 5.25 ROM (Flash Memory for Code Storage) Characteristics (1)**

Conditions: VCC = PLLVCC = AVCC = VCC_USB = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC
VSS = PLLVSS = AVSS = VREFL = VSS_USB = 0 V
Temperature range for the programming/erasure operation: $T_a$ = -40 to +85°C

| Item | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Rewrite/erase cycle*1 | $N_{PEC}$ | 1000 | — | — | Times | |
| Data hold time | $t_{DRP}$ | 30*2 | — | — | Year | $T_a$ = +85°C |

Note 1. Definition of reprogram/erase cycle:
The reprogram/erase cycle is the number of erasing for each block. When the reprogram/erase cycle is n times (n = 1000), erasing can be performed n times for each block. For instance, when 256-byte programming is performed 16 times for different addresses in 4-Kbyte block and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasing is not enabled (overwriting is prohibited).
Note 2. The result obtained from the reliability test.

**Table 5.26 ROM (Flash Memory for Code Storage) Characteristics (2)**

Conditions: VCC = PLLVCC = AVCC = VCC_USB = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC
VSS = PLLVSS = AVSS = VREFL = VSS_USB = 0 V
Temperature range for the programming/erasure operation: $T_a$ = -40 to +85°C

| Item | | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| Programming time | 256 bytes | $t_{P256}$ | — | 2 | 12 | ms | PCLK = 50 MHz<br>$N_{PEC} \leq 100$ |
| | 4 Kbytes | $t_{P4K}$ | — | 23 | 50 | ms | |
| | 16 Kbytes | $t_{P16K}$ | — | 90 | 200 | ms | |
| | 256 byte | $t_{P256}$ | — | 2.4 | 14.4 | ms | PCLK = 50 MHz<br>$N_{PEC} > 100$ |
| | 4 Kbytes | $t_{P4K}$ | — | 27.6 | 60 | ms | |
| | 16 Kbytes | $t_{P16K}$ | — | 108 | 240 | ms | |
| Erasure time | 4 Kbytes | $t_{E4K}$ | — | 25 | 60 | ms | PCLK = 50 MHz<br>$N_{PEC} \leq 100$ |
| | 16 Kbytes | $t_{E16K}$ | — | 100 | 240 | ms | |
| | 4 Kbytes | $t_{E4K}$ | — | 30 | 72 | ms | PCLK = 50 MHz<br>$N_{PEC} > 100$ |
| | 16 Kbytes | $t_{E16K}$ | — | 120 | 288 | ms | |
| Suspend delay time during writing | | $t_{SPD}$ | — | — | 120 | µs | Figure 5.67<br>PCLK = 50-MHz operation |
| First suspend delay time during erasing (in suspend priority mode) | | $t_{SESD1}$ | — | — | 120 | µs | |
| Second suspend delay time during erasing (in suspend priority mode) | | $t_{SESD2}$ | — | — | 1.7 | ms | |
| Suspend delay time during erasing (in erasure priority mode) | | $t_{SEED}$ | — | — | 1.7 | ms | |

## 5.10 Data Flash (Flash Memory for Data Storage) Characteristics

**Table 5.27 Data Flash (Flash Memory for Data Storage) Characteristics**

Conditions: VCC = PLLVCC = AVCC = VCC_USB = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC
VSS = PLLVSS = AVSS = VREFL = VSS_USB = 0 V
Temperature range for the programming/erasure operation: $T_a$ = -40 to +85°C

| Item | | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| Programming time | 8 bytes | $t_{DP8}$ | — | 0.4 | 2 | ms | PCLK = 50-MHz operation |
| | 128 bytes | $t_{DP128}$ | — | 1 | 5 | ms | |
| Erasure time | 2 Kbytes | $t_{DE2K}$ | — | 70 | 250 | ms | PCLK = 50-MHz operation |
| Blank check time | 8 bytes | $t_{DBC8}$ | — | — | 30 | µs | PCLK = 50-MHz operation |
| | 2 Kbytes | $t_{DBC2K}$ | — | — | 0.7 | ms | |
| Rewrite/erase cycle*1 | | $N_{DPEC}$ | 30000*2 | — | — | Times | |
| Suspend delay time during writing | | $t_{DSPD}$ | — | — | 120 | µs | Figure 5.67 PCLK = 50-MHz operation |
| First suspend delay time during erasing (in suspend priority mode) | | $t_{DSESD1}$ | — | — | 120 | µs | |
| Second suspend delay time during erasing (in suspend priority mode) | | $t_{DSESD2}$ | — | — | 1.7 | ms | |
| Suspend delay time during erasing (in erasure priority mode) | | $t_{DSEED}$ | — | — | 1.7 | ms | |
| Data hold time*3 | | $t_{DDRP}$ | 10 | — | — | Year | |

Note 1. Definition of rewrite/erase cycle:
The rewrite/erase cycle is the number of erasing for each block. When the rewrite/erase cycle is n times (n = 30000), erasing can be performed n times for each block. For instance, when 128-byte writing is performed 16 times for different addresses in 2-Kbyte block and then the entire block is erased, the rewrite/erase cycle is counted as one. However, writing to the same address for several times as one erasing is not enabled (over writing is prohibited).

Note 2. This indicates the minimum number that guarantees the characteristics after rewriting. (The guaranteed value is in the range from one to the minimum number.)

Note 3. This indicates the characteristic when rewrite is performed within the specification range including the minimum number.

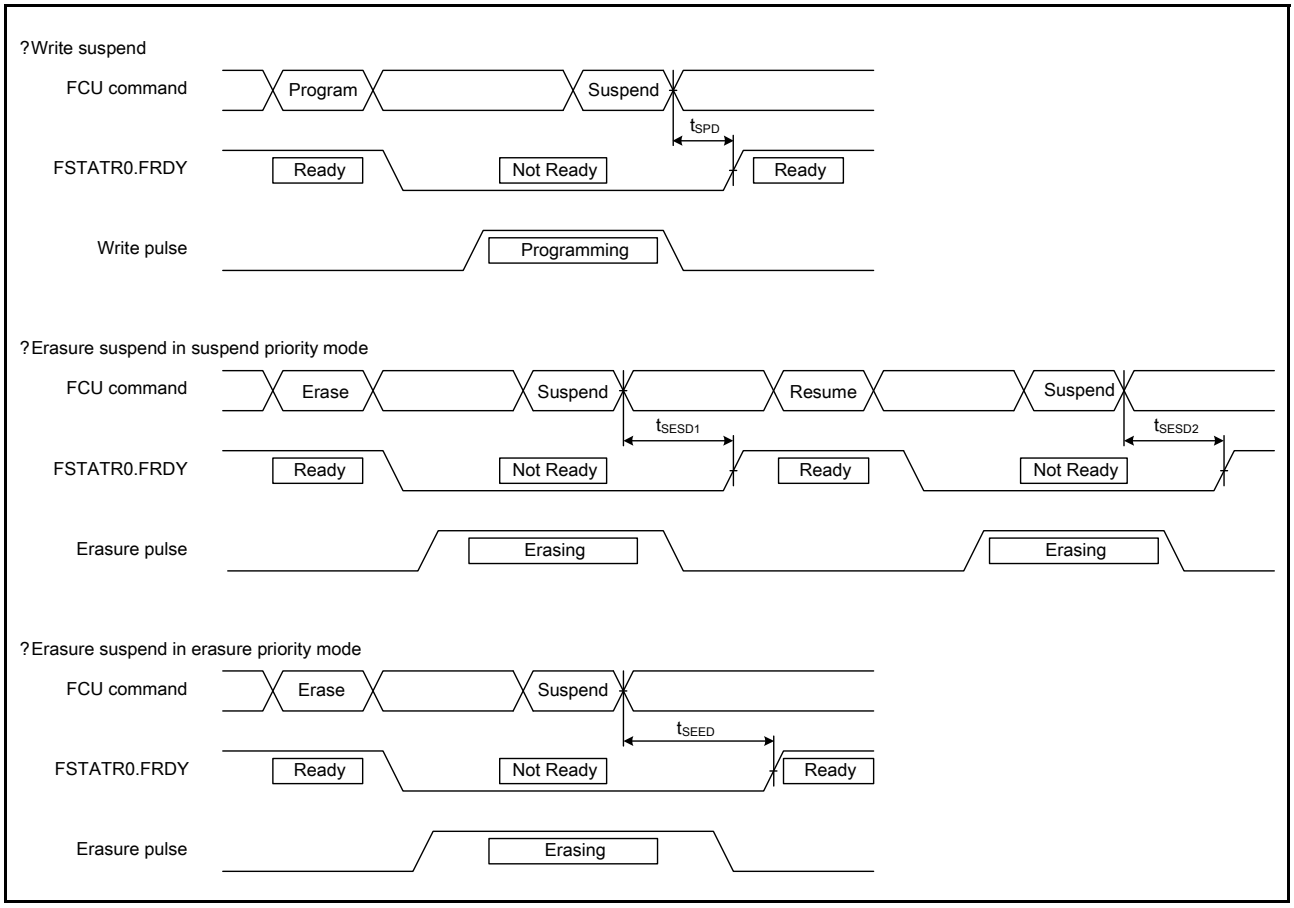
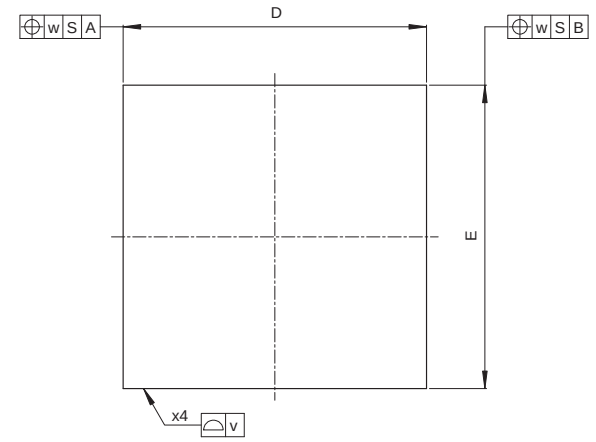


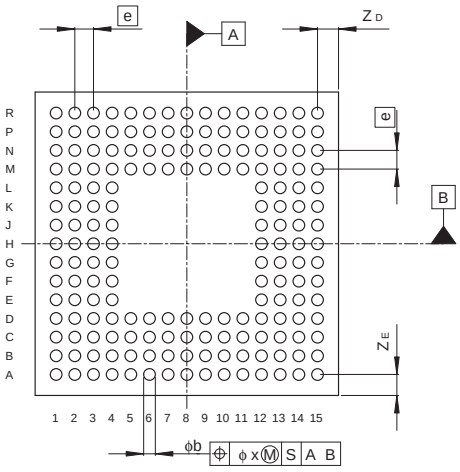

**Figure 5.67 Flash Memory Write/Erase Suspend Timing**

# Appendix 1. Package Dimensions

Information on the latest version of the package dimensions or mountings has been displayed in "Packages" on Renesas Electronics Corp website.

| JEITA Package Code | RENESAS Code | Previous Code | MASS[Typ.] |
|---|---|---|---|
| P-LFBGA176-13x13-0.80 | PLBG0176GA-A | BP-176/BP-176V | 0.45g |

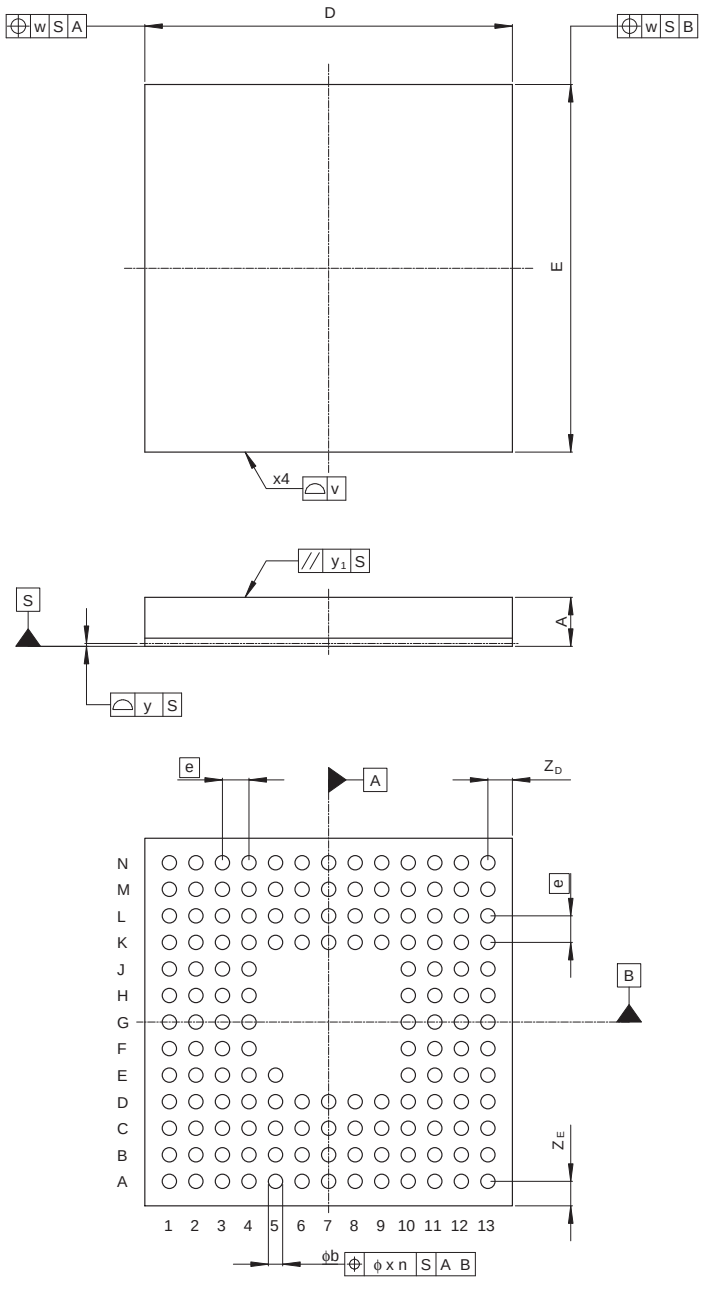



| Reference Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | — | 13.0 | — |
| E | — | 13.0 | — |
| v | — | — | 0.15 |
| w | — | — | 0.20 |
| A | — | — | 1.40 |
| $A_1$ | 0.35 | 0.40 | 0.45 |
| e | — | 0.80 | — |
| b | 0.45 | 0.50 | 0.55 |
| x | — | — | 0.08 |
| y | — | — | 0.10 |
| $y_1$ | — | — | 0.2 |
| $S_D$ | — | — | — |
| $S_E$ | — | — | — |
| $Z_D$ | — | 0.90 | — |
| $Z_E$ | — | 0.90 | — |

**Figure A 176-Pin LFBGA (PLBG0176GA-A) Package Dimensions**

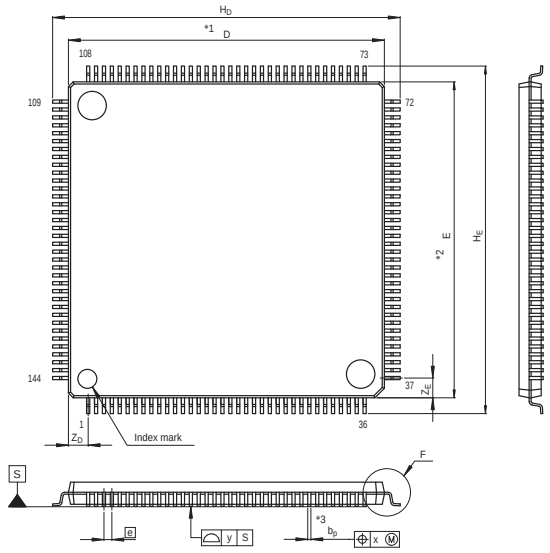
| JEITA Package Code | RENESAS Code | Previous Code | MASS[Typ.] |
|---|---|---|---|
| P-TFLGA145-9x9-0.65 | PTLG0145JB-A | - | 0.15g |

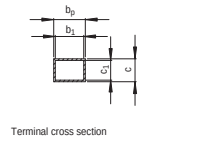


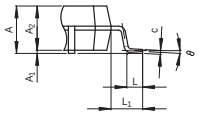

| Reference Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | — | 9.0 | — |
| E | — | 9.0 | — |
| v | — | — | 0.15 |
| w | — | — | 0.20 |
| A | — | — | 1.2 |
| $A_1$ | — | — | — |
| e | — | 0.65 | — |
| b | 0.30 | 0.35 | 0.40 |
| x | — | — | 0.08 |
| y | — | — | 0.1 |
| $y_1$ | — | — | 0.20 |
| $S_D$ | — | — | — |
| $S_E$ | — | — | — |
| $Z_D$ | — | 0.6 | — |
| $Z_E$ | — | 0.6 | — |

**Figure B 145-Pin TFLGA (PTLG0145JB-A) Package Dimensions**

| JEITA Package Code | RENESAS Code | Previous Code | MASS[Typ.] |
|---|---|---|---|
| P-LFQFP144-20x20-0.50 | PLQP0144KA-A | 144P6Q-A / FP-144L / FP-144LV | 1.2g |



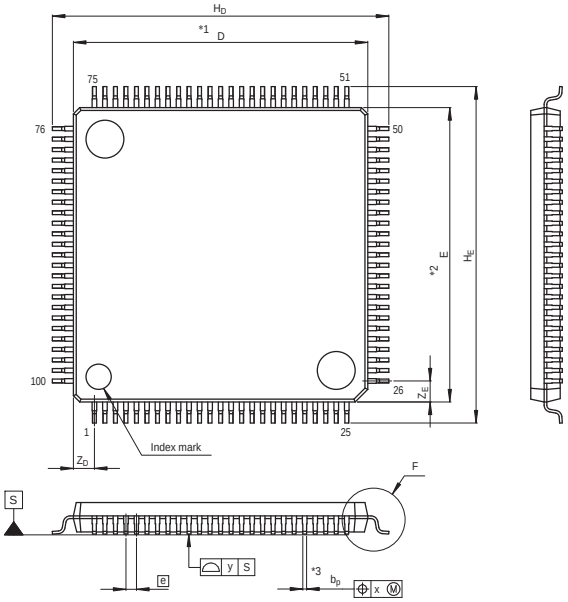



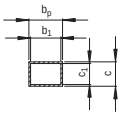

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

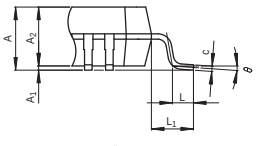
| Reference Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | 19.9 | 20.0 | 20.1 |
| E | 19.9 | 20.0 | 20.1 |
| $A_2$ | — | 1.4 | — |
| $H_D$ | 21.8 | 22.0 | 22.2 |
| $H_E$ | 21.8 | 22.0 | 22.2 |
| A | — | — | 1.7 |
| $A_1$ | 0.05 | 0.1 | 0.15 |
| $b_p$ | 0.17 | 0.22 | 0.27 |
| $b_1$ | — | 0.20 | — |
| c | 0.09 | 0.145 | 0.20 |
| $c_1$ | — | 0.125 | — |
| θ | 0° | — | 8° |
| e | — | 0.5 | — |
| x | — | — | 0.08 |
| y | — | — | 0.10 |
| $Z_D$ | — | 1.25 | — |
| $Z_E$ | — | 1.25 | — |
| L | 0.35 | 0.5 | 0.65 |
| $L_1$ | — | 1.0 | — |

**Figure C 144-Pin LQFP (PLQP0144KA-A) Package Dimensions**

| JEITA Package Code | RENESAS Code | Previous Code | MASS[Typ.] |
|---|---|---|---|
| P-LFQFP100-14x14-0.50 | PLQP0100KB-A | 100P6Q-A / FP-100U / FP-100UV | 0.6g |



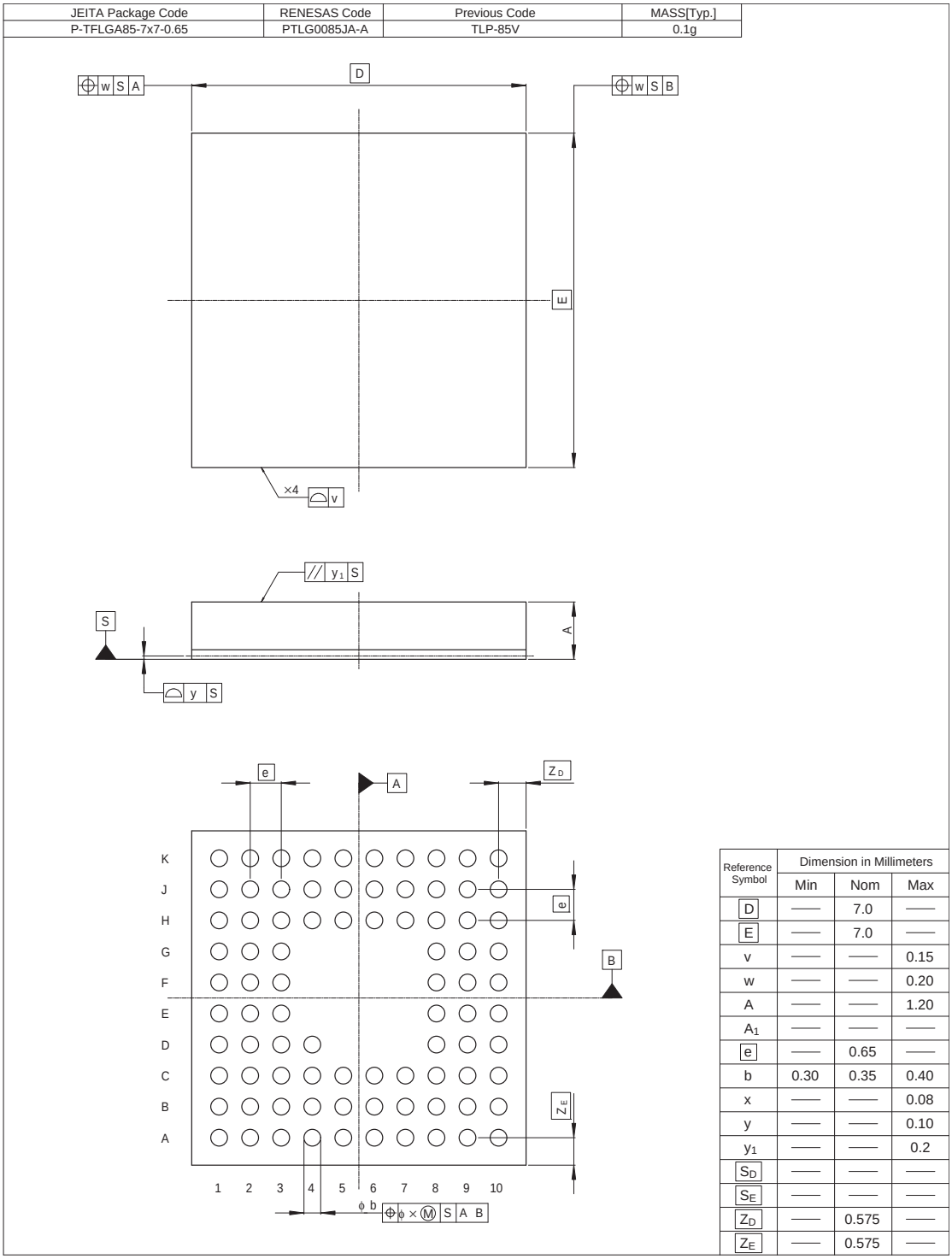




NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

| Reference Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | 13.9 | 14.0 | 14.1 |
| E | 13.9 | 14.0 | 14.1 |
| $A_2$ | — | 1.4 | — |
| $H_D$ | 15.8 | 16.0 | 16.2 |
| $H_E$ | 15.8 | 16.0 | 16.2 |
| A | — | — | 1.7 |
| $A_1$ | 0.05 | 0.1 | 0.15 |
| $b_p$ | 0.15 | 0.20 | 0.25 |
| $b_1$ | — | 0.18 | — |
| c | 0.09 | 0.145 | 0.20 |
| $c_1$ | — | 0.125 | — |
| θ | 0° | — | 8° |
| e | — | 0.5 | — |
| x | — | — | 0.08 |
| y | — | — | 0.08 |
| $Z_D$ | — | 1.0 | — |
| $Z_E$ | — | 1.0 | — |
| L | 0.35 | 0.5 | 0.65 |
| $L_1$ | — | 1.0 | — |

**Figure D 100-Pin LQFP (PLQP0100KB-A) Package Dimensions**

| JEITA Package Code | RENESAS Code | Previous Code | MASS[Typ.] |
|---|---|---|---|
| P-TFLGA85-7x7-0.65 | PTLG0085JA-A | TLP-85V | 0.1g |




| Reference Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | — | 7.0 | — |
| E | — | 7.0 | — |
| v | — | — | 0.15 |
| w | — | — | 0.20 |
| A | — | — | 1.20 |
| $A_1$ | — | — | — |
| e | — | 0.65 | — |
| b | 0.30 | 0.35 | 0.40 |
| x | — | — | 0.08 |
| y | — | — | 0.10 |
| $y_1$ | — | — | 0.2 |
| $S_D$ | — | — | — |
| $S_E$ | — | — | — |
| $Z_D$ | — | 0.575 | — |
| $Z_E$ | — | 0.575 | — |

**Figure E 85-Pin TFLGA (PTLG0085JA-A) Package Dimensions**

# REVISION HISTORY — RX62N Group, RX621 Group Datasheet

| Rev. | Date | Description | |
|---|---|---|---|
| | | Page | Summary |
| 1.00 | 2011.02.04 | — | First Edition issued |
| 1.10 | 2011.02.10 | — | Features reviewed |
| 1.20 | 2011.06.10 | | 1. Overview |
| | | 2 to 5 | Table 1.1 Outline of Specification, Description changed |
| | | 40 to 46 | Table 1.9 Pin Functions, Description changed |
| | | | 4. I/O Registers |
| | | 52 to 86 | Table 4.1 List of I/O Registers (Address Order), Description changed |
| | | | 5. Electrical Characteristics |
| | | 90 | Table 5.2 DC Characteristics (3) , changed |
| | | 111 | Figure 5.23 EDACK0 and EDACK1 Single-Address Transfer Timing (for a CS Area), changed |
| | | 111 | Figure 5.24 EDACK0 and EDACK1 Single-Address Transfer Timing (for SDRAM), changed |
| 1.30 | 2012.01.11 | | 1. Overview |
| | | 2 | Table 1.1 Outline of Specifications (1/4), changed, note 1, note 2 deleted |
| | | 13 | Figure 1.6 Pin Assignment of the 144-Pin LQFP (Assistance Diagram), changed |
| | | 15 | Figure 1.8 Pin Assignment of the 100-Pin LQFP (Assistance Diagram), changed |
| | | 33 | Table 1.7 List of Pins and Pin Functions (100-Pin LQFP) (1/4), changed |
| | | 37 | Table 1.8 List of Pins and Pin Functions (85-Pin TFLGA) (2/3), changed |
| | | | 4. I/O Registers |
| | | 52 to 87 | Table 4.1 List of I/O Registers (Address Order), Description changed |
| | | | 5. Electrical Characteristics |
| | | 91 | Table 5.4 DC Characteristics (3), specification added |
| | | 98 | Table 5.9 Control Signal Timing, note changed |
| | | 122 | Table 5.18 Timing of On-Chip Peripheral Modules (6), conditions changed |

Classifications

- Items with Technical Update document number: Changes according to the corresponding issued Technical Update
- Items without Technical Update document number: Minor changes that do not require Technical Update to be issued

| Rev. | Date | Description | | Classification |
|---|---|---|---|---|
| | | Page | Summary | |
| 1.40 | Jul 16, 2014 | 4. I/O Registers | | |
| | | 69, 70 | Table 5.1 List of I/O Registers (Address Order), changed | TN-RX*-A012A/E |
| | | 5. Electrical Characteristics | | |
| | | 91 | Table 5.4 DC Characteristics (3), Note 1, changed | |
| | | 101 to 104 | Figure 5.10 External Bus Timing/Normal Read Cycle (Bus Clock Synchronized) to Figure 5.14 External Bus Timing/External Wait Control, changed | |
| | | 114 | Table 5.13 Timing of On-Chip Peripheral Modules (2): SCI changed | |
| | | 140 | Table 5.25 ROM (Flash Memory for Code Storage) Characteristics (1), Note 2, changed, Note 3, deleted, Table 5.26 ROM (Flash Memory for Code Storage) Characteristics (2), added | TN-RX*-A051A/E |
| | | Appendix 2. Package Dimensions | | |
| | | 145 | Figure C 144-Pin LQFP (PLQP0144KA-A) Package Dimensions, Figure D 100-Pin LQFP (PLQP0100KB-A) Package Dimensions, changed | |

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## General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   — The characteristics of an MPU or MCU in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

# Notice

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