

MTMC8E2A0LBF

Dual N-channel MOSFET

For lithium-ion secondary battery protection circuit

■ Features

- Low drain-source ON resistance: $R_{DS(on)typ.} = 15\text{ m}\Omega$ ($V_{GS} = 4.5\text{ V}$)
- Built-in gate resistor
- Halogen-free / RoHS compliant
(EU RoHS / UL-94 V-0 / MSL:Level 1 compliant)

■ Marking Symbol: 4B

■ Packaging

MTMC8E2A0LBF Embossed type (Thermo-compression sealing):
3 000 pcs / reel (standard)

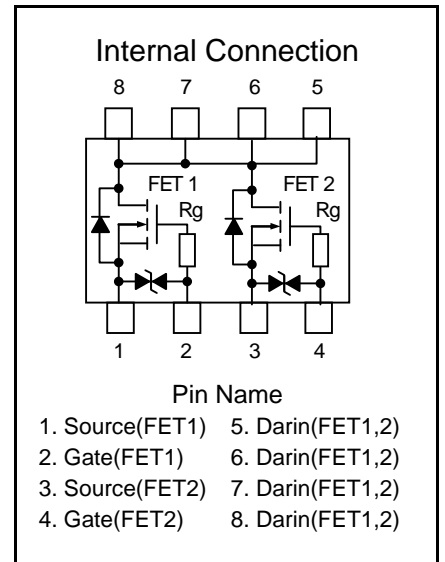
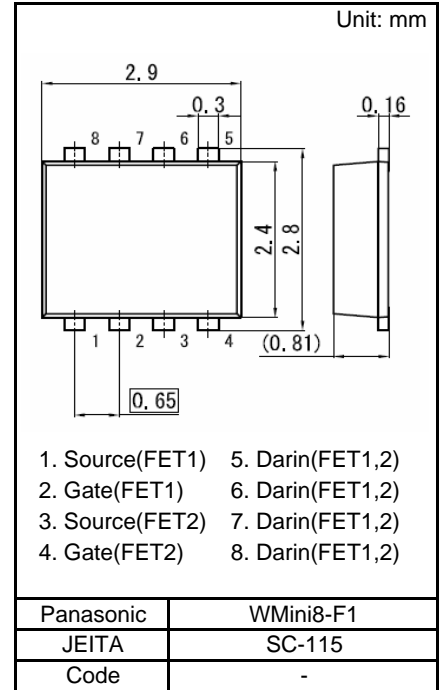
■ Absolute Maximum Ratings $T_a = 25\text{ }^\circ\text{C}$

Parameter		Symbol	Rating	Unit
FET1	Drain-source Voltage	V_{DS}	20	V
	Gate-source Voltage	V_{GS}	± 12	V
FET2	Drain Current	I_D	7.0	A
	Peak Drain Current	I_{Dp}	42	A
Overall	Total Power Dissipation	$PD1^{*1}$	1.0	W
		$PD2^{*1,*2}$	1.2	
		$PD3^{*3}$	0.4	
	Channel Temperature Range	T_{ch}	150	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55 to +150	$^\circ\text{C}$	

Note: *1 Glass epoxy board: 25.4 mm × 25.4 mm × 0.8 mm Copper foil of the drain portion should have a area of 300 mm² or more
PD absolute maximum rating Non-heat sink: 400 mW

*2 $t = 10\text{ s}$

*3 Non-heat sink



Resistance Value	R_g	1	$k\Omega$
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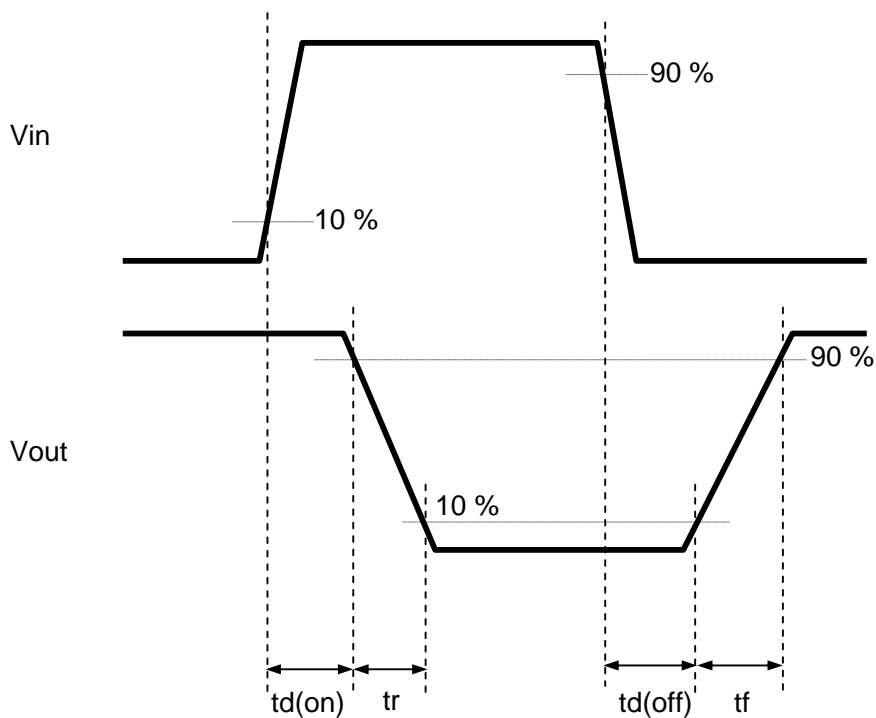
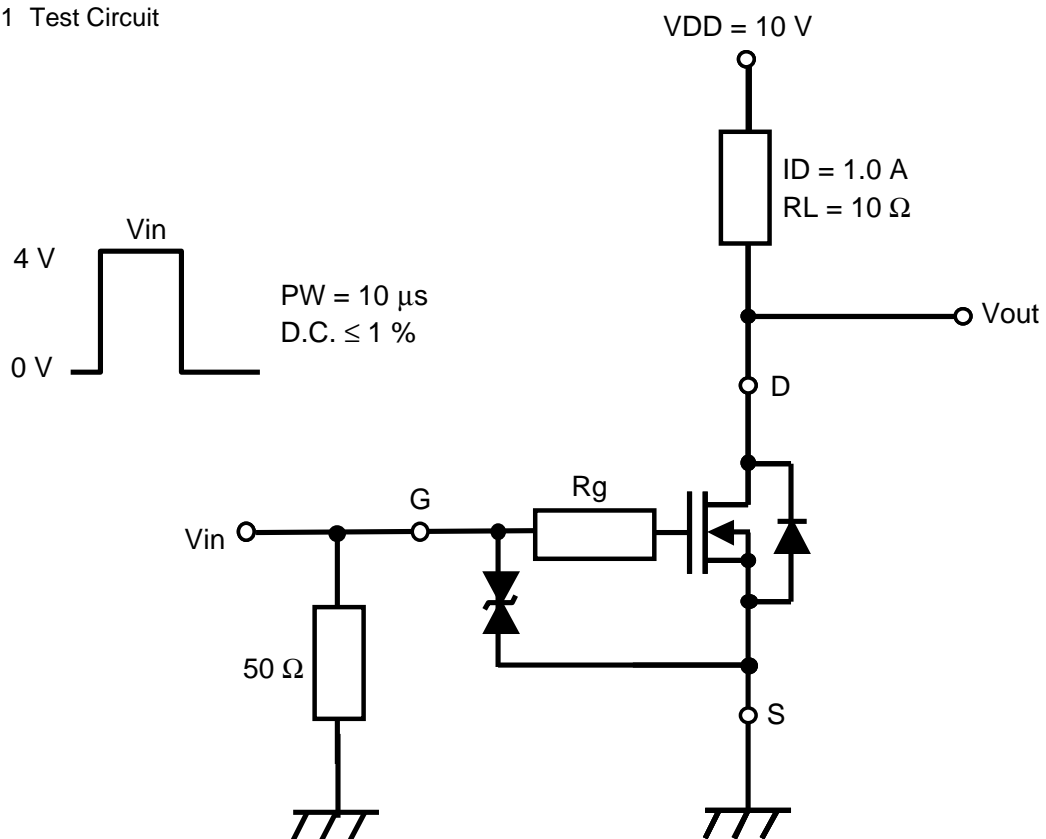
■ Electrical Characteristics Ta = 25 °C ± 3 °C
FET1,FET2

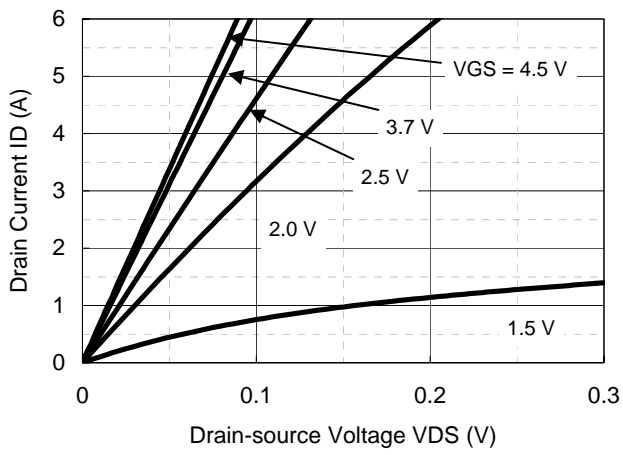
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Drain-source Breakdown Voltage	VDSS	ID = 1.0 mA, VGS = 0 V	20			V
Zero Gate Voltage Drain Current	IDSS	VDS = 20 V, VGS = 0 V			1.0	μA
Gate-source Leakage Current	IGSS	VGS = ±8.0 V, VDS = 0 V			±10	μA
Gate-source Threshold Voltage	Vth	ID = 1.0 mA, VDS = 10 V	0.40	0.85	1.30	V
Drain-source On-state Resistance	RDS(on)1	ID = 2.0 A, VGS = 4.5 V		15	21	mΩ
	RDS(on)2	ID = 2.0 A, VGS = 3.7 V		18	25	
	RDS(on)3	ID = 2.0 A, VGS = 2.5 V		22	33	
Forward transfer admittance	Yfs	ID = 1.0 A, VDS = -10 V	3.0			S
Input Capacitance	Ciss	VDS = 10 V, VGS = 0 V, f = 1 MHz		1 450		pF
Output Capacitance	Coss			100		
Reverse Transfer Capacitance	Crss			90		
Turn-on Delay Time *1	td(on)	VDD = 10 V, VGS = 0 to 4 V, ID = 1.0 A		0.33		μs
Rise Time *1	tr			0.70		
Turn-off Delay Time *1	td(off)	VDD = 10 V, VGS = 4 to 0 V, ID = 1.0 A		4.0		μs
Fall Time *1	tf			2.0		

Note: Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 Measuring methods for transistors.

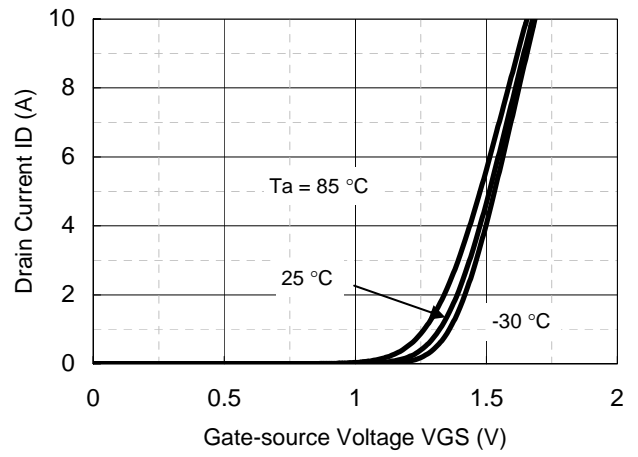
*1 See Test Circuit.

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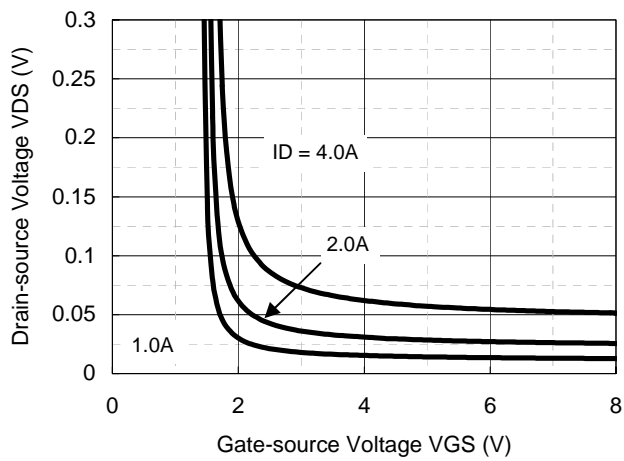




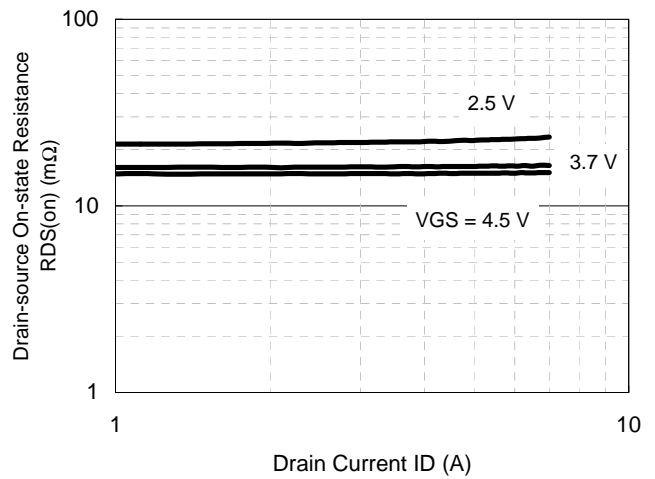
ID - VDS



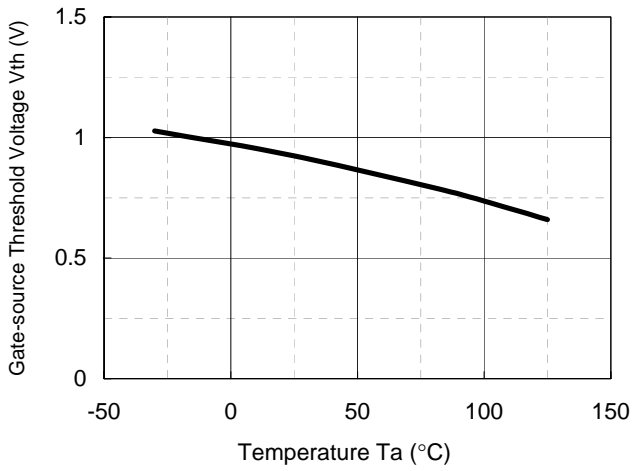
ID - VGS



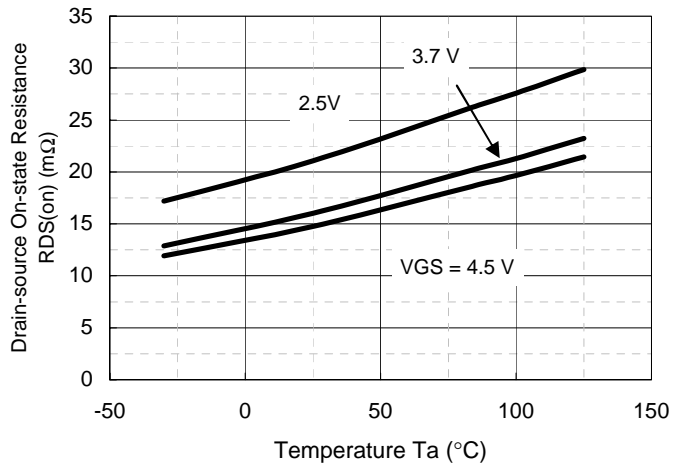
VDS - VGS



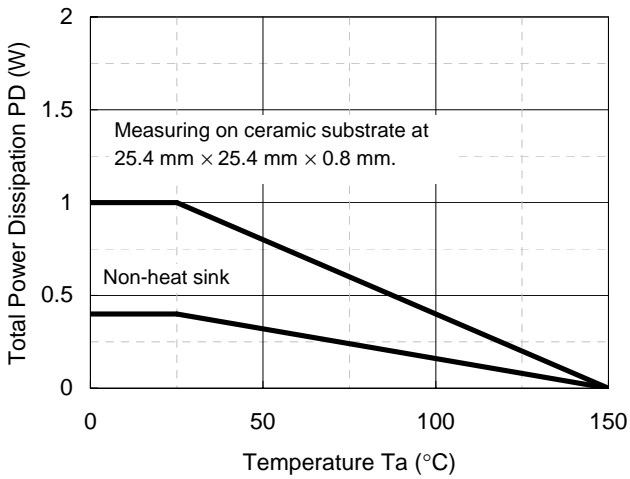
RDS(on) - ID



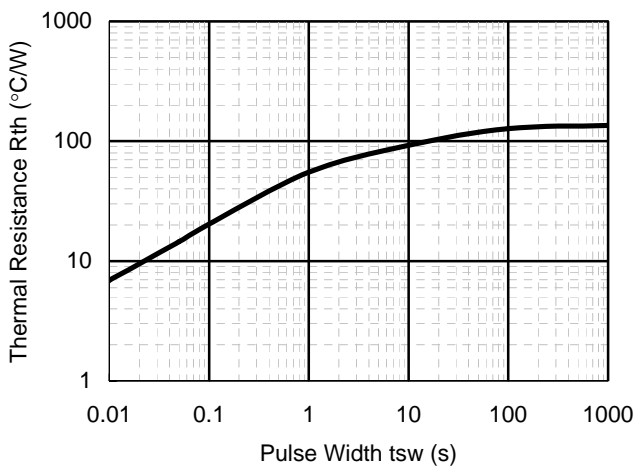
V_{th} - T_a



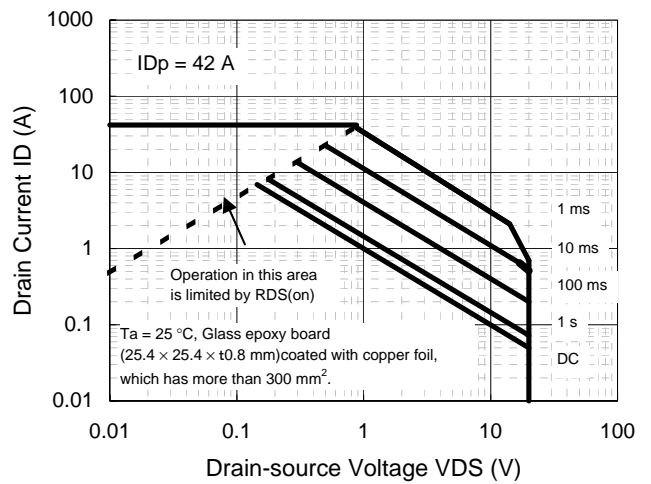
$R_{DS(on)}$ - T_a



P_D - T_a



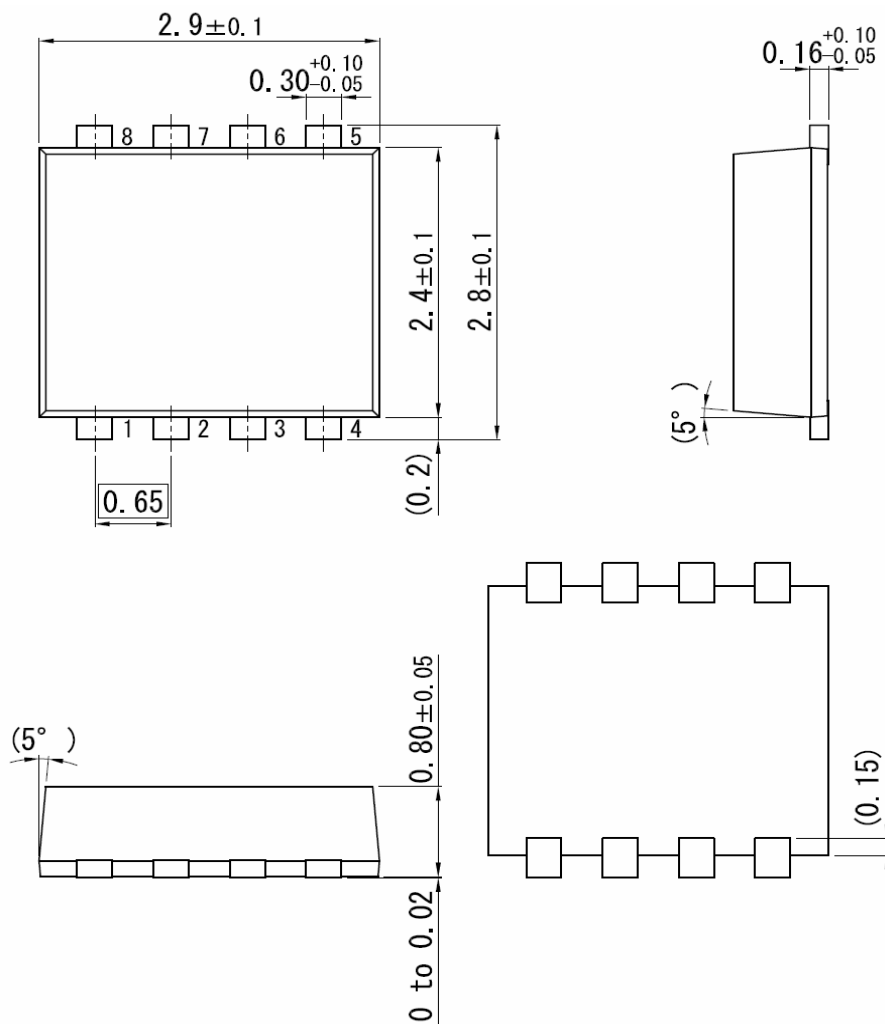
R_{th} - t_{sw}



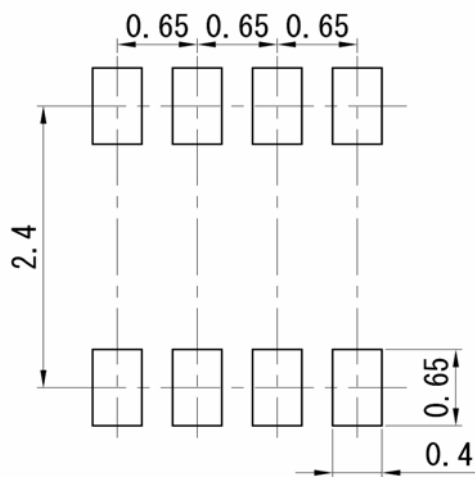
Safe Operating Area

WMini8-F1

Unit: mm



■ Land Pattern (Reference) (Unit: mm)



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