

## PET800-12-074xA



The **PET800-12-074xA** is an 800 Watts, 1 U form factor power supply module with Active PFC (Power Factor Correction) and PMBus (Power Management Bus). It converts standard AC mains power into a main output of 12 V for powering intermediate bus architectures (IBA) in high performance and reliability servers, routers, and network switches.

The PET800-12-074 meets international safety standards and displays the CE-Mark for the European Low Voltage Directive (LVD).

### Key Features & Benefits

- Best-in-Class, 80 PLUS Certified “Platinum” Efficiency
- 750 W INTEL CRPS (Common Redundant Power Supply) Compatible
- Wide Input Voltage Range 90-264 VAC
- AC Input With Power Factor Correction
- Always-On 24 W Standby Output (12 V/2 A)
- Hot-Plug Capable
- Parallel Operation with Active Digital Current Sharing
- DC-DC Digital Controls for Improved Performance
- High Density Design 25 W/in<sup>3</sup>
- Small Form Factor 73.5 x 39.0 x 185 mm
- PMBus™ for Control, Programming and Monitoring
- Over Temperature, Output Over Voltage and Over Current Protection
- One DC OK Signalling Status LED

### Applications

- High Performance Servers
- Routers
- Network Switches

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# PET800-12-074xA

## 1. ORDERING INFORMATION

PET	800	-	12	-	074	x	A
Product Family	Power Level	Dash	V1 Output	Dash	Width	Airflow	Input
PET	800 W		12 V		74 mm	N: Normal R: Reversed	A: AC

## 2. OVERVIEW

The PET800-12-07 AC-DC power supply is a mainly DSP controlled, highly efficient front-end. It incorporates resonance-soft-switching technology and interleaved power trains to reduce component stresses, providing increased system reliability and very high efficiency. With a wide input operating voltage range, the PET800-12-074 maximizes power availability in demanding server, network switch, and router applications. The front-end is fan cooled and ideally suited for server integration with a matching airflow path.

The PFC stage is controlled using interleaved Critical mode to guarantee best efficiency and unity power factor over a wide operating range.

The DC-DC stage uses soft switching resonant technology in conjunction with synchronous rectification. An active OR-ing device on the output ensures no reverse load current and renders the supply ideally suited for operation in redundant power systems.

The always-on standby output, provides power to external power distribution and management controllers. It is protected with an active OR-ing device for maximum reliability.

Status information is provided with front-panel LED. In addition, the power supply can be controlled and the fan speed set via the I2C bus. It allows full monitoring of the supply, including input and output voltage, current, power, and inside temperatures.

Cooling is managed by a fan controlled by the DSP controller. The fan speed is adjusted automatically depending on the actual power demand and supply temperature and can be overridden through the I<sup>2</sup>C bus.

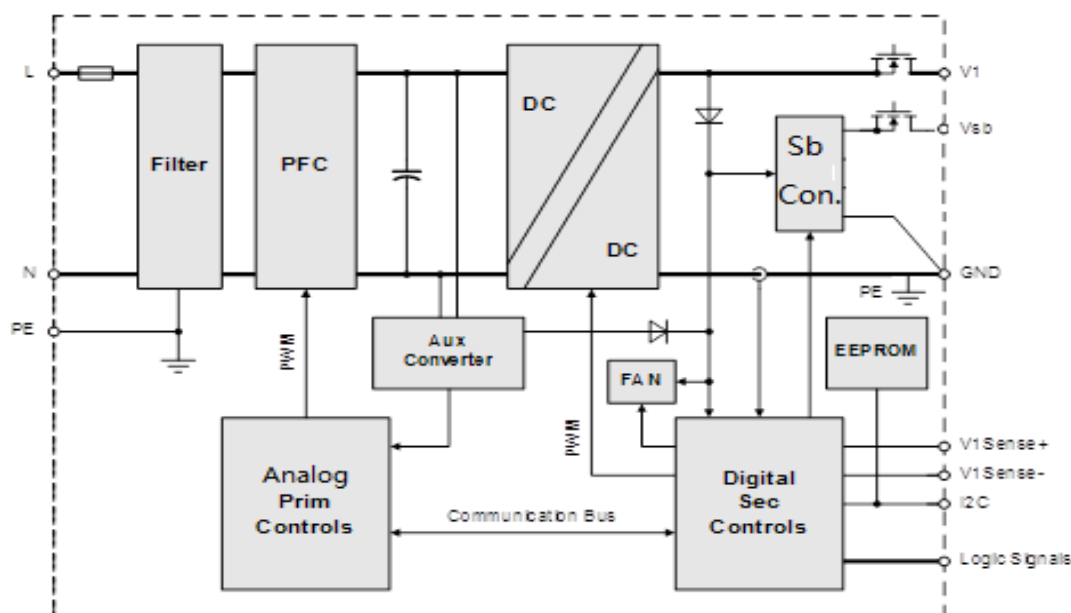


Figure 1 - PET800-12-074 Block Diagram

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## 3. INPUT

General Condition:  $T_A = 0 \dots 50 \text{ }^{\circ}\text{C}$  unless otherwise noted.

PARAMETER		DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
$V_{i\ nom}$	Input Voltage Ranges	Low line	90	115	132	VAC
		High line	180	230	264	VAC
$V_i$	Input Voltage Ranges	Normal operating ( $V_{i\ min}$ to $V_{i\ max}$ )	90		264	VAC
$I_{i\ max}$	Max Input Current				12	A <sub>rms</sub>
$I_{i\ p}$	Inrush Current Limitation <sup>1</sup> (Cold start)	$V_{i\ min}$ to $V_{i\ max}$ , 90°(Phase), $T_{NTC}$ =25 °C			50	A <sub>p</sub>
$I_i$	Input current	90-132 VAC			12	A <sub>rms</sub>
		180-264 VAC			6	A <sub>rms</sub>
$F_i$	Input Frequency		47	50/60	63	Hz
$PF$	Power Factor	Vi nom, 50 Hz, I1 nom	0.93			W/VA
$V_{i\ on}$	Turn-on Input Voltage	Brown in	80	85	90	VAC
$V_{i\ off}$	Turn-off Input Voltage	Brown out	75	80	85	VAC
$\eta$	Efficiency without Fan	$V_{i\ nom}$ , $0.2 \cdot I_{x\ nom}$ , $V_{x\ nom}$ , $T_A = 25\ ^\circ C$		92		
		$V_{i\ nom}$ , $0.5 \cdot I_{x\ nom}$ , $V_{x\ nom}$ , $T_A = 25\ ^\circ C$		94.2		%
		$V_{i\ nom}$ , $I_{x\ nom}$ , $V_{x\ nom}$ , $T_A = 25\ ^\circ C$		93		
$T_{hold}$	Hold-up Time	After last AC zero point		16		mS

<sup>1</sup> The charging currents for X capacitors are not considered as in-rush current

### 3.1. Efficiency

The power supply module efficiency should meet at least 80Plus Platinum rating, the efficiency should be measured at 230 VAC and with external fan power according to 80Plus efficiency measurement specifications.

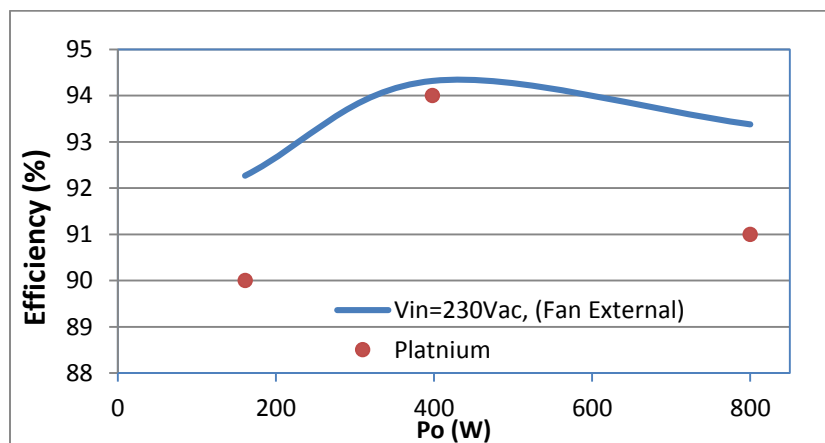


Figure 2 - Efficiency vs. Load Current (Ratio Metric Loading)

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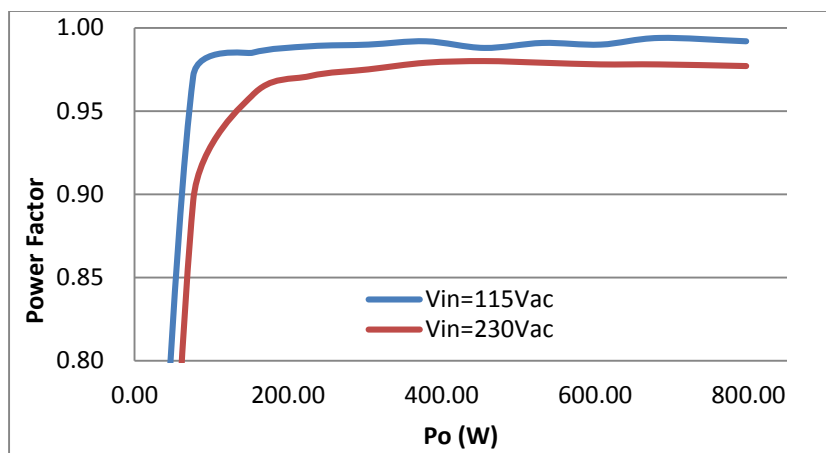


Figure 3 - Power factor vs. Load current

## 4. OUTPUT

General Condition:  $T_a = 0 \dots +50^\circ\text{C}$  unless otherwise noted.

PARAMETER	DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
<b>Main Output <math>V_1</math></b>					
$V_{1\text{ nom}}$	Nominal Output Voltage		12.0		VDC
$V_{1\text{ set}}$	Output Setpoint Accuracy	-0.5		+0.5	% $V_{1\text{ nom}}$
$dV_{SB\text{ tot}}$	Total Regulation	-5		+5	% $V_{SB\text{ nom}}$
$P_{1\text{ nom}}$	Nominal Output Power		780		W
$I_{1\text{ nom}}$	Nominal Output Current <sup>3</sup>		65 59.6		ADC
$V_{1\text{ pp}}$	Output Ripple Voltage <sup>2</sup>			120	mVpp
$dI_{\text{share}}$	Current Sharing	-6.5		+6.5	ADC
$V_{I\text{ share}}$			6.0		VDC
$dV_{\text{dyn}}$	Dynamic Load Regulation	-5		+5	% $V_{1\text{ nom}}$
$T_{\text{rec}}$	Recovery Time			2	mS
$C_{V1\text{ Load}}$	Capacitive Loading			1,1000	$\mu\text{F}$
<b>Standby Output <math>V_{SB}</math></b>					
$V_{SB\text{ nom}}$	Nominal Output Voltage		12.0		VDC
$V_{SB\text{ set}}$	Output Setpoint Accuracy	-1		+1	% $V_{1\text{ nom}}$
$dV_{SB\text{ tot}}$	Total Regulation	-5		+5	% $V_{SB\text{ nom}}$
$P_{SB\text{ nom}}$	Nominal Output Power		24		W
$I_{SB\text{ nom}}$	Nominal Output Current		2		ADC
$V_{SB\text{ pp}}$	Output Ripple Voltage <sup>2</sup>			120	mVpp
$dV_{SB\text{ dyn}}$	Dynamic Load Regulation	-5		+5	% $V_{SB\text{ nom}}$
$T_{\text{rec}}$	Recovery Time			250	$\mu\text{S}$
$C_{VSB\text{ load}}$	Capacitive Loading for $V_{SB}$			350	$\mu\text{F}$

<sup>2</sup> The output noise and ripple measurement was made with 20 MHz bandwidth using a 6 inch twisted pair, terminated with a 10  $\mu\text{F}$  tantalum capacitor in parallel with a 0.1  $\mu\text{F}$  ceramic capacitor. The output ripple voltage on  $V_{SB}$  is influenced by the main output  $V_1$ . Evaluating  $V_{SB}$  output ripple must be done when maximum load is applied to  $V_1$ .

<sup>3</sup> The output power derating at low line only for PET800-12-050NA, for RA model no derating required

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## 4.1. Grounding

The output ground of the pins of the power supply provides the output power return path. The ground output at the PCB card edge shall be connected to the safety ground (power supply enclosure). This grounding should be well designed to ensure passing the max allowed Common Mode Noise levels.

The power supply shall be provided with a reliable protective earth ground. All secondary circuits shall be connected to protective earth ground. Resistance of the ground returns to chassis shall not exceed 1.0 mΩ. This path may be used to carry DC-current.

## 4.2. HOT Swap Requirements

Hot Swapping a power supply is the process of inserting and extracting a power supply from an operating power system. During this process the output voltages shall remain within the limits with the capacitive load specified. The hot swap test must be conducted when the system is operating under static, dynamic and zero loading conditions.

The power supply can be hot swapped by the following method:

**Extraction:** The power supply may be removed from the system while operating with PS\_ON asserted, while in standby mode with PS\_ON de-asserted or with no AC applied. No connector damage should occur during un-mating of the power supply from the power distribution board (PDB).

**Insertion:** The power supply may be inserted into the system with PS\_ON asserted, with PS\_ON de-asserted or with no AC power present for that supply. No connector damage should occur due to the mating of the output and input connector.

In general a failed (of by internal latch or external control) supply may be removed, then replaced with a good power supply, however, hot swap needs to work with operational as well as failed power supplies. The newly inserted power supply will get turned on into standby or Power On mode once inserted.

## 5. PROTECTION

PARAMETER	DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
$F$	Input Fuse (Line)		12.5		A <sub>rms</sub>
$V_{1\text{ OV}}$	OV Threshold $V_1$	13.3		14.5	VDC
$V_{1\text{ UV}}$	UV Threshold $V_1$		10.5		VDC
$I_{V1\text{ lim}}$	Current Limit $V_1$	71.5		97.5	ADC
$I_{V1\text{ SC}}$	Max Short Circuit Current $V_1$		250		ADC
$V_{SB\text{ OV}}$	OV Threshold $V_{SB}$	13.3		14.5	VDC
$I_{SB\text{ lim}}$	Current Limit $V_{SB}$	3.5		4.5	ADC
$T_{SD}$	Over Temperature On Inlet	Automatic recovery with Hysteresis_ for NA model		70	°C
	Over Temperature Oring	Automatic recovery with Hysteresis_ for NA model		100	°C
$T_{SD}$	Over Temperature On Inlet	Automatic recovery with Hysteresis_ for RA model		60	°C
	Over Temperature Oring	Automatic recovery with Hysteresis_ for RA model		105	°C

### 5.1. Over Voltage Protection

The PET front-ends provide a fixed threshold over voltage protection implemented with a HW comparator. Once an over voltage condition has been triggered, the power supply will shut down and latch the fault condition. The latch can be unlatch by disconnecting the supply from the AC mains or by toggling the PS\_ON input.

### 5.2. Under Voltage Protection

The main output will latch off when  $V_1$  drop to below the UV threshold. The latch can be unlatch by disconnecting the supply from the AC mains or by toggling the PS\_ON input. The main output will shut down if the  $V_{SB}$  voltage drop below 8V and recover when  $V_{SB}$  voltage higher than 10 V.

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## 5.3. Current Limitation

### Main Output

The main output exhibits a substantially rectangular output characteristic controlled by a software feedback loop. If it runs in current limitation and its voltage drops below ~10.8 VDC for more than 10 mS, the output will latch off (standby remains on).

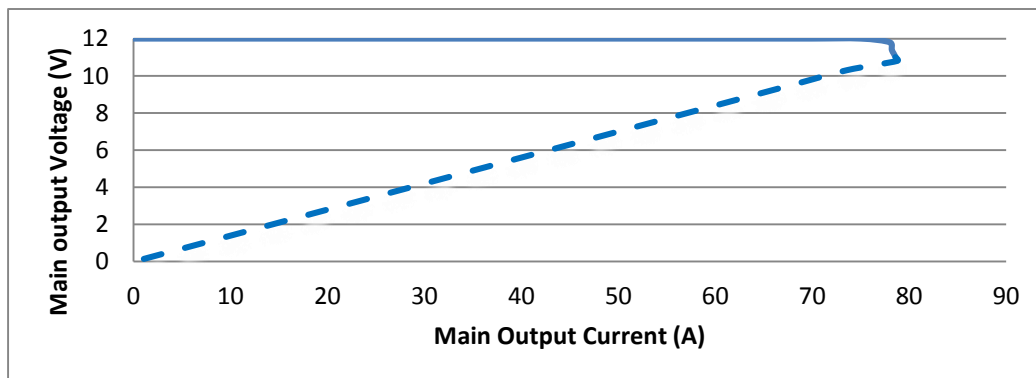


Figure 4 - Current Limitation on V1 ( $V_i = 230$  VAC)

A second current limitation circuit on V1 will immediately switch off the main output if the output current increases beyond the peak current trip point. The latch can be unlocked by disconnecting the supply from the AC mains or by toggling the PS\_ON input.

### Standby Output

The standby output exhibits a substantially rectangular output characteristic down to 0 V (hiccup mode). If it runs in current Limitation and standby output will be shut down and power supply into hiccup mode, the main output will be inhibited during the status.

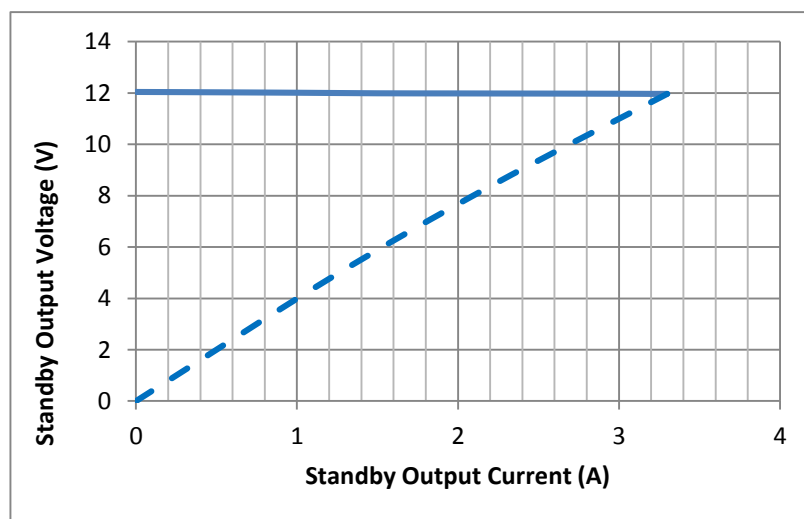


Figure 5 - Current limitation on VSB

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## 6. TIMING SPECIFICATIONS

These are the timing requirements for the power supply operation. The output voltages must rise from 10% to within regulation limits ( $T_{vout\_rise}$ ) within 70 mS. For 12VSB, it is allowed to rise from 1 to 25 mS. All outputs must rise monotonically. Table below shows the timing requirements for the power supply being turned on and off via the AC input, with PS\_ON held low and the PS\_ON signal, with the AC input applied.

### 6.1. Output Voltage Timing

The timing of signals and outputs are specified in the Table below and illustrated in Figure 6.

ITEM	DESCRIPTION	MIN	MAX	UNITS
$T_{vout\_rise}$	Output voltage rise time from each main output		70	mS
$T_{sb\_on\_delay}$	Delay from AC being applied to 12VSB being within regulation.		1500	mS
$T_{ac\_on\_delay}$	Delay from AC being applied to all output voltages being within regulation.		2500	mS
$T_{vout\_holdup}$	Time all main output 12VI voltage stay within regulation after loss of AC.	16		mS
$T_{pwok\_holdup}$	Delay from loss of AC to de-assertion of PWOK.	12		mS
$T_{pson\_on\_delay}$	Delay from PS_ON# active to output voltage within regulation limits.	5	400	mS
$T_{pson\_pwok}$	Delay from PS_ON# deactivate to PWOK being de-asserted.		50	mS
$T_{pwok\_on}$	Delay from output voltage (12V) within regulation limits to PWOK asserted at turn on.	100	500	mS
$T_{pwok\_off}$	Delay from PWOK de-asserted to output voltage dropping out of regulation limits.	4		mS
$T_{pwok\_low}$	Duration of PWOK being in the de-asserted state during an off/on cycle using AC or the PS_ON signal.	100		mS
$T_{sb\_vout}$	Delay from 12VSB being in regulation to main output being in regulation at AC turn on.	50	1000	mS
$T_{VSB\_holdup}$	Time the 12VSB output voltage stays within regulation after loss of AC	70		mS

Table 1 - Turn on/off timing

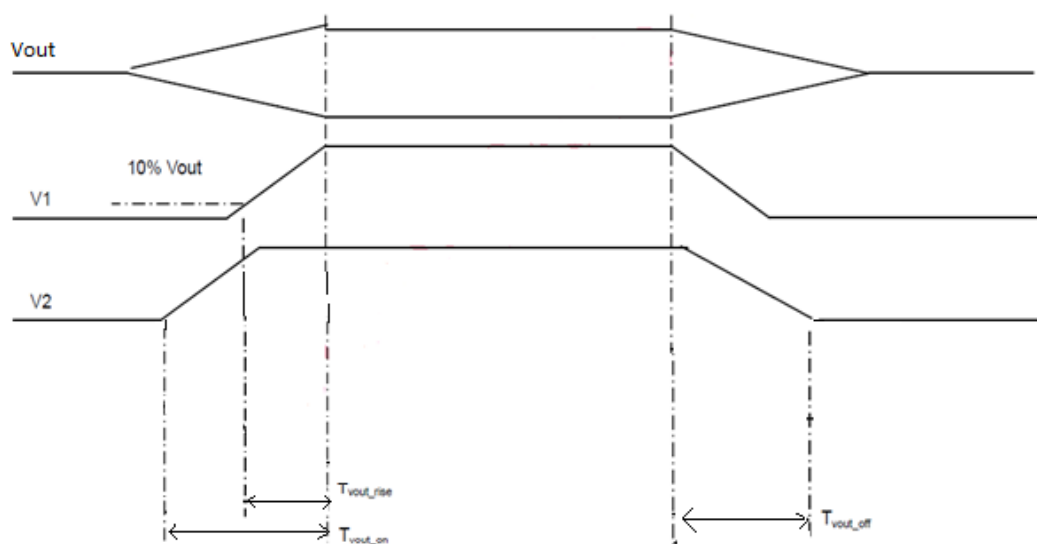
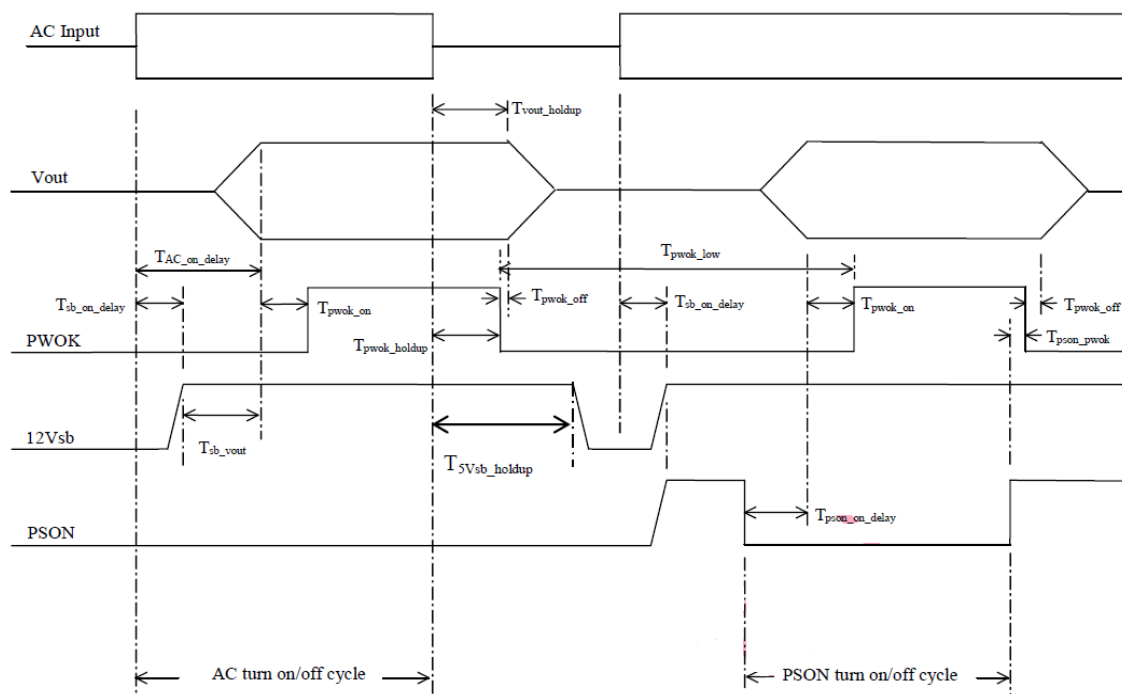


Figure 6 – Output Voltage timing

$T_{vout\_rise}$ : The 12 Vsb and 12 V output rise time shall be 1 mS to 25 mS.



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*Figure 7 - Turn On/Off Timing*

## 6.2. Over Shoot

Any output overshoot at turn on shall be less than 10% of the nominal output value. Any overshoot shall recover to within the specified regulation in less than 10 mS.

### 6.3. Under Shoot

Any output shall not undershoot at turn on or off cycle under any circumstances.

## 6.4. Temperature Coefficient

After operating for 30 minutes or longer at 25 ° C ambient, the output voltages shall not change by more than  $\pm 0.05\%$  per degree C for any given line and load conditions.

## 7. MONITORING FOR PMBus ACCURACY

PARAMETER		DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
$V_{i\ mon}$	Input RMS Voltage	$V_{i\ min} \leq V_i \leq V_{i\ max}$	-3		+3	%
$I_{i\ mon}$	Input RMS Current	$I_i > 4\ A_{rms}$	-10		+10	%
		$I_i \leq 4\ A_{rms}$	-0.4		+0.4	$A_{rms}$
$P_{i\ mon}$	True Input Power	$P_i > 200\ W$	-10		+10	%
		$P_i \leq 200\ W$	-20		+20	W
$V_{1\ mon}$	$V_1$ Voltage		-2		+2	%
$I_{1\ mon}$	$V_1$ Current	$I_1 > 10\ A$	-3		+3	%
		$I_1 \leq 10\ A$	-0.3		+0.3	A
$P_{o\ nom}$	Total Output Power	$P_o > 200\ W$	-5		+5	%
		$P_o \leq 200\ W$	-10		+10	W
$V_{SB\ mon}$	Standby Voltage		-2		+2	%
$I_{SB\ mon}$	Standby Current	$I_{SB} \leq I_{SB\ nom}$	-0.2		+0.2	A

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## 8. SIGNALING AND CONTROL

### 8.1. Electrical Characteristics

PARAMETER	DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
<b>PS ON# Signal Characteristics</b>					
Signal type (Active Low)	Accepts an open collector/drain input from the system. Pul-up to Vsb located in the power supply.				
PSON = Low	ON				
PSON= Open or High	OFF				
PSON = Low	OFF				
Logic level low	power supply ON	0		1.0	V
Logic level high	power supply OFF	2.0		5.25	V
Source current	Vpson = low			4	mA
Power up delay	T pson on delay	5		400	mS
PWOK delay	T pson pwok			50	mS
<b>PWOK Signal Characteristics</b>					
Signal type	Open collector/drain output from power supply. Pull-up to Vsb located in power supply.				
PWOK = High	Power Good				
PWOK = Low	Power Not Good				
Logic level low voltage	Isink = 4 mA	0		0.4	V
Logical level high voltage	Isource = 200 uA	2.4		5.25	V
Sink current	PWOK=low			4	mA
Source current,	PWOK=high			2	mA
PWOK delay	Tpwok on	100		500	mS
PWOK rise and fall time				100	uS
Power down delay	Tpwok off	1		200	mS
<b>SMB Alert Signal Characteristics</b>					
Signal Type	Open collector/drain output from power supply. Pull-up to Vsb located in power supply.				
Alert = High	Power OK				
Alert = Low	Power Alert to system				
Logic level low voltage	Isink=4 mA	0		0.4	V
Logic level high voltage	Isink=50 uA	2.4		3.46	V
Sink current	Alert = low	-		4	mA
Sink current	Alert = high			50	uA

**NOTE:** Signals that can be defined as low true use the following convention: Signal = low true.

### 8.2. Interfacing with Signals

All signal pins have protection diodes implemented to protect internal circuits. When the power supply is not powered, the protection devices start clamping at signal pin voltages exceeding  $\pm 0.5$  V. Therefore all input signals should be driven only by an open collector/drain to prevent back feeding inputs when the power supply is switched off.

If interconnecting of signal pins of several power supplies is required, then this should be done by decoupling with small signal schottky diodes as shown in examples in Figure 7 (except for SMB\_ALERT, PW\_OK pins). This will ensure the pin voltage is not affected by an unpowered power supply.

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## 8.3. Front LEDs

Status information is indicated by front-panel LED, LED is bi-colored: green and yellow. See Table 2 for different LED status.

POWER SUPPLY CONDITION	LED
No AC power to all PSU	OFF
AC present/only standby output on	1 Hz Flashing Green
Power supply DC output ON and OK	Green
Power supply failure	Yellow
Power supply warning	0.5 Hz Flashing Yellow*/Green*

NOTE: \* Flashing frequency: 1 Hz (0.5 sec Yellow/ 0.5 sec Green)

Table 2 - LED Status

## 8.4. PS\_ON

The PS\_ON signal is required to remotely turn on/off the main output of the power supply. PS\_ON is an active low signal that turns on the main output power rail. When this signal is not pulled low by the system or left open, the outputs (except the Standby output) turn off. PS\_ON is pulled to a standby voltage by a pull-up resistor internal to the power supply.

## 8.5. PWOK

PWOK is a power good signal and shall be pulled HIGH by the power supply to indicate that all outputs are within regulation limits. When any output voltage falls below regulation limits, an internal failure or when AC power has been removed for a time sufficiently long, so that power supply operation is no longer guaranteed, PWOK will be de-asserted to a LOW state. The start of the PWOK delay time shall be inhibited as long as any power supply output is in current limit.

## 8.6. SMB Alert

The SMB\_ALERT is an output signal and it is pulled to 3.3 V by a 4.7 K resistor in power supply. This signal indicates that the power supply is experiencing a problem that the user should investigate. This shall be asserted due to Critical events or Warning events. The signal shall activate in the case of critical component temperature reached a warning threshold, general failure, over-current, over-voltage, under-voltage, failed fan. This signal may also indicate the power supply is reaching its end of life or is operating in an environment exceeding the specified limits.

### 8.6.1. Thermal CLST

SMB Alert shall also be utilized for warning of critical thermal component temperatures. The Thermal CLST shall assert when the component temperature, which shall be reported by a dedicated thermal probe, is reaching below specified  $T_c$  to critical shut down. The power supply shall report the temperature in addition to Thermal CLST through.

## 8.7. PDB\_ALERT

To receive ALERT signal from system or PSU backplane, If signal is pulled LOW, the PSU internal fan shall be forced to run at maximum speed to improve thermal performance.

## 8.8. PDB\_FAULT

To receive a FAULT signal from system or PSU backplane. PSU shall shutdown if this pin is pulled HIGH.

## 8.9. Current Share

All outputs shall be capable of operating in a redundant current share mode. Eight power supplies may be operated in parallel. All outputs shall incorporate an isolation diode for fault isolation. Filter capacitors that are located after the isolation diode shall be of high reliability and shall be de-rated sufficiently to minimize failures. The +12 V current sharing shall be a single wire type. Connecting the ISHARE pins of each power supply together shall enable the current share feature. With the current share pins tied together, the output load current shall be balanced as defined below. The load share (ISHARE) shall be a single wire type. Connecting ISHARE pins of each PCM together shall enable the current

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share feature. With the current share pins tied together, the output load current shall be balanced to within 10% of full load (current difference should be less than 6.5 A). Shorting or opening of a current share pin shall not cause the output voltage to go out of steady state regulation. For 65 A the ISHARE voltage shall be 6 V for a single power supply.

## 8.10. Remote Sense

Main output has sense lines implemented to compensate for voltage drop on load wires. The maximum allowed voltage drop is 200 mV on the positive rail and 200 mV on the output return rail.

## 8.11. I<sup>2</sup>C / PMBus Communication

The interface driver in the PET supply is referenced to the V1 Return. The PET supply is a communication Slave device only; it never initiates messages on the I<sup>2</sup>C/SMBus by itself. The communication bus voltage and further characterized referenced in the Figure 8:

- There are 10K internal pull-up resistors
- The SDA/SCL IOs are 3.3/5 V tolerant
- Full SMBus clock speed of 100 kbps
- Clock stretching limited to 1 mS
- SCL low time-out of >25 mS with recovery within 10 mS

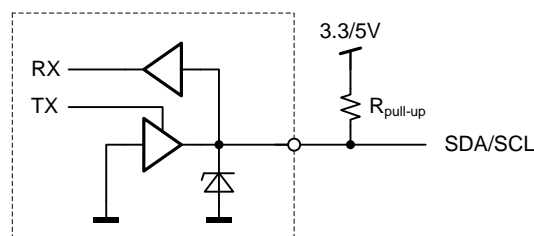


Figure 8 - Physical layer of communication interface

The SMB\_ALERT signal indicates that the power supply is experiencing a problem that the system agent should investigate. This is a logical OR of the Shutdown and Warning events.

Communication to the DSP or the EEPROM will be possible as long as the input AC voltage is provided. If no AC is present, communication to the unit is possible as long as it is connected to a life V1 output (provided e.g. by the redundant unit).

PARAMETER	DESCRIPTION /CONDITION	MIN	MAX	UNIT
$t_r$	Rise time for SDA and SCL		1000	Ns
$t_{of}$	Output fall time $V_{iHmin} \rightarrow V_{iLmax}$	$10 \text{ pF} < C_b^1 < 400 \text{ pF}$	300	Ns
$I_i$	Input current SCL/SDA	$0.1 \text{ VDD} < V_i < 0.9 \text{ VDD}$	-10	$\mu\text{A}$
$C_i$	Internal Capacitance for each SCL/SDA		50	pF
$f_{SCL}$	SCL clock frequency	0	100	kHz
$R_{pu}$	External pull-up resistor	$f_{SCL} \leq 100 \text{ kHz}$	$1000 \text{ ns} / C_b^1$	$\Omega$
$t_{HDSTA}$	Hold time (repeated) START	$f_{SCL} \leq 100 \text{ kHz}$	4.0	$\mu\text{s}$
$t_{LOW}$	Low period of the SCL clock	$f_{SCL} \leq 100 \text{ kHz}$	4.7	$\mu\text{s}$
$t_{HIGH}$	High period of the SCL clock	$f_{SCL} \leq 100 \text{ kHz}$	4.0	$\mu\text{s}$
$t_{SUSTA}$	Setup time for a repeated START	$f_{SCL} \leq 100 \text{ kHz}$	4.7	$\mu\text{s}$
$t_{HDDAT}$	Data hold time	$f_{SCL} \leq 100 \text{ kHz}$	0	$\mu\text{s}$
$t_{SUDAT}$	Data setup time	$f_{SCL} \leq 100 \text{ kHz}$	250	ns
$t_{SUSTO}$	Setup time for STOP condition	$f_{SCL} \leq 100 \text{ kHz}$	4.0	$\mu\text{s}$
$t_{BUF}$	Bus free time between STOP and START	$f_{SCL} \leq 100 \text{ kHz}$	5	mS

Table 3 - I<sup>2</sup>C / SMBus Specification

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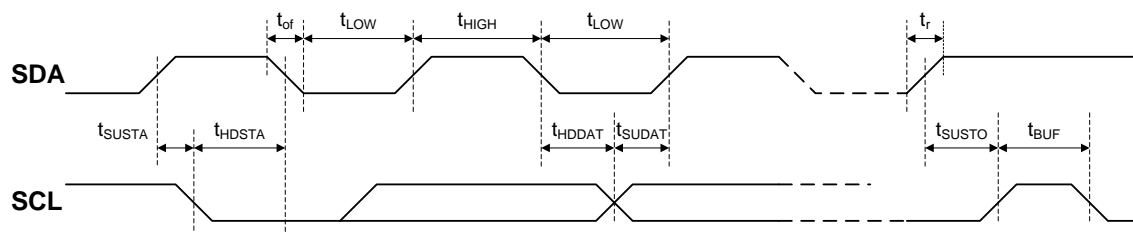


Figure 9 - I<sup>2</sup>C / SMBus Timing

## 8.12. Address Selection

A1	A0	EEPROM Address	Unit Address
0	0	0xA0	0xB0
0	1	0xA2	0xB2
1	0	0xA4	0xB4
1	1	0xA6	0xB6

## 8.13. Controller and EEPROM Access

The controller and the EEPROM in the power supply share the same I2C bus physical layer (see Figure 10). An I2C driver device assures logic level shifting (3.3/5 V) and a glitch-free clock stretching. The driver also pulls the SDA/SCL line to nearly 0 V when driven low by the DSP or the EEPROM providing maximum flexibility when additional external bus repeaters are needed. Such repeaters usually encode the low state with different voltage levels depending on the transmission direction.

The DSP will automatically set the I2C address of the EEPROM with the necessary offset when its own address is changed / set. In order to write to the EEPROM, first the write protection needs to be disabled by sending the appropriate command to the DSP. By default the write protection is on.

The EEPROM provides 2K bytes of user memory. None of the bytes are used for the operation of the power supply.

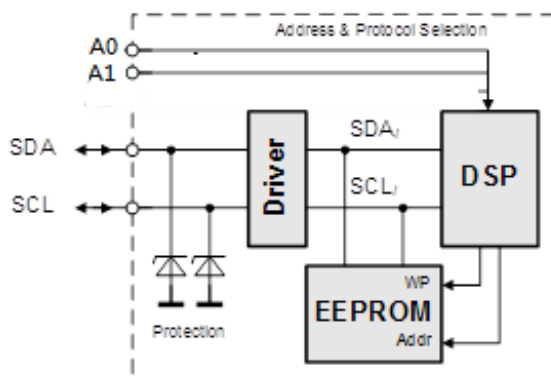


Figure 10 - I2C Bus to DSP and EEPROM

## 8.14. EEPROM Protocol

The EEPROM behaviour the same as the 24C02 series 8 bit address protocol. Even though page write / read commands are defined, it is recommended to use the single byte write / read commands.

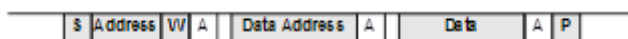
### WRITE

The write command follows the SMBus 1.1 Write Byte protocol. After the device address with the write bit cleared a first byte with the data address to write to is sent followed by the data byte and the STOP condition. A new START condition on the bus should only occur after 5ms of the last STOP condition to allow the EEPROM to write the data into its memory.

866.513.2839

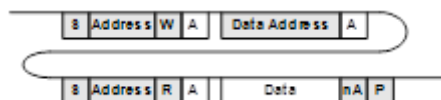
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## READ

The read command follows the SMBus 1.1 Read Byte protocol. After the device address with the write bit cleared the data address byte is sent followed by a repeated start, the device address and the read bit set. The EEPROM will respond with the data byte at the specified location.



## 8.15. PMBus™ PROTOCOL

The Power Management Bus (PMBus™) is an open standard protocol that defines means of communicating with power conversion and other devices. For more information, please see the System Management Interface Forum web site at: [www.powerSIG.org](http://www.powerSIG.org).

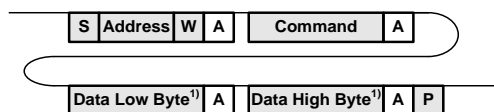
PMBus™ command codes are not register addresses. They describe a specific command to be executed.

The PET800-12-074 supply supports the following basic command structures:

- Clock stretching limited to 1 mS
- SCL low time-out of > 25 mS with recovery within 10 mS
- Recognized any time Start/Stop bus conditions

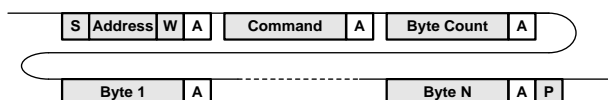
## Write

The write protocol is the SMBus 1.1 Write Byte/Word protocol. Note that the write protocol may end after the command byte or after the first data byte (Byte command) or then after sending 2 data bytes (Word command).



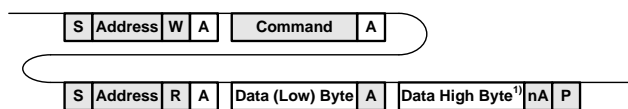
<sup>1)</sup> Optional

In addition, Block write commands are supported with a total maximum length of 255 bytes. See PET800-12-074 Programming Manual for further information.



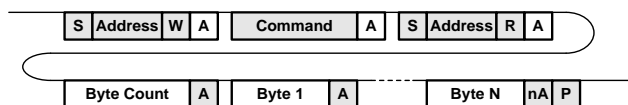
## Read

The read protocol is the SMBus 1.1 Read Byte/Word protocol. Note that the read protocol may request a single byte or word.



<sup>1)</sup> Optional

In addition, Block read commands are supported with a total maximum length of 255 bytes. See PET800-12-074 Programming Manual for further information.



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## 8.16. Graphical User Interface

Bel Power Solutions provide with its "Bel power solutions I2C" a Windows® XP/Vista/Win7 compatible graphical user interface allowing the programming and monitoring of the PET800-12-074 Front-End. The utility can be downloaded on: [www.belpowersolutions.com](http://www.belpowersolutions.com) and supports both the PSML and PMBus™ protocols.

The GUI allows automatic discovery of the units connected to the communication bus and will show them in the navigation tree. In the monitoring view the power supply can be controlled and monitored.

If the GUI is used in conjunction with the PET800-12-074 Evaluation Kit it is also possible to control the PS\_ON pin(s) of the power supply.

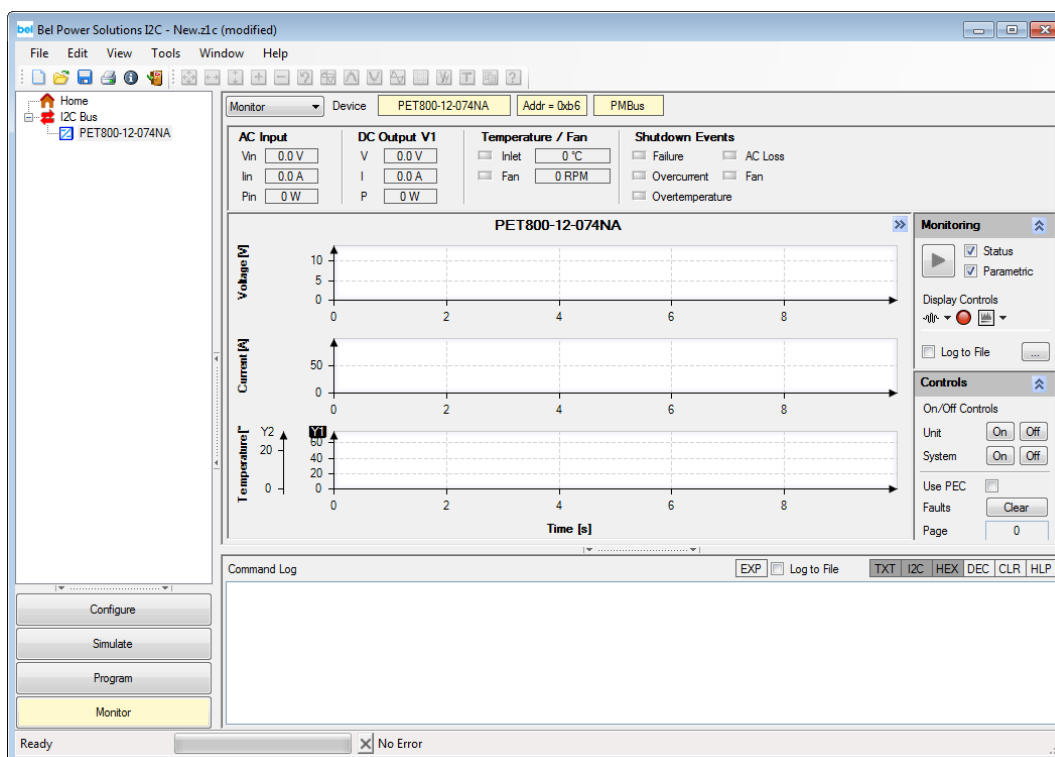


Figure 11 - Monitoring dialog of the I2C Utility

## 9. TEMPERATURE AND FAN CONTROL

To achieve best cooling results sufficient airflow through the supply must be ensured. Do not block or obstruct the airflow at the rear of the supply by placing large objects directly at the output connector. The PET800-12-074 is provided with a normal airflow, which means the air enters through the DC-output of the supply and leaves at the AC-inlet. The fan inside of the supply is controlled by a microprocessor. The RPM of the fan is adjusted to ensure optimal supply cooling and is a function of output power and the inlet temperature.

For the normal airflow version additional constraints apply because of the AC-connector. In a normal airflow unit, the hot air is exiting the power supply unit at the AC-inlet.

The IEC connector on the unit is rated 100 °C. . If 70 °C mating connector is used then end user must derate the input power to meet a maximum 70 °C temperature at the front, the rated output power should be 740W if input voltage less than 100VAC for PET800-12-074NA. don't need derate for PET800-12-074RA.

**NOTE:** It is the responsibility of the user to check the front temperature in such case. The unit will not limit its power automatically to meet such a temperature limitation.

# PET800-12-074xA

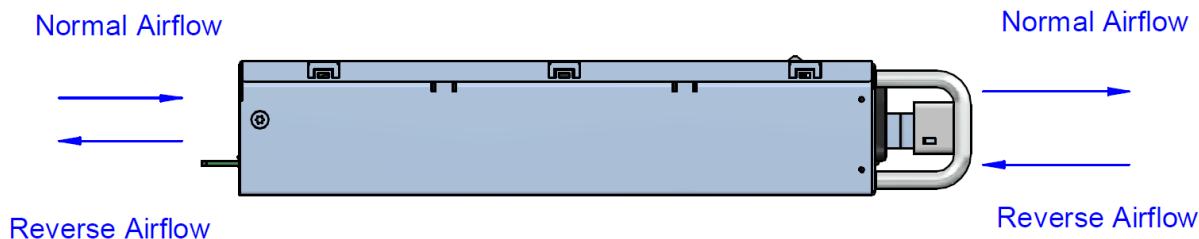


Figure 12 - Airflow direction

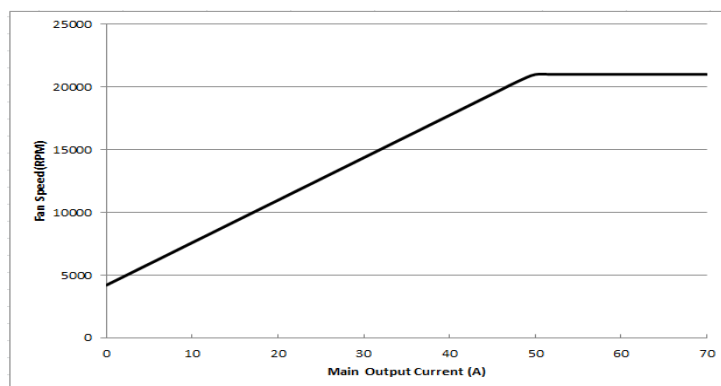


Figure 13 - Fan speed vs. main output load

## 10. ELECTROMAGNETIC COMPATIBILITY

PARAMETER	DESCRIPTION / CONDITION	CRITERION	
Electromagnetic Interference	FCC / ICES-003 Emission (USA/Canada) Verification, CRISP 22 – Emission (International) , EN55022 – Emission (Europe), EN55024 – Immunity (Europe)	Class B	
Harmonics	IEC61000-3-2	A	
Flicker	IEC61000-3-3		
ESD Susceptibility	EN61000-4-2 Electrostatic Discharge: ± 8 KV contact discharge, ±15 KV Air discharge.	B	
Radiated Susceptibility	EN61000-4-3 Radiated RFI Immunity: 10 V/m	A	
EFT/Burst	EN61000-4-4 Electrical Fast Transients: Level 3	B	
Surge Voltage	EN61000-4-5 Electrical Surge: CM: 2 KV, DM: 1 KV	B	
Conducted Susceptibility	EN61000-4-6 RF Conducted: 10 V RMS	A	
Power Frequency Magnetic Field Immunity	EN61000-4-8, 30 A/m	A	
Voltage Dips and Interruptions		30%(Voltage Dips), 10 mS	B
	EN61000-4-11	60%(Voltage Dips), 100 mS	C
		>95%(Voltage Dips), 500 mS	C
Leakage Current	EN60950-1. 3.5 mA@264 VAC/60 Hz		



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## 11. SAFETY / APPROVALS

Maximum electric strength testing is performed in the factory according to IEC/EN 60950, and UL 60950. Input-to-output electric strength tests should not be repeated in the field. Bel Power Solutions will not honor any warranty claims resulting from electric strength field tests.

PARAMETER	DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
Agency Approvals	Approved to the latest revision/amendment of the following standards: • IEC60950-1 • EN60950-1 • UL/CSA0950-1 • GB4943.1, GB9254;GB17625.1 • CNS14336-1, CNS13438	Approved by independent body (see CE Declaration)			
CMTBF	The power supply shall have a minimum MTBF at continuous operation of 200,000 hours calculated at 100%, according to BELL CORE TR-322 at 25 °C excluding the Fan MTBF, and at least 100,000 hours including the fan MTBF.				
Isolation	Input to case (PE) Input (L/N) to output		Basic Reinforced		
$d_c$ Creepage / Clearance	Primary to protective earth (PE) Primary to secondary		3.0 minimum 6.0 minimum		mm
Electrical Strength Test	Input to case	2121			VDC
	Input to output	4242			VDC

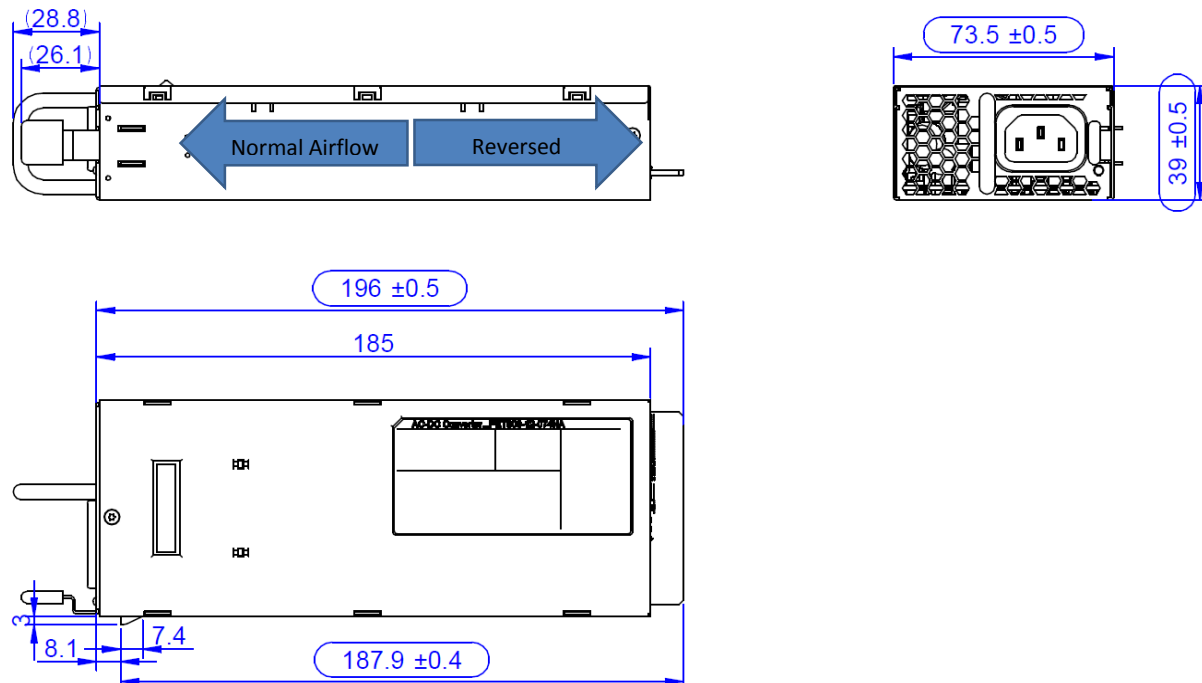
## 12. ENVIRONMENTAL

PARAMETER	DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
Temperature	Operating ambient temperature, normal mode (inlet air): Ta min to Ta max	0		+50	°C
	Operating, T <sub>OP</sub> , standby mode	-5		+50	°C
	Non-operating Ambient_ for NA model	-40		70	°C
	Non-operating Ambient_ for RA model	-40		60	°C
Humidity	Operating (Non-condensing)	10		85	%
	Non-operating (Non-condensing)	5		95	%
Altitude	Operating, above Sea Level	0		5000	M
	Non-operating, above Sea Level	0		15000	M
Mechanical Shock	A) Operation: 10 G, no malfunction B) Non-Operation: 50 G Trapezoidal Wave, Velocity change = 4.3 m/sec. Three drops in each of six directions are applied to each of the samples.				
Vibration	A) Operation: 0.01 g <sub>2</sub> /Hz at 10Hz, 0.02 g <sub>2</sub> /Hz at 20 Hz. B) Non-Operation: - <b>Sine sweep</b> : 5 Hz to 500 Hz @ 0.5 g <sub>RMS</sub> at 0.5 octave/min dwell 15min at each of 3 resonant points; - <b>Random profile</b> : 5 Hz @ 0.01 g <sub>2</sub> /Hz to 20 Hz @ 0.02g <sub>2</sub> (slope up); 20 Hz to 500Hz @ 0.02g <sub>2</sub> /Hz (flat); Input acceleration = 3.13 g <sub>RMS</sub> ; 10 min. per axis for 3 axis on all samples				
Acoustic Noise	1 meter, 25 °C, 50% load		46		dBA

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## 13. MECHANICAL

PARAMETER	DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
Dimensions	Width		73.5		mm
	Height		39		
	Depth		185		
Weight			798		g



**NOTE:** A 3D step file of the power supply casing is available on request.

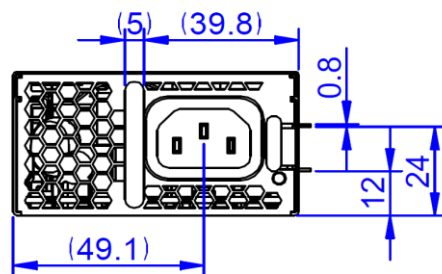


Figure 15 – Front View

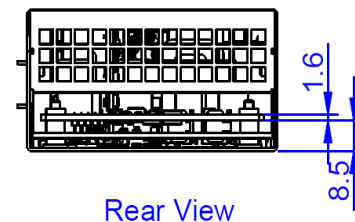


Figure 16 - Rear View

# PET800-12-074xA

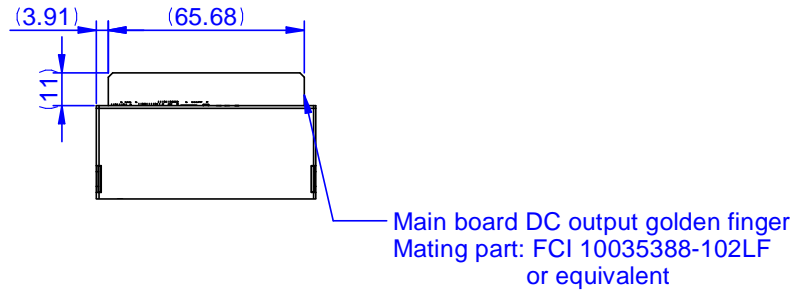


Figure 17 - Mating Connector

## 14. CONNECTIONS

The AC input receptacle shall be a 3 pins IEC320 C14 inlet. This inlet shall be rated for operation at 15A/250 VAC. For the pin assignment of DC connector, please refer to Figure 18 and Table 4.

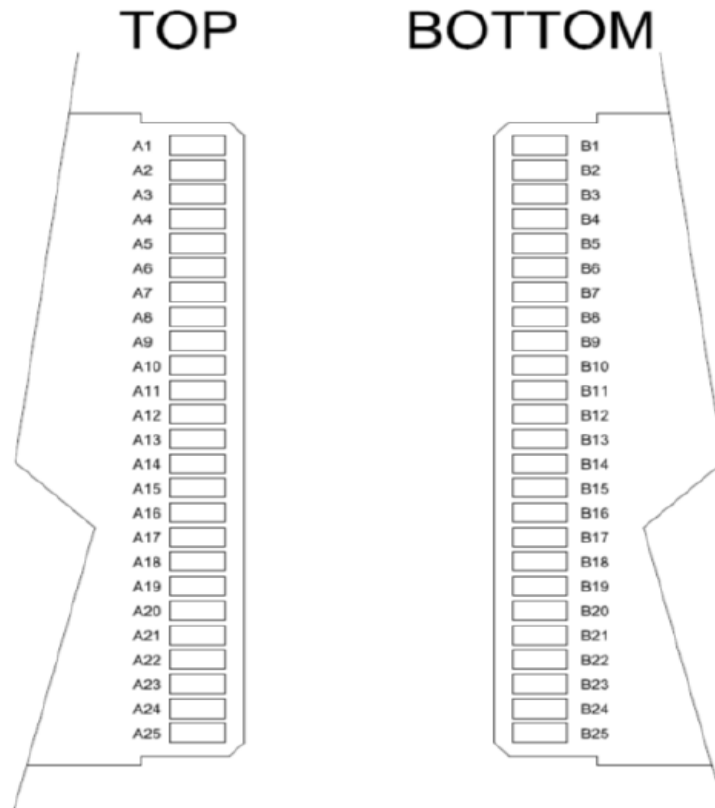


Figure 18 - Pin Assignment of DC Connector

# PET800-12-074xA

PIN	SIGNAL NAME	DESCRIPTION
A1 ~ A9	VS_R	+12 V return
B1 ~ B9	VS_R	+12 V return
A10 ~ A18	VS	+12 V power output
B10 ~ B18	VS	+12V power output
A19	SDA	I <sup>2</sup> C Data signal
A20	SCL	I <sup>2</sup> C Clock signal
A21	PS_ON	Module PS_ON Remote control power On/Off (Pulled LOW=POWER ON)
A22	SMB_ALERT	SMB Alert signal output: active-low
A23	VS_SENSE_R	+12 V Remote sense return
A24	VS_SENSE	+12 V Remote sense
A25	PWOK	Power Good Output. Signal is pulled HIGH to indicate all outputs ok.
B19	A0	I <sup>2</sup> C address bit 0
B20	A1	I <sup>2</sup> C address bit 1
B21	12 VSB	+12 V Standby Output
B22	PDB_FAULT	To receive a FAULT signal from system or PSU backplane. PSU shall shutdown if this pin is pulled HIGH.
B23	ISHARE	+12 V Main output Current share bus
B24	PDB_ALERT	To receive ALERT signal from system or PSU backplane, If signal is pulled LOW, the PSU internal fan shall be forced to run at maximum speed to improve thermal performance.
B25	VSS	Not used

Table 4 Output Pin Assignment

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## 15. ACCESSORIES

ITEM	DESCRIPTION	ORDERING PART NUMBER	SOURCE
	<b>BPS I²C Utility</b> Windows XP/Vista/7 compatible GUI to program, control and monitor PET Front-Ends (and other I²C units)	Download	<a href="http://www.belpowersolutions.com">www.belpowersolutions.com</a>
	<b>USB to I²C</b>		
	<b>Loading Board</b>		
	<b>Dual Connector Board</b> Connector board to operate 2 PET units in parallel. Includes an on-board USB to I²C converter (use I²C Utility as desktop software).	VRA.00334.0	Bel Power Solutions
	<b>Cable</b>		

For more information on these products consult: [tech.support@psbel.com](mailto:tech.support@psbel.com)

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**TECHNICAL REVISIONS** - The appearance of products, including safety agency certifications pictured on labels, may change depending on the date manufactured. Specifications are subject to change without notice.

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