

## Product Summary

$V_{(BR)DSS}$	$R_{DS(on)}$	$I_D$ $T_A = +25^\circ\text{C}$
-50V	$6\Omega @ V_{GS} = -4\text{V}$	-200mA
	$8\Omega @ V_{GS} = -2.5\text{V}$	-160mA

## Description

This new generation MOSFET is designed to minimize the on-state resistance ( $R_{DS(on)}$ ) and yet maintain superior switching performance, making it ideal for high efficiency power management applications.

## Applications

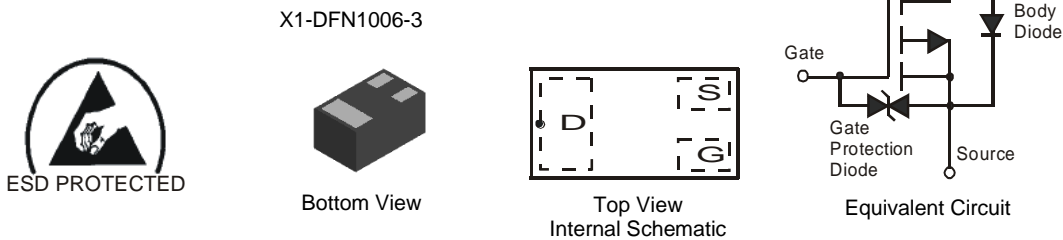
- DC-DC Converters
- Power Management Functions
- Battery Operated Systems and Solid-State Relays

## Features and Benefits

- Low On-Resistance
- ESD Protected Gate
- Low Input/Output Leakage
- Fast Switching Speed
- **Lead-Free Finish; RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **Qualified to AEC-Q101 Standards for High Reliability**

## Mechanical Data

- Case: X1-DFN1006-3
- Case Material: Molded Plastic, "Green" Molding Compound; UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish — NiPdAu over Copper Leadframe; Solderable per MIL-STD-202, Method 208 (e4)
- Terminal Connections: See Diagram
- Weight: 0.001 grams (Approximate)

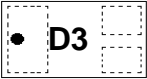
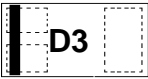
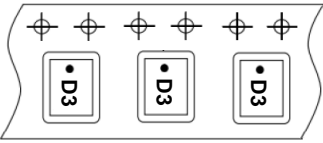
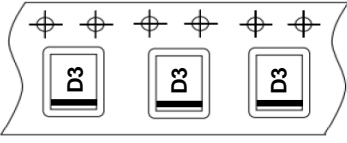
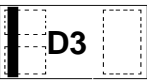
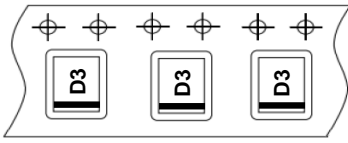


## Ordering Information (Note 4)

Part Number	Case	Packaging
DMP56D0UFB-7	X1-DFN1006-3	3,000/Tape & Reel
DMP56D0UFB-7B	X1-DFN1006-3	10,000/Tape & Reel

- Notes:
1. EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant. All applicable RoHS exemptions applied.
  2. See [http://www.diodes.com/quality/lead\\_free.html](http://www.diodes.com/quality/lead_free.html) for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
  3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
  4. For packaging details, go to our website at <http://www.diodes.com/products/packages.html>

## Marking Information

<p><b>DMP56D0UFB-7</b></p>	<div style="display: flex; justify-content: space-around;"> <div style="text-align: center;">  <p>Top View Dot Denotes Drain Side</p> </div> <div style="text-align: center;"> <p>From date code 1527 (YYWW), this changes to:</p>  <p>Top View Bar Denotes Gate and Source Side</p> </div> </div> <div style="display: flex; justify-content: space-around; margin-top: 20px;">   </div>
<p><b>DMP56D0UFB-7B</b></p>	<div style="text-align: center;">  <p>Top View Bar Denotes Gate and Source Side</p> </div> <div style="text-align: center; margin-top: 20px;">  </div> <p style="text-align: right; margin-top: 20px;">D3 = Part Marking Code</p>

## Maximum Ratings (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Units
Drain-Source Voltage	V <sub>DSS</sub>	-50	V
Gate-Source Voltage	V <sub>GSS</sub>	±8	V
Drain Current (Note 5)      Steady      T <sub>A</sub> = +25°C	I <sub>D</sub>	-200	mA
Pulsed Drain Current (Note 6)	I <sub>DM</sub>	-700	mA

## Thermal Characteristics

Characteristic	Symbol	Value	Units
Total Power Dissipation (Note 5)	P <sub>D</sub>	425	mW
Thermal Resistance, Junction to Ambient @T <sub>A</sub> = +25°C (Note 5)	R <sub>θJA</sub>	275	°C/W
Operating and Storage Temperature Range	T <sub>J</sub> , T <sub>STG</sub>	-55 to +150	°C

Notes:      5. Device mounted on FR-4 PCB. t ≤ 5 sec.  
              6. Pulse width ≤ 10μS, Duty Cycle ≤ 1%.

**Electrical Characteristics** (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
<b>OFF CHARACTERISTICS (Note 7)</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	-50	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = -250μA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	—	—	-10	μA	V <sub>DS</sub> = -50V, V <sub>GS</sub> = 0V
Gate-Source Leakage	I <sub>GSS</sub>	—	—	±1	μA	V <sub>GS</sub> = ±8V, V <sub>DS</sub> = 0V
<b>ON CHARACTERISTICS (Note 7)</b>						
Gate Threshold Voltage	V <sub>GS(th)</sub>	-0.5	—	-1.2	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -250μA
Static Drain-Source On-Resistance	R <sub>DS(on)</sub>	—	4.6 6	6 8	Ω	V <sub>GS</sub> = -4.0V, I <sub>D</sub> = -100mA V <sub>GS</sub> = -2.5V, I <sub>D</sub> = -80mA
Forward Transfer Admittance	Y <sub>fs</sub>	100	—	—	mS	V <sub>DS</sub> = -5V, I <sub>D</sub> = -100mA
Diode Forward Voltage (Note 7)	V <sub>SD</sub>	—	—	-1.2	V	V <sub>GS</sub> = 0V, I <sub>S</sub> = -100mA
<b>DYNAMIC CHARACTERISTICS (Note 8)</b>						
Input Capacitance	C <sub>iSS</sub>	—	50.54	—	pF	V <sub>DS</sub> = -25V, V <sub>GS</sub> = 0V, f = 1.0MHz
Output Capacitance	C <sub>oSS</sub>	—	3.49	—	pF	
Reverse Transfer Capacitance	C <sub>rSS</sub>	—	2.42	—	pF	
Gate Resistance	R <sub>G</sub>	—	201	—	Ω	V <sub>DS</sub> = 0V, V <sub>GS</sub> = 0V, f = 1.0MHz
Total Gate Charge V <sub>GS</sub> = 4.5V	Q <sub>g</sub>	—	0.58	—	nC	V <sub>GS</sub> = -4V, V <sub>DS</sub> = -25V, I <sub>D</sub> = -100mA
Gate-Source Charge	Q <sub>gs</sub>	—	0.09	—	nC	
Gate-Drain Charge	Q <sub>gd</sub>	—	0.14	—	nC	
Turn-On Delay Time	t <sub>D(on)</sub>	—	4.46	—	nS	V <sub>DD</sub> = -30V, I <sub>D</sub> = -0.27A, V <sub>GEN</sub> = -4V, R <sub>GEN</sub> = 6Ω
Turn-On Rise Time	t <sub>r</sub>	—	6.63	—	nS	
Turn-Off Delay Time	t <sub>D(off)</sub>	—	21.9	—	nS	
Turn-Off Fall Time	t <sub>f</sub>	—	15.0	—	nS	

Notes: 7. Short duration pulse test used to minimize self-heating effect.  
8. Guaranteed by design. Not subject to production testing.

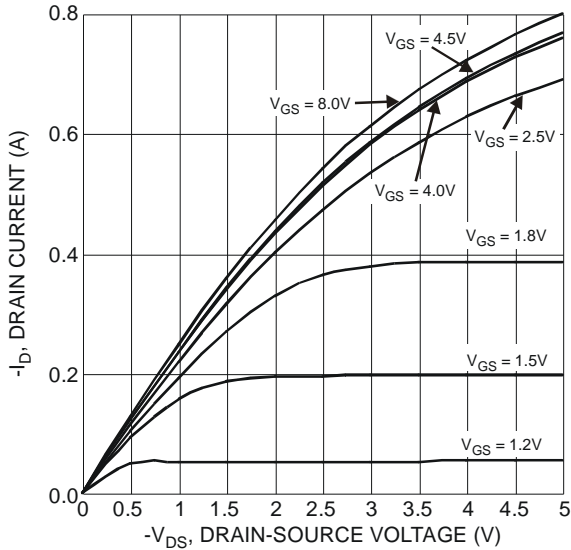


Figure 1 Typical Output Characteristics

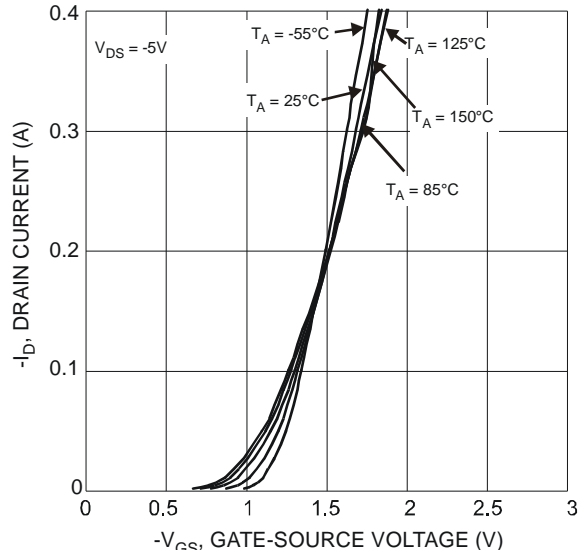


Figure 2 Typical Transfer Characteristics

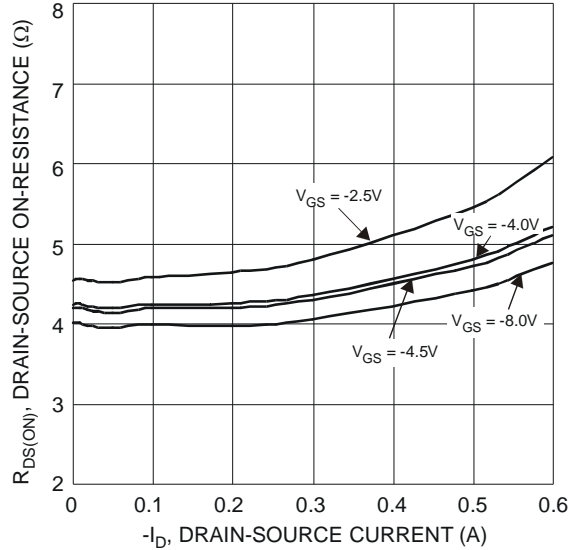


Figure 3 Typical On-Resistance vs. Drain Current and Gate Voltage

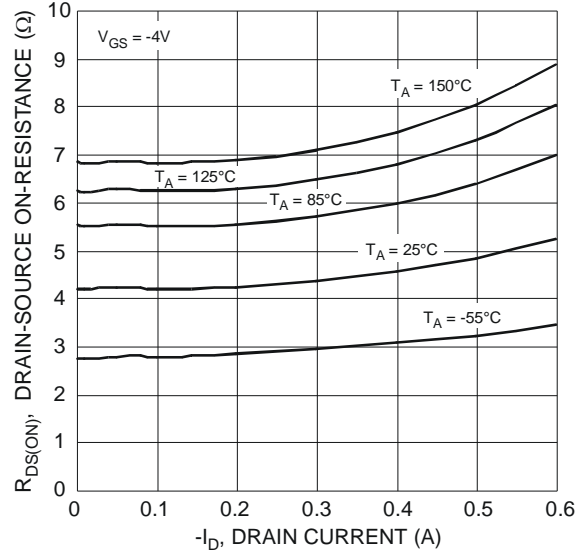


Figure 4 Typical On-Resistance vs. Drain Current and Temperature

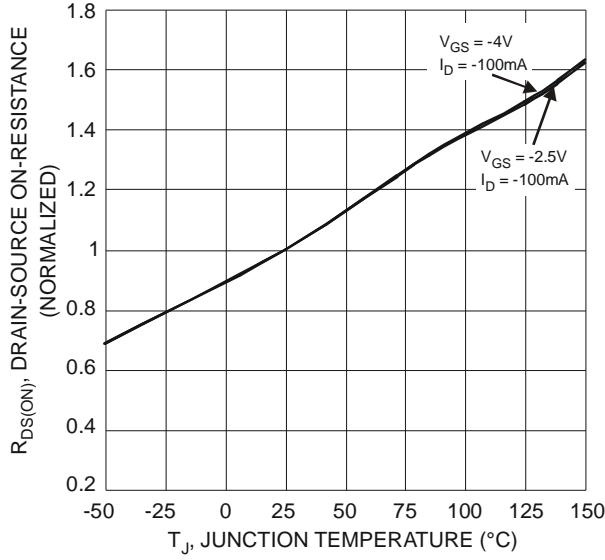


Figure 5 On-Resistance Variation with Temperature

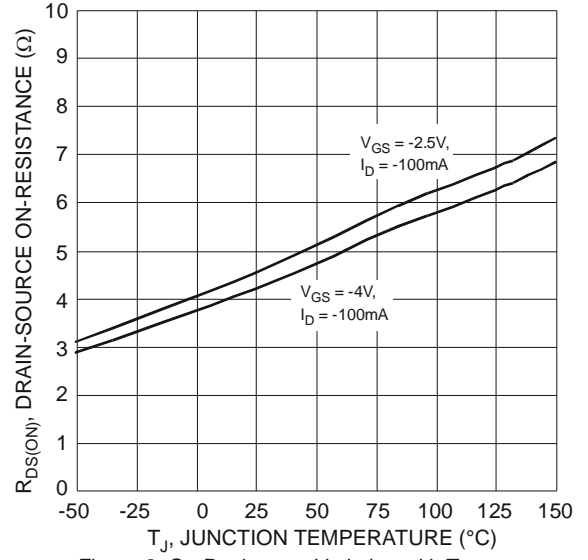


Figure 6 On-Resistance Variation with Temperature

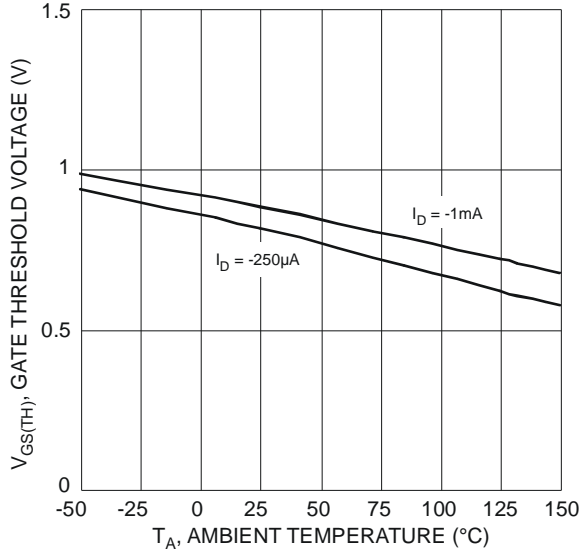


Figure 7 Gate Threshold Variation vs. Ambient Temperature

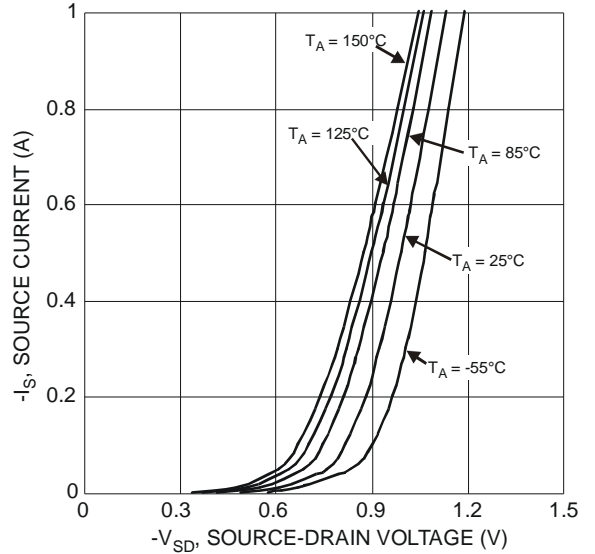


Figure 8 Diode Forward Voltage vs. Current

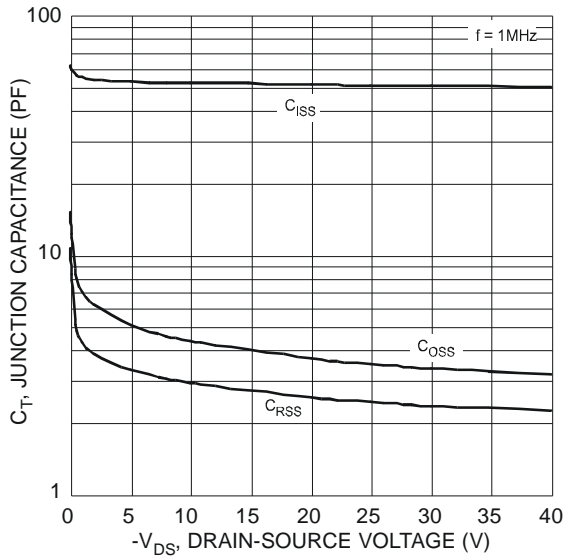


Figure 9 Typical Junction Capacitance

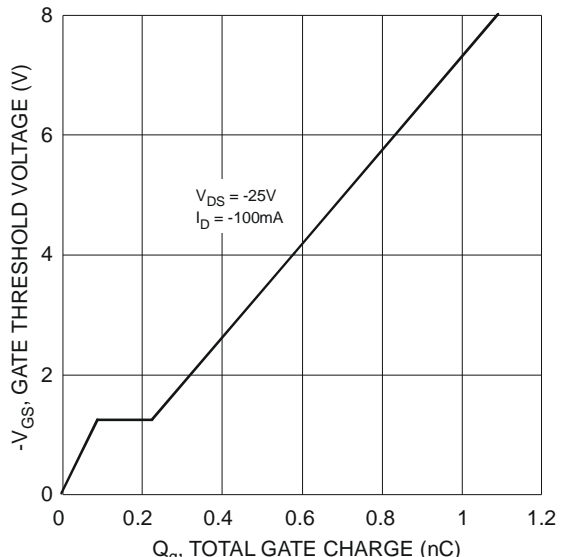


Figure 10 Gate Charge Characteristics



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