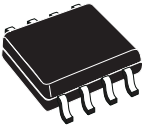




N-channel 30 V, 0.019  $\Omega$ , 10 A, SO-8  
STripFET™ V Power MOSFET

| Type       | V <sub>DSS</sub> | R <sub>DS(on)</sub> max | I <sub>D</sub> |
|------------|------------------|-------------------------|----------------|
| STS10N3LH5 | 30 V             | 0.021 Ω                 | 10 A           |

- 
- SO-8

- Switching applications

This StriP<sup>TM</sup>FET Power MOSFET technology is among the latest improvements, which have been especially tailored to achieve very low on-state resistance providing also one of the best-in-class FOM.

Pin diagram of the SC12830 IC. The IC is shown in a rectangular package with pins numbered 1 through 8. Pins 1, 2, and 3 are labeled 'S' (Source) and pins 4, 5, and 6 are labeled 'D' (Drain). Pins 7 and 8 are labeled 'D' (Drain). A central symbol shows a MOSFET with a circle around the gate, indicating a specific internal structure or connection.

| Order codes | Marking | Package | Packaging     |
|-------------|---------|---------|---------------|
| STS10N3LH5  | 10D3L   | SO-8    | Tape and reel |

Contents

1      **Electrical ratings** ..... 3

2      **Electrical characteristics** ..... 4

      2.1    Electrical characteristics (curves) ..... 6

3      **Test circuits** ..... 8

4      **Package mechanical data** ..... 10

5      **Revision history** ..... 12



# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

| Symbol             | Parameter                                                         | Value       | Unit                  |
|--------------------|-------------------------------------------------------------------|-------------|-----------------------|
| $V_{DS}$           | Drain-source voltage ( $V_{GS} = 0$ )                             | 30          | V                     |
| $V_{GS}$           | Gate-Source voltage                                               | $\pm 22$    | V                     |
| $I_D^{(1)}$        | Drain current (continuous) at $T_C = 25\text{ }^{\circ}\text{C}$  | 10          | A                     |
| $I_D$              | Drain current (continuous) at $T_C = 100\text{ }^{\circ}\text{C}$ | 7           | A                     |
| $I_{DM}^{(2)}$     | Drain current (pulsed)                                            | 40          | A                     |
| $P_{TOT}$          | Total dissipation at $T_C = 25\text{ }^{\circ}\text{C}$           | 2.5         | W                     |
|                    | Derating factor                                                   | 0.02        | W/ $^{\circ}\text{C}$ |
| $E_{AS}^{(3)}$     | Single pulse avalanche energy                                     | 50          | mJ                    |
| $T_J$<br>$T_{stg}$ | Operating junction temperature<br>Storage temperature             | - 55 to 150 | $^{\circ}\text{C}$    |

1. Limited by wire bonding
2. Pulse width limited by safe operating area
3. Starting  $T_J = 25\text{ }^{\circ}\text{C}$ ,  $I_D = 21\text{ A}$ ,  $L = 0.2\text{ mH}$

**Table 3. Thermal resistance**

| Symbol     | Parameter                                      | Value | Unit                 |
|------------|------------------------------------------------|-------|----------------------|
| $R_{thJC}$ | Thermal resistance junction-case max           | 50    | $^{\circ}\text{C/W}$ |
| $R_{thJA}$ | Thermal resistance junction-case max           | 100   | $^{\circ}\text{C/W}$ |
| $T_J$      | Maximum lead temperature for soldering purpose | 275   | $^{\circ}\text{C}$   |

## 2 Electrical characteristics

( $T_{CASE} = 25\text{ }^{\circ}\text{C}$  unless otherwise specified)

**Table 4. Static**

| Symbol        | Parameter                                        | Test conditions                                                                        | Min. | Typ.  | Max.      | Unit                           |
|---------------|--------------------------------------------------|----------------------------------------------------------------------------------------|------|-------|-----------|--------------------------------|
| $V_{(BR)DSS}$ | Drain-source breakdown Voltage                   | $I_D = 250\text{ }\mu\text{A}$ , $V_{GS} = 0$                                          | 30   |       |           | V                              |
| $I_{DSS}$     | Zero gate voltage drain current ( $V_{GS} = 0$ ) | $V_{DS} = 30\text{ V}$<br>$V_{DS} = 30\text{ V}$ , $T_c = 125\text{ }^{\circ}\text{C}$ |      |       | 1<br>10   | $\mu\text{A}$<br>$\mu\text{A}$ |
| $I_{GSS}$     | Gate body leakage current ( $V_{DS} = 0$ )       | $V_{GS} = \pm 22\text{ V}$                                                             |      |       | $\pm 100$ | nA                             |
| $V_{GS(th)}$  | Gate threshold voltage                           | $V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$                                     | 1    |       |           | V                              |
| $R_{DS(on)}$  | Static drain-source on resistance                | $V_{GS} = 10\text{ V}$ , $I_D = 5\text{ A}$                                            |      | 0.019 | 0.021     | $\Omega$                       |
|               |                                                  | $V_{GS} = 4.5\text{ V}$ , $I_D = 5\text{ A}$                                           |      | 0.023 | 0.028     | $\Omega$                       |

**Table 5. Dynamic**

| Symbol    | Parameter                           | Test conditions                                                                               | Min | Typ. | Max. | Unit     |
|-----------|-------------------------------------|-----------------------------------------------------------------------------------------------|-----|------|------|----------|
| $C_{iss}$ | Input capacitance                   | $V_{DS} = 25\text{ V}$ , $f = 1\text{ MHz}$ ,<br>$V_{GS} = 0$                                 | -   | 475  | -    | pF       |
| $C_{oss}$ | Output capacitance                  |                                                                                               |     | 97   |      | pF       |
| $C_{rss}$ | Reverse transfer capacitance        |                                                                                               |     | 19   |      | pF       |
| $Q_g$     | Total gate charge                   | $V_{DD} = 15\text{ V}$ , $I_D = 10\text{ A}$<br>$V_{GS} = 5\text{ V}$<br>( <i>Figure 14</i> ) | -   | 4.6  | -    | nC       |
| $Q_{gs}$  | Gate-source charge                  |                                                                                               |     | 1.7  |      | nC       |
| $Q_{gd}$  | Gate-drain charge                   |                                                                                               |     | 1.9  |      | nC       |
| $Q_{gs1}$ | Pre $V_{th}$ gate-to-source charge  | $V_{DD} = 15\text{ V}$ , $I_D = 10\text{ A}$<br>$V_{GS} = 5\text{ V}$<br>( <i>Figure 19</i> ) | -   | 0.67 | -    | nC       |
| $Q_{gs2}$ | Post $V_{th}$ gate-to-source charge |                                                                                               |     | 0.84 |      | nC       |
| $R_G$     | Gate input resistance               | $f = 1\text{ MHz}$ gate bias<br>Bias = 0 test signal level = 20 mV<br>open drain              | -   | 2.5  | -    | $\Omega$ |

**Table 6. Switching on/off (resistive load)**

| Symbol                | Parameter                        | Test conditions                                                                                                            | Min. | Typ.      | Max. | Unit     |
|-----------------------|----------------------------------|----------------------------------------------------------------------------------------------------------------------------|------|-----------|------|----------|
| $t_{d(on)}$<br>$t_r$  | Turn-on delay time<br>Rise time  | $V_{DD} = 15\text{ V}$ , $I_D = 5\text{ A}$ ,<br>$R_G = 4.7\ \Omega$ , $V_{GS} = 10\text{ V}$<br>(Figure 13 and Figure 18) | -    | 4<br>22   | -    | ns<br>ns |
| $t_{d(off)}$<br>$t_f$ | Turn-off delay time<br>Fall time | $V_{DD} = 15\text{ V}$ , $I_D = 5\text{ A}$ ,<br>$R_G = 4.7\ \Omega$ , $V_{GS} = 10\text{ V}$<br>(Figure 13 and Figure 18) | -    | 13<br>2.8 | -    | ns<br>ns |

**Table 7. Source drain diode**

| Symbol                            | Parameter                                                                    | Test conditions                                                                                        | Min. | Typ.             | Max.     | Unit          |
|-----------------------------------|------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------|------|------------------|----------|---------------|
| $I_{SD}$<br>$I_{SDM}^{(1)}$       | Source-drain current<br>Source-drain current (pulsed)                        |                                                                                                        | -    |                  | 10<br>40 | A<br>A        |
| $V_{SD}$                          | Forward on voltage                                                           | $I_{SD} = 5\text{ A}$ , $V_{GS} = 0$                                                                   | -    |                  | 1.1      | V             |
| $t_{rr}$<br>$Q_{rr}$<br>$I_{RRM}$ | Reverse recovery time<br>Reverse recovery charge<br>Reverse recovery current | $I_{SD} = 10\text{ A}$ , $V_{DD} = 25\text{ V}$<br>$di/dt = 100\text{ A}/\mu\text{s}$ ,<br>(Figure 15) | -    | 16.2<br>7.8<br>1 |          | ns<br>nC<br>A |

1. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5 %

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

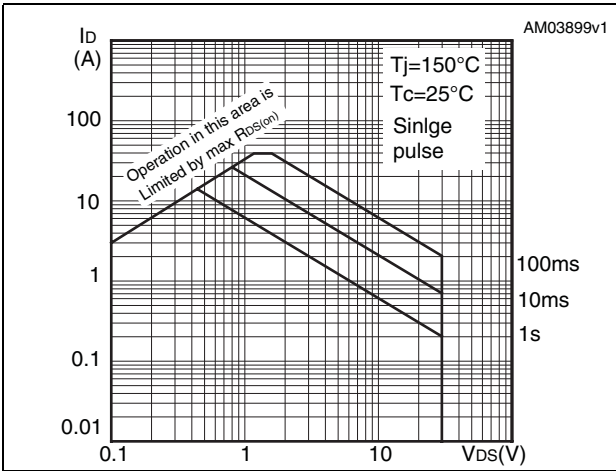


Figure 3. Thermal impedance

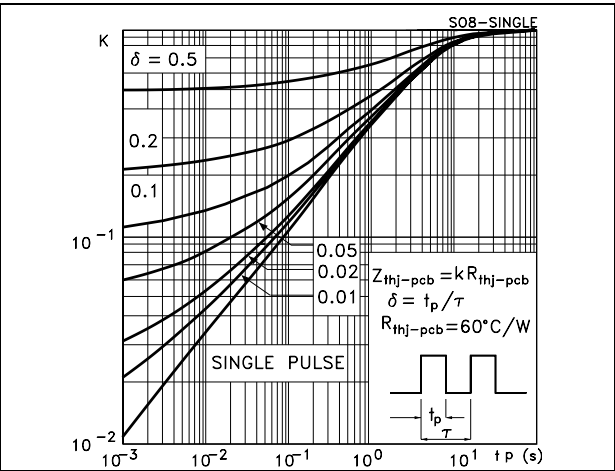


Figure 4. Output characteristics

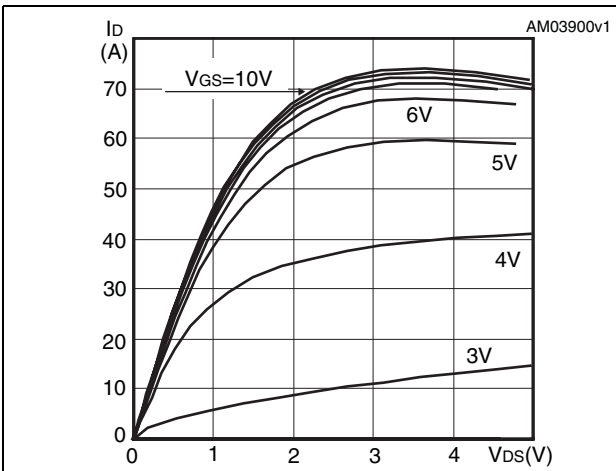


Figure 5. Transfer characteristics

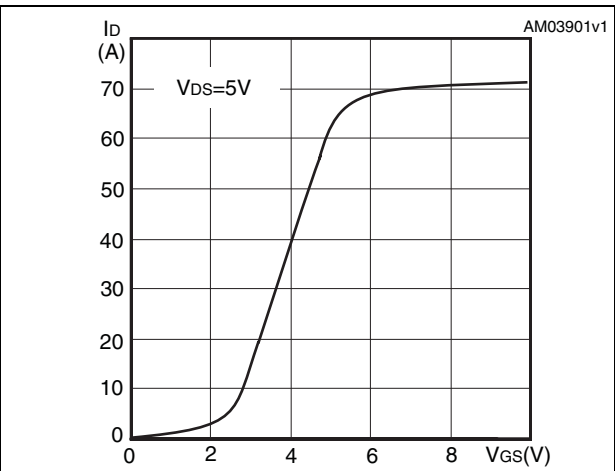


Figure 6. Normalized  $BV_{DSS}$  vs temperature

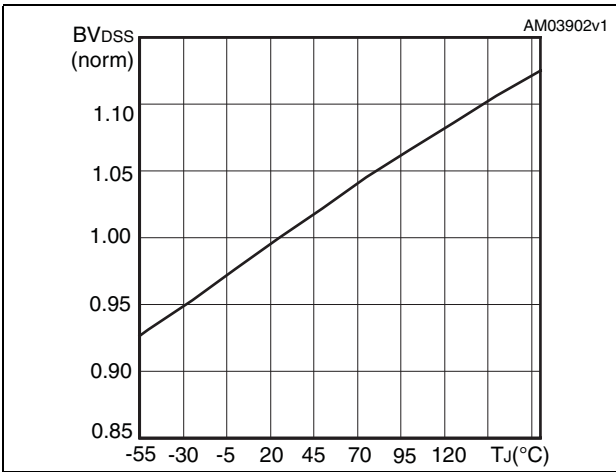


Figure 7. Static drain-source on resistance

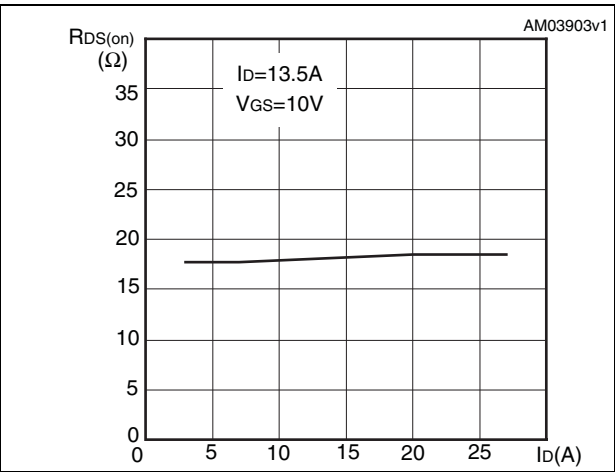


Figure 8. Gate charge vs gate-source voltage Figure 9. Capacitance variations

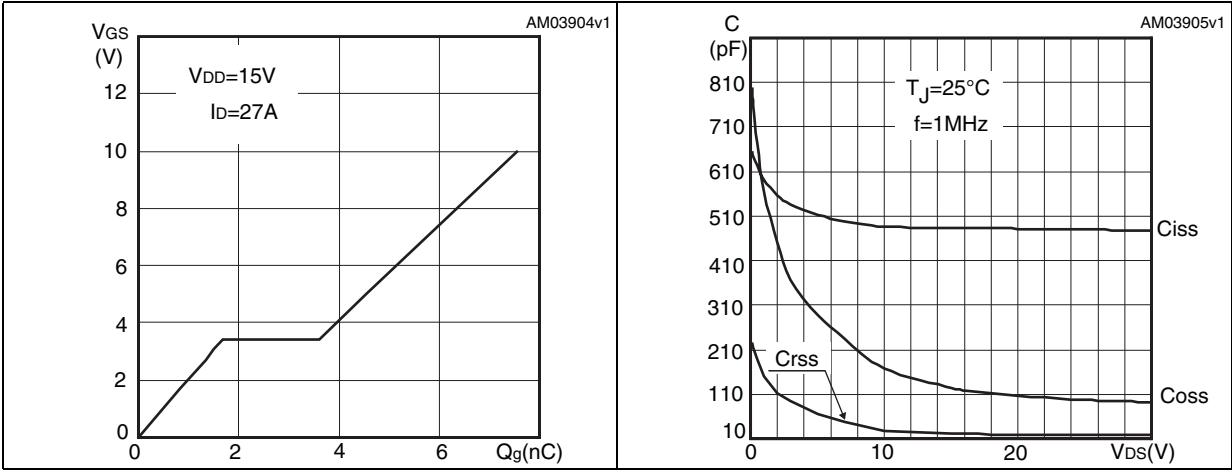


Figure 10. Normalized gate threshold voltage vs temperature Figure 11. Normalized on resistance vs temperature

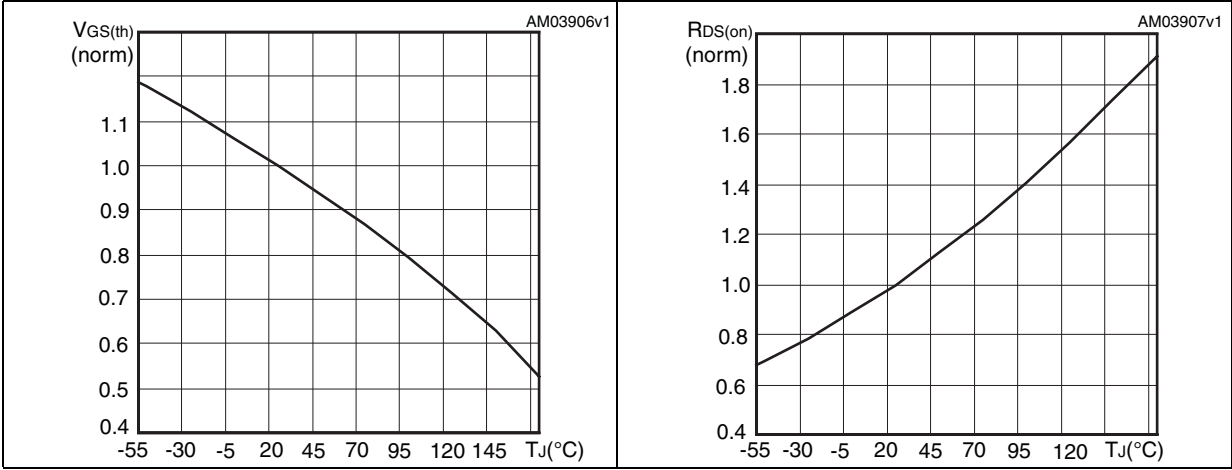
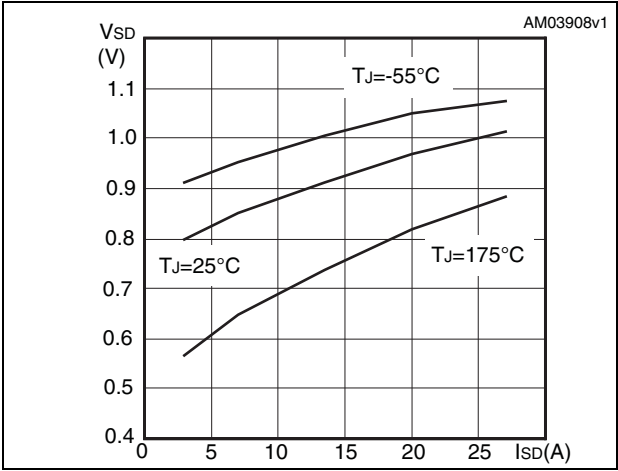
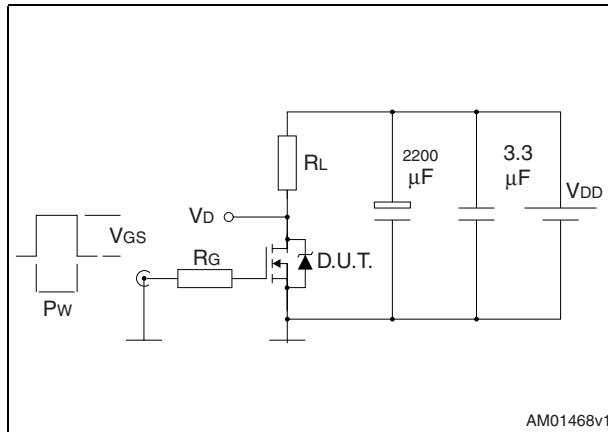


Figure 12. Source-drain diode forward characteristics

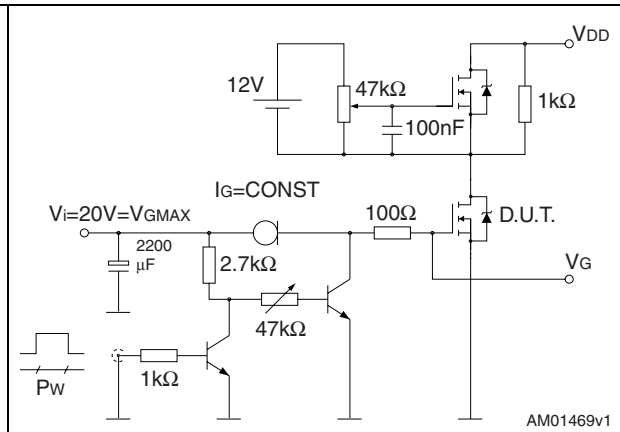


### 3 Test circuits

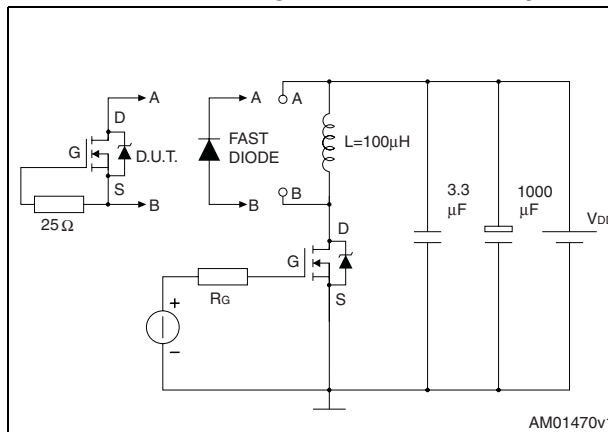
**Figure 13. Switching times test circuit for resistive load**



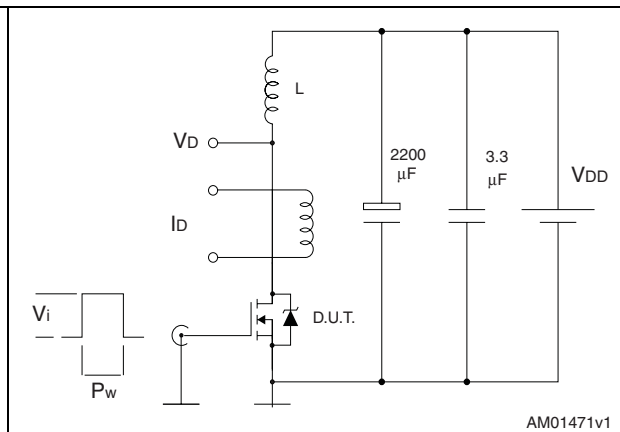
**Figure 14. Gate charge test circuit**



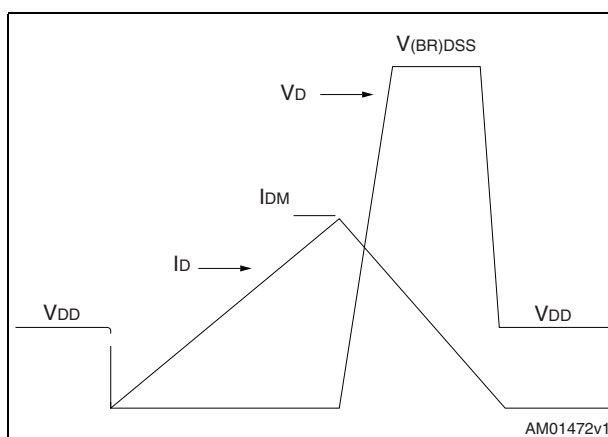
**Figure 15. Test circuit for inductive load switching and diode recovery times**



**Figure 16. Unclamped inductive load test circuit**



**Figure 17. Unclamped inductive waveform**



**Figure 18. Switching time waveform**

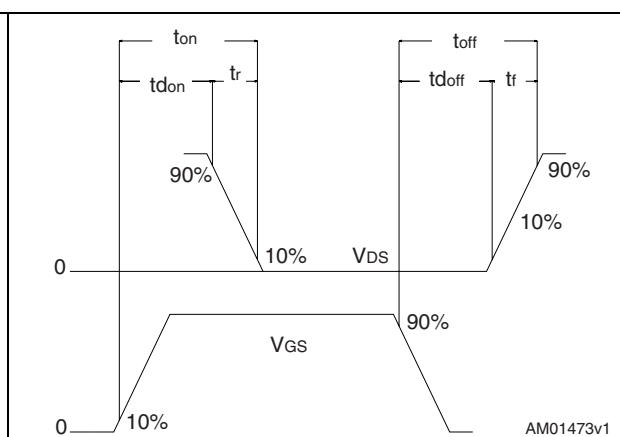
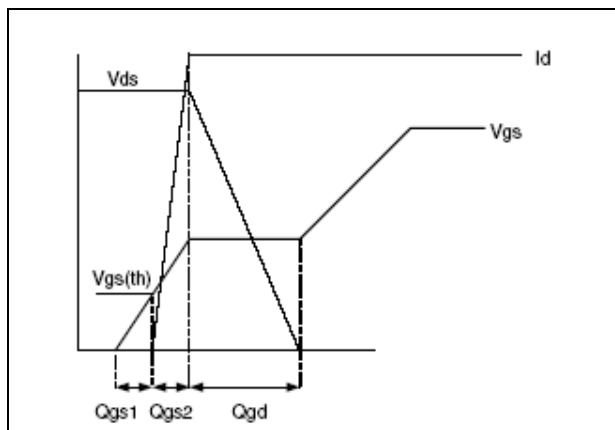




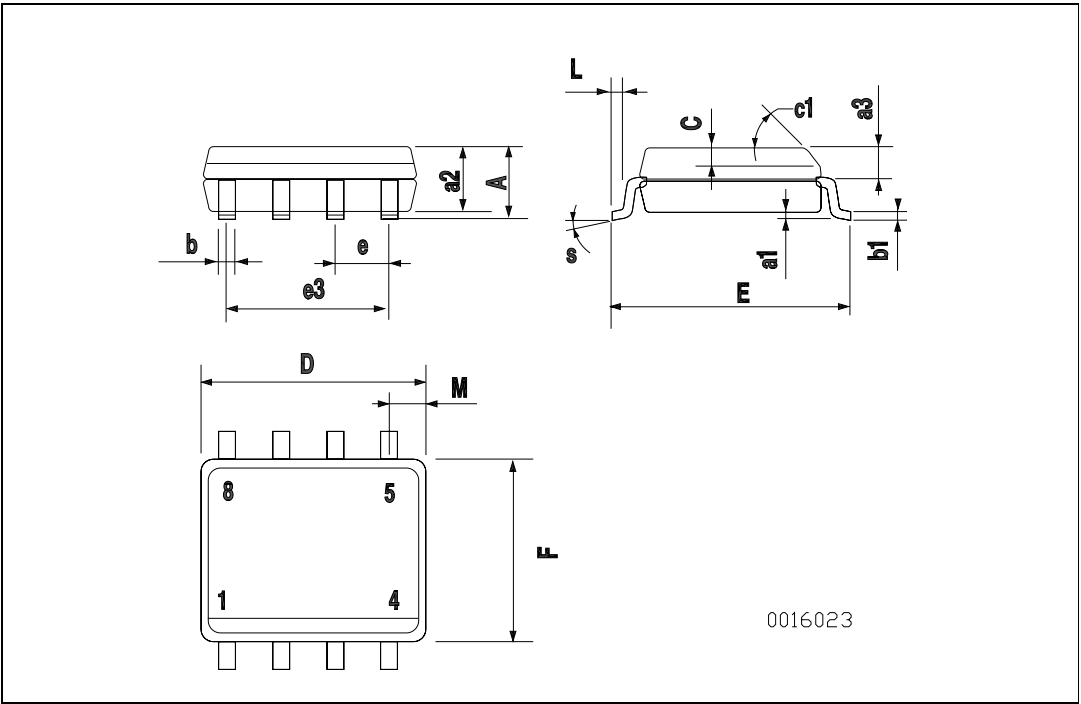
Figure 19. Gate charge waveform



## 4 Package mechanical data

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| SO-8 MECHANICAL DATA |           |      |      |       |       |       |
|----------------------|-----------|------|------|-------|-------|-------|
| DIM.                 | mm.       |      |      | inch  |       |       |
|                      | MIN.      | TYP  | MAX. | MIN.  | TYP.  | MAX.  |
| A                    |           |      | 1.75 |       |       | 0.068 |
| a1                   | 0.1       |      | 0.25 | 0.003 |       | 0.009 |
| a2                   |           |      | 1.65 |       |       | 0.064 |
| a3                   | 0.65      |      | 0.85 | 0.025 |       | 0.033 |
| b                    | 0.35      |      | 0.48 | 0.013 |       | 0.018 |
| b1                   | 0.19      |      | 0.25 | 0.007 |       | 0.010 |
| C                    | 0.25      |      | 0.5  | 0.010 |       | 0.019 |
| c1                   | 45 (typ.) |      |      |       |       |       |
| D                    | 4.8       |      | 5.0  | 0.188 |       | 0.196 |
| E                    | 5.8       |      | 6.2  | 0.228 |       | 0.244 |
| e                    |           | 1.27 |      |       | 0.050 |       |
| e3                   |           | 3.81 |      |       | 0.150 |       |
| F                    | 3.8       |      | 4.0  | 0.14  |       | 0.157 |
| L                    | 0.4       |      | 1.27 | 0.015 |       | 0.050 |
| M                    |           |      | 0.6  |       |       | 0.023 |
| S                    | 8 (max.)  |      |      |       |       |       |



## 5 Revision history

**Table 8. Document revision history**

| Date        | Revision | Changes       |
|-------------|----------|---------------|
| 06-May-2009 | 1        | First release |

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