ATmega8A

Low-Power AVR 8-bit Microcontroller Data Sheet Summary

Introduction

The ATmega8A is a low-power CMOS 8-bit microcontroller based on the AVR® enhanced RISC architecture. By executing powerful instructions in a single clock cycle, the ATmega8A achieves throughputs close to 1 MIPS per MHz. This empowers system designers to optimize the device for power consumption versus processing speed.

Features

- High-performance, Low-power AVR 8-bit Microcontroller
- Advanced RISC Architecture
  - 130 powerful instructions - most single-clock cycle execution
  - 32 x 8 general purpose working registers
  - Fully static operation
  - Up to 16 MIPS throughput at 16 MHz
  - On-chip 2-cycle multiplier
- High Endurance Nonvolatile Memory segments
  - 8 KB of In-System Self-programmable Flash program memory
  - 512B EEPROM
  - 1 KB internal SRAM
  - Write/erase cycles: 10,000 Flash/100,000 EEPROM
  - Data retention: 20 years at 85°C/100 years at 25°C(1)
  - Optional boot code section with independent lock bits
    - In-system programming by on-chip boot program
    - True read-while-write operation
  - Programming lock for software security
- Microchip QTouch® library support
  - Capacitive touch buttons, sliders and wheels
  - QTouch and QMatrix acquisition
  - Up to 64 sense channels
- Peripheral Features
  - Two 8-bit timer/counters with separate prescaler, one compare mode
  - One 16-bit timer/counter with separate prescaler, compare mode, and capture mode
  - Real-time counter with separate oscillator
  - Three PWM channels
  - 8-channel ADC in TQFP and QFN/MLF package

    - Eight channels 10-bit accuracy
  - 6-channel ADC in PDIP package
    - Six channels 10-bit accuracy
  - Byte-oriented two-wire serial interface
  - Programmable serial USART
  - Master/slave SPI serial interface
  - Programmable watchdog timer with separate on-chip oscillator
  - On-chip analog comparator
- Special Microcontroller Features
  - Power-on Reset and programmable Brown-out Detection
  - Internal calibrated RC oscillator
  - External and internal interrupt sources
  - Five sleep modes: Idle, ADC noise reduction, power-save, power-down, and standby
- I/O and Packages
  - 23 programmable I/O lines
  - 28-lead PDIP, 32-lead TQFP, and 32-pad QFN/MLF
- Operating Voltages
  - 2.7 - 5.5V
- Speed Grades
  - 0 - 16 MHz
- Power Consumption at 4 MHz, 3V, 25°C
  - Active: 3.6 mA
  - Idle mode: 1.0 mA
  - Power-down mode: 0.5 µA

Table of Contents

1. Description

The AVR® core combines a rich instruction set with 32 general purpose working registers. All the 32 registers are directly connected to the Arithmetic Logic Unit (ALU), allowing two independent registers to be accessed in one single instruction executed in one clock cycle. The resulting architecture is more code efficient while achieving throughputs up to ten times faster than conventional CISC microcontrollers.

The ATmega8A provides the following features: 8 KB of In-System Programmable Flash with Read-While-Write capabilities, 512 B of EEPROM, 1 KB of SRAM, 23 general purpose I/O lines, 32 general purpose working registers, three flexible timer/counters with compare modes, internal and external interrupts, a serial programmable USART, one byte oriented two-wire serial interface, a 6-channel ADC (eight channels in TQFP and QFN/MLF packages) with 10-bit accuracy, a programmable Watchdog timer with internal oscillator, an SPI serial port, and five software selectable power saving modes. The Idle mode stops the CPU while allowing the SRAM, timer/counters, one SPI port, and interrupt system to continue functioning. The Power-down mode saves the register contents but freezes the oscillator, disabling all other chip functions until the next Interrupt or Hardware Reset. In Power-save mode, the asynchronous timer continues to run, allowing the user to maintain a timer base while the rest of the device is sleeping. The ADC Noise Reduction mode stops the CPU and all I/O modules except asynchronous timer and ADC, to minimize switching noise during ADC conversions. In Standby mode, the crystal/resonator oscillator is running while the rest of the device is sleeping. This allows very fast start-up combined with low-power consumption.

Microchip offers the QTouch library for embedding capacitive touch buttons, sliders and wheels functionality into AVR microcontrollers. The patented charge-transfer signal acquisition offers robust sensing and includes fully debounced reporting of touch keys and includes Adjacent Key Suppression™ (AKS™) technology for unambiguous detection of key events. The easy-to-use QTouch Composer allows you to explore, develop and debug your own touch applications.

The device is manufactured using Microchip's high density nonvolatile memory technology. The on-chip ISP Flash allows the program memory to be reprogrammed In-System through an SPI serial interface, by a conventional nonvolatile memory programmer, or by an on-chip Boot program running on the AVR core. The Boot program can use any interface to download the application program in the Application Flash memory. Software in the Boot Flash section will continue to run while the Application Flash section is updated, providing true Read-While-Write operation. By combining an 8-bit RISC CPU with In-System Self-Programmable Flash on a monolithic chip, the ATmega8A is a powerful microcontroller that provides a highly flexible and cost effective solution to many embedded control applications.

The device is supported with a full suite of program and system development tools including: C Compilers, macro assemblers, program debugger/simulators, In-Circuit Emulators, and evaluation kit.

2. Configuration Summary

Features	ATmega8A
Pin count	32
Flash (KB)	8
SRAM (KB)	1
EEPROM (Bytes)	512
General Purpose I/O pins	23
SPI	1
TWI (I^2C)	1
USART	1
ADC	10-bit 15 ksps
ADC channels	6 (8 in TQFP and QFN/MLF packages)
AC propagation delay	Typ 400 ns
8-bit Timer/Counters	2
16-bit Timer/Counters	1
PWM channels	3
RC Oscillator	+/-3%
Operating voltage	2.7 - 5.5V
Max operating frequency	16 MHz
Temperature range	-40°C to +105°C

3. Ordering Information

Speed (MHz)	Power Supply	Ordering Code[2]	Package[1]	Operational Range
16	2.7 - 5.5V	ATmega8A-AU ATmega8A-AUR[3] ATmega8A-PU ATmega8A-MU ATmega8A-MUR[3]	32A 32A 28P3 32M1-A 32M1-A	Industrial (-40ºC to 85ºC)
		ATmega8A-AN ATmega8A-ANR[3] ATmega8A-MN ATmega8A-MNR[3] ATmega8A-PN	32A 32A 32M1-A 32M1-A 28P3	Extended (-40ºC to 105ºC)

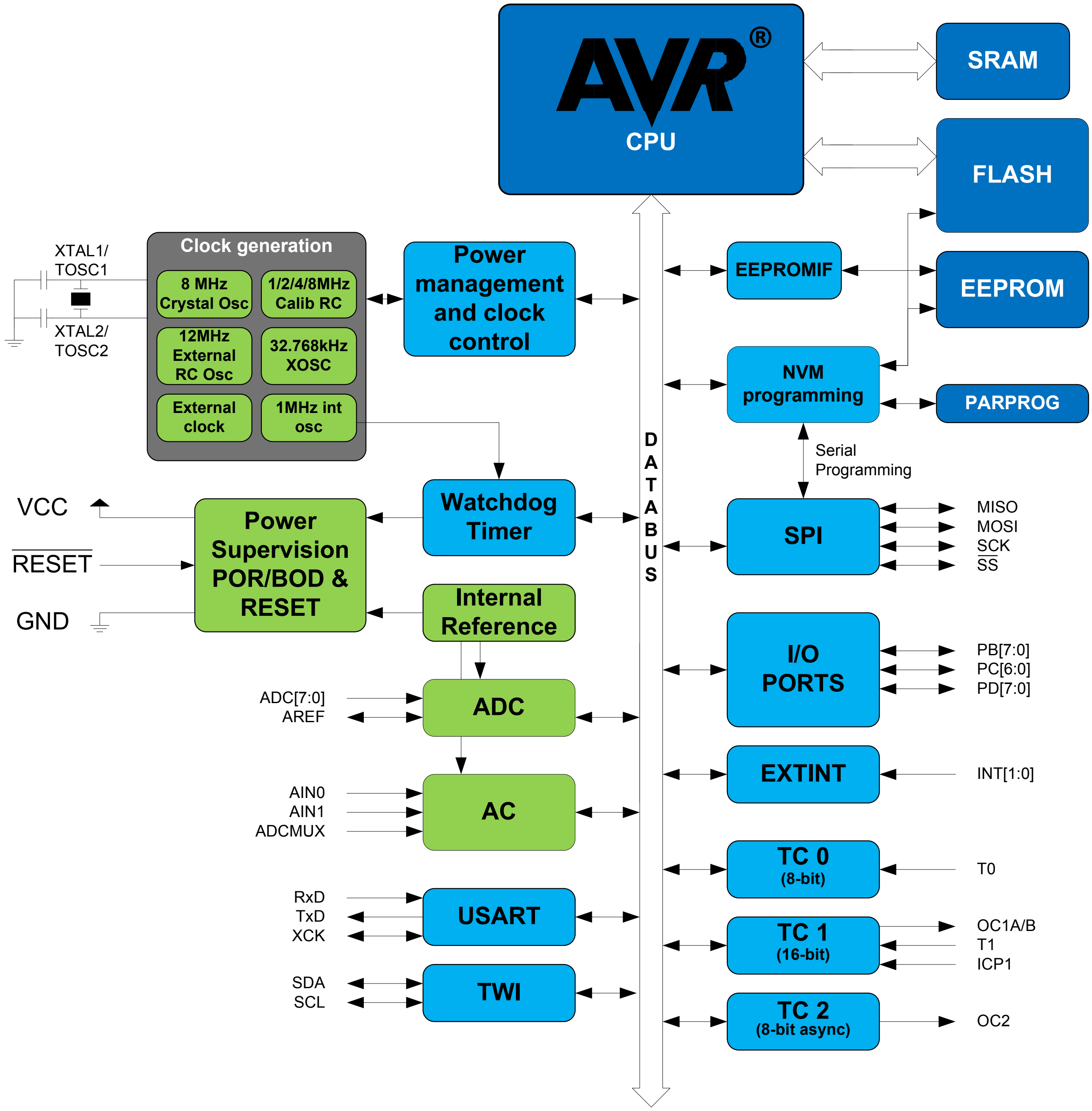
Note:

1. This device can also be supplied in wafer form. Please contact your local Microchip sales office for detailed ordering information and minimum quantities.
2. Pb-free packaging, complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.
3. Tape and Reel

Package Type	
32A	32-lead, Thin (1.0mm) Plastic Quad Flat Package (TQFP)
28P3	28-lead, 0.300” Wide, Plastic Dual Inline Package (PDIP)
32M1-A	32-pad, 5 x 5 x 1.0mm body, lead pitch 0.50mm, Quad Flat No-Lead/Micro Lead Frame Package (QFN/MLF)

4. Block Diagram

Figure 4-1. Block Diagram



5. Pin Configurations

Figure 5-1. PDIP

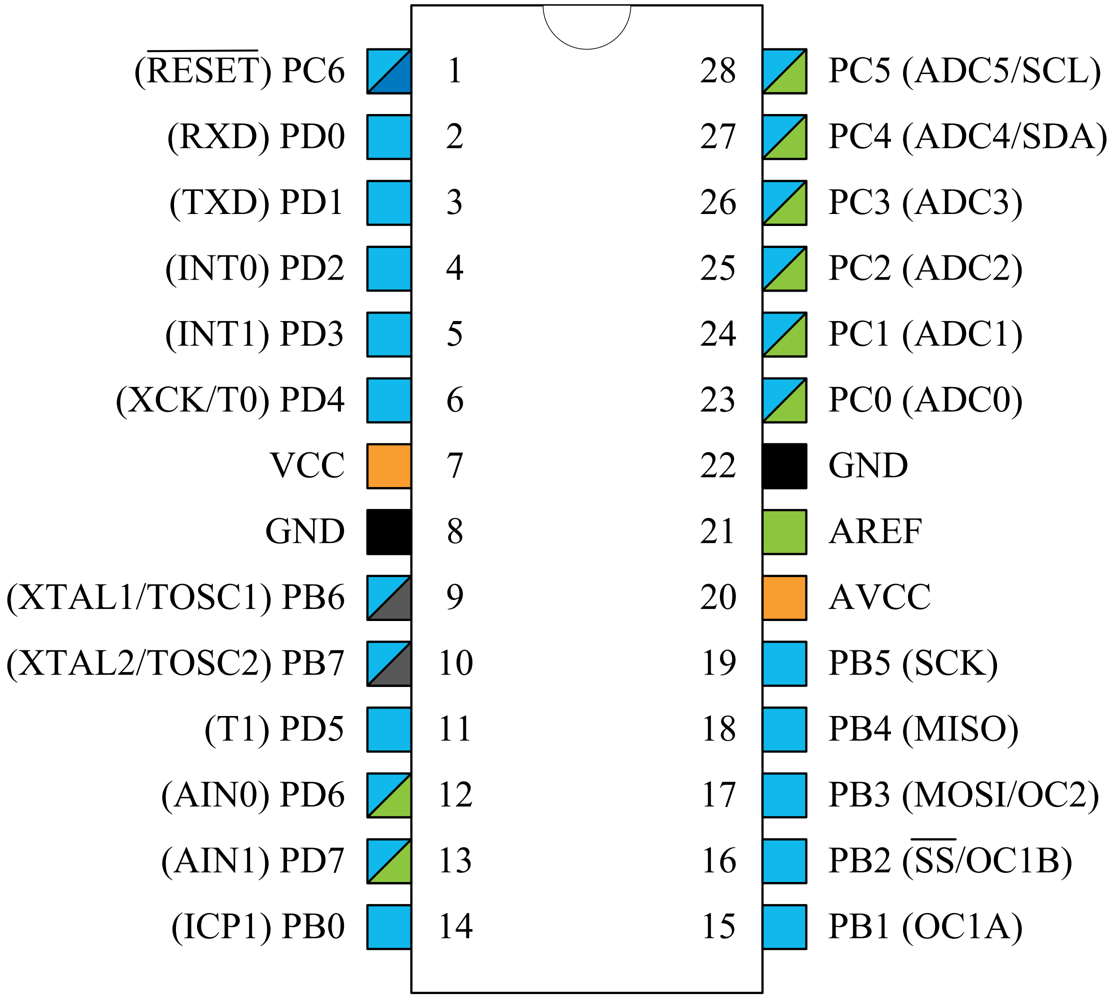


Figure 5-2. TQFP Top View

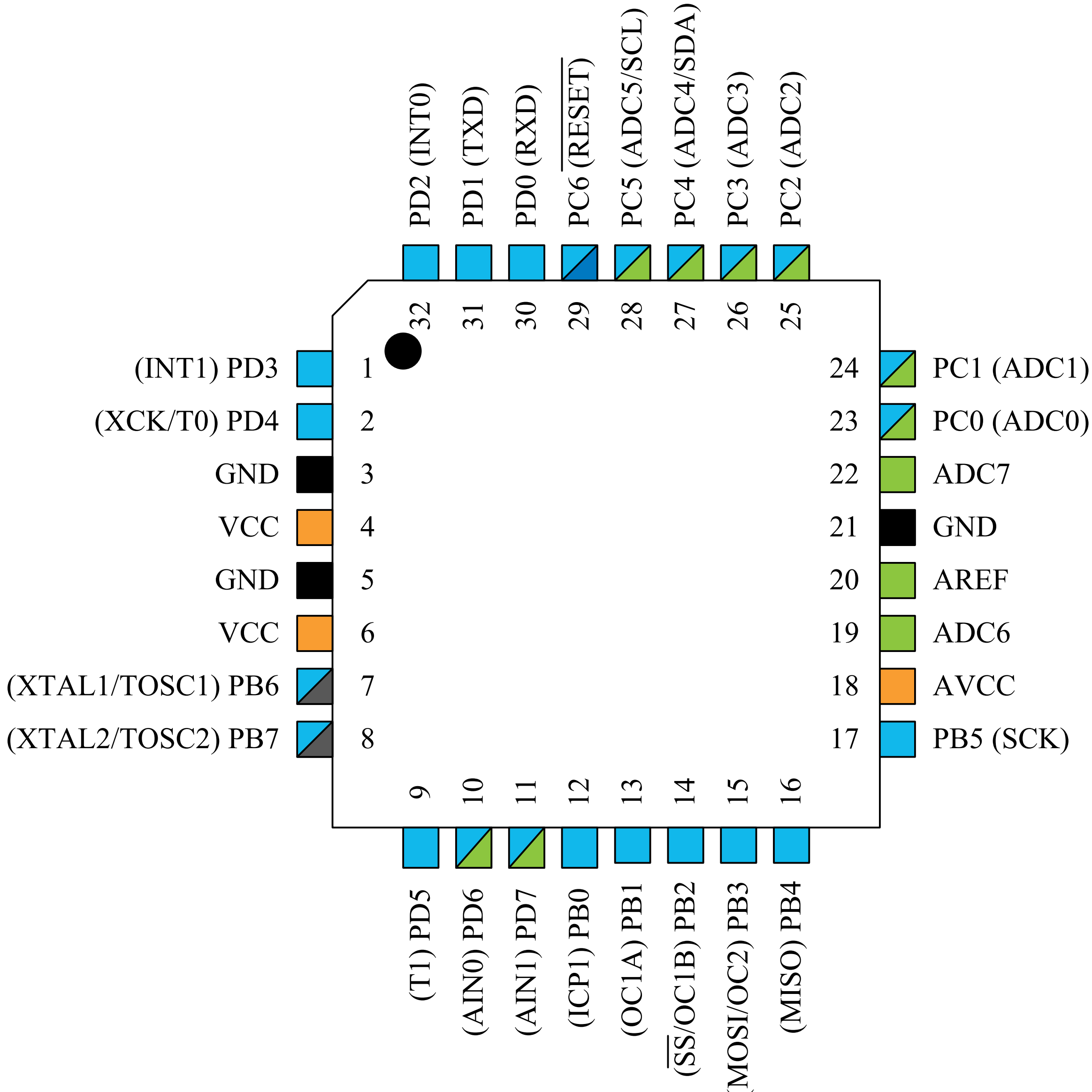
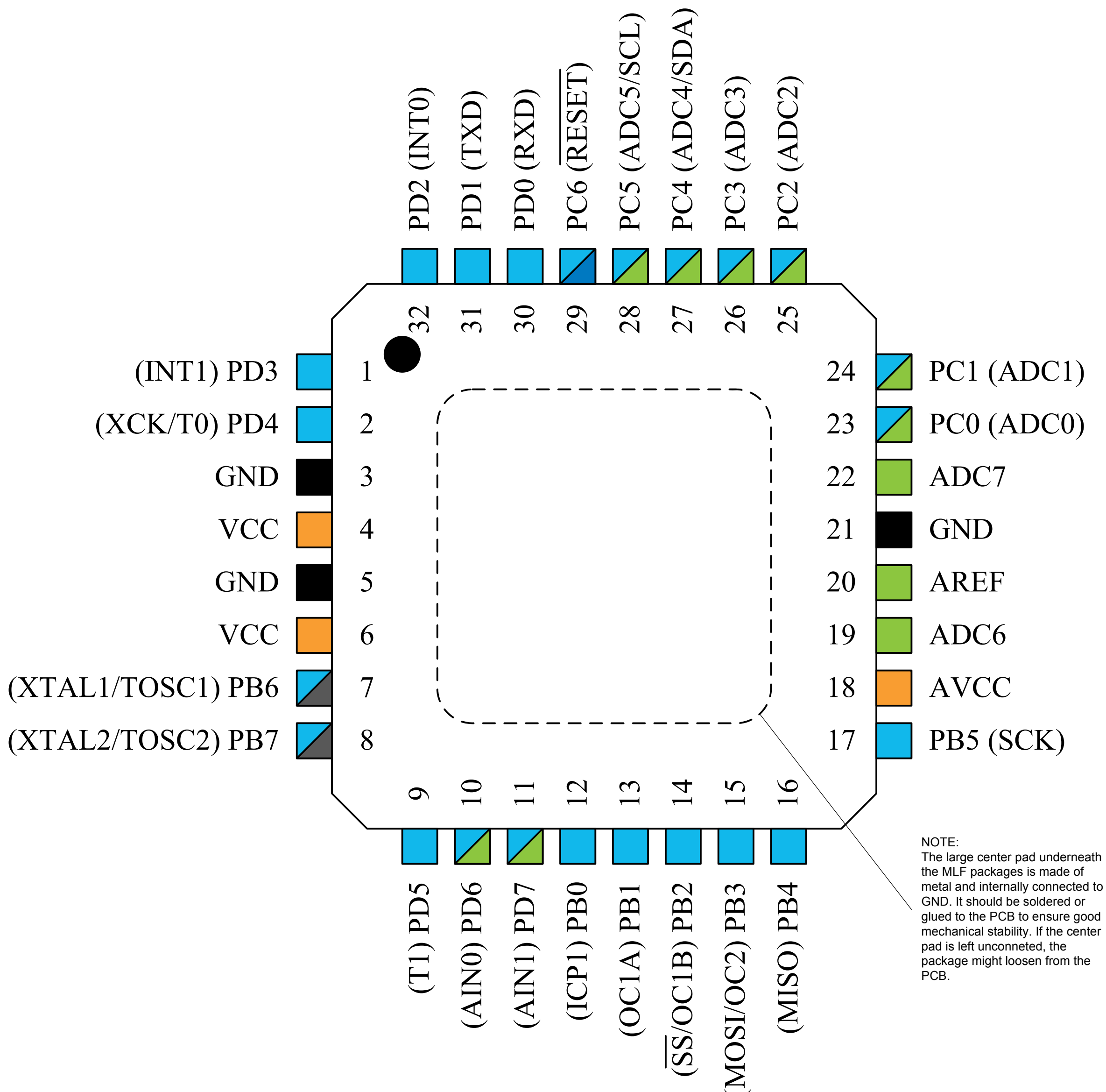


Figure 5-3. MLF Top View



6. I/O Multiplexing

Each pin is by default controlled by the PORT as a general purpose I/O and alternatively it can be assigned to one of the peripheral functions.

The following table describes the peripheral signals multiplexed to the PORT I/O pins.

Table 6-1. 32-Pin TQFP and MLF: PORT Function Multiplexing

No	PAD32	EXTINT	ADC/AC	OSC	T/C # 0	T/C # 1	USART	I2C	SPI
1	PD[3]	INT1							
2	PD[4]				T0		XCK0		
3	GND								
4	VCC								
5	GND								
6	VCC								
7	PB[6]			XTAL1/TOSC1					
8	PB[7]			XTAL2/TOSC2					
9	PD[5]					T1			
10	PD[6]		AIN0						
11	PD[7]		AIN1						
12	PB[0]				ICP1				
13	PB[1]				OC1A				
14	PB[2]				OC1B				$\overline{\text{SS0}}$
15	PB[3]				OC2				MOSI0
16	PB[4]								MISO0
17	PB[5]								SCK0
18	AVCC								
19	ADC6		ADC6						
20	AREF								
21	GND								
22	ADC7		ADC7						
23	PC[0]		ADC0						
24	PC[1]		ADC1						
25	PC[2]		ADC2						
26	PC[3]		ADC3						
27	PC[4]		ADC4					SDA0	
28	PC[5]		ADC5					SCL0	
29	PC[6]/$\overline{\text{RESET}}$								
30	PD[0]						RXD0		

No	PAD32	EXTINT	ADC/AC	OSC	T/C # 0	T/C # 1	USART	I2C	SPI
31	PD[1]						TXD0		
32	PD[2]	INT0							

Table 6-2. 28-Pin PDIP: PORT Function Multiplexing

No	PAD28	EXTINT	ADC/AC	OSC	T/C # 0	T/C # 1	USART	I2C	SPI
1	PC[6]/$\overline{\text{RESET}}$								
2	PD[0]						RXD0		
3	PD[1]						TXD0		
4	PD[2]	INT0							
5	PD[3]	INT1							
6	PD[4]				T0		XCK0		
7	VCC								
8	GND								
9	PB[6]			XTAL1/TOSC1					
10	PB[7]			XTAL2/TOSC2					
11	PD[5]					T1			
12	PD[6]		AIN0						
13	PD[7]		AIN1						
14	PB[0]				ICP1				
15	PB[1]				OC1A				
16	PB[2]				OC1B				$\overline{\text{SS0}}$
17	PB[3]				OC2				MOSI0
18	PB[4]								MISO0
19	PB[5]								SCK0
20	AVCC								
21	AREF								
22	GND								
23	PC[0]		ADC0						
24	PC[1]		ADC1						
25	PC[2]		ADC2						
26	PC[3]		ADC3						
27	PC[4]		ADC4					SDA0	
28	PC[5]		ADC5					SCL0	

7. Resources

A comprehensive set of development tools, application notes and datasheets are available for download on http://www.microchip.com/design-centers/8-bit .

8. Data Retention

Reliability qualification results show that the projected data retention failure rate is much less than 1 PPM over 20 years at 85°C or 100 years at 25°C.

9. About Code Examples

This datasheet contains simple code examples that briefly show how to use various parts of the device. These code examples assume that the part specific header file is included before compilation. Be aware that not all C compiler vendors include bit definitions in the header files and interrupt handling in C is compiler dependent. Please confirm with the C compiler documentation for more details.

10. Capacitive Touch Sensing

10.1 QTouch Library

The QTouch® library provides a simple to use solution to realize touch sensitive interfaces on most AVR® microcontrollers. The QTouch library includes support for the QTouch and QMatrix™ acquisition methods.

Touch sensing can be added to any application by linking the appropriate QTouch library for the AVR microcontroller. This is done by using a simple set of APIs to define the touch channels and sensors, and then calling the touch sensing API's to retrieve the channel information and determine the touch sensor states.

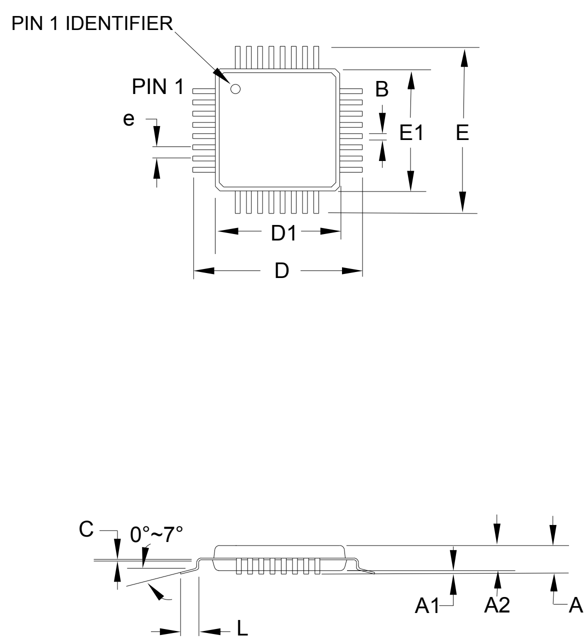
The QTouch library is FREE and downloadable from QTouch Library . For implementation details and other information, refer to the QTouch Library User Guide, also available for download from the Microchip website.

11. Packaging Information

11.1 32-pin 32A

Note:

Note: For the most current package drawings, see the Microchip Packaging Specification located at http://www.microchip.com/packaging



COMMON DIMENSIONS
(Unit of measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.20	
A1	0.05	–	0.15	
A2	0.95	1.00	1.05	
D	8.75	9.00	9.25	
D1	6.90	7.00	7.10	Note 2
E	8.75	9.00	9.25	
E1	6.90	7.00	7.10	Note 2
B	0.30	–	0.45	
C	0.09	–	0.20	
L	0.45	–	0.75	
e	0.80 TYP			

Notes:
1. This package conforms to JEDEC reference MS-026, Variation ABA.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.10mm maximum.

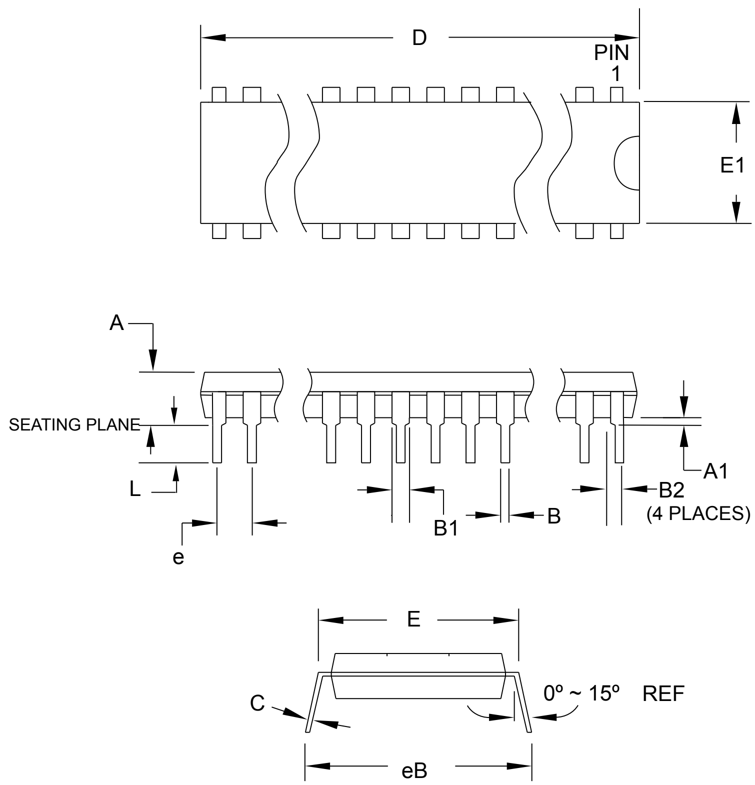
2010-10-20

	TITLE	DRAWING NO.	REV.
Atmel	**32A,** 32-lead, 7 x 7mm body size, 1.0mm body thickness, 0.8mm lead pitch, thin profile plastic quad flat package (TQFP)	32A	C

11.2 28-pin 28P3

Note:

Note: For the most current package drawings, see the Microchip Packaging Specification located at http://www.microchip.com/packaging



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	4.5724	
A1	0.508	–	–	
D	34.544	–	34.798	Note 1
E	7.620	–	8.255	
E1	7.112	–	7.493	Note 1
B	0.381	–	0.533	
B1	1.143	–	1.397	
B2	0.762	–	1.143	
L	3.175	–	3.429	
C	0.203	–	0.356	
eB	–	–	10.160	
e	2.540 TYP			

Note: 1. Dimensions D and E1 do not include mold Flash or Protrusion. Mold Flash or Protrusion shall not exceed 0.25mm (0.010").

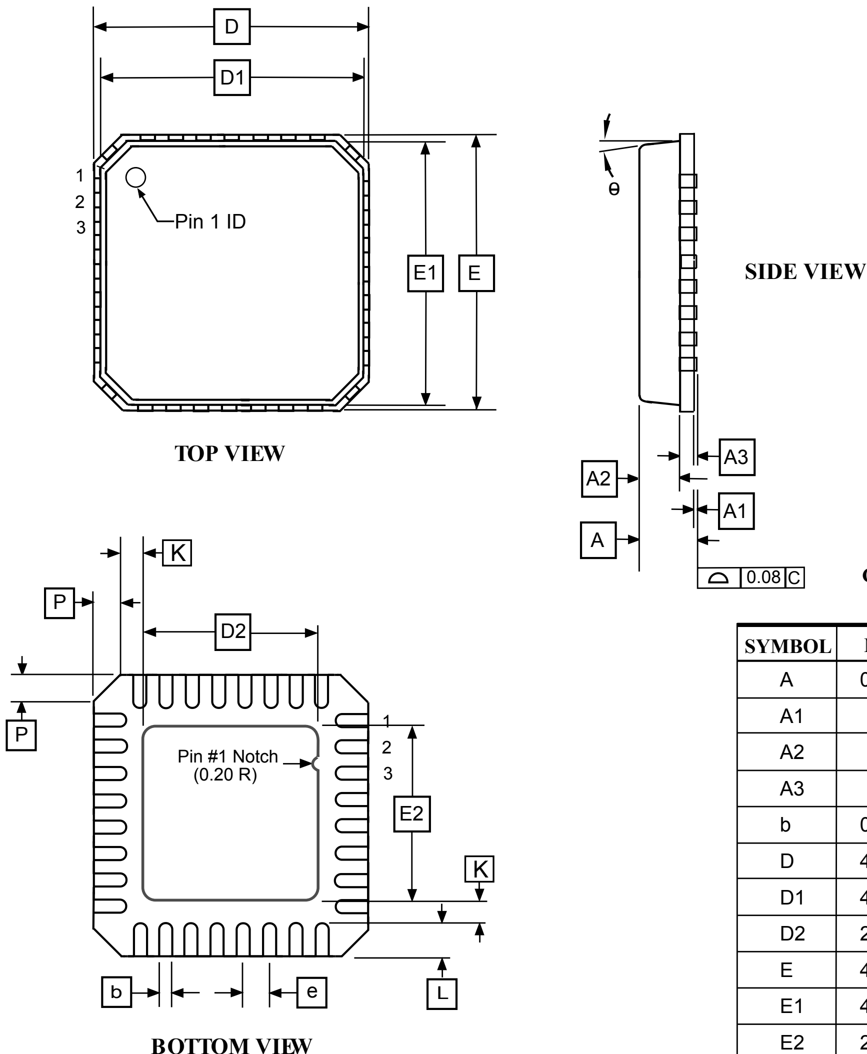
09/28/01

	TITLE	DRAWING NO.	REV.
Atmel 2325 Orchard Parkway San Jose, CA 95131	**28P3**, 28-lead (0.300"/7.62mm Wide) Plastic Dual Inline Package (PDIP)	28P3	B

11.3 32-pin 32M1-A

Note:

Note: For the most current package drawings, see the Microchip Packaging Specification located at http://www.microchip.com/packaging



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	0.80	0.90	1.00	
A1	–	0.02	0.05	
A2	–	0.65	1.00	
A3		0.20 REF		
b	0.18	0.23	0.30	
D	4.90	5.00	5.10	
D1	4.70	4.75	4.80	
D2	2.95	3.10	3.25	
E	4.90	5.00	5.10	
E1	4.70	4.75	4.80	
E2	2.95	3.10	3.25	
e		0.50 BSC		
L	0.30	0.40	0.50	
P	–	–	0.60	
θ	–	–	12^{o}	
K	0.20	–	–	

Note: JEDEC Standard MO-220, Fig. 2 (Anvil Singulation), VHHD-2.

03/14/2014

	TITLE	DRAWING NO.	REV.
Atmel Package Drawing Contact: packagedrawings@atmel.com	**32M1-A**, 32-pad, 5 x 5 x 1.0mm Body, Lead Pitch 0.50mm, 3.10mm Exposed Pad, Micro Lead Frame Package (MLF)	32M1-A	F

12. Errata

The revision letter in this section refers to the revision of the ATmega8A device.

12.1 ATmega8A, rev. L

- **First Analog Comparator conversion may be delayed**
- **Interrupts may be lost when writing the timer registers in the asynchronous timer**
- **Signature may be Erased in Serial Programming Mode**
- **CKOPT Does not Enable Internal Capacitors on XTALn/TOSCn Pins when 32kHz Oscillator is Used to Clock the Asynchronous Timer/Counter2**
- **Reading EEPROM by using ST or STS to set EERE bit triggers unexpected interrupt request**

1. **First Analog Comparator conversion may be delayed**
   If the device is powered by a slow rising V_{CC}, the first analog comparator conversion will take longer than expected on some devices.

   Problem Fix / Workaround:

   When the device has been powered or reset, disable then enable the analog comparator before the first conversion.
2. **Interrupts may be lost when writing the timer registers in the asynchronous timer**
   The interrupt will be lost if a timer register that is synchronous timer clock is written when the asynchronous Timer/Counter register (TCNTx) is 0x00.

   Problem Fix / Workaround:

   Always check that the asynchronous Timer/Counter register neither have the value 0xFF nor 0x00 before writing to the asynchronous Timer Control Register (TCCRx), asynchronous Timer Counter Register (TCNTx), or asynchronous Output Compare Register (OCRx).
3. **Signature may be Erased in Serial Programming Mode**
   If the signature bytes are read before a chiperase command is completed, the signature may be erased causing the device ID and calibration bytes to disappear. This is critical, especially, if the part is running on internal RC oscillator.

   Problem Fix / Workaround:

   Ensure that the chiperase command has exceeded before applying the next command.
4. **CKOPT Does not Enable Internal Capacitors on XTALn/TOSCn Pins when 32kHz Oscillator is Used to Clock the Asynchronous Timer/Counter2**
   When the internal RC oscillator is used as the main clock source, it is possible to run the Timer/Counter2 asynchronously by connecting a 32kHz Oscillator between XTAL1/TOSC1 and XTAL2/TOSC2. But when the internal RC oscillator is selected as the main clock source, the CKOPT fuse does not control the internal capacitors on XTAL1/TOSC1 and XTAL2/TOSC2. As long as there are no capacitors connected to XTAL1/TOSC1 and XTAL2/TOSC2, safe operation of the oscillator is not guaranteed.

   Problem Fix / Workaround:

   Use external capacitors in the range of 20 - 36 pF on XTAL1/TOSC1 and XTAL2/TOSC2. This will be fixed in ATmega8A Rev. G where the CKOPT Fuse will control internal capacitors also when internal RC oscillator is selected as main clock source. For ATmega8A Rev. G, CKOPT = 0 (programmed) will enable the internal capacitors on XTAL1 and XTAL2. Customers who want compatibility between Rev. G and older revisions, must ensure that CKOPT is unprogrammed (CKOPT = 1).

5. **Reading EEPROM by using ST or STS to set EERE bit triggers unexpected interrupt request.**
   Reading EEPROM by using the ST or STS command to set the EERE bit in the EECR register triggers an unexpected EEPROM interrupt request.

   Problem Fix / Workaround:

   Always use OUT or SBI to set EERE in EECR.

13. Appendix A: Revision History

Revision A (January 2018)

- Atmel document number 8159FS is now Microchip **DS40001991A**.

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