

MC74HC367A

Hex 3-State Noninverting Buffer with Separate 2-Bit and 4-Bit Sections

High-Performance Silicon-Gate CMOS

The MC74HC367A is identical in pinout to the LS367. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device is arranged into 2-bit and 4-bit sections, each having its own active-low Output Enable. When either of the enables is high, the affected buffer outputs are placed into high-impedance states. The HC367A has noninverting outputs.

Features

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- These are Pb-Free Devices

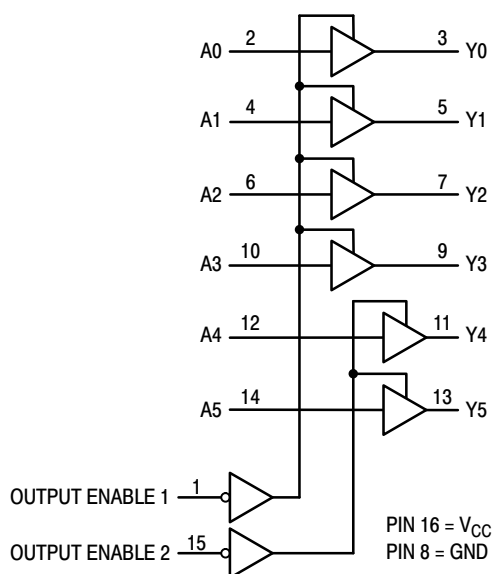
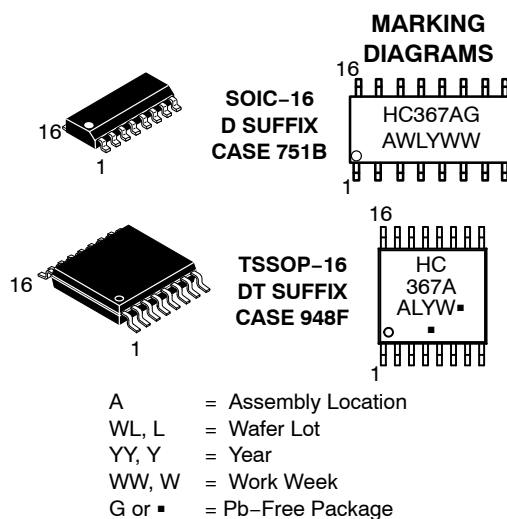


Figure 1. Logic Diagram



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(Note: Microdot may be in either location)

PIN ASSIGNMENT

OUTPUT ENABLE 1	1	16	V _{CC}
A0	2	15	OUTPUT ENABLE 2
Y0	3	14	A5
A1	4	13	Y5
Y1	5	12	A4
A2	6	11	Y4
Y2	7	10	A3
GND	8	9	Y3

FUNCTION TABLE

Inputs		Output
Enable 1, Enable 2	A	Y
L	L	L
L	H	H
H	X	Z

X = don't care

Z = high impedance

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

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MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, SOIC Package TSSOP Package	500 450	mW
T_{stg}	Storage Temperature	-65 to + 150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V _{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V	
T _A	Operating Temperature, All Package Types	−55	+125	°C	
t _r , t _f	Input Rise and Fall Time (Figure 2)	V _{CC} = 2.0 V	0	1000	ns
		V _{CC} = 3.0 V	0	600	
		V _{CC} = 4.5 V	0	500	
		V _{CC} = 6.0 V	0	400	

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DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limit			Unit
				- 55 to 25°C	≤ 85°C	≤ 125°C	
V _{IH}	Minimum High-Level Input Voltage	V _{out} = V _{CC} - 0.1 V I _{out} ≤ 20 μA	2.0	1.5	1.5	1.5	V
			3.0	2.1	2.1	2.1	
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V _{IL}	Maximum Low-Level Input Voltage	V _{out} = 0.1 V I _{out} ≤ 20 μA	2.0	0.50	0.50	0.50	V
			3.0	0.90	0.90	0.90	
			4.5	1.35	1.35	1.35	
			6.0	1.80	1.80	1.80	
V _{OH}	Minimum High-Level Output Voltage	V _{in} = V _{IH} I _{out} ≤ 20 μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
		V _{in} = V _{IH} I _{out} ≤ 3.6 mA I _{out} ≤ 6.0 mA I _{out} ≤ 7.8 mA	3.0	2.48	2.34	2.20	
			4.5	3.98	3.84	3.70	
			6.0	5.48	5.34	5.20	
V _{OL}	Maximum Low-Level Output Voltage	V _{in} = V _{IL} I _{out} ≤ 20 μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
		V _{in} = V _{IL} I _{out} ≤ 3.6 mA I _{out} ≤ 6.0 mA I _{out} ≤ 7.8 mA	3.0	0.26	0.33	0.40	
			4.5	0.26	0.33	0.40	
			6.0	0.26	0.33	0.40	
I _{in}	Maximum Input Leakage Current	V _{in} = V _{CC} or GND	6.0	± 0.1	± 1.0	± 1.0	μA
I _{OZ}	Maximum Three-State Leakage Current	Output in High-Impedance State V _{in} = V _{IL} or V _{IH} V _{out} = V _{CC} or GND	6.0	± 0.5	± 5.0	± 10	μA
I _{CC}	Maximum Quiescent Supply Current (per Package)	V _{in} = V _{CC} or GND I _{out} = 0 μA	6.0	4	40	160	μA

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AC ELECTRICAL CHARACTERISTICS ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			- 55 to 25°C	≤ 85°C	≤ 125°C	
t_{PLH} , t_{PHL}	Maximum Propagation Delay, Input A to Output Y (Figures 2 and 4)	2.0 3.0 4.5 6.0	120 60 24 20	150 75 30 26	180 90 36 31	ns
t_{PLZ} , t_{PHZ}	Maximum Propagation Delay, Output Enable to Output Y (Figures 3 and 5)	2.0 3.0 4.5 6.0	175 90 35 30	220 110 44 37	265 135 53 45	ns
t_{PZL} , t_{PZH}	Maximum Propagation Delay, Output Enable to Output Y (Figures 3 and 5)	2.0 3.0 4.5 6.0	190 95 38 32	240 120 48 21	285 150 57 48	ns
t_{TLH} , t_{THL}	Maximum Output Transition Time, Any Output (Figures 2 and 4)	2.0 3.0 4.5 6.0	60 22 12 10	75 28 15 13	90 34 18 15	ns
C_{in}	Maximum Input Capacitance	–	10	10	10	pF
C_{out}	Maximum Three-State Output Capacitance (Output in High-Impedance State)	–	15	15	15	pF

C _{PD}	Power Dissipation Capacitance (Per Buffer)	Typical @ 25°C, V _{CC} = 5.0 V	pF
		60	

SWITCHING WAVEFORMS

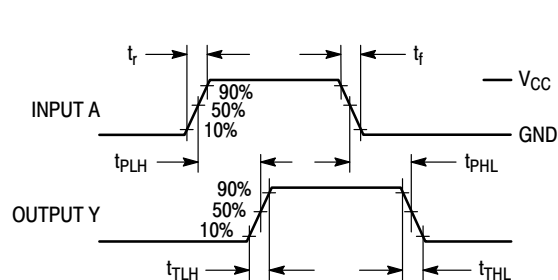


Figure 2.

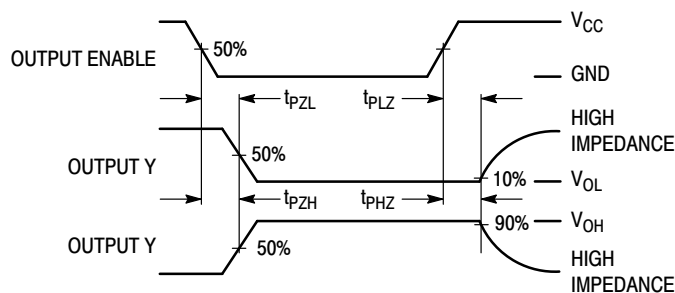
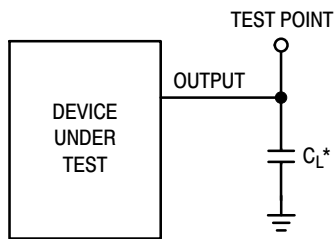


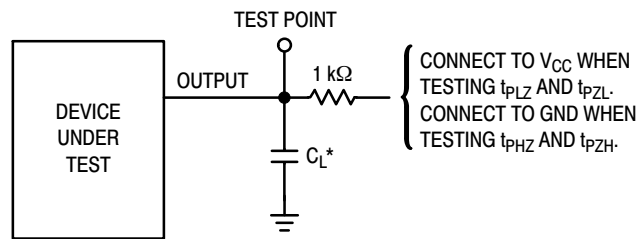
Figure 3.

TEST CIRCUITS



*Includes all probe and jig capacitance

Figure 4.



*Includes all probe and jig capacitance

Figure 5.

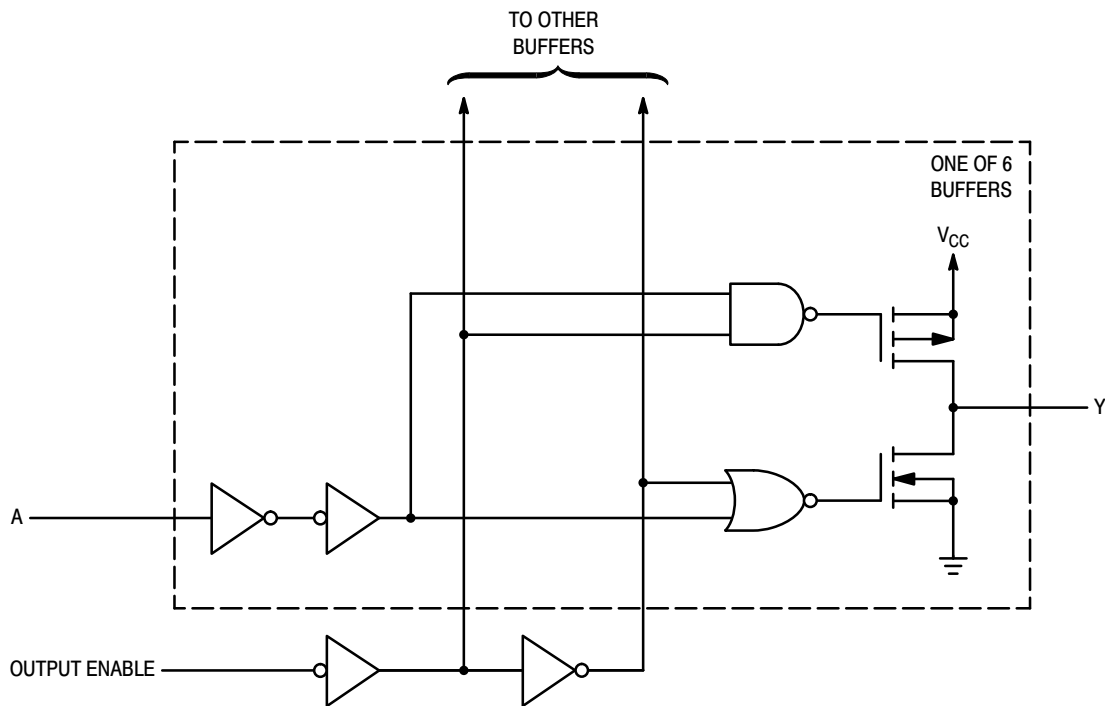


Figure 6. Logic Detail

ORDERING INFORMATION

Device	Package	Shipping [†]
MC74HC367ADG	SOIC–16 (Pb–Free)	48 Units / Rail
MC74HC367ADR2G	SOIC–16 (Pb–Free)	2500 Tape & Reel
MC74HC367ADTR2G	TSSOP–16*	2500 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*This package is inherently Pb-Free.

PACKAGE DIMENSIONS

Technical drawing of a 16-plate seat assembly. The drawing includes a top view showing 16 plates with dimensions A (total width), B (plate width), G (plate spacing), and P (plate thickness). A detail view shows a single plate with dimensions C (plate height), D (plate thickness), K (plate width), and J (plate width). A side view shows the plate with dimensions R (radius) and M (plate width). A cross-section view shows the plate with dimensions F (plate width) and J (plate width). The drawing also includes a table with dimensions and a table with material and finish specifications.

Top View Dimensions:

- A: Total width of the seat assembly.
- B: Width of a single plate.
- G: Spacing between plates.
- P: Thickness of a plate.

Detail View Dimensions:

- C: Height of the plate.
- D: Thickness of the plate.
- K: Width of the plate.
- J: Width of the plate.

Side View Dimensions:

- R: Radius of the plate.
- M: Width of the plate.

Cross-section View Dimensions:

- F: Width of the plate.
- J: Width of the plate.

Table with dimensions:

⊕	0.25 (0.010)	(M)	B	Ⓢ
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Table with material and finish specifications:

⊕	0.25 (0.010)	(M)	T	B	Ⓢ	A	Ⓢ
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1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0 °	7 °	0 °	7 °
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

Diagram illustrating the dimensions and frame numbering of a 16X 8X microfilm cartridge. The cartridge is shown with 16 frames, numbered 1 through 16. The dimensions are given in millimeters:

- Overall width: 6.40 mm (labeled 8X).
- Frame width: 1.12 mm (labeled 16X).
- Frame height: 0.58 mm (labeled 16X).
- Frame pitch: 1.27 mm (labeled PITCH).

The frames are arranged in two columns of 8 frames each. The left column is numbered 1 through 8, and the right column is numbered 16 through 9. The frames are separated by a vertical line.

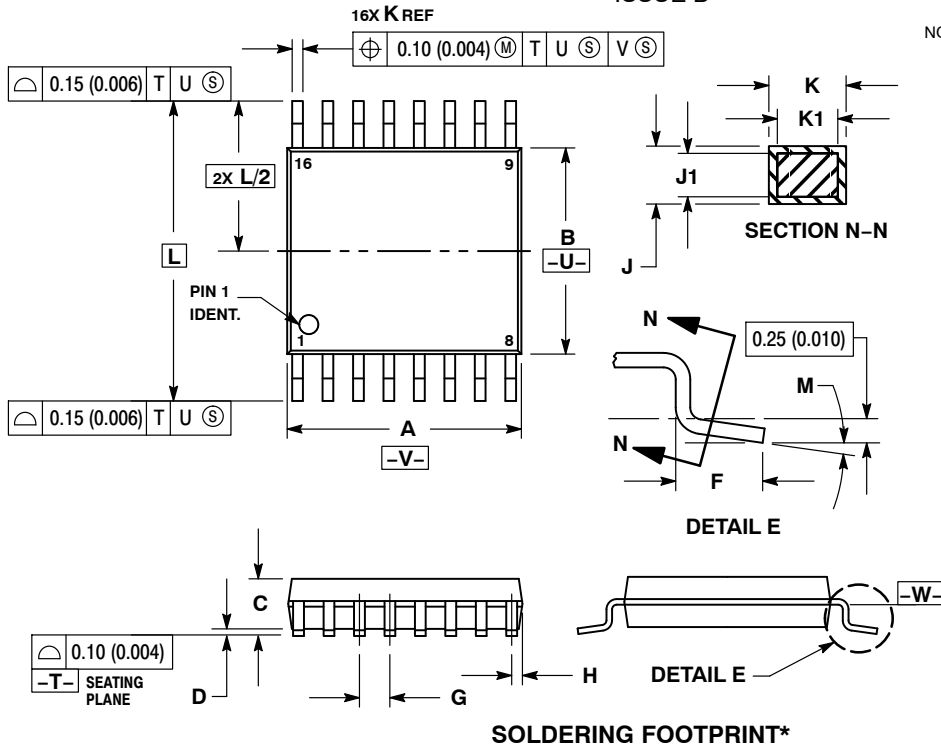
DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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PACKAGE DIMENSIONS

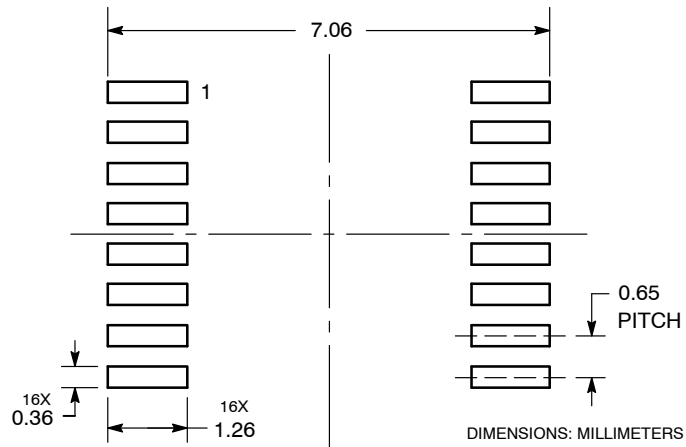
TSSOP-16
DT SUFFIX
CASE 948F-01
ISSUE B



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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