

User manual for MERUS™ evaluation boards

MA12040/MA12040P/MA12070/MA12070P

About this document

Scope and purpose

The evaluation board is an evaluation and demonstration board for [MA12040](#), [MA12040P](#), [MA12070](#), and [MA12070P](#) proprietary multi-level amplifiers.

Intended audience

Audio amplifier design engineers

Attention: *Please read through this user manual before operating the board. When powering up the board make sure to follow the instructions in the “Start Sequence” section.*

Attention: *Please observe proper ESD handling procedures. Failure to do so may result in damage to components on the board.*

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1 Overview

The demonstration board is an evaluation and demonstration board for MERUS™ audio MA12040, MA12040P, MA12070, and MA12070P amplifiers.

It contains a variety of digital/analog input, output and setup/selection features. It also contains two on-board power supply generators (5 V and 3.3 V buck-converted) so only one external power supply (PVDD) are necessary.

The board can be used for evaluating or demonstrating key features/advantages of the MERUS™ technology:

- Energy efficiency
 - Power losses at normal user operating conditions (listening levels)
 - Idle power loss
- Adaptive power management system
- No output filter components
 - Solution cost and size reduction
- Audio performance
 - THD performance and audio quality

1.1 Board features and audio performance

- | | |
|---------------------------------|---------------------------|
| • Number of audio channels | 2 x BTL, 1xBTL+2xSE, 4xSE |
| • Audio input format | |
| – MA120xx | Analog |
| – MA120xxP | Digital (I2S) |
| • Amplifier gain | 20 dB / configurable 26dB |
| • Supply voltage | PVDD |
| – Max PVDD for MA12040/MA12040P | 18 V |
| – Max PVDD for MA12070/MA12070P | 26 V |
| • Output noise level | |
| – MA120xx | <100 uVrms(AW) |
| – MA120xxP | <150 uVrms(AW) |
| • Dynamic range | |
| – MA120xx | >100 dB |
| – MA120xxP | >95 dB |
| • Idle consumption @ PVDD=18V | |
| – MA120xx | <16 mA * |
| – MA120xxP | <19 mA * |
| • Crosstalk | <-85 dB |
| • Efficiency, full-scale, 8 ohm | 91% |

Overview

Note: Idle consumption is the sum of output stage current and 5 V supply and 3.3 V supply current. As all the supplies are tied to PVDD, the efficiency of the buck-converted 5 V and 3.3 V should be taken into account when measuring idle current consumption directly from PVDD. Features on the EVK makes it possible to break the 5V and 3.3V supply lines after the buck converters (see table 1). Please refer to the MA120xx/P device datasheet for exact current figures.

1.2 EVK device type

The type of device (MA12040, MA12040P, MA12070 and MA12070P) on the EVK is printed on the top on the device, and also stated on the serial number label placed on the bottom side of the EVK PCB.

2 Setup guide

Equipment required for operating and evaluating

- Single power supply for PVDD.
- Analog audio source or signal generator with line level output (MA120xx)
- Digital I2S audio source (MA120xxP)
- Cables for input and output connectors
- Audio analyzer with measurement filter

2.1 Connections and interfaces

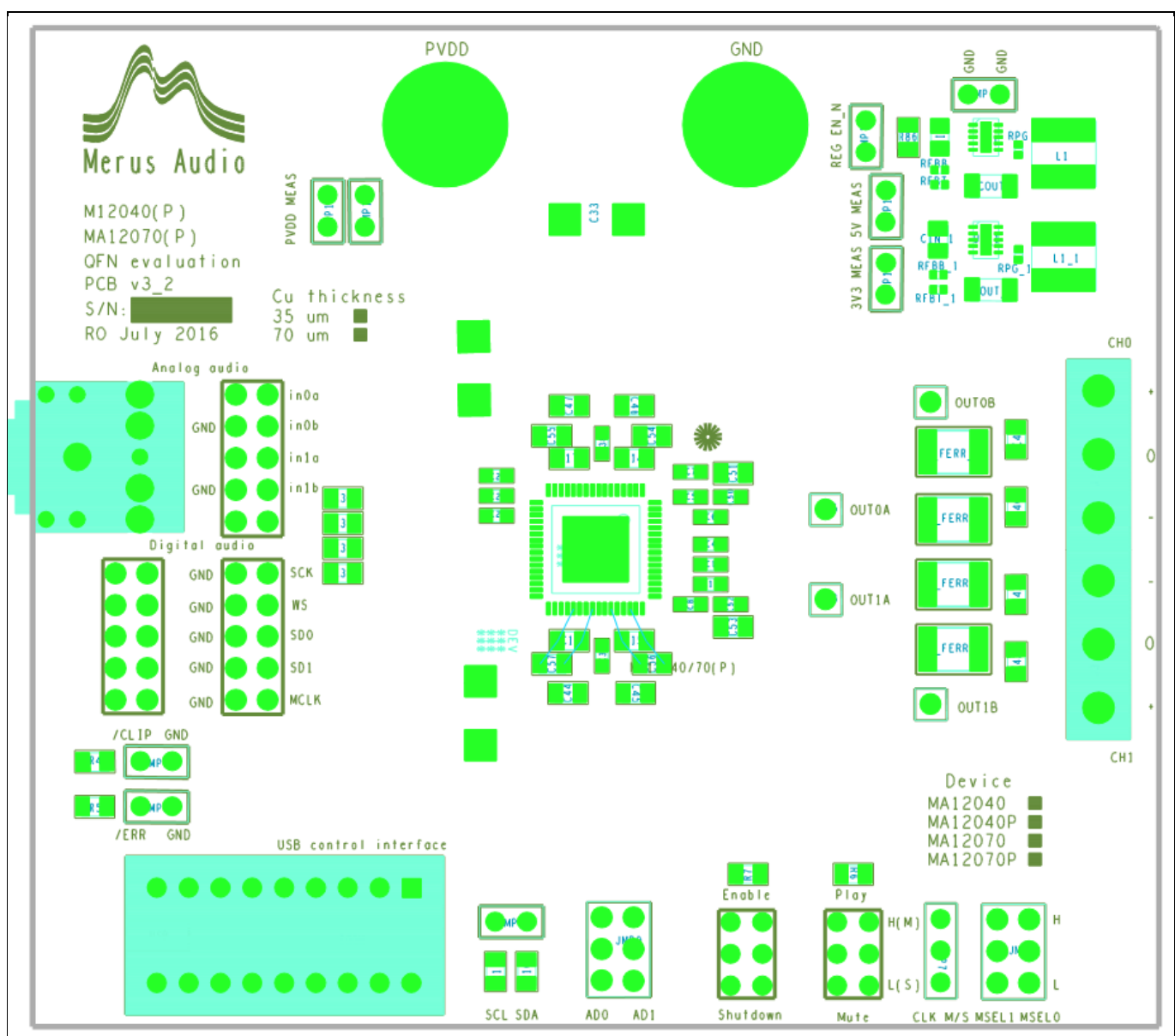


Figure 1 Top block view of EVK board

Note: For schematic: see Figure 5 on page 15.

Table 1 EVK headers and connectors

| Name | Schem. Ref. | Description | Comment |
|----------------|-------------|--|--|
| MSEL0 | JMP1 | Selects in conjunction with MSEL1 the output configuration (see table 2). | Default: 2CH BTL. Jumpered high (H). |
| MSEL1 | JMP1 | Selects in conjunction with MSEL0 the output configuration (see table 2). | Default: 2CH BTL. Jumpered low (L). |
| /CLIP | JMP5 | Audio clipping indicator (open drain output), pulled low when clipping occurs. | I/O pin. Do not jumper. |
| /ERR | JMP6 | Error indicator (open drain output), pulled low when an error occurs. | I/O pin. Do not jumper. |
| CLK M/S | JMP7 | Selects clock mode. | M=Master clock (non P versions). S= Slave (external) clock (P versions). |
| AD0 AD1 | JMP9 | Selects I2C address (see table 3). | Default: I2C address 0B100000. Both jumpered low (GND). |
| REG EN_N | JMP10 | Enables 5 V and 3.3 V supplies. | Default: Jumpered. |
| PVDD MEAS | JMP11 | Breaks PVDD for PVDD current measurements. | Default: Jumpered. Parallel with JMP16. |
| 5V MEAS | JMP12 | Breaks 5 V supply for 5 V circuit current measurements. | Default: Jumpered. |
| 3V3 MEAS | JMP13 | Breaks 3.3 V supply for 3.3 V circuit current measurements. | Default: Jumpered. |
| GND GND | JMP14 | Two ground connections. | Default: Not jumpered. |
| SCL SDA | JMP15 | I2C bus serial clock and data. | I/O Pin. Do not jumper. |
| PVDD MEAS | JMP16 | Breaks PVDD for current measurements. | Default: Jumpered Parallel with JMP11. |
| CH0 | J2 | Channel0 speaker connection. | 3 way screw terminal with positive and negative speaker outputs. Center GND. |
| CH1 | J3 | Channel1 speaker connection. | 3 way screw terminal with positive and negative speaker outputs. Center GND. |
| JACK | J6 | Single ended, stereo analog audio input. | Tip = CH0 Ring = CH1 Sleeve = GND |
| DIGITAL AUDIO1 | J7 | I2S Digital audio input. NOTE: see section 2.2 for setting up. | I/O pins. Do not jumper. |

Setup guide

| Name | Schem. Ref. | Description | Comment |
|----------------|-------------|--|--|
| ANALOG AUDIO | J9 | Balanced analog audio input connector. Also selects "JACK" input. NOTE: see section 2.2 for setting up. | Jack input = All Jumped. Balanced input = use pins for balanced analog audio input. NOTE: Should NOT be jumpered for P (digital audio) versions. |
| PVDD | J12 | External power supply POSITIVE terminal. | PVDD : +18 V MAX (MA12040/-P) PVDD : +26V MAX (MA12070/-P). |
| GND | J13 | External power supply GND terminal. | GND. |
| DIGITAL AUDIO2 | J14 | I2S Digital audio input. NOTE: see section 2.2 for setting up. | I/O pins. Do not jumper. |
| OUT0A | J15 | Direct connection to device output node vsw_a0. | Output measuring pin. |
| OUT0B | J16 | Direct connection to device output node vsw_b0. | Output measuring pin. |
| OUT1B | J17 | Direct connection to device output node vsw_b1. | Output measuring pin. |
| OUT1A | J18 | Direct connection to device output node vsw_a1. | Output measuring pin. |

Table 2 Signal configuration (JMP1)

| MSEL0 | MSEL1 | Configuration |
|-------|-------|--|
| L | L | 1 channel parallel bridge tied load (PBTL) |
| L | H | 2 channels single ended load (SE) and 1 channel bridge tied load (BTL) |
| H | L | 2 channels bridge tied load (BTL) |
| H | H | 4 channels single ended load (SE) |

Table 3 I2C address decoding (JMP9)

| I2C device address | AD0 | AD1 | 7-bit I2C address |
|--------------------|-----|-----|-------------------|
| 0x20 | L | L | 0b0100000 |
| 0x21 | L | H | 0b0100010 |
| 0x22 | H | L | 0b0100001 |

2.2 Notes to digital audio and analog audio headers

When using the 'Digital Audio Header' for using digital I2S input stream (MA120xxP), the connection scheme should look like as follows (from top to bottom, left side of the header):

- SCK: Word clock; also known as Bit clock
- WS: Word select; also known as left right clock (LRCLK)
- SD0: Multiplexed data line 0 containing two digital input stream channels
- SD1: Multiplexed data line 1 containing two digital input stream channels
- MCLK: Master clock (typically 256 x fs)

When using analog input, the board has been set up to initially evaluate with an unbalanced input source (see 'Analog Audio Header', jumpers connected). However, for full system performance evaluation it is recommended to apply a balanced analog input signal. This can be done by removing the four jumpers from the 'Analog Input Header' and connecting the analog balanced input signal as follows (from top to bottom, left side of the header):

- ch0 input in0a (+)
- ch0 input in0b (-)
- ch1 input in1a (+)
- ch1 input in1b (-)

3 Operating the demonstration board

3.1 Recommended operating conditions

Table 4 Recommended operating conditions

| | Minimum | Nominal | Maximum | Unit |
|---|---------|---------|---------|------|
| PVDD (MA12040/MA12040P) | 5.5 | | 18 | V |
| PVDD (MA12070/MA12070P) | 5.5 | | 26 | V |
| Output peak current (MA12040/MA12040P) | | | 6.0 | A |
| Output peak current (MA12070/MA12070P) | | | 8.0 | A |

3.2 Toggle switches

The board has two toggle switches. The toggle switches have the following functions:

Table 5 Switch function

| | Function |
|----------|---|
| Switch-1 | Shutdown/Enable (default set to “shutdown”) |
| Switch-2 | Mute/Play (default set to “mute”) |

3.3 Speaker load

The demonstration board is configured as a filterless amplifier. This means that no LC filter is placed between the amplifier outputs and the load. In normal use the amplifier relies on the inherent inductance of the loudspeaker and therefore no extra inductance needed.

Inductors for use in series with power resistors are included with the demonstration board. These can be used when making any measurements without a real loudspeaker as the load and having no external low-pass filter in front of the audio analyzer input section.

Please note that many audio measurement analyzers do not perform correctly when connected directly to a filterless amplifier output.

3.4 GUI

The demonstration board is used with GUI PC software to control the MA120xx device. The GUI software is included with the demonstration board and runs on Windows PCs.

Unzip the file package on your PC in your preferred location. See next section for correct startup sequence incl. start of the GUI.

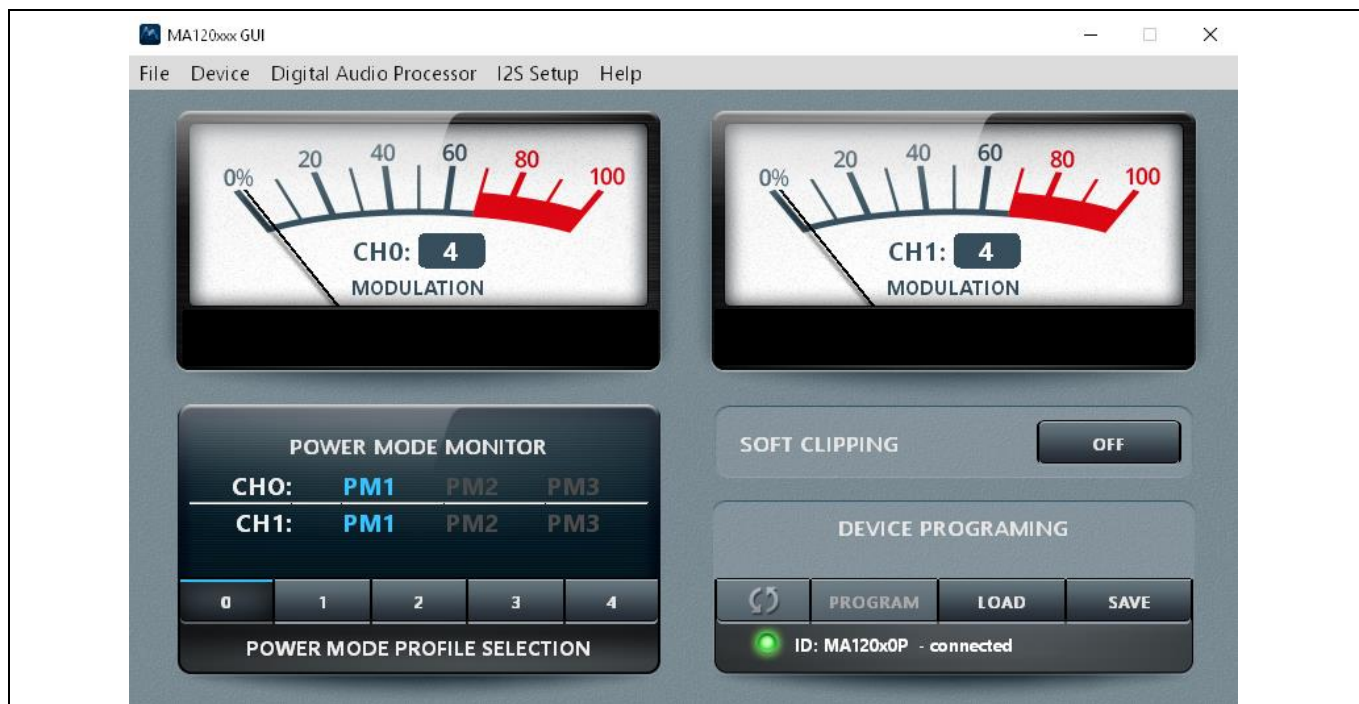


Figure 2 GUI main window

By default the MA12xx/P will automatically select the relevant power mode (PM1, PM2 or PM3), based on detection of audio level during operation. The selected power mode is indicated by a blue color in the power mode indicator.

A set of sliders are available above the power mode indicator. The first slider is used for setting the levels for transitions between PM1 and PM2. When setting the values at higher levels the transition from PM1 to PM2 will occur at a higher output power level. The second slider is used in the same way, for transitions between PM2 and PM3.

Power Mode Profiles can be selected in the “Power Mode Profile Select” section. This gives a specific profile to the amplifier for optimization on low idle power consumption, audio performance or EMI. Please refer to the specific device datasheet for more detailed information on Power Mode Profiles.

The “Digital Audio Processor” button is for digital input (I2S) use and will be discussed in the start-up section for I2S configuration. Note that “Digital Audio Processor” part of the GUI can only be used in combination with MA120xxP devices.

3.5 Start sequence

Important – GUI software revisions: Current GUI software version is 6.5.0. Please note that the current GUI only accepts I2C address 0x20.

3.6 Analog input configuration (MA120xx devices)

Follow this (recommended) sequence to start the evk:

1. Make sure toggle buttons are in “shutdown” and “mute” positions.
2. Connect all cables, including PC by USB cable.
3. Make sure active analog audio source is connected.
4. Turn on the PVDD supply.

Operating the demonstration board

5. Start board by setting toggle switch to “enable” position.
6. Start the GUI software by running the executable file to monitor device status.
7. Make sure the GUI indicates a valid Device ID and connection status (bottom right GUI).
8. Start playing music by setting toggle switch to “play” position.
9. Additional “optimized” settings can be programmed to the device: Hit Load → select config file in configs subfolder → hit program.

Mute and turn off PVDD power supply.

3.7 Digital (I2S) input configuration (MA120xxP devices)

Follow this (recommended) sequence to start the board:

1. Make sure toggle buttons are in “shutdown” and “mute” positions.
2. Connect all cables, including PC by USB cable.
3. Connect I2S connection to the I2S Audio Input header.
4. Make sure that the clock select jumper is set to ‘Slave’ mode.
5. Turn on PVDD power supply.
6. Make sure that the I2S Master Clock is present before for enabling the amplifier.
7. Start board by setting toggle switch to “enable” position.
8. Start the GUI software by running the “MA Device GUI 6.5.0.exe” file.
9. Make sure the GUI indicates a valid Device ID and connection status (bottom right GUI).
10. Open the “Digital Audio Processor” in the GUI.
11. In the DAP window check “Digital audio enable” and “Audio processor enable”.
12. I2S setup window will open when clicking “I2S setup”. The correct I2S settings should be set here.
13. Start playing sound by setting toggle switch to “play” position.
14. Additional “optimized” settings can be programmed to the device: Hit Load → select config file in configs subfolder → hit program.

Mute and turn off PVDD power supply.

User manual for MA evaluation boards

MA12040/MA12040P/MA12070/MA12070P

Operating the demonstration board



Figure 3 Digital audio processing window (top) and I2S setup window (bottom)

4 Measurement methods

Setting up a reliable measurement configuration for MA120xx or MA120xxP takes a little bit more effort than linear amplifiers and even “regular” switching amplifiers. This is mainly because MA120xx and MA120xxP are filterless amplifiers, which means that it does not require an external (usually expensive and bulky) LC filter to remove switching residuals. The filterless application is enabled by MERUS™ Audio multilevel technique, which makes sure that the switching residual is orders lower compared to “regular” switching amplifiers. For more information on the multilevel switching technique, please refer to the datasheet.

To obtain reliable measurement results when measuring MA120xx or MA120xxP devices requires a separate external low-pass filter in front of the input stage of the audio analyzer. Most audio analyzers are bandwidth limited at their input stage, which means that they cannot follow the rapid changes of the amplifiers output stage. This can result in inaccurate and high THD+N measurements.

Figure 4 1 shows the recommended measurement setup. The setup shows a low-pass filter stage (AUX-2500) in front of the audio analyzer (APX-515). In this case the measurement setup has been built around Audio Precision hardware, but this can also be some other audio analyzer hardware. Please note that it is recommended to use both balanced input and output measurement configurations. Note that Figure 4 shows the setup for analog input (MA120xx). To use the setup for digital input (MA120xxP), simply replace the balanced analog input path with the I2S input path.

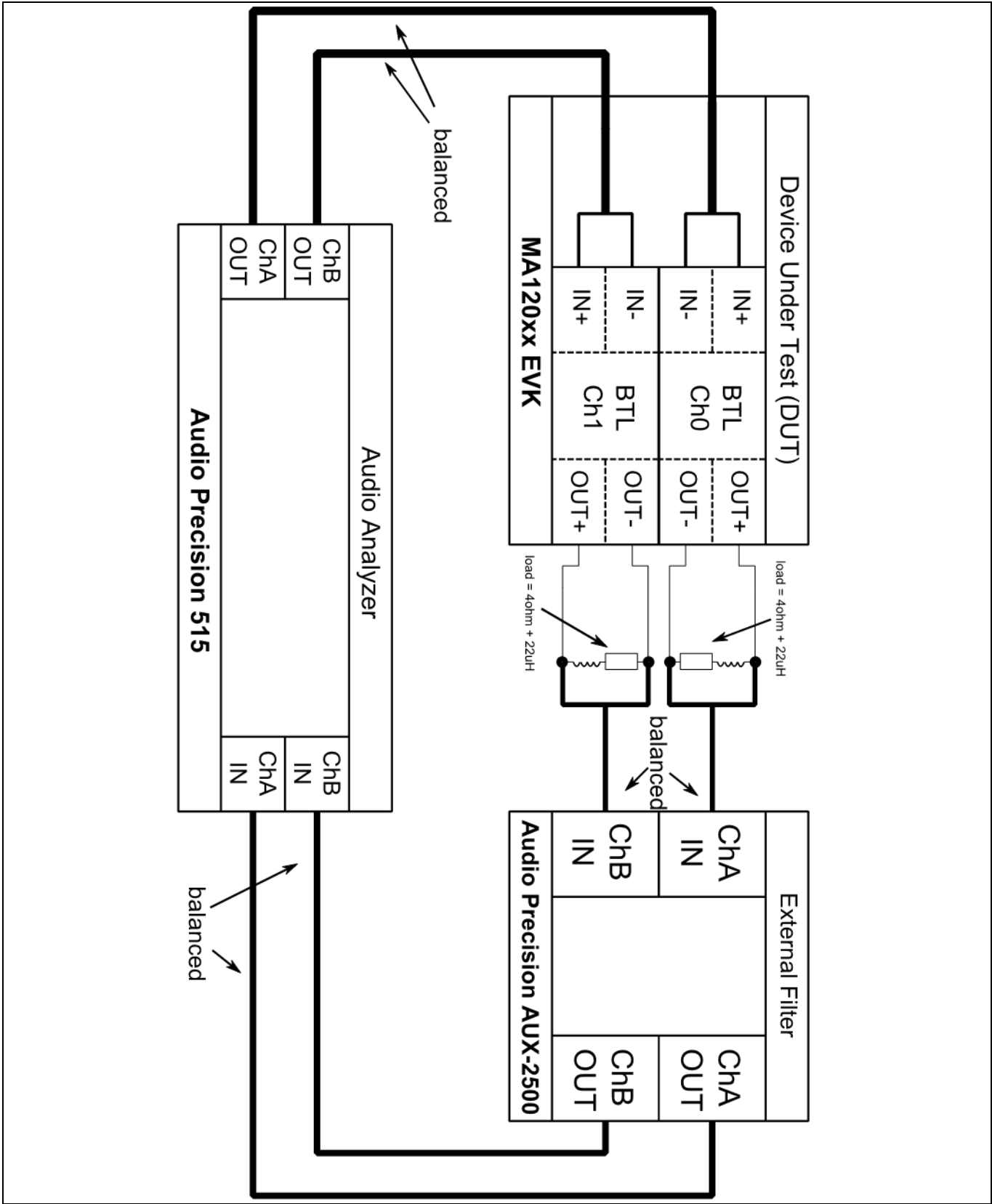


Figure 4 Recommended measurement setup for analog input (MA12040).



EVK schematic

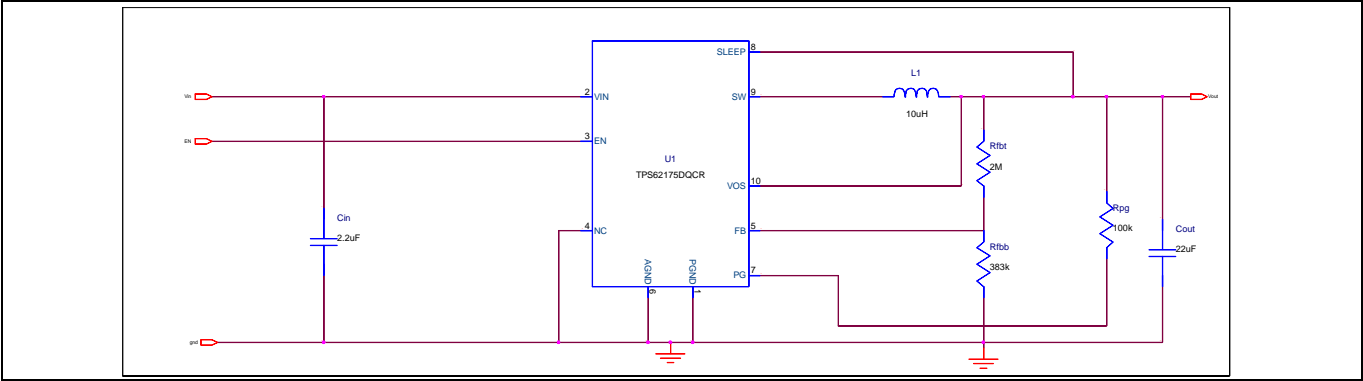


Figure 6 EVK 5 V buck converter schematic

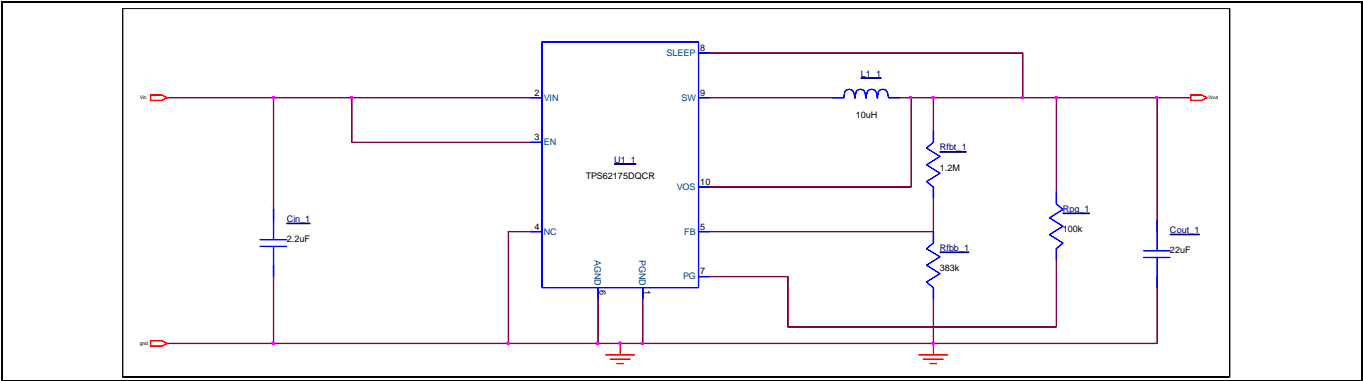


Figure 7 EVK 5 V buck converter schematic

6 Revision history

| Document version | Date of release | Description of changes |
|------------------|-----------------|-------------------------------|
| V 1.0 | 19-07-2018 | Initial release |
| V 1.1 | 18-12-2018 | Updates in content and layout |
| | | |

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