MIC2875

4.8A I$_{SW}$, Synchronous Boost Regulator with Bi-Directional Load Disconnect

General Description

The MIC2875 is a compact and highly-efficient 2MHz synchronous boost regulator with a 4.8A switch. It features a bi-directional load disconnect function which prevents any leakage current between the input and output when the device is disabled. The MIC2875 operates in bypass mode automatically when the input voltage is greater than the target output voltage. At light loads, the boost converter goes to the PFM mode to improve the efficiency.

To minimize switching artifacts in the audio band, the MIC2875 is designed to operate with a minimum switching frequency of 45kHz. The MIC2875 also features an integrated anti-ringing switch to minimize EMI.

The MIC2875 is available in a 8-pin 2mm × 2mm Thin DFN (TDFN) package, with a junction temperature range of −40°C to +125°C.

Datasheets and support documentation are available on Micrel's web site at: www.micrel.com.

Features

- Input voltage range: 2.5V to 5.5V
- Fully-integrated, high-efficiency, 2MHz synchronous boost regulator
- Bi-directional true load disconnect
- Integrated anti-ringing switch
- Minimum switching frequency of 45kHz
- Up to 95% efficiency
- <1µA shutdown current
- Bypass mode for $V_{IN} \geq V_{OUT}$
- Overcurrent protection and thermal shutdown
- Fixed and adjustable output versions
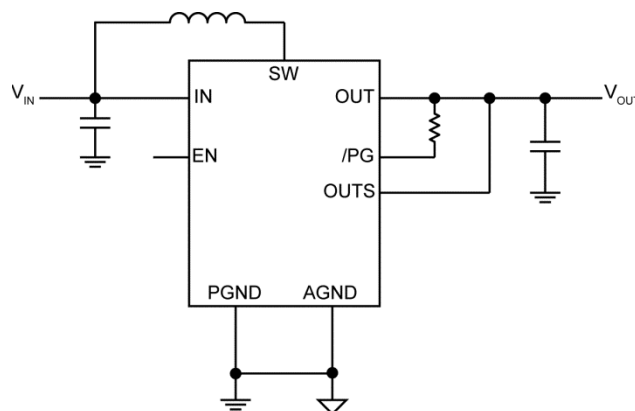- 8-pin 2mm × 2mm TDFN package

Applications

- Tablet and smartphones
- USB OTG and HDMI hosts
- Portable power reserve supplies
- Low-noise audio applications
- Portable equipment

Simplified Application Schematics
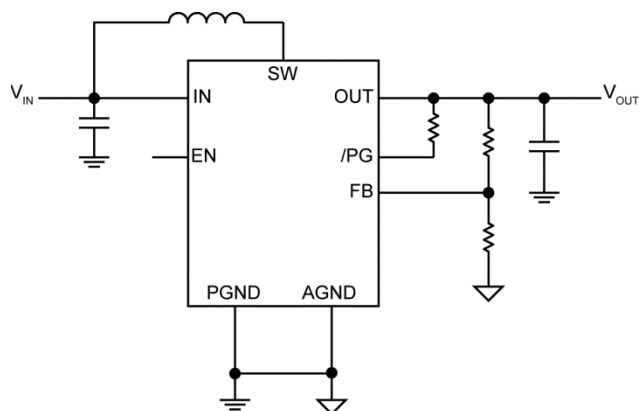
MIC2875 (Adjustable Output)


MIC2875 (Fixed Output)

Ordering Information

| Part Number	Mark Code	Output Voltage	Temperature Range	Package[1, 2]
MIC2875-4.75YMT	87F	4.75V	−40°C to +125°C	8-Pin 2mm × 2mm TDFN
MIC2875-5.0YMT	87G	5.00V	−40°C to +125°C	8-Pin 2mm × 2mm TDFN
MIC2875-5.25YMT	87H	5.25V	−40°C to +125°C	8-Pin 2mm × 2mm TDFN
MIC2875-5.5YMT	87J	5.50V	−40°C to +125°C	8-Pin 2mm × 2mm TDFN
MIC2875-AYMT	87A	Adjustable	−40°C to +125°C	8-Pin 2mm × 2mm TDFN

Notes:

1. TDFN is a RoHS-compliant package. Lead finish is Pb free and Matte Tin. Mold compound is Halogen free.

2. ▲ = TDFN Pin 1 identifier.

Pin Configuration
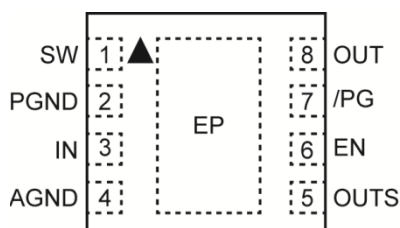
8-Pin 2mm × 2mm TDFN (MT)
Fixed Output
(Top View)
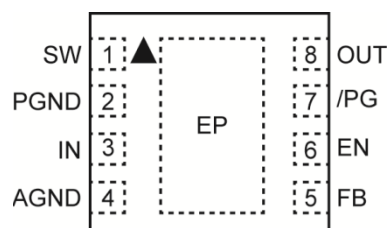
8-Pin 2mm × 2mm TDFN (MT)
Adjustable Output
(Top View)

Pin Description

Pin Number Fixed Output	Pin Number Adjustable Output	Pin Name	Pin Function
1	1	SW	Boost Converter Switch Node: Connect the inductor between IN and SW pins.
2	2	PGND	Power Ground: The power ground for the synchronous boost DC-to-DC converter power stage.
3	3	IN	Supply Input: Connect at least 1µF ceramic capacitor between IN and AGND pins.
4	4	AGND	Analog Ground: The analog ground for the regulator control loop.
5	–	OUTS	Output Voltage Sense Pin: For output voltage regulation in fixed voltage version. Connect to the boost converter output.
–	5	FB	Feedback Pin: For output voltage regulation in adjustable voltage version. Connect to the feedback resistor divider.
6	6	EN	Boost Converter Enable: When this pin is driven low, the IC enters shutdown mode. The EN pin has an internal 2.5MΩ pull-down resistor. The output is disabled when this pin is left floating.

Pin Description (Continued)

Pin Number Fixed Output	Pin Number Adjustable Output	Pin Name	Pin Function
7	7	/PG	Open Drain Power Good Output (Active Low): The /PG pin is high impedance when the output voltage is below the power good threshold, and becomes low once the output is above the power good threshold. The /PG pin has a typical $R_{DS(ON)}$ = 90Ω and requires a pull up resistor of 1MΩ. Connect /PG pin to AGND when the /PG signal is not used.
8	8	OUT	Boost Converter Output.
EP	EP	ePad	Exposed Heat Sink Pad. Connect to AGND for best thermal performance.

Absolute Maximum Ratings[3]

IN, EN, OUT, FB, /PG to PGND .... −0.3V to +6V
AGND to PGND. .... −0.3V to +0.3V
Power Dissipation .... Internally Limited[5]
Lead Temperature (soldering, 10s) .... 260°C
Storage Temperature (T_S) .... −65°C to +150°C
ESD Rating[6]
    Human Body Model 1.5kV
    Machine Model 200V

Operating Ratings[4]

Supply Voltage (V_{IN}) .... +2.5V to +5.5V
Output Voltage (V_{OUT}) .... Up to 5.5V
Enable Voltage (V_{EN}) .... 0V to V_{IN}
Junction Temperature (T_J) .... −40°C to +125°C
Package Thermal Resistance
    8-Pin 2mm × 2mm TDFN (θ_{JA}) .... 90°C/W

Electrical Characteristics[7]

V_{IN} = 3.6V, V_{OUT} = 5V, C_{IN} = 4.7µF, C_{OUT} = 22µF, L = 1µH T_A = 25°C, **bold** values indicate −40°C ≤ T_J ≤ +125°C, unless otherwise noted.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Power Supply						
V_{IN}	Supply Voltage Range		**2.5**		**5.5**	V
V_{UVLOR}	UVLO Rising Threshold			2.32	**2.49**	V
V_{UVLOH}	UVLO Hysteresis			200		mV
I_{VIN}	Quiescent Current	Operating at minimum switching frequency		1		mA
I_{VINSD}	V_{IN} Shutdown Current	V_{EN} = 0V, V_{IN} = 5.5V, V_{OUT} = 0V		1	**3**	µA
I_{VOUTSD}	V_{OUT} Shutdown Current	V_{EN} = 0V, V_{IN} = 0.3V, V_{OUT} = 5.5V		2	**5**	µA
V_{OUT}	Output Voltage		V_{IN}		5.5	V
V_{FB}	Feedback Voltage	Adjustable version, I_{OUT} = 0A	**0.8865**	0.9	**0.9135**	V
	Voltage Accuracy	Fixed version, I_{OUT} = 0A	**−1.5**		**+1.5**	%
	Line Regulation	2.5V < V_{IN} < 4.5V, I_{OUT} = 500mA		0.3		%/V
	Load Regulation	I_{OUT} = 200mA to 1200mA		0.2		%/A
D_{MAX}	Maximum Duty Cycle			92		%
D_{MIN}	Minimum Duty Cycle			6.5		%
I_{LS}	Low-Side Switch Current Limit[8]	V_{IN} = 2.5V	**3.8**	4.8	**5.8**	A
PMOS	Switch On-Resistance	V_{IN} = 3.0V, I_{SW} = 200mA, V_{OUT} = 5.0V		79		mΩ
NMOS		V_{IN} = 3.0V, I_{SW} = 200mA, V_{OUT} = 5.0V		82		
I_{SW}	Switch Leakage Current[8]	V_{EN} = 0V, V_{IN} = 5.5V		0.2	**5**	µA
F_{SWMIN}	Minimum Switching Frequency	I_{OUT} = 0mA		45		kHz
F_{OSC}	Oscillator Frequency		**1.6**	2	**2.4**	MHz
T_{SD}	Overtemperature Shutdown Threshold			155		°C
	Overtemperature Shutdown Hysteresis			15		

Notes:

3. Exceeding the absolute maximum ratings may damage the device.

4. The device is not guaranteed to function outside its operating ratings.

5. The maximum allowable power dissipation of any T_A (ambient temperature) is $P_{D(max)} = (T_{J(max)} − T_A) / \theta_{JA}$. Exceeding the maximum allowable power dissipation will result in excessive die temperature, and the regulator will go into thermal shutdown

6. Devices are ESD sensitive. Handling precautions are recommended. Human body model, 1.5kΩ in series with 100pF.

7. Specification for packaged product only.

8. Guaranteed by design and characterization.

Electrical Characteristics[7] (Continued)

V_{IN} = 3.6V, V_{OUT} = 5V, C_{IN} = 4.7µF, C_{OUT} = 22µF, L = 1µH T_A = 25°C, **bold** values indicate −40°C ≤ T_J ≤ +125°C, unless otherwise noted.

| Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Soft-Start						
T_{SS}	Soft-Start Time	V_{OUT} = 5.0V		1.1		ms
EN, /PG Control Pins						
V_{EN}	EN Threshold Voltage	Boost converter and chip logic ON	**1.5**			V
		Boost converter and chip logic OFF			**0.4**	
	EN Pin Current	V_{IN} = V_{EN} = 3.6V		1.5	**3**	µA
$V_{/PG-THR}$	Power-Good Thershold (Rising)			0.90 × V_{OUT}		V
$V_{/PG-THF}$	Power-Good Thershold (Falling)			0.83 × V_{OUT}		V

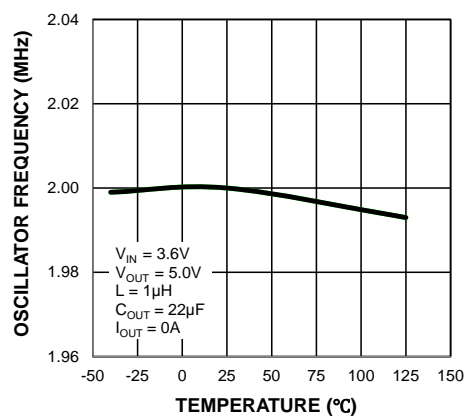# Typical Characteristics

**Efficiency
vs. Load Current**
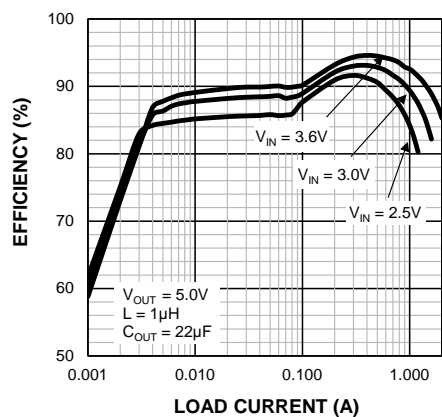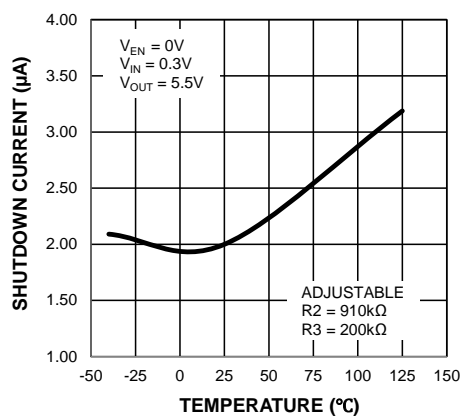

**Output Voltage
vs. Load Current**
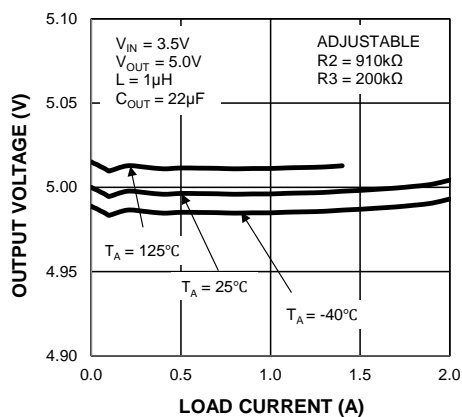
**Output Voltage
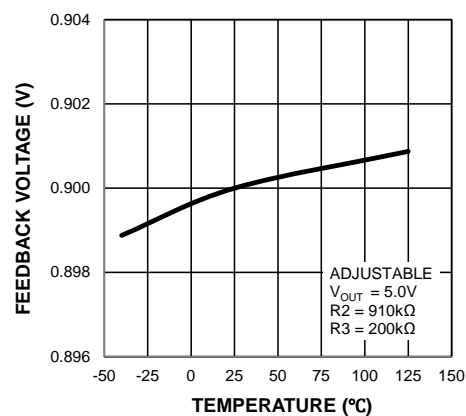vs. Input Voltage**
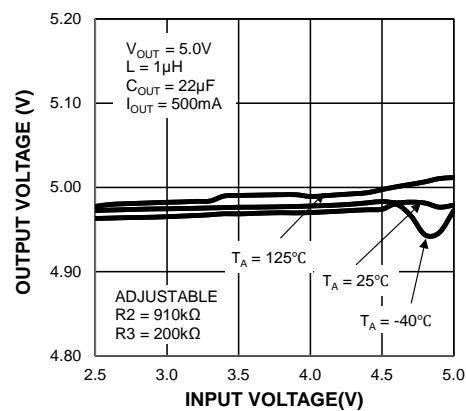
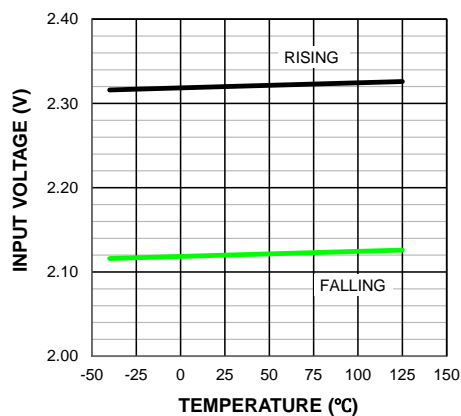**Oscillator Frequency
vs. Temperature**

**Output Shutdown Current
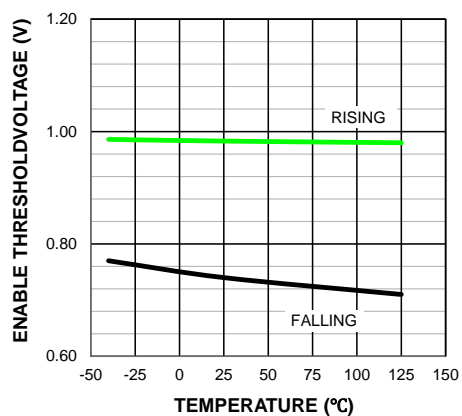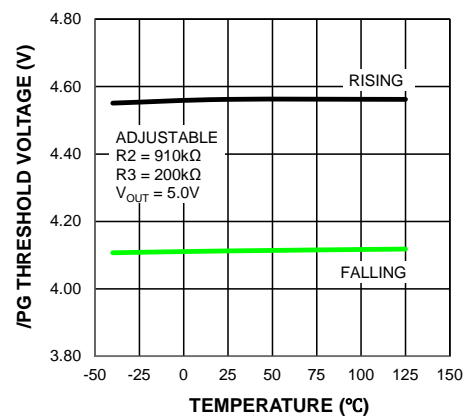vs. Temperature**

**Feedback Voltage
vs. Temperature**

**UVLO Threshold
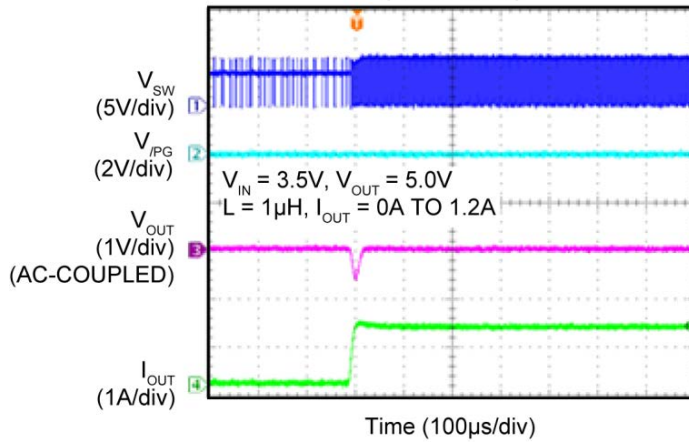vs. Temperature**

**Enable Threshold
vs. Temperature**

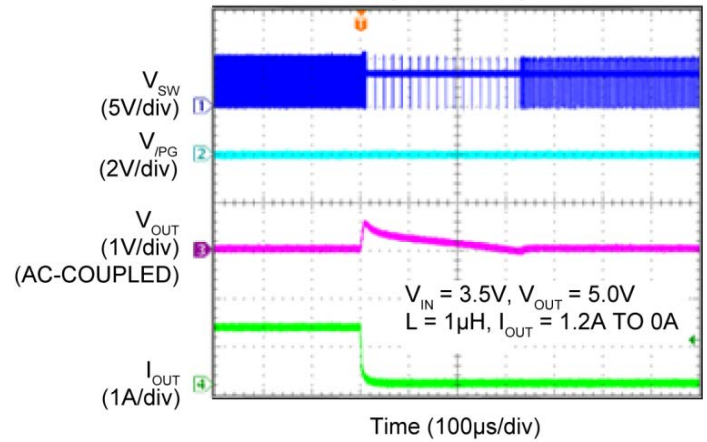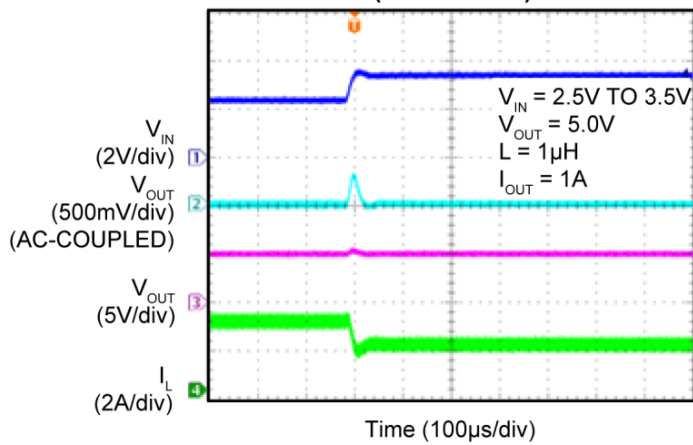**Power Good Threshold
vs. Temperature**

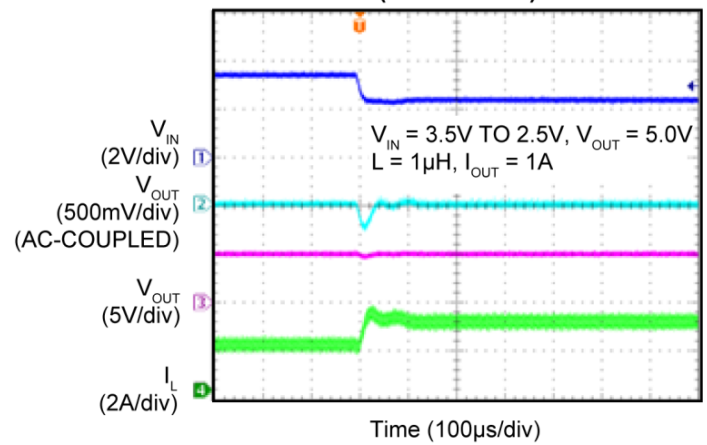# Functional Characteristics

Load Transient
(0A to 1.2A)

V_{SW}
(5V/div)

$V_{/PG}$
(2V/div)

V_{IN} = 3.5V, V_{OUT} = 5.0V
L = 1µH, I_{OUT} = 0A TO 1.2A

V_{OUT}
(1V/div)
(AC-COUPLED)

I_{OUT}
(1A/div)

Time (100µs/div)

Load Transient
(1.2A to 0A)

V_{SW}
(5V/div)

$V_{/PG}$
(2V/div)

V_{OUT}
(1V/div)
(AC-COUPLED)

V_{IN} = 3.5V, V_{OUT} = 5.0V
L = 1µH, I_{OUT} = 1.2A TO 0A

I_{OUT}
(1A/div)

Time (100µs/div)

Line Transient
(2.5V to 3.5V)

V_{IN} = 2.5V TO 3.5V
V_{OUT} = 5.0V
L = 1µH
I_{OUT} = 1A

V_{IN}
(2V/div)
V_{OUT}
(500mV/div)
(AC-COUPLED)

V_{OUT}
(5V/div)

I_{L}
(2A/div)

Time (100µs/div)

Line Transient
(3.5V to 2.5V)

V_{IN} = 3.5V TO 2.5V, V_{OUT} = 5.0V
L = 1µH, I_{OUT} = 1A

V_{IN}
(2V/div)
V_{OUT}
(500mV/div)
(AC-COUPLED)

V_{OUT}
(5V/div)

I_{L}
(2A/div)

Time (100µs/div)

Line Transient
(2.5V to 5.5V)

V_{IN} = 2.5V TO 5.5V
V_{OUT} = 5.0V
L = 1µH
I_{OUT} = 1A

V_{IN}
(2V/div)
V_{OUT}
(2V/div)
(AC-COUPLED)

V_{OUT}
(5V/div)

I_{L}
(5A/div)

Time (100µs/div)
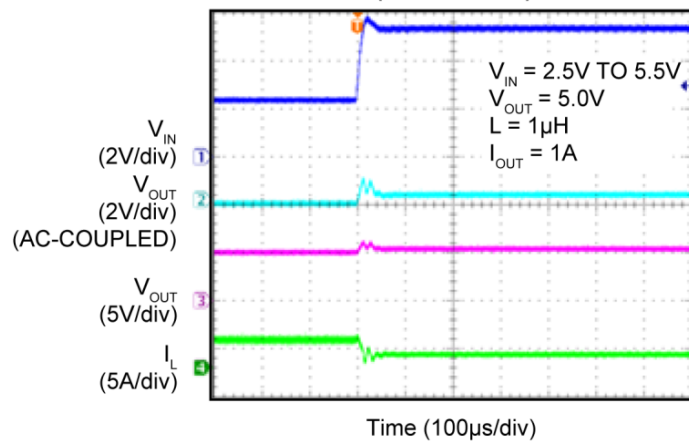
Line Transient
(5.5V to 2.5V)

V_{IN} = 5.5V TO 2.5V
V_{OUT} = 5.0V, L = 1µH
I_{OUT} = 1A

V_{IN}
(2V/div)
V_{OUT}
(2V/div)
(AC-COUPLED)

V_{OUT}
(5V/div)

I_{L}
(5A/div)

Time (100µs/div)

Functional Characteristics (Continued)

**Output Ripple
(Pulse Skipping Mode)**

V$_{SW}$
(2V/div)

V$_{OUT}$
(50mV/div)
(AC-COUPLED)

PULSE SKIPPING MODE
V$_{IN}$ = 3.5V, V$_{OUT}$ = 5.0V, I$_{OUT}$ = 50mA

I$_L$
(200mA/div)

Time (4µs/div)

**Output Ripple
(PWM Mode)**

V$_{SW}$
(5V/div)

V$_{OUT}$
(50mV/div)
(AC-COUPLED)

PWM MODE
V$_{IN}$ = 3.5V, V$_{OUT}$ = 5.0V, I$_{OUT}$ = 1.2A

I$_L$
(1A/div)

Time (200ns/div)

**Soft-Start
(Boost Mode)**

V$_{EN}$
(2V/div)

BOOST MODE
V$_{IN}$ = 3.5V
V$_{OUT}$ = 5.0V
I$_{OUT}$ = 500mA

V$_{/PG}$
(2V/div)

V$_{OUT}$
(5V/div)

I$_L$
(1A/div)

Time (400µs/div)

**Soft-Start
(Bypass Mode)**

V$_{EN}$
(2V/div)

BYPASS MODE
V$_{IN}$ = 5.5V
V$_{OUT}$ = 5.0V
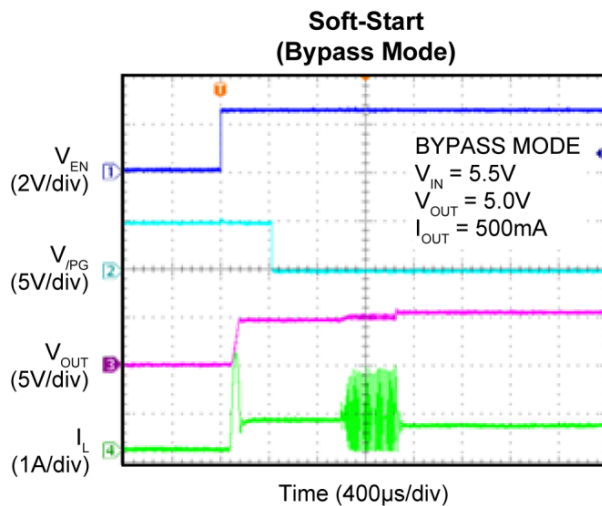I$_{OUT}$ = 500mA

V$_{/PG}$
(5V/div)

V$_{OUT}$
(5V/div)

I$_L$
(1A/div)

Time (400µs/div)

Minimum Switching

V$_{SW}$
(2V/div)

V$_{IN}$ = 3.5V, F$_{SWMIN}$ = 45kHz, I$_{OUT}$ = 0A

I$_L$
(200mA/div)

Time (20µs/div)

**Minimum Switching
(Zoom-In)**

V$_{SW}$
(2V/div)

V$_{IN}$ = 3.5V
F$_{SWMIN}$ = 45kHz
I$_{OUT}$ = 0A

I$_L$
(200mA/div)

Time (400ns/div)

Functional Characteristics (Continued)

Bypass Mode

V_{OUT} = 5.0V | V_{OUT} = 5.0V

V_{OUT} (1V/div)

BYPASS MODE – V_{IN} > 5.0V
V_{OUT} = V_{IN}

V_{IN} (1V/div)

I_{OUT} = 0A

Time (1s/div)

Bypass Mode

V_{OUT} = 5.0V | V_{OUT} = 5.0V

V_{OUT} (1V/div)

BYPASS MODE – V_{IN} > 5.0V
V_{OUT} = V_{IN}

V_{IN} (1V/div)

I_{OUT} = 500mA

Time (1s/div)

Functional Diagram
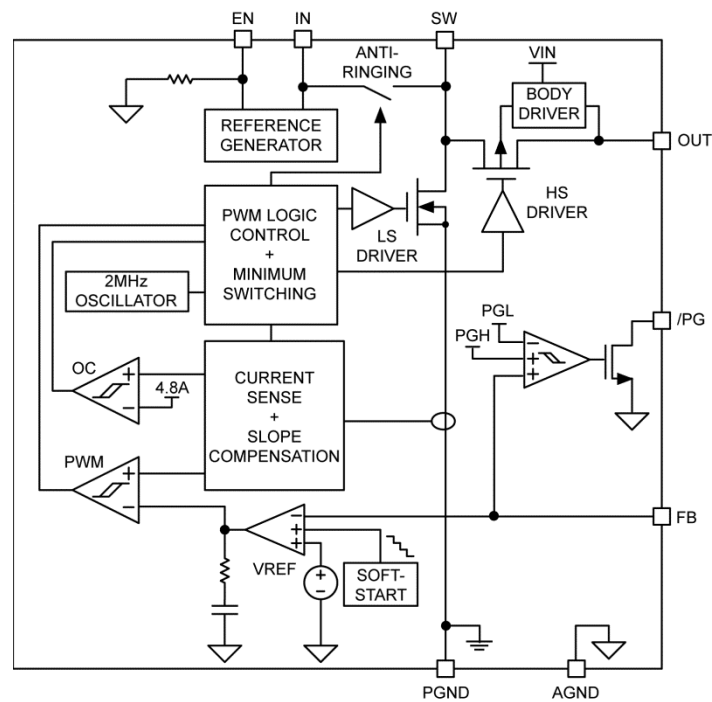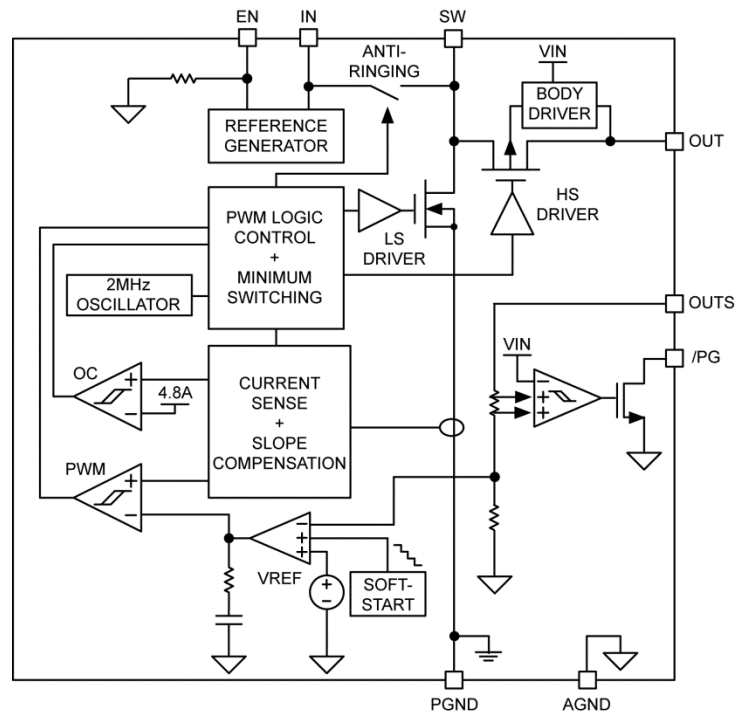

Simplified Adjustable Output

Simplified Fixed Output

Functional Description

Input (IN)

The input supply provides power to the internal MOSFETs gate drivers and control circuitry for the boost regulator. The operating input voltage range is from 2.5V to 5.5V. A 1µF low-ESR ceramic input capacitor should be connected from IN to AGND as close to MIC2875 as possible to ensure a clean supply voltage for the device. A minimum voltage rating of 10V is recommended for the input capacitor.

Switch Node (SW)

The MIC2875 has internal low-side and synchronous MOSFET switches. The switch node (SW) between the internal MOSFET switches connects directly to one end of the inductor and provides the current path during switching cycles. The other end of the inductor is connected to the input supply voltage. Due to the high-speed switching on this pin, the switch node should be routed away from sensitive nodes wherever possible.

Ground Path (AGND)

The ground path (AGND) is for the internal biasing and control circuitry. AGND should be connected to the PCB pad for the package exposed pad. The current loop of the analog ground should be separated from that of the power ground (PGND). AGND should be connected to PGND and EP at a single point.

Power Ground (PGND)

The power ground (PGND) is the ground path for the high current in the boost switches. The current loop for the power ground should be as short as possible and separate from the AGND loop as applicable.

Boost Converter Output (OUT)

A low-ESR ceramic capacitor of 22µF (for operation with $V_{IN} \leq 5.0V$), or 66µF (for operation with $V_{IN} > 5.0V$) should be connected from VOUT to PGND as close as possible to the MIC2875. A minimum voltage rating of 10V is recommended for the output capacitor.

Enable (EN)

Enable pin of the MIC2875. A logic high on this pin enables the MIC2875. When this pin is driven low, the MIC2875 enters the shutdown mode. When the EN pin is left floating, it is pulled-down internally by a built-in 2.5MΩ resistor.

Feedback/Output Voltage Sense (FB/OUTS)

Feedback or output voltage sense pin for the boost converter. For the fixed voltage version, this pin should be connected to the OUT pin. For the adjustable version, connect a resistor divider to set the output voltage (see "Output Voltage Programming" for more information).

Power-Good Output (/PG)

The open-drain active-low power-good output (/PG) is low when the output voltage is above the power-good threshold. A pull-up resistor of 1MΩ is recommended.

Exposed Heat Sink Pad (EP)

The exposed heat sink pad, or ePad (EP), should be connected to AGND for best thermal performance.

Application Information

General Description

The MIC2875 is a 2MHz, current-mode, PWM, synchronous boost converter with an operating input voltage range of 2.5V to 5.5V. At light load, the converter enters pulse-skipping mode to maintain high efficiency over a wide range of load current. The maximum peak current in the boost switch is limited to 4.8A (typical).

Bi-Directional Output Disconnect

The power stage of the MIC2875 consists of a NMOS transistor as the main switch and a PMOS transistor as the synchronous rectifier. A control circuit turns off the back gate diode of the PMOS to isolate the output from the input supply when the chip is disabled (V_{EN} = 0V). An "always on" maximum supply selector switches the cathode of the back gate diode to either the IN or the OUT (whichever of the two has the higher voltage). As a result, the output of the MIC2875 is bi-directionally isolated from the input as long as the device is disabled. The maximum supply selector and hence the output disconnect function requires only 0.3V at the IN pin to operate.

Minimum Switching Frequency

When the MIC2875 enters the pulse-skipping mode for more than 20µs, an internal control circuitry forces the PMOS to turn on briefly to discharge V_{OUT} to V_{IN} through the inductor. When the inductor current reaches a predetermined threshold, the PMOS is turned off and the NMOS is turned on so that the inductor current can decrease gradually. Once the inductor current reaches zero, the NMOS is eventually turned off. The above cycle repeats if there is no switching activity for another 20µs, effectively maintaining a minimum switching frequency of 45 kHz. The frequency control circuit is disabled when V_{OUT} is less than or within 200mV of V_{IN}. This minimum switching frequency feature is advantageous for applications that are sensitive to low-frequency EMI, such as audio systems.

Integrated Anti-Ringing Switch

The MIC2875 includes an anti-ringing switch that eliminates the ringing on the SW node of a conventional boost converter operating in the discontinuous conduction mode (DCM). At the end of a switching cycle during DCM operation, both the NMOS and PMOS are turned off. The anti-ringing switch in the MIC2875 clamps the SW pin voltage to IN to dissipate the remaining energy stored in the inductor and the parasitic elements of the power switches.

Automatic Bypass Mode (when V_{IN} > V_{OUT})

The MIC2875 automatically operates in bypass mode when the input voltage is higher than the target output voltage. In bypass mode, the NMOS is turned off while the PMOS is fully turned-on to provide a very low impedance path from IN to OUT.

Soft-Start

The MIC2875 integrates an internal soft-start circuit to limit the inrush current during start-up. When the device is enabled, the PMOS is turned-on slowly to charge the output capacitor to a voltage close to the input voltage. Then, the device begins boost switching cycles to gradually charge up the output voltage to the target VOUT.

Output Voltage Programming

The MIC2875 has an adjustable version that allows the output voltage to be set by an external resistor divider R2 and R3. The typical feedback voltage is 900mV, the recommended maximum and minimum output voltage is 5.5V and 3.2V, respectively. The current through the resistor divider should be significantly larger than the current into the FB pin (typically 0.01µA). It is recommended that the total resistance of R2 + R3 should be around 1MΩ. The appropriate R2 and R3 values for the desired output voltage are calculated as in Equation 1:

$$R2 = R3 \times \left(\frac{V_{OUT}}{0.9V} - 1 \right) \qquad \textbf{Eq. 1}$$

Component Selection

Inductor

Inductor selection is a trade-off between efficiency, stability, cost, size, and rated current. Since the boost converter is compensated internally, the recommended inductance is limited from 1µH to 2.2µH to ensure system stability and presents a good balance between these considerations.

A large inductance value reduces the peak-to-peak inductor ripple current hence the output ripple voltage. This also reduces both the DC loss and the transition loss at the same inductor's DC resistance (DCR). However, the DCR of an inductor usually increases with the inductance in the same package size. This is due to the longer windings required for an increase in inductance. Since the majority of the input current passes through the inductor, the higher the DCR the lower the efficiency is, and more significantly at higher load currents. On the other hand, inductor with smaller DCR but the same inductance usually has a larger size. The saturation current rating of the selected inductor must be higher than the maximum peak inductor current to be encountered and should be at least 20% to 30% higher than the average inductor current at maximum output current.

Input Capacitor to the Device Supply

A ceramic capacitor of 1µF or larger with low ESR is recommended to reduce the input voltage ripple to ensure a clean supply voltage for the device. The input capacitor should be placed as close as possible to the MIC2875 IN pin and AGND pin with short traces to ensure good noise performance. X5R or X7R type ceramic capacitors are recommended for better tolerance over temperature. The Y5V and Z5U type temperature rating ceramic capacitors are not recommended due to their large reduction in capacitance over temperature and increased resistance at high frequencies. The use of these reduces the ability to filter out high-frequency noise. The rated voltage of the input capacitor should be at least 20% higher than the maximum operating input voltage over the operating temperature range.

Input Capacitor to the Power Path

A ceramic capacitor of a 4.7µF of larger with low ESR is recommended to reduce the input voltage fluctuation at the voltage supply of the high current power path. An input capacitor should be placed close to the V_{IN} supply to the power inductor and PGND for good device performance at heavy load condition. X5R or X7R type ceramic capacitors are recommended for better tolerance overtemperature.

The Y5V and Z5U type temperature rating ceramic capacitors are not recommended due to their large reduction in capacitance over temperature and increased resistance at high frequencies. These reduce their ability to filter out high-frequency noise. The rated voltage of the input capacitor should be at least 20% higher than the maximum operating input voltage over the operating temperature range.

Output Capacitor

Output capacitor selection is also a trade-off between performance, size, and cost. Increasing output capacitor will lead to an improved transient response, however, the size and cost also increase. For operation with $V_{IN} \leq 5.0V$, a minimum of 22µF output capacitor with ESR less than 10mΩ is required. For operation with $V_{IN} > 5.0V$, a minimum of 66µF output capacitor with ESR less than 10mΩ is required. X5R or X7R type ceramic capacitors are recommended for better tolerance over temperature. Additional capacitors can be added to improve the transient response, and to reduce the ripple of the output when the MIC2875 operates in and out of bypass mode.

The Y5V and Z5U type ceramic capacitors are not recommended due to their wide variation in capacitance over temperature and increased resistance at high frequencies. The rated voltage of the output capacitor should be at least 20% higher than the maximum operating output voltage over the operating temperature range. 0805 size ceramic capacitor is recommended for smaller ESL at output capacitor which contributes smaller voltage spike at the output voltage of high-frequency switching boost converter.

Power Dissipation

As with all power devices, the ultimate current rating of the output is limited by the thermal properties of the device package and the PCB on which the device is mounted. There is a simple, Ohm's law-type relationship between thermal resistance, power dissipation, and temperature which are analogous to an electrical circuit (Figure 1):
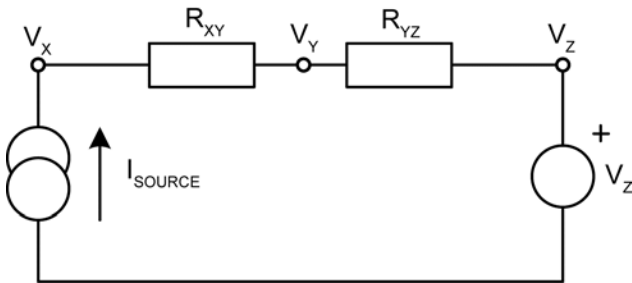

Figure 1. Series Electrical Resistance Circuit

From this simple circuit we can calculate V_X if we know I_{SOURCE}, V_Z and the resistor values, R_{XY} and R_{YZ} using Equation 2:

$$V_X = I_{SOURCE} \times (R_{XY} + R_{YZ}) + V_Z \qquad \textbf{Eq. 2}$$

Thermal circuits can be considered using this same rule and can be drawn similarly by replacing current sources with power dissipation (in watts), resistance with thermal resistance (in °C/W) and voltage sources with temperature (in °C).
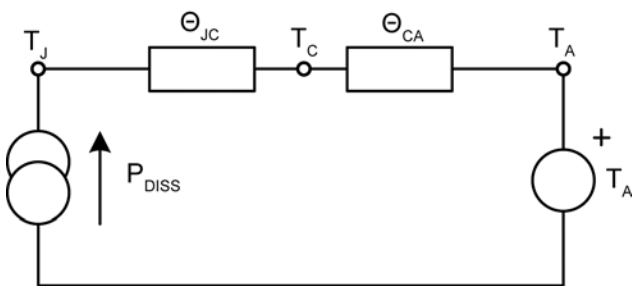

Figure 2. Series Thermal Resistance Circuit

Now replacing the variables in the equation for V_X, we can find the junction temperature (T_J) from the power dissipation, ambient temperature and the known thermal resistance of the PCB (θ_{CA}) and the package (θ_{JC}).

$$T_J = P_{DISS} \times (\theta_{JC} + \theta_{CA}) + T_A \qquad \textbf{Eq. 3}$$

As can be seen in the diagram, total thermal resistance $\theta_{JA} = \theta_{JC} + \theta_{CA}$. This can also be written as in Equation 4:

$$T_J + P_{DISS} \times (\theta_{JA}) + T_A \qquad \textbf{Eq. 4}$$

Given that all of the power losses (minus the inductor losses) are effectively in the converter are dissipated within the MIC2875 package, P_{DISS} can be calculated thusly:

Linear Mode: $P_{DISS} = \left[P_{OUT} \times \left(\dfrac{1}{\eta} - 1 \right) \right] - I_{OUT}^2 \times DCR$

$$\textbf{Eq. 5}$$

Boost Mode: $P_{DISS} = \left[P_{OUT} \times \left(\dfrac{1}{\eta} - 1 \right) \right] - \left(\dfrac{I_{OUT}}{1-D} \right)^2 \times DCR$

$$\textbf{Eq. 6}$$

Duty Cycle (Boost Mode): $D + \dfrac{V_{OUT} - V_{IN}}{V_{OUT}}$ **Eq. 7**

where:

η = Efficiency taken from efficiency curves and DCR = inductor DCR. θ_{JC} and θ_{JA} are found in the operating ratings section of the datasheet.

Where the real board area differs from 1" square, θ_{CA} (the PCB thermal resistance), values for various PCB copper areas can be taken from Figure 3. (**Note**: Figure 3 taken from *Designing with Low Dropout Voltage Regulators* available from Micrel's web site at: www.micrel.com.)

PC Board Heat Sink Thermal Resistance vs. Area
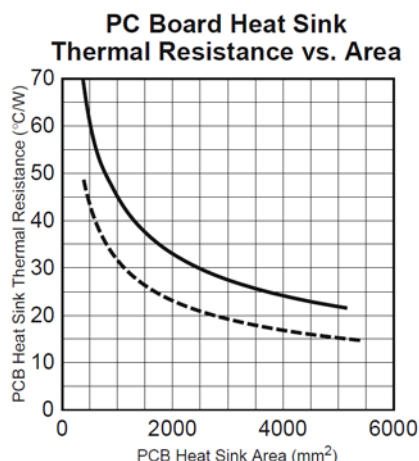
Figure 3. Determining PC Board Area for a Given PCB Thermal Resistance

Figure 3 shows the total area of a round or square pad, centered on the device. The solid trace represents the area of a square, single-sided, horizontal, solder-masked, copper PC board trace heat sink, measured in square millimeters. No airflow is assumed. The dashed line shows PC boards trace heat sink covered in black oil-based paint and with 1.3m/sec (250 feet per minute) airflow. This approaches a "best case" pad heat sink. Conservative design dictates using the solid trace data, which indicates that a maximum pad size of 5000 mm^2 is needed. This is a pad 71mm × 71mm (2.8 inches per side).

PCB Layout Guidelines

PCB layout is critical to achieve reliable, stable and efficient performance. A ground plane is required to control EMI and minimize the inductance in power, signal and return paths. The following guidelines should be followed to ensure proper operation of the device:

IC (Integrated Circuit)

- Place the IC close to the point-of-load.

- Use fat traces to route the input and output power lines.

- Analog grounds and power ground should be kept separate and connected at a single location at the PCB pad for exposed pad of the IC.

- Place as much as thermal vias on the PCB pad for exposed pad and connected it to the ground plane to ensure a good PCB thermal resistance can be achieved.

IN Decoupling Capacitor

- The IN decoupling capacitor must be placed close to the IN pin of the IC and preferably connected directly to the pin and not through any via. The capacitor must be located right at the IC.

- The IN decoupling capacitor should be connected as close as possible to AGND.

- The IN terminal is noise sensitive and the placement of capacitor is very critical.

VIN Power Path Bulk Capacitor

- The V_{IN} power path bulk capacitor should be placed and connected close to the V_{IN} supply to the power inductor and the PGND of the IC.

- Use either X5R or X7R temperature rating ceramic capacitors. Do not use Y5V or Z5U type ceramic capacitors.

Inductor

- Keep both the inductor connections to the switch node (SW) and input power line short and wide enough to handle the switching current. Keep the areas of the switching current loops small to minimize the EMI problem.

- Do not route any digital lines underneath or close to the inductor.

- Keep the switch node (SW) away from the noise sensitive pins.

- To minimize noise, place a ground plane underneath the inductor.

Output Capacitor

- Use wide and short traces to connect the output capacitor as close as possible to the OUT and PGND pins without going through via holes to minimize the switching current loop during the main switch off cycle and the switching noise.

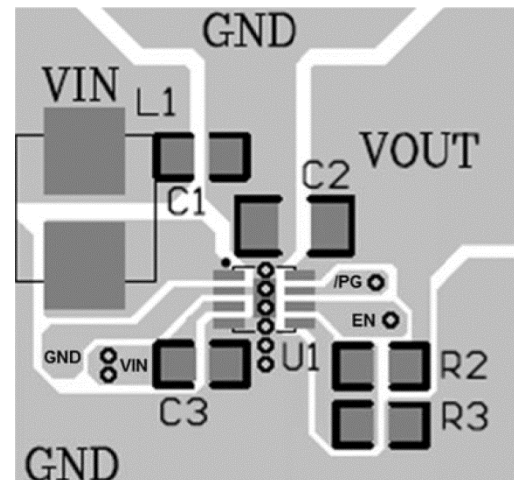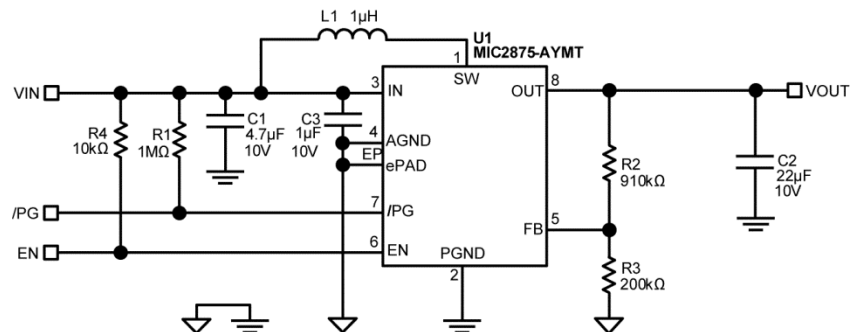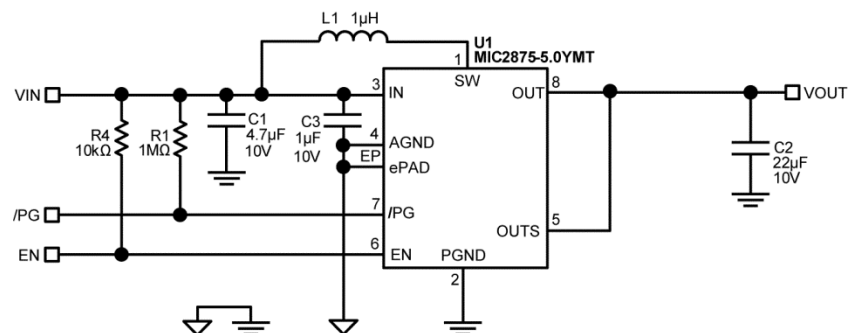- Use either X5R or X7R temperature rating ceramic capacitors. Do not use Y5V or Z5U type ceramic capacitors.
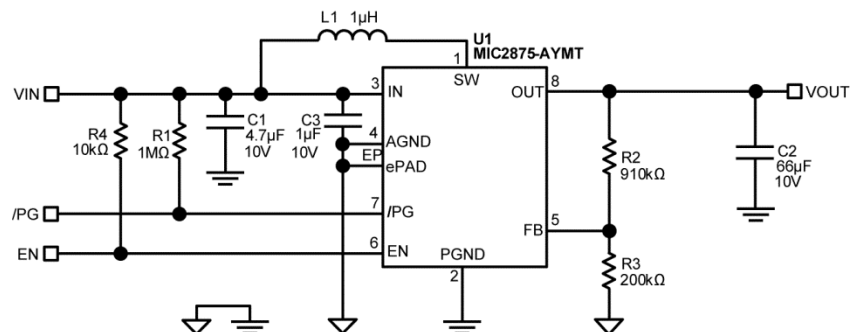

Figure 4. Suggested PCB Routing

Typical Application Schematics
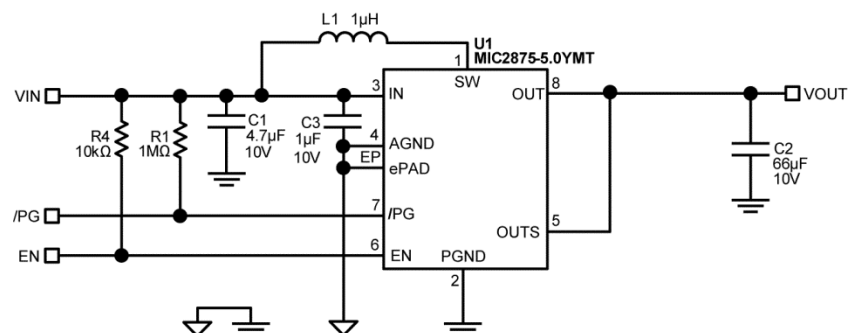

MIC2875-AYMT Typical Application Schematic – V$_{IN}$ ≤ 5.0V

MIC2875-5.0YMT Typical Application Schematic – V$_{IN}$ ≤ 5.0V

MIC2875-AYMT Typical Application Schematic – V$_{IN}$ > 5.0V

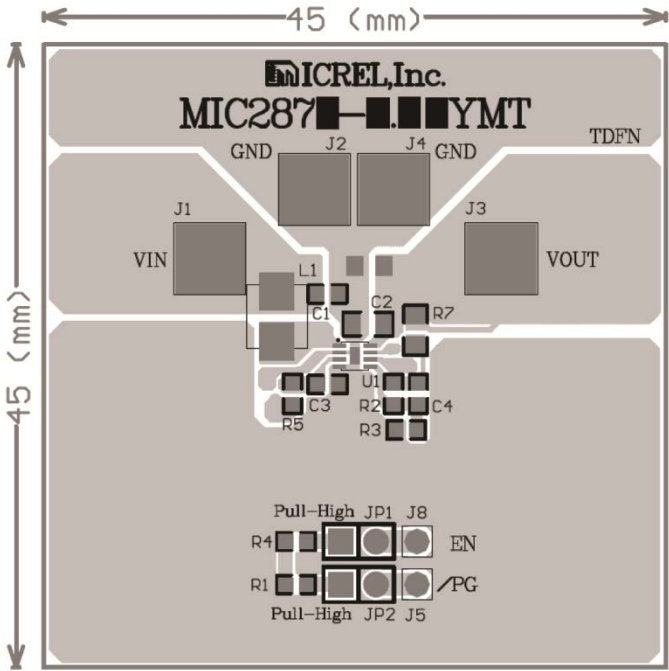**MIC2875-5.0YMT Typical Application Schematic – V$_{IN}$ > 5.0V**

Bill of Materials

Item	Part Number	Manufacturer	Description	Qty.
C1	C1608X5R1A475K080AC	TDK[9]	Capacitor 4.7µF, 10V, 10%, X5R, 0603	1
C2	LMK212BJ226MG-T	Taiyo Yuden[10]	Capacitor 22µF, 10V, 20%, X5R, 0805 ($V_{IN} \leq 5.00V$)	1
			Capacitor 22µF, 10V, 20%, X5R, 0805 ($V_{IN} > 5.00V$, in parallel)	3
C3	GRM188R61A105KA61J	Murata[11]	Capacitor 1µF, 10V, 10%, X5R, 0603	1
L1	PIMB042T-1R0MS-39	Cyntec[12]	Inductor 1µH, 4.5A, SMD, 4.2mm × 4.0mm × 1.8mm	1
R1	ERJ-3GEYJ105V	Panasonic[13]	Resistor 1MΩ, 5%, 0603	1
R2	1-1879417-8	TE[14]	Resistor 910kΩ, 0.1%, 0603	1
R3	ERA-3AEB204V	Panasonic	Resistor 200kΩ, 0.1%, 0603	1
R4	ERJ-3GEYJ103V	Panasonic	Resistor 10kΩ, 5%, 0603	1
UI	**MIC2875-xxxYMT**	**Micrel, Inc.[15]**	**4.8A I_{SW}, Synchronous Boost Regulator with Bi-Directional Load Disconnect**	1

Notes:

9. TDK: www.tdk.com.

10. Taiyo Yuden: www.t-yuden.com.

11. Murata: www.murata.com.

12. Cyntec: www.cyntec.com.

13. Panasonic: www.panasonic.com.

14. TE: www.te.com.

15. Micrel, Inc.: www.micrel.com.

PCB Layout Recommendations

Top Layer
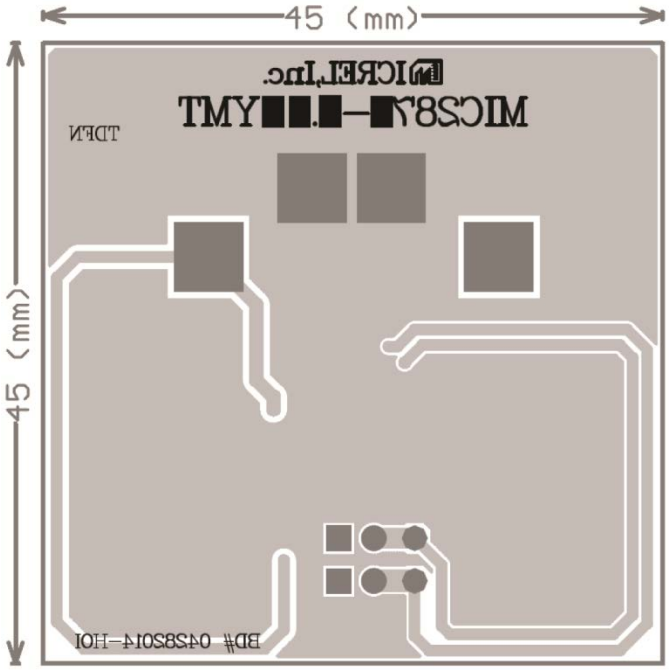
Bottom Layer

Package Information and Recommended Landing Pattern[16]

TOP VIEW
NOTE: 1, 2, 3

BOTTOM VIEW
NOTE: 1, 2, 3

END VIEW
NOTE: 1, 2, 3

RECOMMENDED LAND PATTERN
NOTE: 4, 5

NOTE:
1. MAX PACKAGE WARPAGE IS 0.05 MM
2. MAX ALLOWABLE BURR IS 0.076MM IN ALL DIRECTIONS
3. PIN #1 IS ON TOP WILL BE LASER MARKED
4. RED CIRCLE IN LAND PATTERN REPRESENTS THERMAL VIA. SIZE SHOULD BE 0.30-0.3 MM IN DIAMETER AND SHOULD BE CONNECTED TO GND FOR MAX THERMAL PERFORMANCE
5. GREEN RECTANGLES (SHADED AREA) REPRESENTS SOLDER STENCIL OPENING ON EXPOSED PAD AREA. SIZE SHOULD BE 0.40×0.90 MM.

8-Pin 2mm × 2mm TDFN (MT)

Note:

16. Package information is correct as of the publication date. For updates and most current information, go to www.micrel.com.

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