

**DATA SHEET**

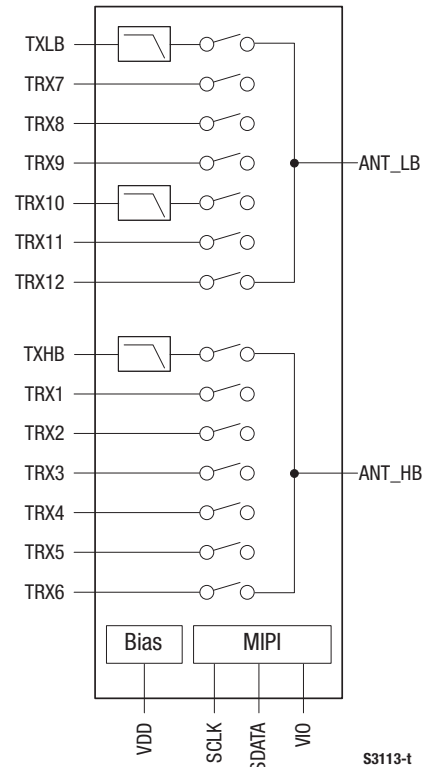
# SKY13456: 0.6 to 2.7 GHz DP14T Switch with MIPI® RFFE Interface

## Applications

- 2G/3G/4G multimode cellular handsets (LTE, UMTS, CDMA2000, EDGE, GSM)
- Embedded data cards
- Carrier aggregation (low band/high band)

## Features

- Broadband frequency range: 0.6 to 2.7 GHz
- Low insertion loss
- High isolation and linearity
- Integrated GSM harmonic filter
- Integrated, programmable MIPI interface using separate registers for low and high bands
- Twelve TRX ports, one GSM low band transmit port, and one GSM high band transmit port
- Integrated B17 3<sup>rd</sup> harmonic filter on TRx10 port designed for ultra-high linearity
- Small MCM (26-pin, 2.8 x 3.2 mm) package (MSL3, 260 °C per JEDEC J-STD-020)



**Figure 1. SKY13456 Block Diagram**



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## Description

The SKY13456 is a Double-Pole, Fourteen-Throw (DP14T) antenna switch. The device maintains low insertion loss and high isolation for both transmit and receive switching paths. The high linearity performance and low insertion loss makes the SKY13456 an ideal choice for carrier aggregation applications.

The device contains two Single-Pole, Seven-Throw (SP7T) switches that can accommodate UMTS, CDMA2000, EDGE, GSM, and LTE applications. Switching is controlled by the MIPI decoder. There is an external MIPI select pin that enables how the switch responds to power mode triggers. When this pin is grounded, the switch responds to any of the power mode triggers. When this pin

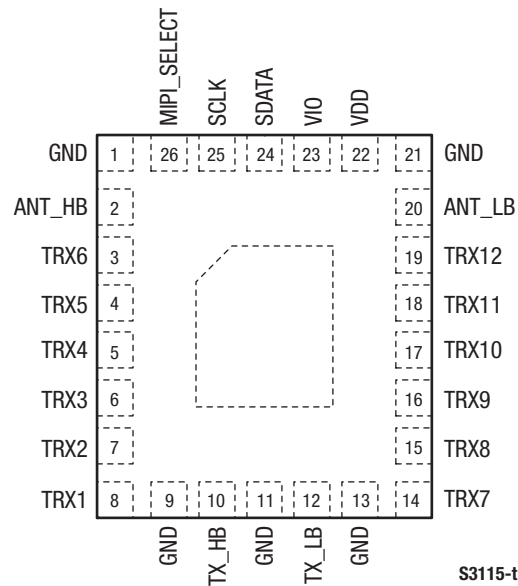
is left open, the switch responds to individual power mode triggers.

The high and low band SP7T switch bank can be independently controlled with two separate registers. Register 0 controls the high bands (pin signals TRX1 to TRX6) and Register 1 controls the low bands (pin signals TRX7 to TRX12). No external DC blocking capacitors are required on the RF path as long as no DC voltage is applied. There is an integrated B17 3<sup>rd</sup> Harmonic filter on the TRx10 port.

The switch also provides an excellent triple beat ratio and 2<sup>nd</sup>/3<sup>rd</sup> Order Intermodulation Distortion (IMD2/IMD3) performance.

The SKY13456 is manufactured in a small, 2.8 x 3.2 mm, 26-pin Multi-Chip Module (MCM) package.

A functional block diagram is shown in Figure 1. The pin configuration and package are shown in Figure 2. Signal pin assignments and functional pin descriptions are provided in Table 1.



**Figure 2. SKY13456 Pinout – 26-Pin MCM (Top View)**

**Table 1. SKY13456 Signal Descriptions (Note 1)**

| Pin | Name   | Description  | Pin | Name        | Description  |
|-----|--------|--|-----|-------------|--|
| 1   | GND    | Ground   | 14  | TRX7        | RF input/output port 7   |
| 2   | ANT_HB | High band antenna RF port  | 15  | TRX8        | RF input/output port 8   |
| 3   | TRX6   | RF input/output port 6   | 16  | TRX9        | RF input/output port 9   |
| 4   | TRX5   | RF input/output port 5   | 17  | TRX10       | RF input/output port 10. Designed for Band 17 transmit.  |
| 5   | TRX4   | RF input/output port 4   | 18  | TRX11       | RF input/output port 11  |
| 6   | TRX3   | RF input/output port 3   | 19  | TRX12       | RF input/output port 12  |
| 7   | TRX2   | RF input/output port 2   | 20  | ANT_LB      | Low band antenna RF port   |
| 8   | TRX1   | RF input/output port 1   | 21  | GND         | Ground   |
| 9   | GND    | Ground   | 22  | VDD         | DC power supply  |
| 10  | TX_HB  | GSM high band transmit RF input port with integrated harmonic filter | 23  | VIO         | Interface supply voltage   |
| 11  | GND    | Ground   | 24  | SDATA       | Data   |
| 12  | TX_LB  | GSM low band transmit RF input port with integrated harmonic filter  | 25  | SCLK        | Clock  |
| 13  | GND    | Ground   | 26  | MIPI_SELECT | MIPI interface select. When this pin is grounded, the switch responds to any of the power mode triggers. When this pin is left open, the switch is RFFE MIPI compliant and responds to individual power mode triggers. |

**Note 1:** Bottom ground paddles must be connected to ground.

**Electrical and Mechanical Specifications**

The absolute maximum ratings of the SKY13456 are provided in Table 2. Electrical specifications are provided in Table 3.

IMD2 and IMD3 test conditions for various frequencies are listed in Tables 4, 5, and 6. Triple Beat Ratio (TBR) frequencies and power levels are noted in Table 7.

Figure 3 illustrates the typical test setup used to measure intermodulation products. This industry standardized test is used to simulate the WCDMA Band 1 linearity of the antenna switch. A +20 dBm Continuous Wave (CW) signal,  $f_{FUND}$ , is sequentially applied to the TRX1 through TRX12 ports, while a -15 dBm CW blocker signal,  $f_{BLK}$ , is applied to the ANT\_LB port.

The resulting 3<sup>rd</sup> Order Intermodulation Distortion (IMD3),  $f_{TRX}$ , is measured over all phases of  $f_{FUND}$ . The SKY13456 exhibits exceptional performance for all TRXx ports.

Table 8 shows the isolation matrix for "Ant" to "Off" arms for the Low Band. Table 9 shows the isolation matrix for "On" arms to "Off" arms for the Low Band. Table 10 shows the isolation matrix for "Ant" to "Off" arms for the High Band. Table 11 shows the isolation matrix for "On" Arms to "Off" arms for the High Band.

Table 12 describes the register content and programming read/write sequences. Refer to the *MIPI Alliance Specification for RF Front-End Control Interface (RFFE)*, v1.10 (26 July 2011) for additional information on MIPI programming sequences and MIPI bus specifications.

Figures 4 and 5 provide the timing diagrams for register write commands and read commands, respectively.

Table 13 provides the Register 0 logic and Table 14 provides the logic for Register 1. Table 15 describes the register parameters and bit values.

**Table 2. SKY13456 Absolute Maximum Ratings (Note 1)**

| Parameter              | Symbol | Minimum | Maximum | Units |
|------------------------|--------|---------|---------|-------|
| Power supply           | VDD    | 2.5     | 5.0     | V     |
| Digital control signal | VIO    |         | 2       | V     |
| RF input power:        | PIN    |         |         |       |
| TX_LB pin              |        |         | +36     | dBm   |
| TX_HB pin              |        |         | +34     | dBm   |
| All TRXx pins          |        |         | +31     | dBm   |
| Storage temperature    | TSTG   | -55     | +150    | °C    |
| Operating temperature  | TOP    | -30     | +90     | °C    |

**Note 1:** Exposure to maximum rating conditions for extended periods may reduce device reliability. There is no damage to device with only one parameter set at the limit and all other parameters set at or below their nominal value. Exceeding any of the limits listed here may result in permanent damage to the device.

**CAUTION:** Although this device is designed to be as robust as possible, Electrostatic Discharge (ESD) can damage this device. This device must be protected at all times from ESD. Static charges may easily produce potentials of several kilovolts on the human body or equipment, which can discharge without detection. Industry-standard ESD precautions should be used at all times.

**Table 3. SKY13456 Electrical Specifications (Note 1) (1 of 2)**  
**(V<sub>DD</sub> = 2.85 V, T<sub>OP</sub> = +25 °C, Characteristic Impedance [Z<sub>0</sub>] = 50 Ω, Unless Otherwise Noted)**

| Parameter  | Symbol     | Test Condition  | Min | Typical | Max   | Units |
|--|------------|---|-----|---------|-------|-------|
| <b>RF Specifications</b>                                     |            |   |     |         |       |       |
| Operating frequency  | f          |   | 0.6 |         | 2.7   | GHz   |
| Insertion loss   | IL         | TXLB to ANT_LB,<br>824 to 915 MHz                         |     | 1.25    | 1.50  | dB    |
|  |            | TRX7, 8, 9, 11, 12 to<br>ANT_LB, 600 to 960 MHz           |     | 0.50    | 0.80  | dB    |
|  |            | TRX10 to ANT_LB,<br>704 to 716 MHz<br>(band 17 transmit)  |     | 0.85    | 0.95  | dB    |
|  |            | TXHB to ANT_HB,<br>1710 to 1910 MHz                       |     | 1.25    | 1.5   | dB    |
|  |            | TRX1/6 to ANT_HB,<br>1710 to 1990 MHz                     |     | 0.55    | 0.8   | dB    |
|  |            | TRX1/6 to ANT_HB,<br>up to 2690 MHz                       |     | 0.75    | 1.0   | dB    |
| GSM harmonic attenuation                                     | H2LB       | Transmit low band to<br>ANT_LB, 2fo<br>1648 to 1830 MHz   | 23  | 28      |       | dB    |
|  | H3LB       | Transmit low band to<br>ANT_LB, 3fo<br>2472 to 2745 MHz   | 23  | 28      |       | dB    |
|  | past 3fo   | Transmit low band to<br>ANT_LB, past 3fo<br>to 12.75 GHz  |     | 17      |       | dB    |
|  | H2HB       | Transmit high band to<br>ANT_HB, 2fo<br>3420 to 3820 MHz  | 23  | 28      |       | dB    |
|  | H3HB       | Transmit high band to<br>ANT_HB, 3fo<br>5130 to 5730 MHz  | 23  | 28      |       | dB    |
|  | H past 3fo | Transmit high band to<br>ANT_HB, past 3fo to<br>12.75 GHz |     | 17      |       | dB    |
| Isolation: TRx to any “off” TRx port<br>(non-adjacent ports) | Iso        | Up to 960 MHz   | 32  | 35      |       | dB    |
|  |            | Up to 2170 MHz  | 27  | 30      |       | dB    |
|  |            | Up to 2690 MHz  | 23  | 26      |       | dB    |
| Isolation: TRx to any “off” TRx port<br>(adjacent ports)     | Iso        | Up to 960 MHz   | 27  | 30      |       | dB    |
|  |            | Up to 2170 MHz  | 22  | 25      |       | dB    |
|  |            | Up to 2690 MHz  | 17  | 22      |       | dB    |
| Isolation: TXLB to TRX7/12                                   | Iso        | 824 to 915 MHz  | 31  | 36      |       | dB    |
| Isolation: TXHB to TRX1/6                                    | Iso        | 1710 to 1910 MHz  | 31  | 29      |       | dB    |
| Isolation: opposite side TRx ports<br>(TRX1/6 to TRX7/12)    | Iso        | Up to 2690 MHz  | 28  | 37      |       | dB    |
| Isolation: ANT_LB to ANT_HB port                             | Iso        | Up to 2690 MHz  |     | 25      |       | dB    |
| “On” state match   | VSWR       | Up to 2.7 GHz   |     |         | 1.5:1 | –     |

**Table 3. SKY13456 Electrical Specifications (Note 1) (2 of 2)**  
**(V<sub>DD</sub> = 2.85 V, T<sub>OP</sub> = +25 °C, Characteristic Impedance [Z<sub>0</sub>] = 50 Ω, Unless Otherwise Noted)**

| Parameter  | Symbol          | Test Condition   | Min                   | Typical | Max                   | Units |
|--|-----------------|--|-----------------------|---------|-----------------------|-------|
| <b>RF Specifications (continued)</b>   |                 |  |                       |         |                       |       |
| Low band GSM harmonics   | 2fo, 3fo        | PIN = +35 dBm, 50 Ω<br>PIN = +35 dBm,<br>5:1 VSWR  |                       | -55     | -45                   | dBm   |
|  |                 |  |                       | -43     | -36                   | dBm   |
| High band GSM harmonics  | 2fo, 3fo        | PIN = +33 dBm, 50 Ω<br>PIN = +33 dBm,<br>5:1 VSWR  |                       | -55     | -45                   | dBm   |
|  |                 |  |                       | -47     | -40                   | dBm   |
| Band 13 harmonics with no external filter  | 2fo             | TRX7/12 ports to ANT_LB port @ 786.5 MHz, PIN <+25 dBm, VSWR = 1:1                               |                       | -78     |                       | dBm   |
| Low band TRx harmonics   | 2fo, 3fo        | TRX7/12 ports to ANT_LB port, PIN =+26 dBm   |                       | -62     | -55                   | dBm   |
| High band TRx harmonics  | 2fo, 3fo        | TRX1/6 ports to ANT_LB port, PIN =+26 dBm  |                       | -62     | -55                   |       |
| Band 17 harmonics  | 3fo             | TRX10 port to ANT_LB port @ 710 MHz, PIN = +25 dBm, VSWR = 2:1, all phases                       |                       | -92     |                       | dBm   |
| 2nd Order Input Intercept Point  | IIP2            | AWS, PCS, IMT, CDMA2000 modes (see Table 4)<br>Cellular (see Table 4)<br>UMTS mode (see Table 6) | +95.5                 |         |                       | dBm   |
|  |                 |  | +113.5                |         |                       | dBm   |
|  |                 |  | +102.0                |         |                       | dBm   |
| 3rd Order Input Intercept Point  | IIP3            | UMTS mode (see Table 5)  | +61                   |         |                       | dBm   |
| Triple beat ratio  | TBR             | See Table 7  | +81                   | +87     |                       | dBc   |
| Turn-on time   | ton             | From application of V <sub>DD</sub> and V <sub>IO</sub>  |                       |         | 20                    | μs    |
| Wake-up time   | tw              | From isolation state   |                       | 2       | 5                     | μs    |
| Switching speed  | ts              | Port-to-port, 50% V <sub>CTL</sub> to final RF power ±1 dB                                       |                       | 2       | 5                     | μs    |
| <b>DC Specifications</b>   |                 |  |                       |         |                       |       |
| Supply voltage   | V <sub>DD</sub> |  | 2.50                  | 2.85    | 3.30                  | V     |
| Supply current:<br>GSM850/EGSM900/DCS1800/<br>PCS1900 transmit<br>WCDMA/CDMA2000<br>transmit/receive | I <sub>DD</sub> |  |                       | 50      | 100                   | μA    |
|  |                 |  |                       | 50      | 100                   | μA    |
| Digital data and clock signals:<br>High<br>Low<br>Current  | SDATA, SCLK     |  | 0.8 × V <sub>IO</sub> |         | V <sub>IO</sub>       | V     |
|  |                 |  | 0                     |         | 0.2 × V <sub>IO</sub> | V     |
|  |                 |  |                       |         | 5                     | μA    |
| Interface supply voltage level   | V <sub>IO</sub> |  | 1.65                  | 1.80    | 1.95                  | V     |
| Supply ripple  |                 |  |                       |         | 20                    | mVp-p |

**Note 1:** Performance is guaranteed only under the conditions listed in this Table.

**Table 4. CDMA2000 IIP2 Test Conditions**

| Band     | Temperature (°C) | In-Band (MHz) | CW Tone 1 (MHz) | CW Tone 1 (dBm) | CW Tone 2 (MHz) | CW Tone 2 (dBm) |
|----------|------------------|---------------|-----------------|-----------------|-----------------|-----------------|
| Cellular | 25               | 869.28        | 824.28          | +26             | 1693.56         | -20             |
|          | 0, 25, 90        | 881.61        | 836.61          | +26             | 1718.22         | -20             |
|          | 25               | 893.31        | 848.31          | +26             | 1741.62         | -20             |
| PCS      | 25               | 1930.05       | 1850.05         | +26             | 3780.10         | -20             |
|          | 0, 25, 90        | 1965.00       | 1885.00         | +26             | 3850.00         | -20             |
|          | 25               | 1989.95       | 1909.95         | +26             | 3899.90         | -20             |
| AWS      | 25               | 2110.00       | 1710.00         | +26             | 3820.00         | -20             |
|          | 0, 25, 90        | 2132.50       | 1732.50         | +26             | 3865.00         | -20             |
|          | 25               | 2155.00       | 1755.00         | +26             | 3910.00         | -20             |

**Table 5. IIP3 Test Conditions (UMTS Linearity)**

| Band        | CW Tone 1 (MHz) | CW Tone 1 (dBm) | CW Tone 2 (MHz) | CW Tone 2 (dBm) |
|-------------|-----------------|-----------------|-----------------|-----------------|
| 2600 MHz    | 2535            | +20             | 2415            | -15             |
| IMT         | 1950            | +20             | 1760            | -15             |
| PCS         | 1880            | +20             | 1800            | -15             |
| DCS         | 1745            | +20             | 1650            | -15             |
| PDC         | 1440            | +20             | 1392            | -15             |
| 900 MHz     | 892             | +20             | 847             | -15             |
| US cellular | 835             | +20             | 790             | -15             |

**Note:** Power levels are referenced to the antenna port and may be increased to facilitate measurement.

**Table 6. IIP2 Test Conditions (UMTS Linearity)**

| Band        | CW Tone 1 (MHz) | CW Tone 1 (dBm) | CW Tone 2 (MHz) | CW Tone 2 (dBm) |
|-------------|-----------------|-----------------|-----------------|-----------------|
| 2600 MHz    | 2535            | +20             | 120             | -15             |
| IMT         | 1950            | +20             | 190             | -15             |
| PCS         | 1880            | +20             | 80              | -15             |
| DCS         | 1745            | +20             | 95              | -15             |
| PDC         | 1440            | +20             | 48              | -15             |
| 900 MHz     | 892             | +20             | 45              | -15             |
| US cellular | 835             | +20             | 45              | -15             |

**Note:** Power levels are referenced to the antenna port and may be increased to facilitate measurement.

**Table 7. Triple Beat Ratio Frequencies and Power Levels**

| Band | Transmit Frequency 1 (MHz) | Transmit Power 1 (dBm) | Transmit Frequency 2 (MHz) | Transmit Power 2 (dBm) | Frequency Blocker ANT (MHz) | Power Blocker (dBm) | Triple Beat Product Frequency (MHz) |
|------|----------------------------|------------------------|----------------------------|------------------------|-----------------------------|---------------------|-------------------------------------|
| 2    | 1880.0                     | +21.5                  | 1881.0                     | +21.5                  | 1960.0                      | -30                 | 1960.0 ± 1                          |
| 5    | 836.5                      | +21.5                  | 837.5                      | +21.5                  | 881.5                       | -30                 | 881.5 ± 1                           |

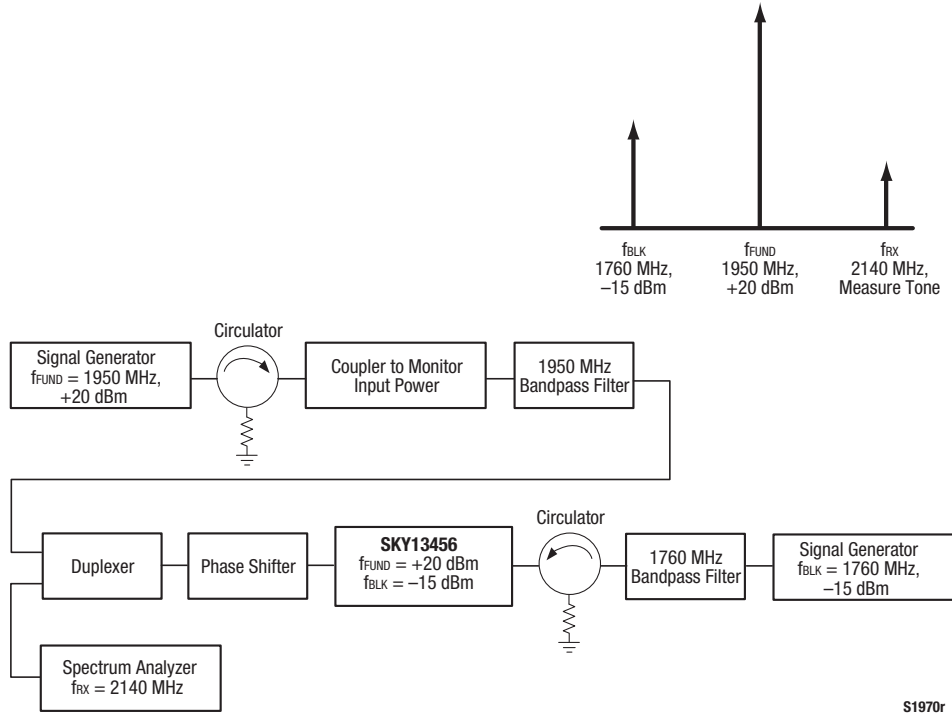


Figure 3. Typical 3<sup>rd</sup> Order Intermodulation Test Setup

Table 8. SKY13456 Isolation Matrix “On” Arms to “Off” Arms

| ON_Throw | Freq (GHz) | Isolation (dB) |       |       |      |      |      |      |
|----------|------------|----------------|-------|-------|------|------|------|------|
|          |            | TRx12          | TRx11 | TRx10 | TRx9 | TRx8 | TRx7 | TxLB |
| TxLB     | 0.915      | -36            | -43   | -34   | -40  | -38  | -36  |      |
| TRx7     | 0.915      | -37            | -44   | -36   | -37  | -24  |      | -31  |
| TRx8     | 0.915      | -37            | -43   | -33   | -32  |      | -27  | -32  |
| TRx9     | 0.915      | -38            | -38   | -26   |      | -28  | -36  | -32  |
| TRx10    | 0.915      | -35            | -26   |       | -26  | -36  | -41  | -24  |
| TRx11    | 0.915      | -29            |       | -25   | -37  | -40  | -45  | -32  |
| TRx12    | 0.915      |                | -29   | -32   | -41  | -40  | -44  | -32  |

Table 9. SKY13456 Isolation Matrix “ANT” to “Off” Arms

| ON_Throw | Freq (GHz) | Isolation (dB) |       |       |      |      |      |      |
|----------|------------|----------------|-------|-------|------|------|------|------|
|          |            | TRx12          | TRx11 | TRx10 | TRx9 | TRx8 | TRx7 | TxLB |
| TxLB     | 0.915      | -28            | -37   | -31   | -35  | -36  | -39  |      |
| TRx7     | 0.915      | -28            | -40   | -44   | -35  | -37  |      | -31  |
| TRx8     | 0.915      | -28            | -41   | -49   | -37  |      | -37  | -31  |
| TRx9     | 0.915      | -28            | -41   | -37   |      | -36  | -36  | -32  |
| TRx10    | 0.915      | -25            | -36   |       | -35  | -40  | -41  | -24  |
| TRx11    | 0.915      | -27            |       | -43   | -44  | -41  | -43  | -32  |
| TRx12    | 0.915      |                | -39   | -34   | -44  | -41  | -44  | -32  |

**Table 10. SKY13456 Isolation Matrix “On” Arms to “Off” Arms**

| ON_Throw | Freq (GHz) | Isolation (dB) |      |      |      |      |      |      |
|----------|------------|----------------|------|------|------|------|------|------|
|          |            | TRx6           | TRx5 | TRx4 | TRx3 | TRx2 | TRx1 | TxHB |
| TRx1     | 1.910      | -30            | -37  | -38  | -27  | -19  |      | -32  |
| TRx1     | 2.170      | -28            | -35  | -36  | -26  | -18  |      | -34  |
| TRx1     | 2.700      | -26            | -32  | -34  | -24  | -16  |      | -39  |
| TRx2     | 1.910      | -30            | -35  | -35  | -22  |      | -20  | -39  |
| TRx2     | 2.170      | -29            | -33  | -34  | -21  |      | -18  | -38  |
| TRx2     | 2.700      | -26            | -30  | -32  | -20  |      | -17  | -36  |
| TRx3     | 1.910      | -30            | -31  | -26  |      | -25  | -32  | -39  |
| TRx3     | 2.170      | -29            | -29  | -25  |      | -23  | -30  | -40  |
| TRx3     | 2.700      | -26            | -27  | -23  |      | -21  | -28  | -43  |
| TRx4     | 1.910      | -30            | -20  |      | -25  | -34  | -37  | -39  |
| TRx4     | 2.170      | -29            | -19  |      | -24  | -33  | -36  | -40  |
| TRx4     | 2.700      | -25            | -17  |      | -23  | -31  | -33  | -45  |
| TRx5     | 1.910      | -25            |      | -21  | -33  | -37  | -38  | -37  |
| TRx5     | 2.170      | -23            |      | -20  | -31  | -36  | -37  | -38  |
| TRx5     | 2.700      | -20            |      | -8   | -30  | -33  | -34  | -41  |
| TRx6     | 1.910      |                | -24  | -29  | -37  | -38  | -38  | -36  |
| TRx6     | 2.170      |                | -23  | -27  | -35  | -37  | -37  | -36  |
| TRx6     | 2.700      |                | -20  | -25  | -33  | -34  | -33  | -39  |
| TxHB     | 1.910      | -29            | -38  | -39  | -40  | -35  | -30  |      |
| TxHB     | 2.170      | -28            | -37  | -38  | -40  | -35  | -31  |      |
| TxHB     | 2.700      | -29            | -38  | -39  | -47  | -35  | -32  |      |



**Table 11. SKY13456 Isoaltion Matrix “ANT” Arms to “Off” Arms**

| ON_Throw | Freq (GHz) | Isolation (dB) |      |      |      |      |      |      |
|----------|------------|----------------|------|------|------|------|------|------|
|          |            | TRx6           | TRx5 | TRx4 | TRx3 | TRx2 | TRx1 | TxHB |
| TRx1     | 1.910      | -23            | -35  | -33  | -36  | -27  |      | -31  |
| TRx1     | 2.170      | -22            | -34  | -32  | -35  | -25  |      | -29  |
| TRx1     | 2.700      | -21            | -32  | -29  | -32  | -22  |      | -28  |
| TRx2     | 1.910      | -23            | -36  | -33  | -32  |      | -28  | -28  |
| TRx2     | 2.170      | -22            | -34  | -31  | -31  |      | -27  | -28  |
| TRx2     | 2.700      | -21            | -33  | -28  | -28  |      | -24  | -28  |
| TRx3     | 1.910      | -23            | -37  | -34  |      | -31  | -28  | -30  |
| TRx3     | 2.170      | -22            | -35  | -33  |      | -30  | -26  | -30  |
| TRx3     | 2.700      | -20            | -33  | -30  |      | -27  | -24  | -31  |
| TRx4     | 1.910      | -21            | -31  |      | -35  | -39  | -38  | -34  |
| TRx4     | 2.170      | -20            | -29  |      | -34  | -38  | -36  | -34  |
| TRx4     | 2.700      | -18            | -26  |      | -31  | -35  | -33  | -36  |
| TRx5     | 1.910      | -23            |      | -31  | -36  | -39  | -38  | -34  |
| TRx5     | 2.170      | -21            |      | -30  | -34  | -37  | -36  | -34  |
| TRx5     | 2.700      | -19            |      | -27  | -31  | -35  | -33  | -37  |
| TRx6     | 1.910      |                | -32  | -32  | -8   | -39  | -38  | -35  |
| TRx6     | 2.170      |                | -31  | -31  | -37  | -37  | -36  | -34  |
| TRx6     | 2.700      |                | -28  | -28  | -34  | -34  | -33  | -37  |
| TxHB     | 1.910      | -23            | -33  | -33  | -38  | -36  | -37  |      |
| TxHB     | 2.170      | -21            | -31  | -31  | -36  | -34  | -35  |      |
| TxHB     | 2.700      | -18            | -28  | -28  | -34  | -34  | -32  |      |

**Table 12. Command Sequence Bit Definitions**

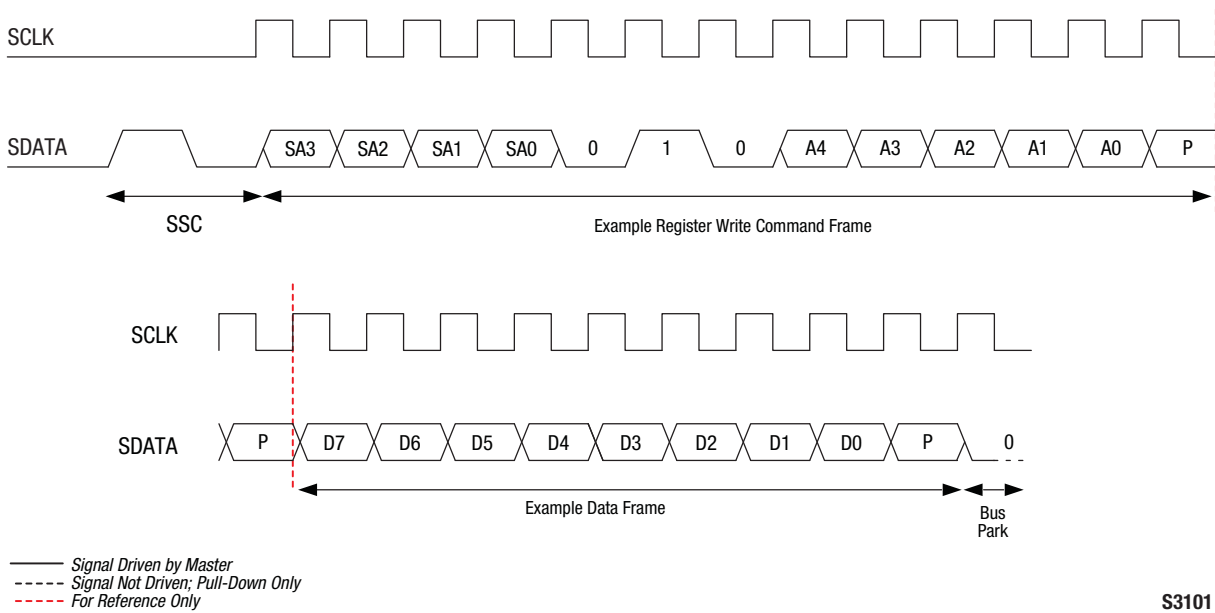
| Type        | SSC | C11-C8  | C7 | C6-C5     | C4      | C3-C0     | Parity Bits | BPC | Extended Operation |             |     |               |             |     |
|-------------|-----|---------|----|-----------|---------|-----------|-------------|-----|--------------------|-------------|-----|---------------|-------------|-----|
|             |     |         |    |           |         |           |             |     | DA7(1)-DA0(1)      | Parity Bits | BPC | DA7(n)-DA0(n) | Parity Bits | BPC |
| Reg 0 Write | Y   | SA[3:0] | 1  | Data[6:5] | Data[4] | Data[3:0] | Y           | Y   | -                  | -           | -   | -             | -           | -   |
| Reg Write   | Y   | SA[3:0] | 0  | 10        | Addr[4] | Addr[3:0] | Y           | -   | Data[7:0]          | -           | -   | -             | Y           | Y   |
| Reg Read    | Y   | SA[3:0] | 0  | 11        | Addr[4] | Addr[3:0] | Y           | Y   | Data[7:0]          | -           | -   | -             | Y           | Y   |

**Legend:**

SSC = Sequence start command  
C = Command frame bits

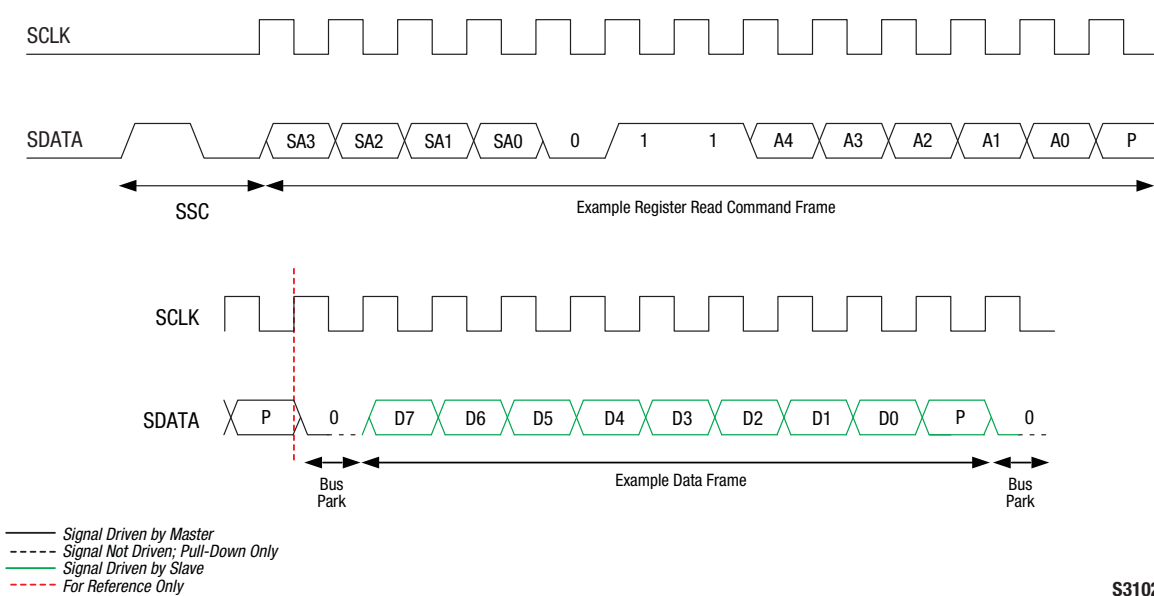
DA = Data/address frame bits  
BPC = Bus park cycle

BC = Byte count (# of consecutive addresses)



S3101

Figure 4. Register Write Command Timing Diagram



S3102

Figure 5. Register Read Command Timing Diagram

**Table 13. Register 0 Truth Table**

| State | Mode                | Register Bits |     |     |     |     |    |    |    |
|-------|---------------------|---------------|-----|-----|-----|-----|----|----|----|
|       |                     | D7            | D6  | D5  | D4  | D3  | D2 | D1 | D0 |
| 1     | Isolation (default) | N/U           | N/U | N/U | N/U | N/U | 0  | 0  | 0  |
| 2     | ANT_HB to TRX1      | N/U           | N/U | N/U | N/U | N/U | 0  | 0  | 1  |
| 3     | ANT_HB to TRX2      | N/U           | N/U | N/U | N/U | N/U | 0  | 1  | 0  |
| 4     | ANT_HB to TRX3      | N/U           | N/U | N/U | N/U | N/U | 0  | 1  | 1  |
| 5     | ANT_HB to TRX4      | N/U           | N/U | N/U | N/U | N/U | 1  | 0  | 0  |
| 6     | ANT_HB to TRX5      | N/U           | N/U | N/U | N/U | N/U | 1  | 0  | 1  |
| 7     | ANT_HB to TRX6      | N/U           | N/U | N/U | N/U | N/U | 1  | 1  | 0  |
| 8     | ANT_HB to TXHB      | N/U           | N/U | N/U | N/U | N/U | 1  | 1  | 1  |

Note: N/U = Not used

**Table 14. Register 1 Truth Table**

| State | Mode                | Register Bits |     |     |     |     |    |    |    |
|-------|---------------------|---------------|-----|-----|-----|-----|----|----|----|
|       |                     | D7            | D6  | D5  | D4  | D3  | D2 | D1 | D0 |
| 1     | Isolation (default) | N/U           | N/U | N/U | N/U | N/U | 0  | 0  | 0  |
| 2     | ANT_LB to TRX7      | N/U           | N/U | N/U | N/U | N/U | 0  | 0  | 1  |
| 3     | ANT_LB to TRX8      | N/U           | N/U | N/U | N/U | N/U | 0  | 1  | 0  |
| 4     | ANT_LB to TRX9      | N/U           | N/U | N/U | N/U | N/U | 0  | 1  | 1  |
| 5     | ANT_LB to TRX10     | N/U           | N/U | N/U | N/U | N/U | 1  | 0  | 0  |
| 6     | ANT_LB to TXLB      | N/U           | N/U | N/U | N/U | N/U | 1  | 0  | 1  |
| 7     | ANT_LB to TRX11     | N/U           | N/U | N/U | N/U | N/U | 1  | 1  | 0  |
| 8     | ANT_LB to TRX12     | N/U           | N/U | N/U | N/U | N/U | 1  | 1  | 1  |

Note: N/U = Not used

**Table 15. Register Description and Programming (1 of 2)**

| Register    |               | Parameter                | Description  | Default (Binary) |
|-------------|---------------|--------------------------|--|------------------|
| Name        | Address (Hex) |                          |  |                  |
| Register 0  | 00000         | MODE_CTRL                | Bits[7:0]:<br>Switch control. See Table 9 for Register 0 logic   | –                |
| Register 1  | 00001         | MODE_CTRL                | Bits[7:0]:<br>Switch control. See Table 10 for Register 1 logic  | –                |
| RFFE_STATUS | 001A          | SOFTWARE RESET           | Bit[7]:<br>Resets all data to default values except for USID, GSID, or the contents of the PM_TRIG Register.<br>0 = Normal operation<br>1 = Software reset | 0                |
|             |               | COMMAND_FRAME_PARITY_ERR | Bit[6]:<br>Command sequence received with parity error – discard command.  | 0                |
|             |               | COMMAND_LENGTH_ERR       | Bit[5]:<br>Command length error.   | 0                |
|             |               | ADDRESS_FRAME_PARITY_ERR | Bit[4]:<br>Address frame parity error = 1.   | 0                |
|             |               | DATA_FRAME_PARITY_ERR    | Bit[3]:<br>Data frame with parity error.   | 0                |
|             |               | READ_UNUSED_REG          | Bit[2]:<br>Read command to an invalid address.   | 0                |
|             |               | WRITE_UNUSED_REG         | Bit[1]:<br>Write command to an invalid address.  | 0                |
|             |               | BID_GID_ERR              | Bit[0]:<br>Read command with a BROADCAST_ID (refer to the <i>MIPI Alliance Specification</i> ) or GSID.  | 0                |
| GROUP_SID   | 001B          | Reserved                 | Bits[7:4]: Reserved  | 0000             |
|             |               | GSID                     | Bits[3:0]:<br>Group slave ID   | 0000             |

**Table 15. Register Description and Programming (2 of 2)**

| Register            |               | Parameter       | Description   | Default (Binary) |
|---------------------|---------------|-----------------|---|------------------|
| Name                | Address (Hex) |                 |   |                  |
| PM_TRIG<br>(Note 1) | 001C          | PWR_MODE        | Bits[7:6]:<br>00 = Normal operation (active)<br>01 = Default settings (startup)<br>10 = Low power (low power)<br>11 = Reserved  | 00               |
|                     |               | Trigger_Mask_2  | Bit[5]:<br>If this bit is set, trigger 2 is disabled. When all triggers are disabled, if writing to a register that is associated with trigger 2, the data goes directly to the destination register.   | 0                |
|                     |               | Trigger_Mask_1  | Bit[4]:<br>If this bit is set, trigger 1 is disabled. When all triggers are disabled, if writing to a register that is associated with trigger 1, the data goes directly to the destination register.   | 0                |
|                     |               | Trigger_Mask_0  | Bit[3]:<br>If this bit is set, trigger 0 is disabled. When all triggers are disabled, if writing to a register that is associated with trigger 0, the data goes directly to the destination register.   | 0                |
|                     |               | Trigger_2       | Bit[2]:<br>If this bit is set, data is loaded into the trigger 2 registers.   | 0                |
|                     |               | Trigger_1       | Bit[1]:<br>If this bit is set, data is loaded into the trigger 1 registers.   | 0                |
|                     |               | Trigger_0       | Bit[0]:<br>If this bit is set, data is loaded into the trigger 0 registers.   | 0                |
| PRODUCT_ID          | 001D          | PRODUCT_ID      | Bits[7:0]:<br>This is a read-only register. However, during the programming of the Unique Slave Identifier (USID), a write command sequence is performed on this register but the value is not changed. | 01000100         |
| MANUFACTURER_ID     | 001E          | MANUFACTURER_ID | Bits[7:0]:<br>Read-only register  | 10100101         |
| MAN_USID            | 001F          | Reserved        | Bits[7:6]:<br>Reserved  | 00               |
|                     |               | MANUFACTURER_ID | Bits[5:4]:<br>Read-only register  | 01               |
|                     |               | USID            | Bits[3:0]:<br>Programmable USID. A write to these bits programs the USID.   | 1011             |

**Note 1:** Unlike the complete independence between triggers 0, 1, and 2, and also between the associated trigger masks 0, 1, and 2, respectively, as described in the MIPI RFFE Specification, this device uses additional interactions between the provided trigger functions.

The delayed application of updated data to all triggerable registers in this device may be accomplished using any of the three triggers (0, 1, or 2), provided that the particular trigger used is not currently masked off. If multiple triggers are enabled, any or all of those are sufficient to cause the data to be transferred from shadow registers to destination registers for all triggerable registers in the device.

It is also necessary to disable all three triggers (i.e., set all three trigger masks) to ensure that data written to any triggerable register will immediately be written to the destination register at the conclusion of the RFFE command sequence where the data is written.

### Evaluation Board Description

The SKY13456 Evaluation Board is used to test the performance of the SKY13456 DP14T Switch. An Evaluation Board schematic diagram is provided in Figure 6. A recommended ESD protection circuit diagram is provided in Figure 7. An assembly drawing for the Evaluation Board is shown in Figure 8.

### Package Dimensions

The PCB layout footprint for the SKY13456 is provided in Figure 9. Typical case markings are shown in Figure 10. Package dimensions for the 26-pin MCM are shown in Figure 11, and tape and reel dimensions are provided in Figure 12.

### Package and Handling Information

Since the device package is sensitive to moisture absorption, it is baked and vacuum packed before shipping. Instructions on the shipping container label regarding exposure to moisture after the container seal is broken must be followed. Otherwise, problems related to moisture absorption may occur when the part is subjected to high temperature during solder assembly.

The SKY13456 is rated to Moisture Sensitivity Level 3 (MSL3) at 260 °C. It can be used for lead or lead-free soldering. For additional information, refer to the Skyworks Application Note, *PCB Design and SMT Assembly/Rework Guidelines for MCM-L Packages*, document number 101752.

Care must be taken when attaching this product, whether it is done manually or in a production solder reflow environment. Production quantities of this product are shipped in a standard tape and reel format.

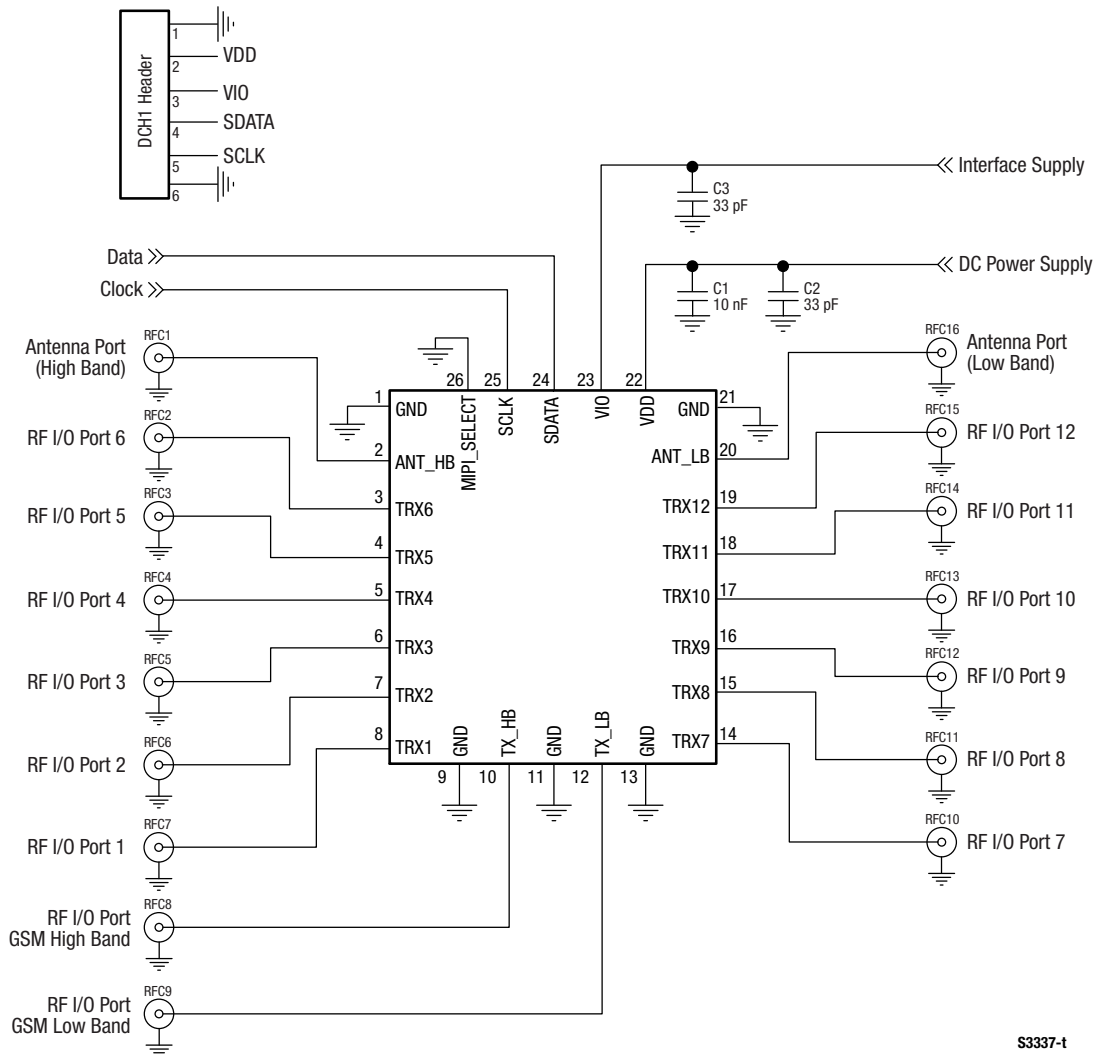
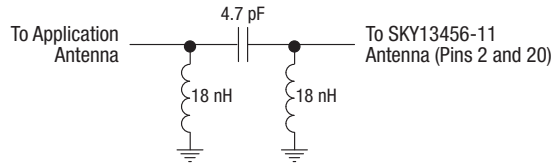
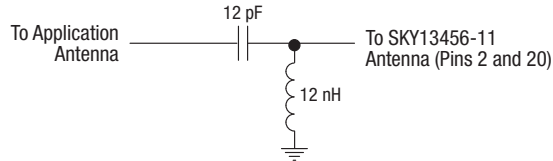


Figure 6. SKY13456 Evaluation Board Schematic



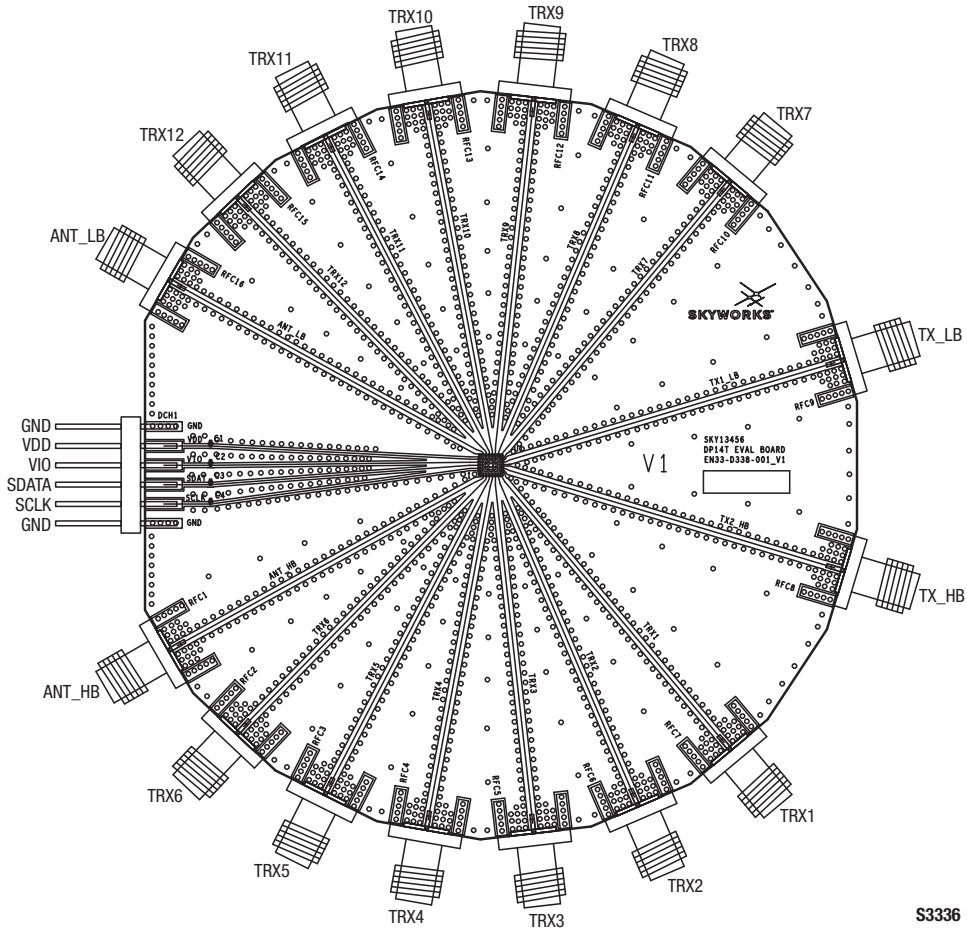
ESD Circuit 1



ESD Circuit 2

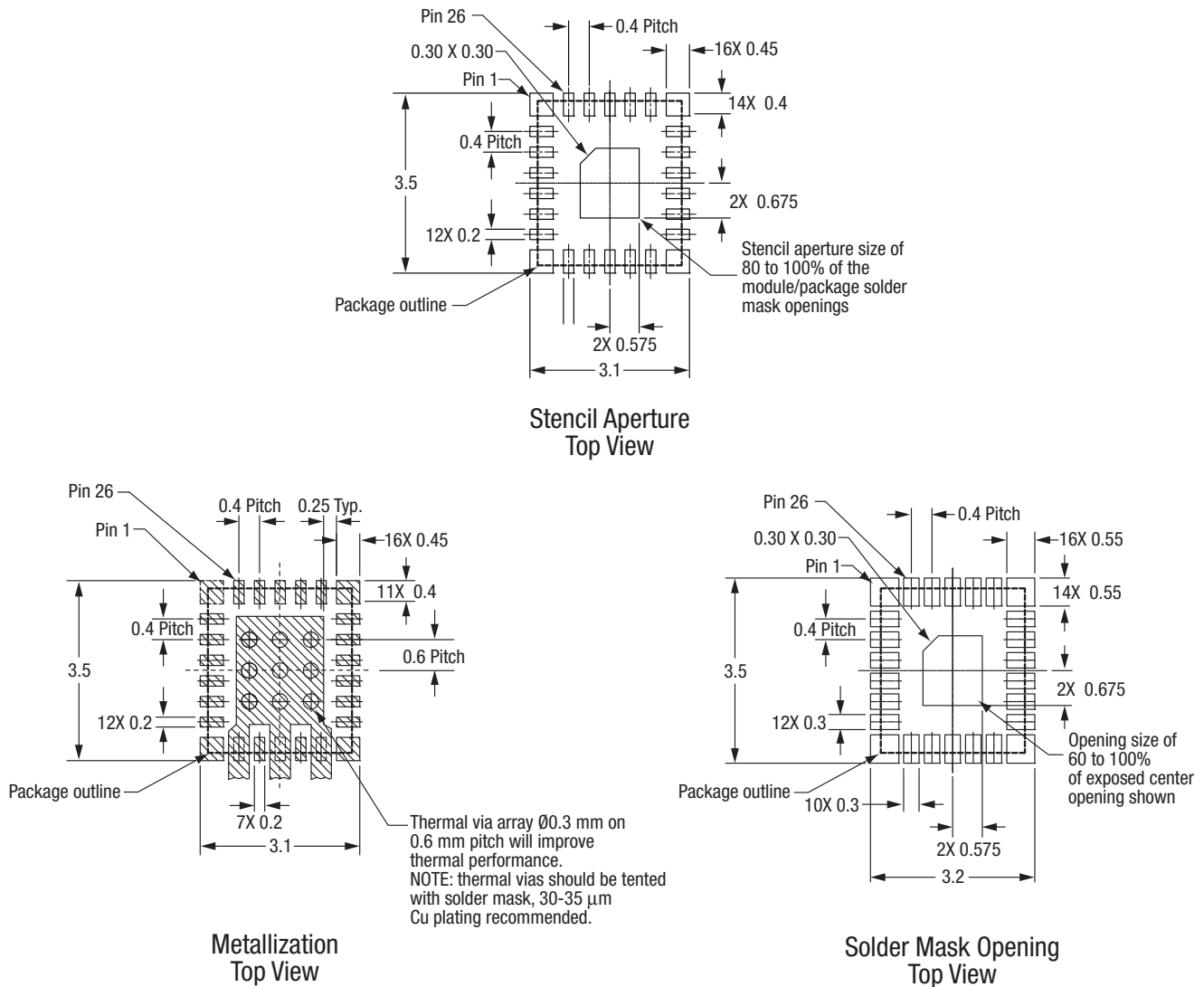
S2520m

Figure 7. SKY13456 Recommended ESD Protection Circuits



S3336

Figure 8. SKY13456 Evaluation Board Assembly Diagram

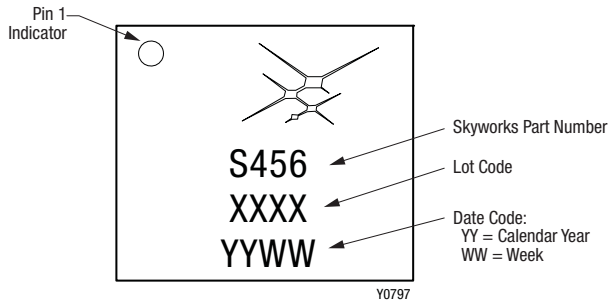


All dimensions are in millimeters

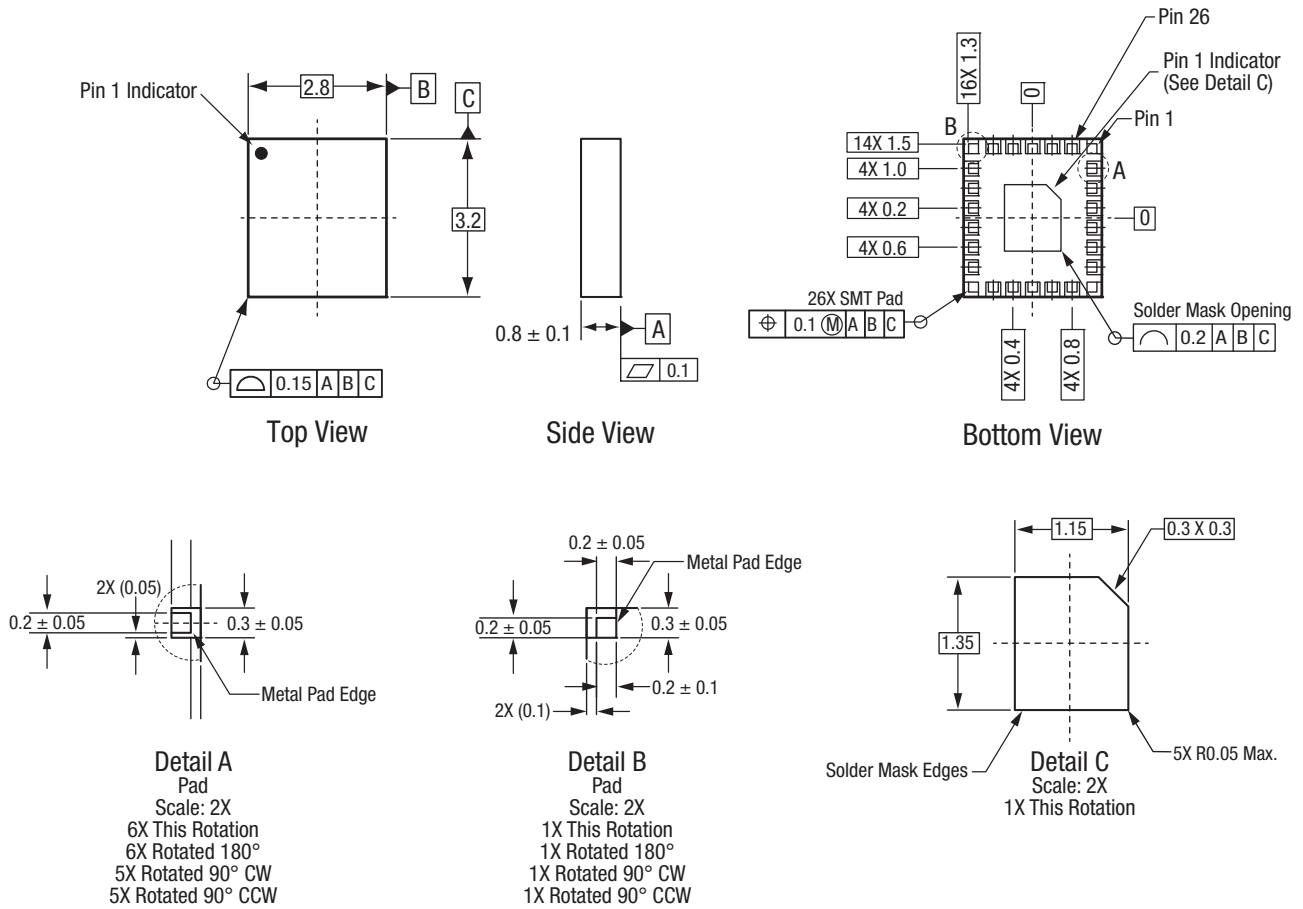
S3116

**Figure 9. SKY13456 PCB Layout Footprint (Top View)**





**Figure 10. Typical Part Markings (Top View)**

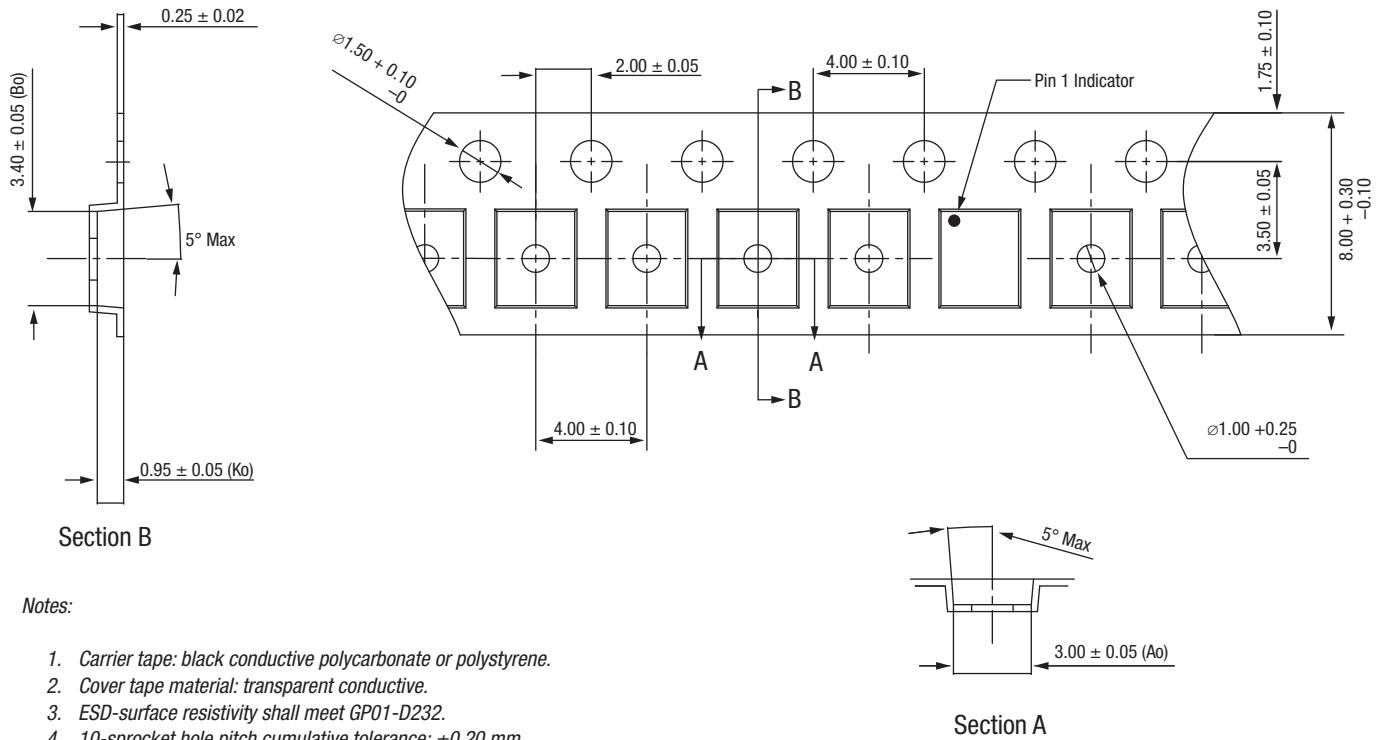


All measurements are in millimeters

Dimensioning and tolerancing according to ASME Y14.5M-1994

S3314

**Figure 11. SKY13456 26-Pin MCM Package Dimensions**



Notes:

1. Carrier tape: black conductive polycarbonate or polystyrene.
2. Cover tape material: transparent conductive.
3. ESD-surface resistivity shall meet GP01-D232.
4. 10-sprocket hole pitch cumulative tolerance:  $\pm 0.20$  mm.
5. Ao and Bo measurement point to be 0.30 mm from bottom pocket.
6. All dimensions are in millimeters.

Y0799

Figure 12. SKY13456 Tape and Reel Dimensions

**Ordering Information**

| Model Name   | Manufacturing Part Number | Evaluation Board Part Number |
|--|---------------------------|------------------------------|
| SKY13456: 0.6 to 2.7 GHz DP14T Switch with MIPI RFFE Interface | SKY13456                  | SKY13456-EVB                 |

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