

# 3.3 V, 125-MHz Multi-Output Zero Delay Buffer

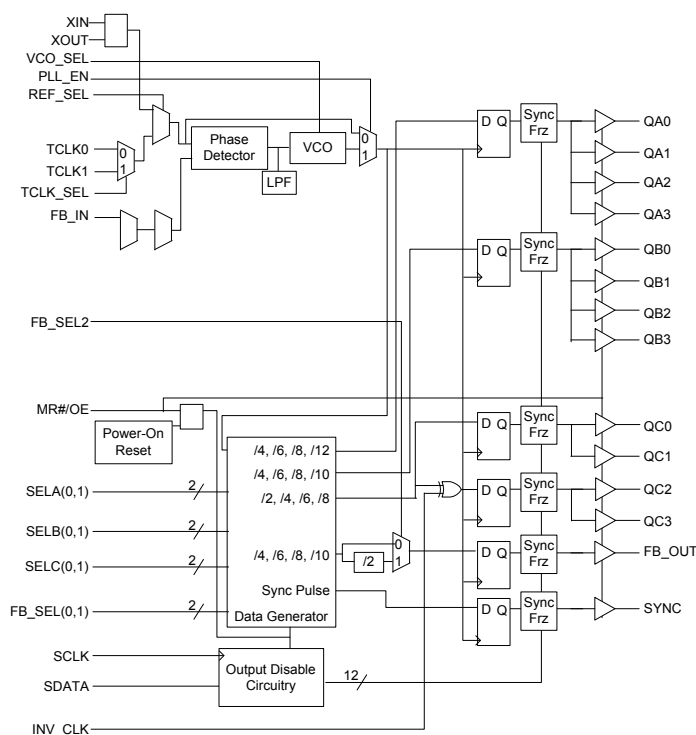
## Features

- Output frequency up to 125 MHz
- 12 Clock outputs: frequency configurable
- 350 ps max. output-to-output skew
- Configurable output disable
- Two reference clock inputs for dynamic toggling
- Oscillator or crystal reference input
- Spread-spectrum-compatible
- Glitch-free output clocks transitioning
- 3.3 V power supply
- Pin-compatible with MPC972
- Industrial temperature range: -40 °C to +85 °C
- 52-pin Thin quad flat package (TQFP) package

**Table 1. Frequency Table<sup>[1]</sup>**

| VC0_SEL | FB_SEL2 | FB_SEL1 | FB_SEL0 | F <sub>VC0</sub> |
|---------|---------|---------|---------|------------------|
| 0       | 0       | 0       | 0       | 8x               |
| 0       | 0       | 0       | 1       | 12x              |
| 0       | 0       | 1       | 0       | 16x              |
| 0       | 0       | 1       | 1       | 20x              |
| 0       | 1       | 0       | 0       | 16x              |
| 0       | 1       | 0       | 1       | 24x              |
| 0       | 1       | 1       | 0       | 32x              |
| 0       | 1       | 1       | 1       | 40x              |
| 1       | 0       | 0       | 0       | 4x               |
| 1       | 0       | 0       | 1       | 6x               |
| 1       | 0       | 1       | 0       | 8x               |
| 1       | 0       | 1       | 1       | 10x              |
| 1       | 1       | 0       | 0       | 8x               |
| 1       | 1       | 0       | 1       | 12x              |
| 1       | 1       | 1       | 0       | 16x              |
| 1       | 1       | 1       | 1       | 20x              |

## Block Diagram



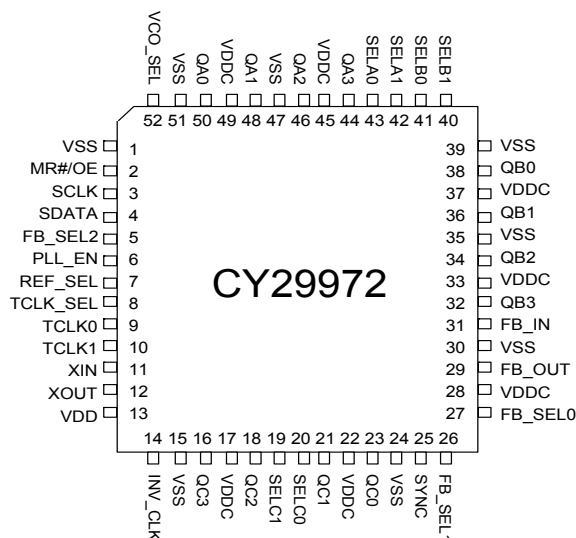
### Note

1. x = the reference input frequency, 200 MHz < F<sub>VCO</sub> < 480 MHz.

## Contents

|                                                       |          |                                                      |           |
|-------------------------------------------------------|----------|------------------------------------------------------|-----------|
| <b>Pin Configuration</b> .....                        | <b>3</b> | <b>Ordering Code Definition</b> .....                | <b>9</b>  |
| <b>Pin Description</b> .....                          | <b>3</b> | <b>Package Drawing and Dimension</b> .....           | <b>10</b> |
| <b>Description</b> .....                              | <b>5</b> | <b>Acronyms</b> .....                                | <b>11</b> |
| <b>Glitch-Free Output Frequency Transitions</b> ..... | <b>5</b> | <b>Document Conventions</b> .....                    | <b>11</b> |
| <b>SYNC Output</b> .....                              | <b>6</b> | Units of Measure .....                               | 11        |
| <b>Power Management</b> .....                         | <b>7</b> | <b>Document History Page</b> .....                   | <b>12</b> |
| <b>Absolute Maximum Ratings</b> .....                 | <b>7</b> | <b>Sales, Solutions, and Legal Information</b> ..... | <b>13</b> |
| <b>DC Parameters</b> .....                            | <b>8</b> | Worldwide Sales and Design Support .....             | 13        |
| <b>AC Parameters</b> .....                            | <b>8</b> | Products .....                                       | 13        |
| <b>Ordering Information</b> .....                     | <b>9</b> | PSoC Solutions .....                                 | 13        |

## Pin Configuration



## Pin Description<sup>[2]</sup>

| Pin            | Name              | PWR               | I/O | Type | Description                                                                                                                                                                                                                                                                  |
|----------------|-------------------|-------------------|-----|------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 11             | X <sub>IN</sub>   | –                 | I   | –    | <b>Oscillator input.</b> Connect to a crystal.                                                                                                                                                                                                                               |
| 12             | X <sub>OUT</sub>  | –                 | O   | –    | <b>Oscillator output.</b> Connect to a crystal.                                                                                                                                                                                                                              |
| 9              | T <sub>CLK0</sub> | –                 | I   | PU   | <b>External reference/test clock input.</b>                                                                                                                                                                                                                                  |
| 10             | T <sub>CLK1</sub> | –                 | I   | PU   | <b>External reference/test clock input.</b>                                                                                                                                                                                                                                  |
| 44, 46, 48, 50 | QA(3:0)           | V <sub>D</sub> DC | O   | –    | <b>Clock outputs.</b> See <a href="#">Table 2</a> for frequency selections.                                                                                                                                                                                                  |
| 32, 34, 36, 38 | QB(3:0)           | V <sub>D</sub> DC | O   | –    | <b>Clock outputs.</b> See <a href="#">Table 2 on page 5</a> for frequency selections.                                                                                                                                                                                        |
| 16, 18, 21, 23 | QC(3:0)           | V <sub>D</sub> DC | O   | –    | <b>Clock outputs.</b> See <a href="#">Table 2 on page 5</a> for frequency selections.                                                                                                                                                                                        |
| 29             | FB_OUT            | V <sub>D</sub> DC | O   | –    | <b>Feedback clock output.</b> Connect to FB_IN for normal operation. The divider ratio for this output is set by FB_SEL(0:2). See <a href="#">Table 1 on page 1</a> . A bypass delay capacitor at this output will control Input Reference/Output Banks phase relationships. |
| 25             | SYNC              | V <sub>D</sub> DC | O   | –    | <b>Synchronous pulse output.</b> This output is used for system synchronization. The rising edge of the output pulse is in sync with both the rising edges of QA (0:3) and QC(0:3) output clocks regardless of the divider ratios selected.                                  |
| 42, 43         | SELA(1,0)         | –                 | I   | PU   | <b>Frequency select inputs.</b> These inputs select the divider ratio at QA(0:3) outputs. See <a href="#">Table 2</a> .                                                                                                                                                      |
| 40, 41         | SELB(1,0)         | –                 | I   | PU   | <b>Frequency select inputs.</b> These inputs select the divider ratio at QB(0:3) outputs. See <a href="#">Table 2</a> .                                                                                                                                                      |
| 19, 20         | SELC(1,0)         | –                 | I   | PU   | <b>Frequency select inputs.</b> These inputs select the divider ratio at QC(0:3) outputs. See <a href="#">Table 2</a> .                                                                                                                                                      |

### Note

- A bypass capacitor (0.1 mF) should be placed as close as possible to each positive power (< 0.2"). If these bypass capacitors are not close to the pins, their high-frequency filtering characteristics will be cancelled by the lead inductance of the traces

## Pin Description<sup>[2]</sup>

| Pin                           | Name             | PWR | I/O | Type | Description                                                                                                                                                                                                                           |
|-------------------------------|------------------|-----|-----|------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 5, 26, 27                     | FB_SEL(2:0)      | –   | I   | PU   | <b>Feedback select inputs.</b> These inputs select the divide ratio at FB_OUT output. See <a href="#">Table 1 on page 1</a> .                                                                                                         |
| 52                            | VCO_SEL          | –   | I   | PU   | <b>VCO divider select input.</b> When set LOW, the VCO output is divided by 2. When set HIGH, the divider is bypassed. See <a href="#">Table 1 on page 1</a> .                                                                        |
| 31                            | FB_IN            | –   | I   | PU   | <b>Feedback clock input.</b> Connect to FB_OUT for accessing the PLL.                                                                                                                                                                 |
| 6                             | PLL_EN           | –   | I   | PU   | <b>PLL enable input.</b> When asserted HIGH, PLL is enabled; when LOW, PLL is bypassed.                                                                                                                                               |
| 7                             | REF_SEL          | –   | I   | PU   | <b>Reference select input.</b> When HIGH, the crystal oscillator is selected; when LOW, TCLK (0,1) is the reference clock.                                                                                                            |
| 8                             | TCLK_SEL         | –   | I   | PU   | <b>TCLK select input.</b> When LOW, TCLK0 is selected and when HIGH TCLK1 is selected.                                                                                                                                                |
| 2                             | MR#/OE           | –   | I   | PU   | <b>Master reset/output enable input.</b> When asserted LOW, resets all of the internal flip-flops and also disables all of the outputs. When pulled high, releases the internal flip-flops from reset and enables all of the outputs. |
| 14                            | INV_CLK          | –   | I   | PU   | <b>Inverted clock input.</b> When set HIGH, QC(2,3) outputs are inverted. When set LOW, the inverter is bypassed.                                                                                                                     |
| 3                             | S_CLK            | –   | I   | PU   | <b>Serial clock input.</b> Clocks data at SDATA into the internal register.                                                                                                                                                           |
| 4                             | S_DATA           | –   | I   | PU   | <b>Serial data input.</b> Input data is clocked to the internal register to enable/disable individual outputs. This provides flexibility in power management.                                                                         |
| 17, 22, 28, 33, 37, 45, 49    | V <sub>DDC</sub> | –   | –   | –    | 3.3 V power supply for output clock buffers.                                                                                                                                                                                          |
| 13                            | V <sub>DD</sub>  | –   | –   | –    | 3.3 V power supply for PLL.                                                                                                                                                                                                           |
| 1, 15, 24, 30, 35, 39, 47, 51 | V <sub>SS</sub>  | –   | –   | –    | Common ground.                                                                                                                                                                                                                        |

## Description

The CY29972 has an integrated PLL that provides low skew and low jitter clock outputs for high-performance microprocessors. Three independent banks of four outputs and an independent PLL feedback output (FB\_OUT) provide exceptional flexibility for possible output configurations. The PLL is ensured stable operation given that the  $V_{CO}$  is configured to run between 200 MHz and 480 MHz. This allows a wide range of output frequencies up to 125 MHz.

The phase detector compares the input reference clock to the external feedback input. For normal operation, the external feedback input (FB\_IN) is connected to the feedback output (FB\_OUT). The internal  $V_{CO}$  is running at multiples of the input reference clock set by FB\_SEL(0:2) and VCO\_SEL select inputs (refer to Frequency Table). The  $V_{CO}$  frequency is then divided to provide the required output frequencies. These dividers are set by SELA(0,1), SELB(0,1), SELC(0,1) select inputs (see the following Table). For situations where the  $V_{CO}$  needs to run at relatively low frequencies and hence might not be stable, assert VCO\_SEL low to divide the VCO frequency by 2. This maintains the desired output relationships but provides an enhanced PLL lock range.

The CY29972 is also capable of providing inverted output clocks. When INV\_CLK is asserted HIGH, QC2 and QC3 output clocks are inverted. These clocks could be used as feedback outputs to the CY29972 or a second PLL device to generate early or late clocks for a specific design. This inversion does not affect the output to output skew.

## Glitch-Free Output Frequency Transitions

Customarily, when output buffers have their internal counters changed "on the fly," their output clock periods will:

1. contain short or "runt" clock periods. These are clock cycles in which the cycle(s) are shorter in period than either the old or new frequencies to which the cycles are being transitioned.
2. contain stretched clock periods. These are clock cycles in which the cycle(s) are longer in period than either the old or new frequencies to which the cycles are being transitioned.

This device specifically includes logic to guarantee that runt and stretched clock pulses do not occur if the device logic levels of any or all of the following pins changed "on the fly" while it is operating: SELA, SELB, SELC, and VCO\_SEL.

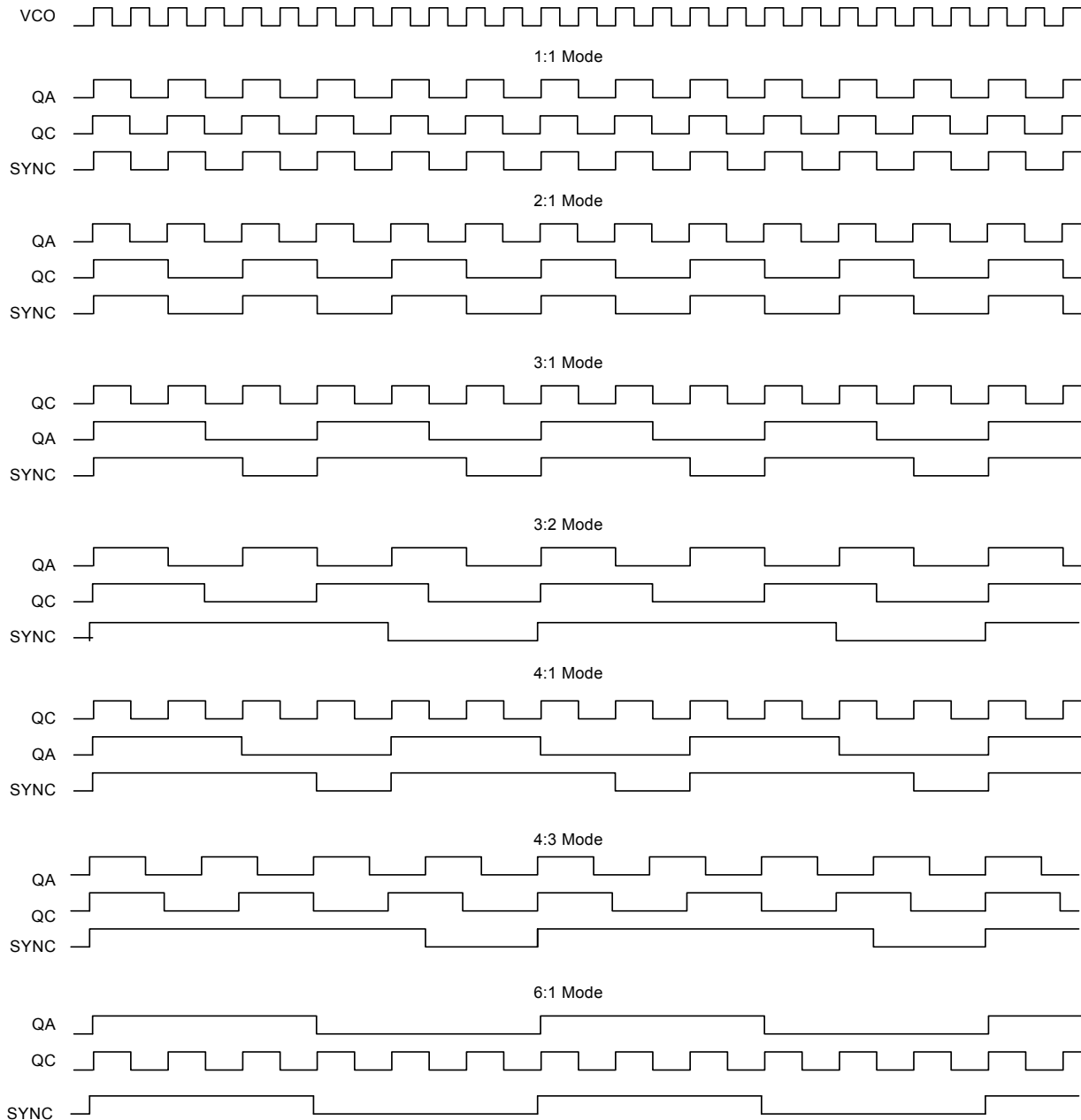
| VCO_SEL | SELA1 | SELA0 | QA     | SELB1 | SELB0 | QB     | SELC1 | SELC0 | QC     |
|---------|-------|-------|--------|-------|-------|--------|-------|-------|--------|
| 0       | 0     | 0     | VCO/8  | 0     | 0     | VCO/8  | 0     | 0     | VCO/4  |
| 0       | 0     | 1     | VCO/12 | 0     | 1     | VCO/12 | 0     | 1     | VCO/8  |
| 0       | 1     | 0     | VCO/16 | 1     | 0     | VCO/16 | 1     | 0     | VCO/12 |
| 0       | 1     | 1     | VCO/24 | 1     | 1     | VCO/20 | 1     | 1     | VCO/16 |
| 1       | 0     | 0     | VCO/4  | 0     | 0     | VCO/4  | 0     | 0     | VCO/2  |
| 1       | 0     | 1     | VCO/6  | 0     | 1     | VCO/6  | 0     | 1     | VCO/4  |
| 1       | 1     | 0     | VCO/8  | 1     | 0     | VCO/8  | 1     | 0     | VCO/6  |
| 1       | 1     | 1     | VCO/12 | 1     | 1     | VCO/10 | 1     | 1     | VCO/8  |

## SYNC Output

In situations where output frequency relationships are not integer multiples of each other, the SYNC output provides a signal for system synchronization. The CY29972 monitors the relationship between the QA and QC output clocks. It provides a LOW-going pulse, one period in duration, one period prior to the coincident

rising edges of the QA and QC outputs. The duration and placement of the pulse depend on the higher of the QA and QC output frequencies. The following timing diagram illustrates various waveforms for the SYNC output. Note that the SYNC output is defined for all possible combinations of QA and QC outputs, even though under some relationships the lower frequency clock could be used as a synchronizing signal.

**Figure 1. Timing Diagram**

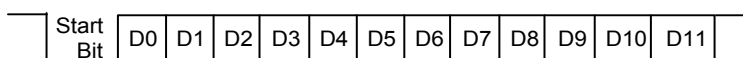


## Power Management

The individual output enable/freeze control of the CY29972 allows the user to implement unique power management schemes into the design. The outputs are stopped in the logic '0' state when the freeze control bits are activated. The serial input register contains one programmable freeze enable bit for 12 of the 14 output clocks. The QC0 and FB\_OUT outputs can not be frozen with the serial port, this avoids any potential lock up situation should an error occur in the loading of the serial data.

An output is frozen when a logic '0' is programmed and enabled when a logic '1' is written. The enabling and freezing of individual outputs is done in such a manner as to eliminate the possibility of partial "runt" clocks.

The serial input register is programmed through the SDATA input by writing a logic '0' start bit followed by 12 NRZ freeze enable bits. The period of each SDATA bit equals the period of the free running SCLK signal. The SDATA is sampled on the rising edge of SCLK.



D0-D3 are the control bits for QA0-QA3, respectively  
 D4-D7 are the control bits for QB0-QB3, respectively  
 D8-D10 are the control bits for QC1-QC3, respectively  
 D11 is the control bit for SYNC

**Table 2. Suggested Oscillator Crystal Parameters**

| Parameter        | Characteristic                    | Min. | Typ. | Max. | Unit   | Conditions                                    |
|------------------|-----------------------------------|------|------|------|--------|-----------------------------------------------|
| T <sub>C</sub>   | Frequency tolerance               | –    | –    | ±100 | PPM    | Note 3                                        |
| T <sub>S</sub>   | Frequency temperature stability   | –    | –    | ±100 | PPM    | (T <sub>A</sub> –10 to +60 °C) <sup>[3]</sup> |
| T <sub>A</sub>   | Aging                             | –    | –    | 5    | PPM/Yr | (first 3 years at 25 °C) <sup>[3]</sup>       |
| C <sub>L</sub>   | Load capacitance                  | –    | 20   | –    | pF     | The crystal's rated load. <sup>[3]</sup>      |
| R <sub>ESR</sub> | Effective series resistance (ESR) | –    | 40   | 80   | Ohms   | Note 4                                        |

## Absolute Maximum Ratings<sup>[5]</sup>

Maximum input voltage relative to V<sub>SS</sub>:..... V<sub>SS</sub> – 0.3 V

Maximum input voltage relative to V<sub>DD</sub>:..... V<sub>DD</sub> + 0.3 V

Storage temperature:..... –65 °C to +150 °C

Operating temperature: ..... –40 °C to +85 °C

Maximum ESD protection..... 2 kV

Maximum power supply:..... 5.5 V

Maximum input current: ..... ±20 mA

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, V<sub>IN</sub> and V<sub>OUT</sub> should be constrained to the range:

V<sub>SS</sub> < (V<sub>IN</sub> or V<sub>OUT</sub>) < V<sub>DD</sub>. Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>SS</sub> or V<sub>DD</sub>).

### Notes

3. For best performance and accurate frequencies from this device, It is recommended but not mandatory that the chosen crystal meet or exceed these specifications.
4. Larger values may cause this device to exhibit oscillator start-up problems.
5. **Multiple Supplies:** The voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.

**DC Parameters**  $V_{DD} = 2.9 \text{ V to } 3.6 \text{ V}$ ,  $V_{DDC} = 3.3 \text{ V} \pm 10\%$ ,  $T_A = -40^\circ\text{C to } +85^\circ\text{C}$ 

| Parameter | Description                        | Test Conditions                                          | Min      | Typ | Max      | Unit          |
|-----------|------------------------------------|----------------------------------------------------------|----------|-----|----------|---------------|
| $V_{IL}$  | Input Low voltage                  |                                                          | $V_{SS}$ | –   | 0.8      | V             |
| $V_{IH}$  | Input High voltage                 |                                                          | 2.0      | –   | $V_{DD}$ | V             |
| $I_{IL}$  | Input Low current <sup>[6]</sup>   |                                                          | –        | –   | –120     | $\mu\text{A}$ |
| $I_{IH}$  | Input High current                 |                                                          | –        | –   | 10       | $\mu\text{A}$ |
| $V_{OL}$  | Output Low voltage <sup>[7]</sup>  | $I_{OL} = 20 \text{ mA}$                                 | –        | –   | 0.5      | V             |
| $V_{OH}$  | Output High voltage <sup>[7]</sup> | $I_{OH} = -20 \text{ mA}$                                | 2.4      | –   | –        | V             |
| $I_{DDQ}$ | Quiescent supply current           |                                                          | –        | 10  | 15       | mA            |
| $I_{DDA}$ | PLL supply current                 | $V_{DD}$ only                                            | –        | 15  | 20       | mA            |
| $I_{DD}$  | Dynamic supply current             | QA and QB at 60 MHz, QC at 120 MHz, $CL = 30 \text{ pF}$ | –        | 225 | –        | mA            |
|           |                                    | QA and QB at 25 MHz, QC at 50 MHz, $CL = 30 \text{ pF}$  | –        | 125 | –        |               |
| $C_{IN}$  | Input pin capacitance              |                                                          | –        | 4   | –        | pF            |

**AC Parameters**  $V_{DD} = 2.9 \text{ V to } 3.6 \text{ V}$ ,  $V_{DDC} = 3.3 \text{ V} \pm 10\%$ ,  $T_A = -40^\circ\text{C to } +85^\circ\text{C}$ <sup>[8]</sup>

| Parameter          | Description                                          | Conditions                         | Min            | Typ       | Max            | Unit |
|--------------------|------------------------------------------------------|------------------------------------|----------------|-----------|----------------|------|
| $T_r / T_f$        | TCLK input rise/fall                                 |                                    | –              | –         | 3.0            | ns   |
| $f_{ref}$          | Reference input frequency                            |                                    | Note 9         | –         | Note 9         | MHz  |
| $f_{xtal}$         | Crystal Oscillator Frequency                         | see Table 2                        | 10             | –         | 25             | MHz  |
| $f_{refDC}$        | Reference input duty cycle                           |                                    | 25             | –         | 75             | %    |
| $f_{vco}$          | PLL VCO lock range                                   |                                    | 200            | –         | 480            | MHz  |
| $t_{lock}$         | Maximum PLL lock time                                |                                    | –              | –         | 10             | ms   |
| $T_r / T_f$        | Output clocks rise / fall time <sup>[10]</sup>       | 0.8 V to 2.0 V                     | 0.15           | –         | 1.2            | ns   |
| $f_{out}$          | Maximum Output Frequency                             | Q ( <sup>3</sup> 2)                | –              | –         | 125            | MHz  |
|                    |                                                      | Q ( <sup>3</sup> 4)                | –              | –         | 120            |      |
|                    |                                                      | Q ( <sup>3</sup> 6)                | –              | –         | 80             |      |
|                    |                                                      | Q ( <sup>3</sup> 8)                | –              | –         | 60             |      |
| $f_{outDC}$        | Output duty cycle <sup>[10]</sup>                    |                                    | TCYCLE/2 – 750 | –         | TCYCLE/2 + 750 | ps   |
| $t_{pZL}, t_{pZH}$ | Output enable time <sup>[10]</sup> (all outputs)     |                                    | 2              | –         | 10             | ns   |
| $t_{pLZ}, t_{pHZ}$ | Output disable time <sup>[10]</sup> (all outputs)    |                                    | 2              | –         | 8              | ns   |
| $TCCJ$             | Cycle to cycle jitter <sup>[10]</sup> (peak to peak) |                                    | –              | $\pm 100$ | –              | ps   |
| $TSKEW$            | Any output to any output skew <sup>[10,11]</sup>     |                                    | –              | 250       | 350            | ps   |
| $T_{pd}$           | Propagation delay <sup>[11,12]</sup>                 | $T_{CLK0}$ QFB = ( <sup>3</sup> 8) | –270           | 130       | 530            | ps   |
|                    |                                                      | $T_{CLK1}$                         | –330           | 70        | 470            |      |

**Notes**

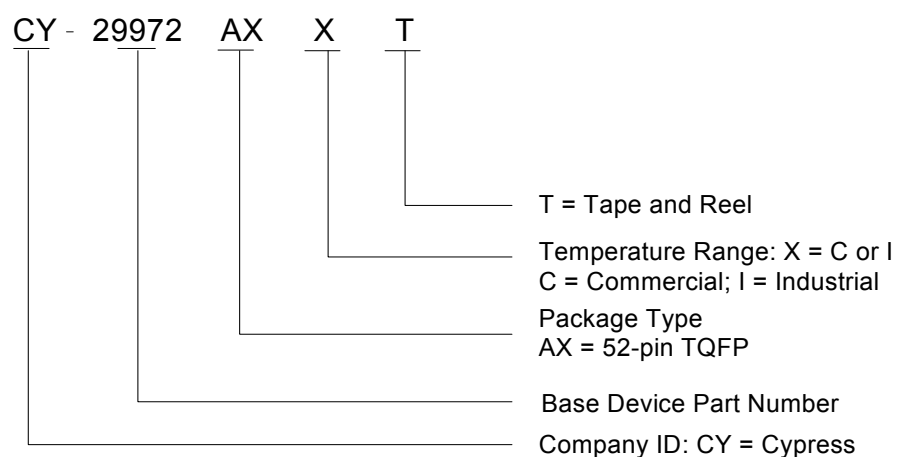
6. Inputs have pull-up/pull-down resistors that effect input current.
7. Driving series or parallel terminated 50  $\Omega$  (or 50  $\Omega$  to  $V_{DD/2}$ ) transmission lines.
8. Parameters are guaranteed by design and characterization. Not 100% tested in production.
9. Maximum and minimum input reference is limited by VCO lock range.
10. Outputs loaded with 30 pF each.
11. 50  $\Omega$  transmission line terminated into  $V_{DD/2}$ .
12.  $T_{pd}$  is specified for a 50-MHz input reference.  $T_{pd}$  does not include jitter.



## Ordering Information

| Part Number    | Package Type                | Production Flow              |
|----------------|-----------------------------|------------------------------|
| CY29972AI      | 52-pin TQFP                 | Industrial, -40 °C to +85 °C |
| CY29972AIT     | 52-pin TQFP - Tape and Reel | Industrial, -40 °C to +85 °C |
| <b>Pb-free</b> |                             |                              |
| CY29972AXI     | 52-pin TQFP                 | Industrial, -40 °C to +85 °C |
| CY29972AXIT    | 52-pin TQFP - Tape and Reel | Industrial, -40 °C to +85 °C |

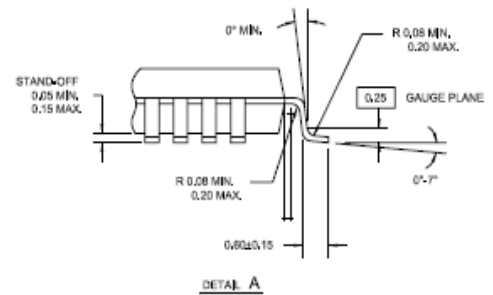
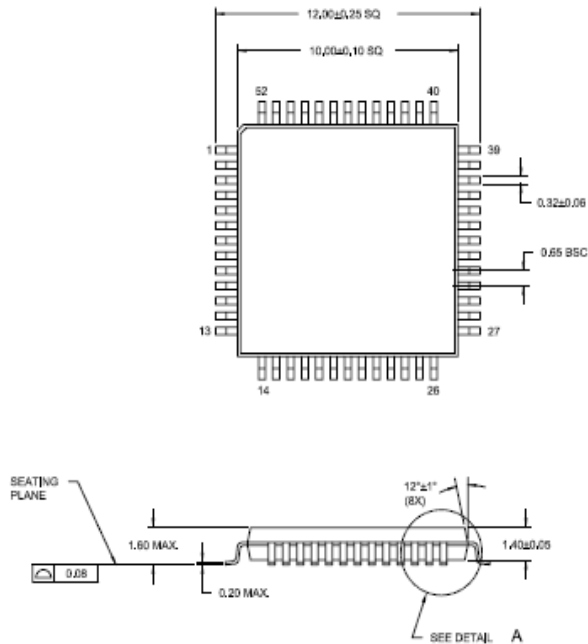
## Ordering Code Definition



## Package Drawing and Dimension

### 52-Lead Thin Plastic Quad Flat Pack (10 x 10 x 1.0 mm) A52B

DIMENSIONS ARE IN MILLIMETERS



51-85131 \*A

## Acronyms

| Acronym | Description         |
|---------|---------------------|
| I/O     | input/output        |
| PLL     | phase locked loop   |
| TQFP    | Thin quad flat pack |

## Document Conventions

### Units of Measure

| Symbol | Units of Measure |
|--------|------------------|
| °C     | degree celsius   |
| μA     | micro amperes    |
| mA     | milli amperes    |
| ms     | milli seconds    |
| MHz    | mega hertz       |
| ns     | nano seconds     |
| pF     | pico farad       |
| ps     | pico seconds     |
| V      | volts            |

## Document History Page

| Document Title: CY29972 3.3V, 125-MHz Multi-Output Zero Delay Buffer<br>Document Number: 38-07290 |         |            |                 |                                                                                                           |
|---------------------------------------------------------------------------------------------------|---------|------------|-----------------|-----------------------------------------------------------------------------------------------------------|
| REV.                                                                                              | ECN NO. | Issue Date | Orig. of Change | Description of Change                                                                                     |
| **                                                                                                | 111101  | 02/07/02   | BRK             | New Data Sheet                                                                                            |
| *A                                                                                                | 122882  | 12/22/02   | RBI             | Added power up requirements to Maximum Ratings                                                            |
| *B                                                                                                | 387764  | See ECN    | RGL             | Changed the package drawing and dimension to Cypress Standard<br>Added Pb-free devices                    |
| *C                                                                                                | 404340  | See ECN    | RGL             | Minor Change: corrected the package diagram                                                               |
| *D                                                                                                | 3270575 | 06/03/2011 | BASH            | Updated as per template<br>Updated package diagram 51-85131.<br>Added Acronyms and Units of Measure Table |

## Sales, Solutions, and Legal Information

### Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at [Cypress Locations](#).

### Products

|                          |                                                                                                                                      |
|--------------------------|--------------------------------------------------------------------------------------------------------------------------------------|
| Automotive               | <a href="http://cypress.com/go/automotive">cypress.com/go/automotive</a>                                                             |
| Clocks & Buffers         | <a href="http://cypress.com/go/clocks">cypress.com/go/clocks</a>                                                                     |
| Interface                | <a href="http://cypress.com/go/interface">cypress.com/go/interface</a>                                                               |
| Lighting & Power Control | <a href="http://cypress.com/go/powerpsoc">cypress.com/go/powerpsoc</a><br><a href="http://cypress.com/go/plc">cypress.com/go/plc</a> |
| Memory                   | <a href="http://cypress.com/go/memory">cypress.com/go/memory</a>                                                                     |
| Optical & Image Sensing  | <a href="http://cypress.com/go/image">cypress.com/go/image</a>                                                                       |
| PSoC                     | <a href="http://cypress.com/go/psoc">cypress.com/go/psoc</a>                                                                         |
| Touch Sensing            | <a href="http://cypress.com/go/touch">cypress.com/go/touch</a>                                                                       |
| USB Controllers          | <a href="http://cypress.com/go/USB">cypress.com/go/USB</a>                                                                           |
| Wireless/RF              | <a href="http://cypress.com/go/wireless">cypress.com/go/wireless</a>                                                                 |

### PSoC Solutions

[psoc.cypress.com/solutions](http://psoc.cypress.com/solutions)  
PSoC 1 | PSoC 3 | PSoC 5

© Cypress Semiconductor Corporation, 2005-2011. The information contained herein is subject to change without notice. Cypress Semiconductor Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in a Cypress product. Nor does it convey or imply any license under patent or other rights. Cypress products are not warranted nor intended to be used for medical, life support, life saving, critical control or safety applications, unless pursuant to an express written agreement with Cypress. Furthermore, Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress products in life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Any Source Code (software and/or firmware) is owned by Cypress Semiconductor Corporation (Cypress) and is protected by and subject to worldwide patent protection (United States and foreign), United States copyright laws and international treaty provisions. Cypress hereby grants to licensee a personal, non-exclusive, non-transferable license to copy, use, modify, create derivative works of, and compile the Cypress Source Code and derivative works for the sole purpose of creating custom software and or firmware in support of licensee product to be used only in conjunction with a Cypress integrated circuit as specified in the applicable agreement. Any reproduction, modification, translation, compilation, or representation of this Source Code except as specified above is prohibited without the express written permission of Cypress.

Disclaimer: CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Cypress reserves the right to make changes without further notice to the materials described herein. Cypress does not assume any liability arising out of the application or use of any product or circuit described herein. Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress' product in a life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Use may be limited by and subject to the applicable Cypress software license agreement.

Компания «Океан Электроники» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

Наши преимущества:

- Поставка оригинальных импортных электронных компонентов напрямую с производств Америки, Европы и Азии, а так же с крупнейших складов мира;
- Широкая линейка поставок активных и пассивных импортных электронных компонентов (более 30 млн. наименований);
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Помощь Конструкторского Отдела и консультации квалифицированных инженеров;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Поставка электронных компонентов под контролем ВП;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- При необходимости вся продукция военного и аэрокосмического назначения проходит испытания и сертификацию в лаборатории (по согласованию с заказчиком);
- Поставка специализированных компонентов военного и аэрокосмического уровня качества (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Actel, Aeroflex, Peregrine, VPT, Syfer, Eurofarad, Texas Instruments, MS Kennedy, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits, General Dynamics и др.);

Компания «Океан Электроники» является официальным дистрибьютором и эксклюзивным представителем в России одного из крупнейших производителей разъемов военного и аэрокосмического назначения «JONHON», а так же официальным дистрибьютором и эксклюзивным представителем в России производителя высокотехнологичных и надежных решений для передачи СВЧ сигналов «FORSTAR».



## JONHON

«JONHON» (основан в 1970 г.)

Разъемы специального, военного и аэрокосмического назначения:

(Применяются в военной, авиационной, аэрокосмической, морской, железнодорожной, горно- и нефтедобывающей отраслях промышленности)

«FORSTAR» (основан в 1998 г.)

ВЧ соединители, коаксиальные кабели,  
кабельные сборки и микроволновые компоненты:

(Применяются в телекоммуникациях гражданского и специального назначения, в средствах связи, РЛС, а так же военной, авиационной и аэрокосмической отраслях промышленности).



Телефон: 8 (812) 309-75-97 (многоканальный)

Факс: 8 (812) 320-03-32

Электронная почта: [ocean@oceanchips.ru](mailto:ocean@oceanchips.ru)

Web: <http://oceanchips.ru/>

Адрес: 198099, г. Санкт-Петербург, ул. Калинина, д. 2, корп. 4, лит. А