



MICROCHIP

TC4467/TC4468/TC4469

Logic-Input CMOS Quad Drivers

Features

- High Peak Output Current: 1.2 A
- Wide Operating Range:
 - 4.5 V to 18 V
- Symmetrical Rise/Fall Times: 25 nsec
- Short, Equal Delay Times: 75 nsec
- Latch-proof. Will Withstand 500 mA Inductive Kickback
- 3 Input Logic Choices:
 - AND / NAND / AND + Inv
- ESD Protection on All Pins: 2 kV

Applications

- General Purpose CMOS Logic Buffer
- Driving All Four MOSFETs in an H-Bridge
- Direct Small Motor Driver
- Relay or Peripheral Drivers
- CCD Driver
- Pin-Switching Network Driver

General Description

The TC4467/TC4468/TC4469 devices are a family of four-output CMOS buffers/MOSFET drivers with 1.2 A peak drive capability. Unlike other MOSFET drivers, these devices have two inputs for each output. The inputs are configured as logic gates: NAND (TC4467), AND (TC4468) and AND/INV (TC4469).

The TC4467/TC4468/TC4469 drivers can continuously source up to 250 mA into ground referenced loads. These devices are ideal for direct driving low current motors or driving MOSFETs in a H-bridge configuration for higher current motor drive (see Section 5.0 for details). Having the logic gates onboard the driver can help to reduce component count in many designs.

The TC4467/TC4468/TC4469 devices are very robust and highly latch-up resistant. They can tolerate up to 5 V of noise spiking on the ground line and can handle up to 0.5 A of reverse current on the driver outputs.

The TC4467/4468/4469 devices are available in commercial, industrial and military temperature ranges.

Package Types



TC4467/TC4468/TC4469

Logic Diagrams



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

| | |
|--|------------------------------------|
| Supply Voltage | +20 V |
| Input Voltage | (GND – 5 V) to ($V_{DD} + 0.3$ V) |
| Package Power Dissipation: ($T_A \leq 70^\circ\text{C}$) | |
| PDIP | 800 mW |
| CERDIP | 840 mW |
| SOIC | 760 mW |
| Package Thermal Resistance: | |
| CERDIP $R_{\theta J-A}$ | 100°C/W |
| CERDIP $R_{\theta J-C}$ | 23°C/W |
| PDIP $R_{\theta J-A}$ | 80°C/W |
| PDIP $R_{\theta J-C}$ | 35°C/W |
| SOIC $R_{\theta J-A}$ | 95°C/W |
| SOIC $R_{\theta J-C}$ | 28°C/W |
| Operating Temperature Range: | |
| C Version | 0°C to +70°C |
| E Version | -40°C to +85°C |
| M Version | -55°C to +125°C |
| Maximum Chip Temperature | +150°C |
| Storage Temperature Range | -65°C to +150°C |

†**Notice:** Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL SPECIFICATIONS

| Electrical Characteristics: Unless otherwise noted, $T_A = +25^\circ\text{C}$, with $4.5\text{ V} \leq V_{DD} \leq 18\text{ V}$. | | | | | | |
|--|----------|------------------|-----|----------|---------------|--|
| Parameters | Sym | Min | Typ | Max | Units | Conditions |
| Input | | | | | | |
| Logic 1, High Input Voltage | V_{IH} | 2.4 | — | V_{DD} | V | Note 3 |
| Logic 0, Low Input Voltage | V_{IL} | — | — | 0.8 | V | Note 3 |
| Input Current | I_{IN} | -1.0 | — | +1.0 | μA | $0\text{ V} \leq V_{IN} \leq V_{DD}$ |
| Output | | | | | | |
| High Output Voltage | V_{OH} | $V_{DD} - 0.025$ | — | — | V | $I_{LOAD} = 100\ \mu\text{A}$ (Note 1) |
| Low Output Voltage | V_{OL} | — | — | 0.15 | V | $I_{LOAD} = 10\ \text{mA}$ (Note 1) |
| Output Resistance | R_O | — | 10 | 15 | Ω | $I_{OUT} = 10\ \text{mA}$, $V_{DD} = 18\text{ V}$ |
| Peak Output Current | I_{PK} | — | 1.2 | — | A | |
| Continuous Output Current | I_{DC} | — | — | 300 | mA | Single Output |
| | | — | — | 500 | | Total Package |
| Latch-Up Protection Withstand Reverse Current | I | — | 500 | — | mA | $4.5\text{ V} \leq V_{DD} \leq 16\text{ V}$ |
| Switching Time (Note 1) | | | | | | |
| Rise Time | t_R | — | 15 | 25 | nsec | Figure 4-1 |
| Fall Time | t_F | — | 15 | 25 | nsec | Figure 4-1 |
| Delay Time | t_{D1} | — | 40 | 75 | nsec | Figure 4-1 |
| Delay Time | t_{D2} | — | 40 | 75 | nsec | Figure 4-1 |
| Power Supply | | | | | | |
| Power Supply Current | I_S | — | 1.5 | 4 | mA | Note 2 |
| Power Supply Voltage | V_{DD} | 4.5 | — | 18 | V | |

- Note 1:** Totem pole outputs should not be paralleled because the propagation delay differences from one to the other could cause one driver to drive high a few nanoseconds before another. The resulting current spike, although short, may decrease the life of the device. Switching times are ensured by design.
- Note 2:** When driving all four outputs simultaneously in the same direction, V_{DD} will be limited to 16 V. This reduces the chance that internal dV/dt will cause high-power dissipation in the device.
- Note 3:** The input threshold has approximately 50 mV of hysteresis centered at approximately 1.5 V. Input rise times should be kept below 5 μsec to avoid high internal peak currents during input transitions. Static input levels should also be maintained above the maximum, or below the minimum, input levels specified in the "Electrical Characteristics" to avoid increased power dissipation in the device.

TC4467/TC4468/TC4469

ELECTRICAL SPECIFICATIONS (OPERATING TEMPERATURES)

| Electrical Characteristics: Unless otherwise noted, over operating temperature range with $4.5\text{ V} \leq V_{DD} \leq 18\text{ V}$. | | | | | | |
|---|----------|------------------|-----|------|---------------|---|
| Parameters | Sym | Min | Typ | Max | Units | Conditions |
| Input | | | | | | |
| Logic 1, High Input Voltage | V_{IH} | 2.4 | — | — | V | Note 3 |
| Logic 0, Low Input Voltage | V_{IL} | — | — | 0.8 | V | Note 3 |
| Input Current | I_{IN} | -10 | — | 10 | μA | $0\text{ V} \leq V_{IN} \leq V_{DD}$ |
| Output | | | | | | |
| High Output Voltage | V_{OH} | $V_{DD} - 0.025$ | — | — | V | $I_{LOAD} = 100\ \mu\text{A}$ (Note 1) |
| Low Output Voltage | V_{OL} | — | — | 0.30 | V | $I_{LOAD} = 10\ \text{mA}$ (Note 1) |
| Output Resistance | R_O | — | 20 | 30 | Ω | $I_{OUT} = 10\ \text{mA}$, $V_{DD} = 18\ \text{V}$ |
| Peak Output Current | I_{PK} | — | 1.2 | — | A | |
| Continuous Output Current | I_{DC} | — | — | 300 | mA | Single Output |
| | | — | — | 500 | | Total Package |
| Latch-Up Protection Withstand Reverse Current | I | — | 500 | — | mA | $4.5\text{ V} \leq V_{DD} \leq 16\text{ V}$ |
| Switching Time (Note 1) | | | | | | |
| Rise Time | t_R | — | 15 | 50 | nsec | Figure 4-1 |
| Fall Time | t_F | — | 15 | 50 | nsec | Figure 4-1 |
| Delay Time | t_{D1} | — | 40 | 100 | nsec | Figure 4-1 |
| Delay Time | t_{D2} | — | 40 | 100 | nsec | Figure 4-1 |
| Power Supply | | | | | | |
| Power Supply Current | I_S | — | — | 8 | mA | Note 2 |
| Power Supply Voltage | V_{DD} | 4.5 | — | 18 | V | |

- Note 1:** Totem pole outputs should not be paralleled because the propagation delay differences from one to the other could cause one driver to drive high a few nanoseconds before another. The resulting current spike, although short, may decrease the life of the device. Switching times are ensured by design.
- Note 2:** When driving all four outputs simultaneously in the same direction, V_{DD} will be limited to 16 V. This reduces the chance that internal dv/dt will cause high-power dissipation in the device.
- Note 3:** The input threshold has approximately 50 mV of hysteresis centered at approximately 1.5 V. Input rise times should be kept below 5 μsec to avoid high internal peak currents during input transitions. Static input levels should also be maintained above the maximum, or below the minimum, input levels specified in the "Electrical Characteristics" to avoid increased power dissipation in the device.

TRUTH TABLE

| Part No. | TC4467 NAND | | | | TC4468 AND | | | | TC4469 AND/INV | | | |
|----------------|-------------|---|---|---|------------|---|---|---|----------------|---|---|---|
| Inputs A | H | H | L | L | H | H | L | L | H | H | L | L |
| Inputs B | H | L | H | L | H | L | H | L | H | L | H | L |
| Outputs TC446X | L | H | H | H | H | L | L | L | L | H | L | L |

Legend: H = High L = Low

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: $T_A = +25^\circ\text{C}$, with $4.5\text{ V} \leq V_{DD} \leq 18\text{ V}$.



FIGURE 2-1: Rise Time vs. Supply Voltage.



FIGURE 2-4: Fall Time vs. Supply Voltage.



FIGURE 2-2: Rise Time vs. Capacitive Load.



FIGURE 2-5: Fall Time vs. Capacitive Load.



FIGURE 2-3: Rise/Fall Times vs. Temperature.



FIGURE 2-6: Propagation Delay Time vs. Supply Voltage.

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2.0 TYPICAL PERFORMANCE CURVES (CONTINUED)

Note: $T_A = +25^\circ\text{C}$, with $4.5\text{ V} \leq V_{DD} \leq 18\text{ V}$.



FIGURE 2-7: Input Amplitude vs. Delay Times.



FIGURE 2-10: Propagation Delay Times vs. Temperatures.



FIGURE 2-8: Quiescent Supply Current vs. Supply Voltage.



FIGURE 2-11: Quiescent Supply Current vs. Temperature.



FIGURE 2-9: High-State Output Resistance.



FIGURE 2-12: Low-State Output Resistance.

2.0 TYPICAL PERFORMANCE CURVES (CONTINUED)

Note: (Load on single output only).



FIGURE 2-13: Supply Current vs. Capacitive Load.



FIGURE 2-16: Supply Current vs. Frequency.



FIGURE 2-14: Supply Current vs. Capacitive Load.



FIGURE 2-17: Supply Current vs. Frequency.



FIGURE 2-15: Supply Current vs. Capacitive Load.



FIGURE 2-18: Supply Current vs. Frequency.

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3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

| 14-Pin PDIP, CERDIP | 16-Pin SOIC (Wide) | Description |
|------------------------|-----------------------|---|
| Symbol | Symbol | |
| 1A | 1A | Input A for Driver 1, TTL/CMOS Compatible Input |
| 1B | 1B | Input B for Driver 1, TTL/CMOS Compatible Input |
| 2A | 2A | Input A for Driver 2, TTL/CMOS Compatible Input |
| 2B | 2B | Input B for Driver 2, TTL/CMOS Compatible Input |
| 3A | 3A | Input A for Driver 3, TTL/CMOS Compatible Input |
| 3B | 3B | Input B for Driver 3, TTL/CMOS Compatible Input |
| GND | GND | Ground |
| — | GND | Ground |
| 4A | 4A | Input A for Driver 4, TTL/CMOS Compatible Input |
| 4B | 4B | Input B for Driver 4, TTL/CMOS Compatible Input |
| 4Y | 4Y | Output for Driver 4, CMOS Push-Pull Output |
| 3Y | 3Y | Output for Driver 3, CMOS Push-Pull Output |
| 2Y | 2Y | Output for Driver 2, CMOS Push-Pull Output |
| 1Y | 1Y | Output for Driver 1, CMOS Push-Pull Output |
| V _{DD} | V _{DD} | Supply Input, 4.5 V to 18 V |
| — | V _{DD} | Supply Input, 4.5 V to 18 V |

4.0 DETAILED DESCRIPTION

4.1 Supply Bypassing

Large currents are required to charge and discharge large capacitive loads quickly. For example, charging a 1000 pF load to 18 V in 25 nsec requires 0.72 A from the device's power supply.

To ensure low supply impedance over a wide frequency range, a 1 μ F film capacitor in parallel with one or two low-inductance, 0.1 μ F ceramic disk capacitors with short lead lengths (<0.5 in.) normally provide adequate bypassing.

4.2 Grounding

The TC4467 and TC4469 contain inverting drivers. Potential drops developed in common ground impedances from input to output will appear as negative feedback and degrade switching speed characteristics. Instead, individual ground returns for input and output circuits, or a ground plane, should be used.

4.3 Input Stage

The input voltage level changes the no-load or quiescent supply current. The N-channel MOSFET input stage transistor drives a 2.5 mA current source load. With logic "0" outputs, maximum quiescent supply current is 4 mA. Logic "1" output level signals reduce quiescent current to 1.4 mA, maximum. Unused driver inputs must be connected to V_{DD} or V_{SS} . Minimum power dissipation occurs for logic "1" outputs.

The drivers are designed with 50 mV of hysteresis, which provides clean transitions and minimizes output stage current spiking when changing states. Input voltage thresholds are approximately 1.5 V, making any voltage greater than 1.5 V, up to V_{DD} , a logic "1" input. Input current is less than 1 μ A over this range.

4.4 Power Dissipation

The supply current versus frequency and supply current versus capacitive load characteristic curves will aid in determining power dissipation calculations. Microchip Technology's CMOS drivers have greatly reduced quiescent DC power consumption.

Input signal duty cycle, power supply voltage and load type influence package power dissipation. Given power dissipation and package thermal resistance, the maximum ambient operating temperature is easily calculated. The 14-pin plastic package junction-to-ambient thermal resistance is 83.3°C/W. At +70°C, the package is rated at 800 mW maximum dissipation. Maximum allowable chip temperature is +150°C.

Three components make up total package power dissipation:

1. Load-caused dissipation (P_L).
2. Quiescent power (P_Q).
3. Transition power (P_T).

A capacitive-load-caused dissipation (driving MOSFET gates), is a direct function of frequency, capacitive load and supply voltage. The power dissipation is:

EQUATION

$$P_L = fCV_S^2$$

f = Switching Frequency

C = Capacitive Load

V_S = Supply Voltage

A resistive-load-caused dissipation for ground-referenced loads is a function of duty cycle, load current and load voltage. The power dissipation is:

EQUATION

$$P_L = D(V_S - V_L)I_L$$

D = Duty Cycle

V_S = Supply Voltage

V_L = Load Voltage

I_L = Load Current

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A resistive-load-caused dissipation for supply-referenced loads is a function of duty cycle, load current and output voltage. The power dissipation is

EQUATION

$$P_L = DV_O I_L$$

D = Duty Cycle
 V_O = Device Output Voltage
 I_L = Load Current

Quiescent power dissipation depends on input signal duty cycle. Logic HIGH outputs result in a lower power dissipation mode, with only 0.6 mA total current drain (all devices driven). Logic LOW outputs raise the current to 4 mA maximum. The quiescent power dissipation is:

EQUATION

$$P_Q = V_S(D(I_H) + (1 - D)I_L)$$

I_H = Quiescent Current with all outputs LOW
 (4 mA max.)
 I_L = Quiescent Current with all outputs HIGH
 (0.6 mA max.)
 D = Duty Cycle
 V_S = Supply Voltage

Transition power dissipation arises in the complimentary configuration (TC446X) because the output stage N-channel and P-channel MOS transistors are ON simultaneously for a very short period when the output changes. The transition power dissipation is approximately:

EQUATION

$$P_T = fV_S(10 \times 10^{-9})$$

$C = 1000$ pF Capacitive Load
 $V_S = 15$ V
 $D = 50\%$
 $f = 200$ kHz
 $P_D =$ Package Power Dissipation
 $= P_L + P_Q + P_T$
 $= 45mW + 35mW + 30mW$
 $= 110mW$

Package power dissipation is the sum of load, quiescent and transition power dissipations. An example shows the relative magnitude for each term:

Maximum operating temperature is:

EQUATION

$$T_J - \theta_{JA}(P_D) = 141^\circ\text{C}$$

T_J = Maximum allowable junction temperature
 (+150°C)
 θ_{JA} = Junction-to-ambient thermal resistance
 (83.3°C/W) 14-pin plastic package

Note: Ambient operating temperature should not exceed +85°C for "EJD" device or +125°C for "MJD" device.



FIGURE 4-1: Switching Time Test Circuit.

5.0 APPLICATIONS INFORMATION



FIGURE 5-1: Stepper Motor Drive.



FIGURE 5-2: Quad Driver For H-bridge Motor Control.

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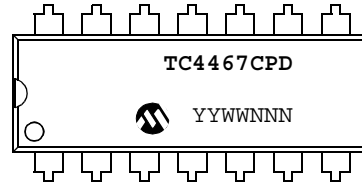
6.0 PACKAGING INFORMATION

6.1 Package Marking Information

14-Lead PDIP (300 mil)



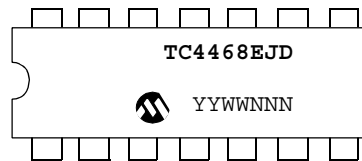
Example:



14-Lead CERDIP (300 mil)



Example:



16-Lead SOIC (300 mil)



Example:



| | | |
|----------------|--------|--|
| Legend: | XX...X | Customer-specific information |
| | Y | Year code (last digit of calendar year) |
| | YY | Year code (last 2 digits of calendar year) |
| | WW | Week code (week of January 1 is week '01') |
| | NNN | Alphanumeric traceability code |
| | (e3) | Pb-free JEDEC designator for Matte Tin (Sn) |
| | * | This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package. |

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

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14-Lead Plastic Dual In-line (P) – 300 mil (PDIP)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



| Units | | INCHES* | | | MILLIMETERS | | |
|----------------------------|------|---------|------|------|-------------|-------|-------|
| Dimension Limits | | MIN | NOM | MAX | MIN | NOM | MAX |
| Number of Pins | n | | 14 | | | 14 | |
| Pitch | p | | .100 | | | 2.54 | |
| Top to Seating Plane | A | .140 | .155 | .170 | 3.56 | 3.94 | 4.32 |
| Molded Package Thickness | A2 | .115 | .130 | .145 | 2.92 | 3.30 | 3.68 |
| Base to Seating Plane | A1 | .015 | | | 0.38 | | |
| Shoulder to Shoulder Width | E | .300 | .313 | .325 | 7.62 | 7.94 | 8.26 |
| Molded Package Width | E1 | .240 | .250 | .260 | 6.10 | 6.35 | 6.60 |
| Overall Length | D | .740 | .750 | .760 | 18.80 | 19.05 | 19.30 |
| Tip to Seating Plane | L | .125 | .130 | .135 | 3.18 | 3.30 | 3.43 |
| Lead Thickness | c | .008 | .012 | .015 | 0.20 | 0.29 | 0.38 |
| Upper Lead Width | B1 | .045 | .058 | .070 | 1.14 | 1.46 | 1.78 |
| Lower Lead Width | B | .014 | .018 | .022 | 0.36 | 0.46 | 0.56 |
| Overall Row Spacing | § eB | .310 | .370 | .430 | 7.87 | 9.40 | 10.92 |
| Mold Draft Angle Top | α | 5 | 10 | 15 | 5 | 10 | 15 |
| Mold Draft Angle Bottom | β | 5 | 10 | 15 | 5 | 10 | 15 |

* Controlling Parameter

§ Significant Characteristic

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed

.010" (0.254mm) per side.

JEDEC Equivalent: MS-001

Drawing No. C04-005

TC4467/TC4468/TC4469

14-Lead Ceramic Dual In-line – 300 mil (CERDIP)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>

14-Pin CERDIP (Narrow)



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16-Lead Plastic Small Outline (SO) – Wide, 300 mil (SOIC)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



| Dimension Limits | Units | INCHES* | | | MILLIMETERS | | |
|--------------------------|-------|---------|------|------|-------------|-------|-------|
| | | MIN | NOM | MAX | MIN | NOM | MAX |
| Number of Pins | n | | 16 | | | 16 | |
| Pitch | p | | .050 | | | 1.27 | |
| Overall Height | A | .093 | .099 | .104 | 2.36 | 2.50 | 2.64 |
| Molded Package Thickness | A2 | .088 | .091 | .094 | 2.24 | 2.31 | 2.39 |
| Standoff § | A1 | .004 | .008 | .012 | 0.10 | 0.20 | 0.30 |
| Overall Width | E | .394 | .407 | .420 | 10.01 | 10.34 | 10.67 |
| Molded Package Width | E1 | .291 | .295 | .299 | 7.39 | 7.49 | 7.59 |
| Overall Length | D | .398 | .406 | .413 | 10.10 | 10.30 | 10.49 |
| Chamfer Distance | h | .010 | .020 | .029 | 0.25 | 0.50 | 0.74 |
| Foot Length | L | .016 | .033 | .050 | 0.41 | 0.84 | 1.27 |
| Foot Angle | φ | 0 | 4 | 8 | 0 | 4 | 8 |
| Lead Thickness | c | .009 | .011 | .013 | 0.23 | 0.28 | 0.33 |
| Lead Width | B | .014 | .017 | .020 | 0.36 | 0.42 | 0.51 |
| Mold Draft Angle Top | α | 0 | 12 | 15 | 0 | 12 | 15 |
| Mold Draft Angle Bottom | β | 0 | 12 | 15 | 0 | 12 | 15 |

* Controlling Parameter
§ Significant Characteristic

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

JEDEC Equivalent: MS-013

Drawing No. C04-102

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7.0 REVISION HISTORY

Revision C (December 2012)

Added a note to each package outline drawing.

THE MICROCHIP WEB SITE

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Device: TC4467/4468/4469

Literature Number: DS21425C

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1. What are the best features of this document?

2. How does this document meet your hardware and software development needs?

3. Do you find the organization of this document easy to follow? If not, why?

4. What additions to the document do you think would enhance the structure and subject?

5. What deletions from the document could be made without affecting the overall usefulness?

6. Is there any incorrect or misleading information (what and where)?

7. How would you improve this document?

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

| <u>PART NO.</u> | <u>X</u> | <u>XX</u> |
|--------------------|---|-----------|
| Device | Temperature Range | Package |
| Device: | TC4467: 1.2A Quad MOSFET Driver, NAND TC4468: 1.2A Quad MOSFET Driver, AND TC4469: 1.2A Quad MOSFET Driver, AND/INV | |
| Temperature Range: | C = 0°C to +70°C E = -40°C to +85°C (CERDIP only) M = -55°C to +125°C (CERDIP only) | |
| Package: | PD = Plastic DIP, (300 mil body), 14-lead JD = Ceramic DIP, (300 mil body), 14-lead OE = SOIC (Wide), 16-lead OE713 = SOIC (Wide), 16-lead (Tape and Reel) | |

Examples:

- a) TC4467COE: Commercial Temperature, SOIC package.
- b) TC4467CPD: Commercial Temperature, PDIP package.
- c) TC4467MJD: Military Temperature, Ceramic DIP package.

- a) TC4468COE713: Tape and Reel, Commercial Temp., SOIC package.
- b) TC4468CPD: Commercial Temperature, PDIP package.

- a) TC4469COE: Commercial Temperature, SOIC package.
- b) TC4469CPD: Commercial Temperature, PDIP package.

Sales and Support

Data Sheets

Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Worldwide Site (www.microchip.com)

Please specify which device, revision of silicon and Data Sheet (include Literature #) you are using.

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NOTES:

Note the following details of the code protection feature on Microchip devices:

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