

74HC4538

Dual retriggerable precision monostable multivibrator

Rev. 5 — 17 March 2017

Product data sheet

1 General description

The 74HC4538 is a dual retriggerable-resettable monostable multivibrator. Each multivibrator has two trigger/retrigger inputs ($n\bar{A}$ and nB), a direct reset input ($n\bar{CD}$), two complementary outputs (nQ and $n\bar{Q}$), and two pins ($nREXT/CEXT$ and $nCEXT$) for connecting the external timing components C_{EXT} and R_{EXT} . Typical pulse width variation over temperature range is $\pm 0.2\%$. The device may be triggered by either the positive or the negative edges of the input pulse. The duration and accuracy of the output pulse are determined by the external timing components C_{EXT} and R_{EXT} . The output pulse width (T_W) is equal to $0.7 \times R_{EXT} \times C_{EXT}$. The linear design techniques guarantee precise control of the output pulse width. A LOW level at $n\bar{CD}$ terminates the output pulse immediately. Schmitt-trigger action in the trigger inputs makes the circuit highly tolerant to slower rise and fall times. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC} .

2 Features and benefits

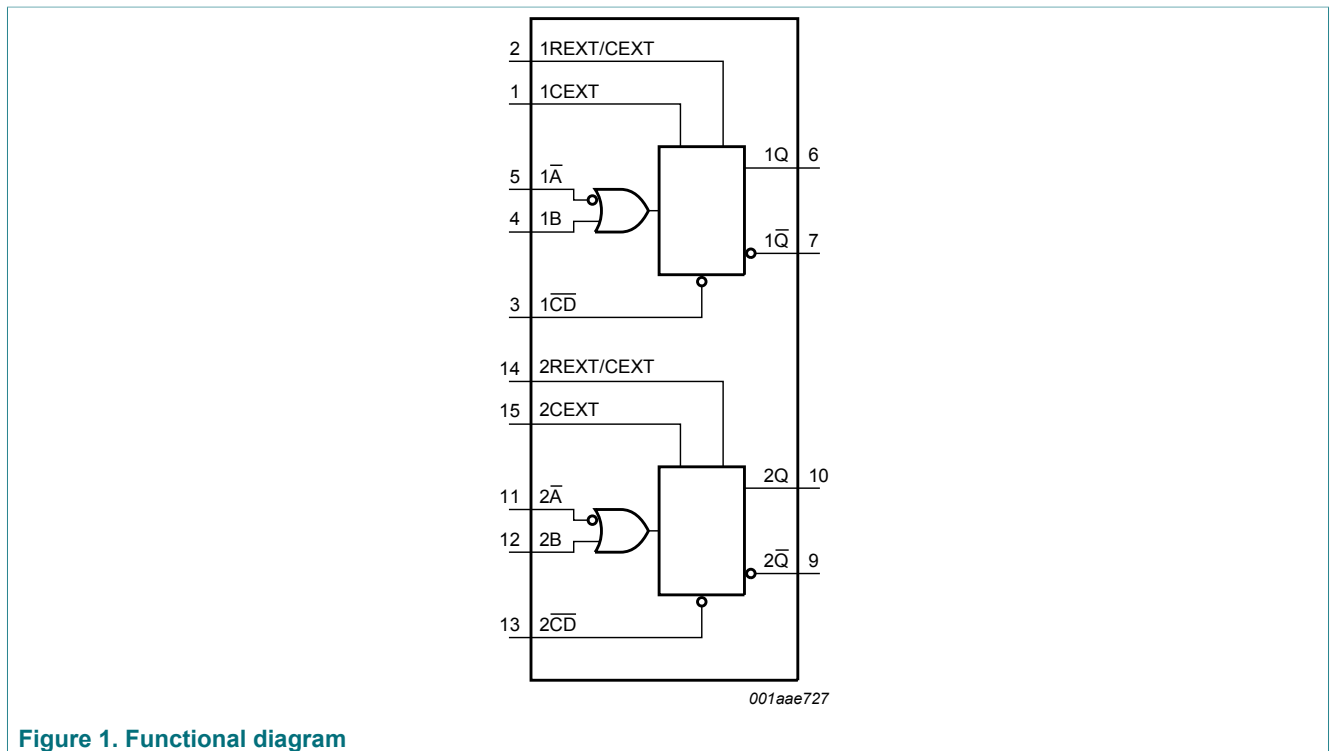
- Tolerant of slow trigger rise and fall times
- Separate reset inputs
- Triggering from falling or rising edge
- Complies with JEDEC standard no. 7A
- CMOS input levels:
- ESD protection:
 - HBM JESD22-A114F exceeds 2000 V
 - MM JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from $-40\text{ }^\circ\text{C}$ to $+85\text{ }^\circ\text{C}$ and from $-40\text{ }^\circ\text{C}$ to $+125\text{ }^\circ\text{C}$

3 Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74HC4538D	-40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74HC4538DB	-40 °C to +125 °C	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1
74HC4538PW	-40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1

4 Functional diagram



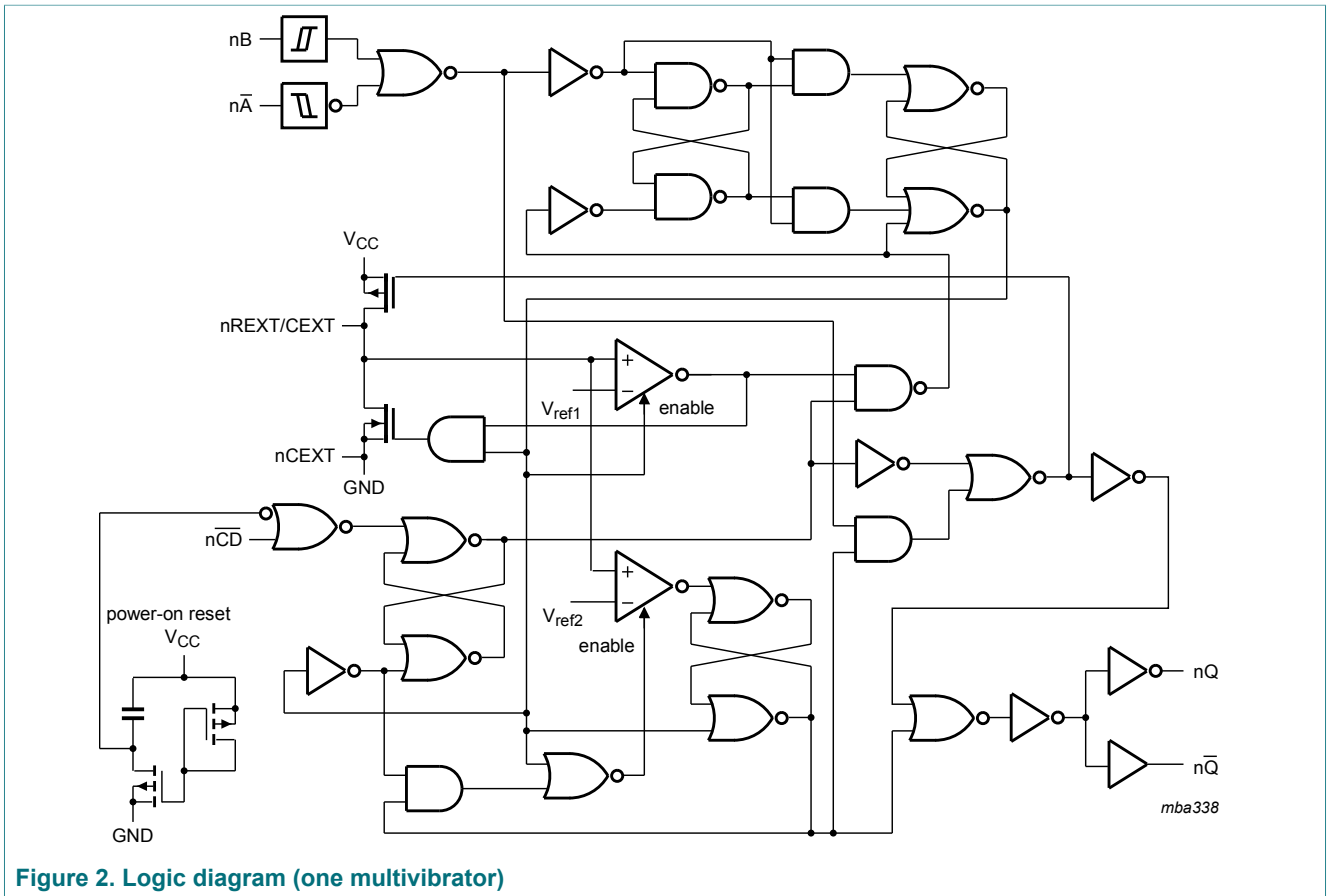


Figure 2. Logic diagram (one multivibrator)

5 Pinning information

5.1 Pinning

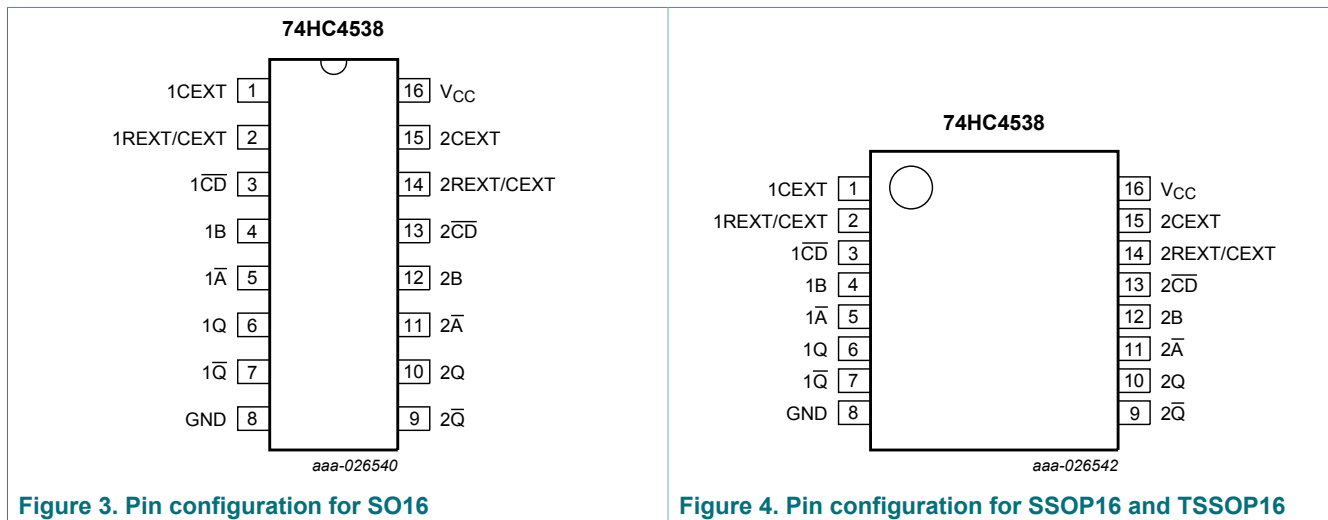


Figure 3. Pin configuration for SO16

Figure 4. Pin configuration for SSOP16 and TSSOP16

5.2 Pin description

Table 2. Pin description

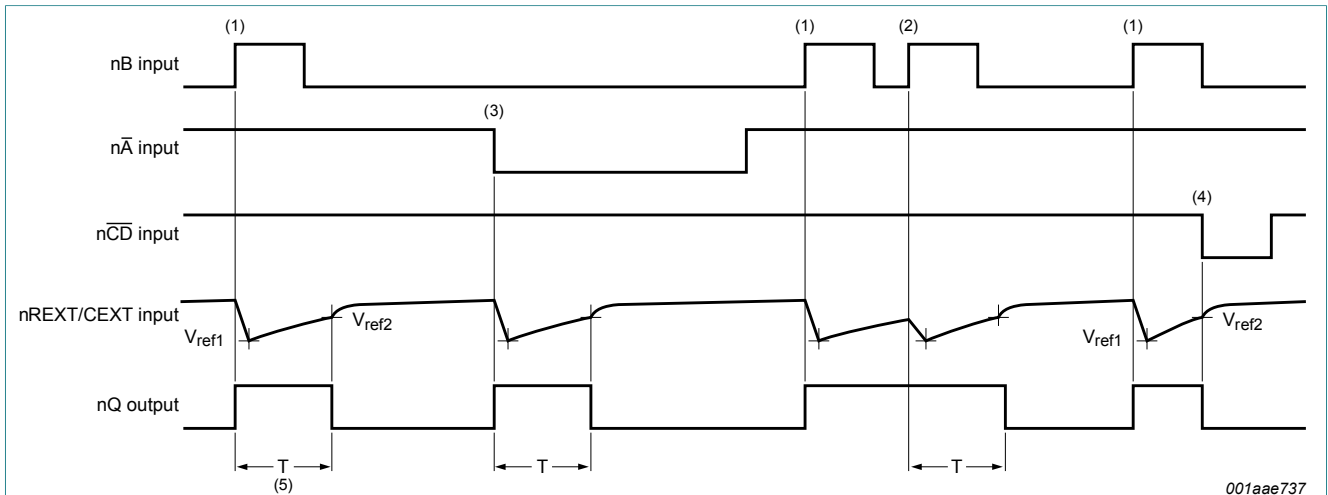
Symbol	Pin	Description
1CEXT, 2CEXT	1, 15	external capacitor connection (always connected to ground)
1REXT/CEXT, 2REXT/CEXT	2, 14	external capacitor/resistor connection
1 \overline{CD} , 2 \overline{CD}	3, 13	direct reset input (active LOW)
1B, 2B	4, 12	input (LOW to HIGH triggered)
1 \overline{A} , 2 \overline{A}	5, 11	input (HIGH to LOW triggered)
1Q, 2Q	6, 10	output
1 \overline{Q} , 2 \overline{Q}	7, 9	complementary output (active LOW)
GND	8	ground (0 V)
V _{CC}	16	supply voltage

6 Functional description

Table 3. Function table ^[1]

Inputs			Outputs	
n \bar{A}	nB	n \bar{CD}	nQ	n \bar{Q}
↓	L	H		
H	↑	H		
X	X	L	L	H

- [1] H = HIGH voltage level; L = LOW voltage level; X = don't care;
 ↑ = positive-going transition; ↓ = negative-going transition;
 = one HIGH level output pulse, with the pulse width determined by C_{EXT} and R_{EXT};
 = one LOW level output pulse, with the pulse width determined by C_{EXT} and R_{EXT}.



- (1) Positive edge triggering.
- (2) Positive edge re-triggering (pulse lengthening).
- (3) Negative edge triggering.
- (4) Reset (pulse shortening).
- (5) $T_W = 0.7 \times R_{EXT} \times C_{EXT}$ (see also [Figure 6](#)).

Figure 5. Timing diagram

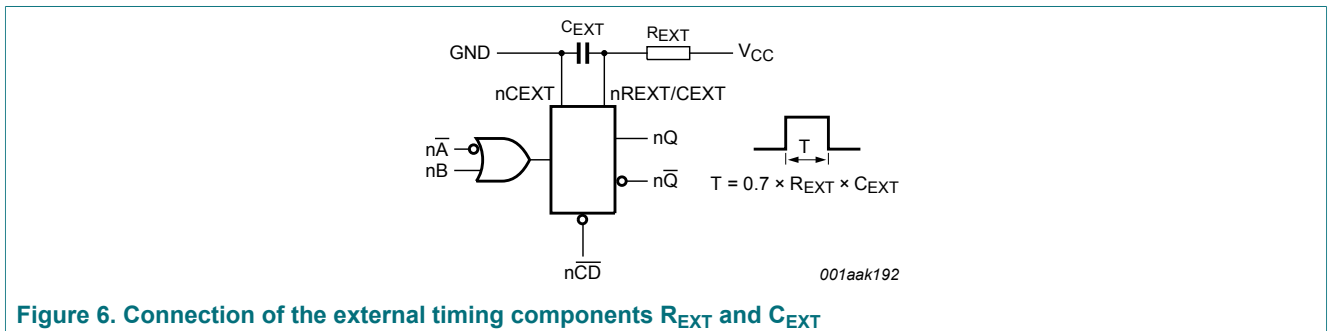


Figure 6. Connection of the external timing components R_{EXT} and C_{EXT}

7 Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+7.0	V
I_{IK}	input clamping current	$V_I < -0.5 \text{ V}$ or $V_I > V_{CC} + 0.5 \text{ V}$ [1]	-	± 20	mA
I_{OK}	output clamping current	$V_O < -0.5 \text{ V}$ or $V_O > V_{CC} + 0.5 \text{ V}$ [1]	-	± 20	mA
I_O	output current	$V_O = -0.5 \text{ V}$ to $V_{CC} + 0.5 \text{ V}$	-	± 25	mA
I_{CC}	supply current		-	+50	mA
I_{GND}	ground current		-50	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	$T_{amb} = -40 \text{ °C}$ to $+125 \text{ °C}$			
		SO16 package [2]	-	500	mW
		(T)SSOP16 package [3]	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] P_{tot} derates linearly with 8 mW/K above 70 °C.

[3] P_{tot} derates linearly with 5.5 mW/K above 60 °C.

8 Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		2.0	5.0	6.0	V
V_I	input voltage		0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	V
T_{amb}	ambient temperature		-40	-	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 2.0 \text{ V}$	-	-	625	ns/V
		$V_{CC} = 4.5 \text{ V}$	-	1.67	139	ns/V
		$V_{CC} = 6.0 \text{ V}$	-	-	83	ns/V

9 Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
V _{IH}	HIGH-level input voltage	V _{CC} = 2.0 V	1.5	1.2	-	1.5	-	1.5	-	V
		V _{CC} = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V
		V _{CC} = 6.0 V	4.2	3.2	-	4.2	-	4.2	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 2.0 V	-	0.8	0.5	-	0.5	-	0.5	V
		V _{CC} = 4.5 V	-	2.1	1.35	-	1.35	-	1.35	V
		V _{CC} = 6.0 V	-	2.8	1.8	-	1.8	-	1.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}								
		I _O = -20 µA; V _{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I _O = -20 µA; V _{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = -20 µA; V _{CC} = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	V
		I _O = -4.0 mA; V _{CC} = 4.5 V	3.98	4.32	-	3.84	-	3.7	-	V
		I _O = -5.2 mA; V _{CC} = 6.0 V	5.48	5.81	-	5.34	-	5.2	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}								
		I _O = 20 µA; V _{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 20 µA; V _{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 20 µA; V _{CC} = 6.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 4.0 mA; V _{CC} = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
		I _O = 5.2 mA; V _{CC} = 6.0 V	-	0.16	0.26	-	0.33	-	0.4	V
I _I	input leakage current	V _I = V _{CC} or GND; V _{CC} = 6.0 V	-	-	±0.1	-	±1	-	±1	µA
		pin nREXT/CEXT; V _I = 2.0 V or GND; other inputs at V _{CC} or GND; V _{CC} = 6.0 V ^[1]	-	-	±50	-	±500	-	±500	nA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 6.0 V	-	-	8.0	-	80	-	160	µA
C _I	input capacitance		-	3.5	-	-	-	-	-	pF

[1] This measurement can only be carried out after a trigger pulse is applied.

10 Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 9](#).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	Min	Max	
t _{PLH}	LOW to HIGH propagation delay	n \bar{A} , nB to nQ; see Figure 7								
		V _{CC} = 2.0 V	-	85	265	-	330	-	400	ns
		V _{CC} = 4.5 V	-	31	53	-	66	-	80	ns
		V _{CC} = 5.0 V; C _L = 15 pF	-	27	-	-	-	-	-	ns
		V _{CC} = 6.0 V	-	25	45	-	56	-	68	ns
		n $\bar{C}\bar{D}$ to n \bar{Q} ; see Figure 7								
		V _{CC} = 2.0 V	-	83	265	-	340	-	400	ns
		V _{CC} = 4.5 V	-	30	53	-	68	-	80	ns
t _{PHL}	HIGH to LOW propagation delay	n \bar{A} , nB to n \bar{Q} ; see Figure 7								
		V _{CC} = 2.0 V	-	83	265	-	330	-	400	ns
		V _{CC} = 4.5 V	-	30	53	-	66	-	80	ns
		V _{CC} = 5.0 V; C _L = 15 pF	-	27	-	-	-	-	-	ns
		V _{CC} = 6.0 V	-	24	45	-	56	-	68	ns
		n $\bar{C}\bar{D}$ to nQ; see Figure 7								
		V _{CC} = 2.0 V	-	80	265	-	330	-	400	ns
		V _{CC} = 4.5 V	-	29	53	-	66	-	80	ns
t _t	transition time	nQ and n \bar{Q} ; see Figure 7 ^[2]								
		V _{CC} = 2.0 V	-	19	75	-	95	-	119	ns
		V _{CC} = 4.5 V	-	7	15	-	19	-	22	ns
		V _{CC} = 6.0 V	-	6	13	-	16	-	19	ns
t _w	pulse width	n \bar{A} LOW; see Figure 8								
		V _{CC} = 2.0 V	80	17	-	100	-	120	-	ns
		V _{CC} = 4.5 V	16	6	-	20	-	24	-	ns
		V _{CC} = 6.0 V	14	5	-	17	-	20	-	ns
		nB HIGH; see Figure 8								
		V _{CC} = 2.0 V	80	17	-	100	-	120	-	ns
		V _{CC} = 4.5 V	16	6	-	20	-	24	-	ns
		V _{CC} = 6.0 V	14	5	-	17	-	20	-	ns
		n $\bar{C}\bar{D}$ LOW; see Figure 8								
		V _{CC} = 2.0 V	80	19	-	100	-	120	-	ns

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	Min	Max	
		V _{CC} = 4.5 V	16	7	-	20	-	24	-	ns
		V _{CC} = 6.0 V	14	6	-	17	-	20	-	ns
		nQ and nQ̄ HIGH or LOW; see Figure 8								
		V _{CC} = 5.0 V; C _{EXT} = 0.1 μF; R _{EXT} = 10 kΩ	630	700	770	602	798	595	805	μs
t _{rec}	recovery time	nCD to nA, nB; see Figure 8								
		V _{CC} = 2.0 V	35	6	-	45	-	55	-	ns
		V _{CC} = 4.5 V	7	2	-	9	-	11	-	ns
		V _{CC} = 6.0 V	6	2	-	8	-	9	-	ns
t _{trig}	retrigger time	nA, nB; see Figure 8 ; X = C _{EXT} / (4.5 × V _{CC})								
		V _{CC} = 2.0 V	-	455+X	-	-	-	-	-	ns
		V _{CC} = 4.5 V	-	80+X	-	-	-	-	-	ns
		V _{CC} = 6.0 V	-	55+X	-	-	-	-	-	ns
R _{EXT}	external timing resistor	V _{CC} = 2.0 V	10	-	1000	-	-	-	-	kΩ
		V _{CC} = 5.0 V	2	-	1000	-	-	-	-	kΩ
C _{EXT}	external timing capacitor		no limits							
C _{PD}	power dissipation capacitance	per multivibrator; V _I = GND to V _{CC}	^[3]	136	-	-	-	-	-	pF

[1] Typical values are measured at nominal supply voltage (V_{CC} = 3.3 V and V_{CC} = 5.0 V).

[2] t_r is the same as t_{THL} and t_{TLH}.

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

P_D = C_{PD} × V_{CC}² × f_i + Σ(C_L × V_{CC}² × f_o) + 0.48 × C_{EXT} × V_{CC}² × f_o + D × 0.8 × V_{CC} where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

Σ(C_L × V_{CC}² × f_o) = sum of the outputs;

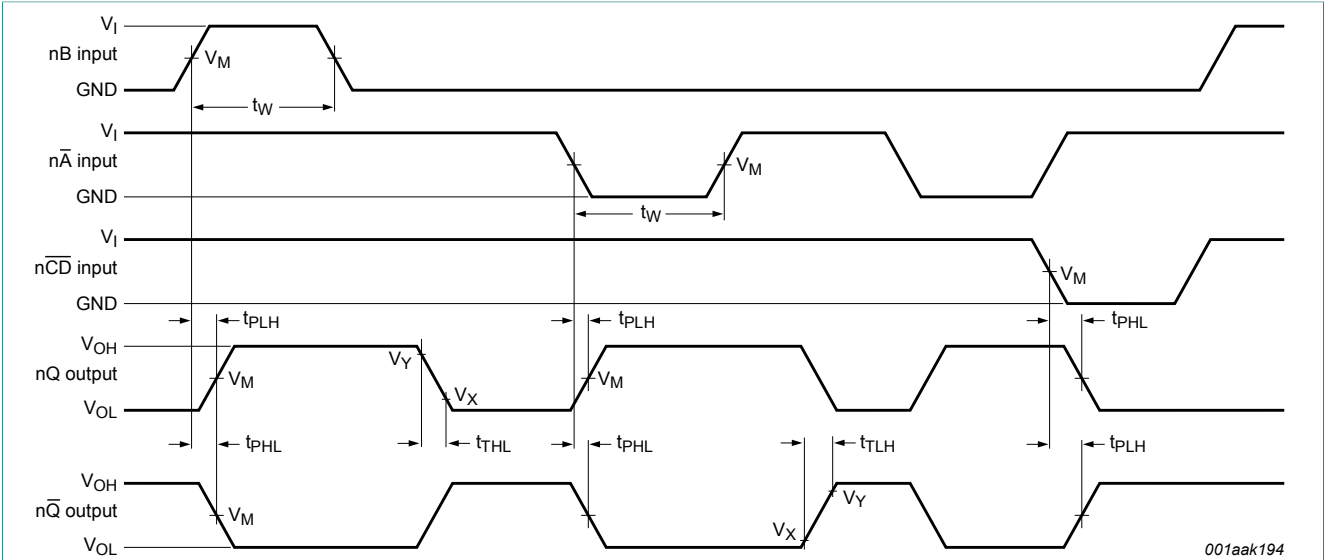
C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

D = duty cycle factor in %;

C_{EXT} = external timing capacitance in pF.

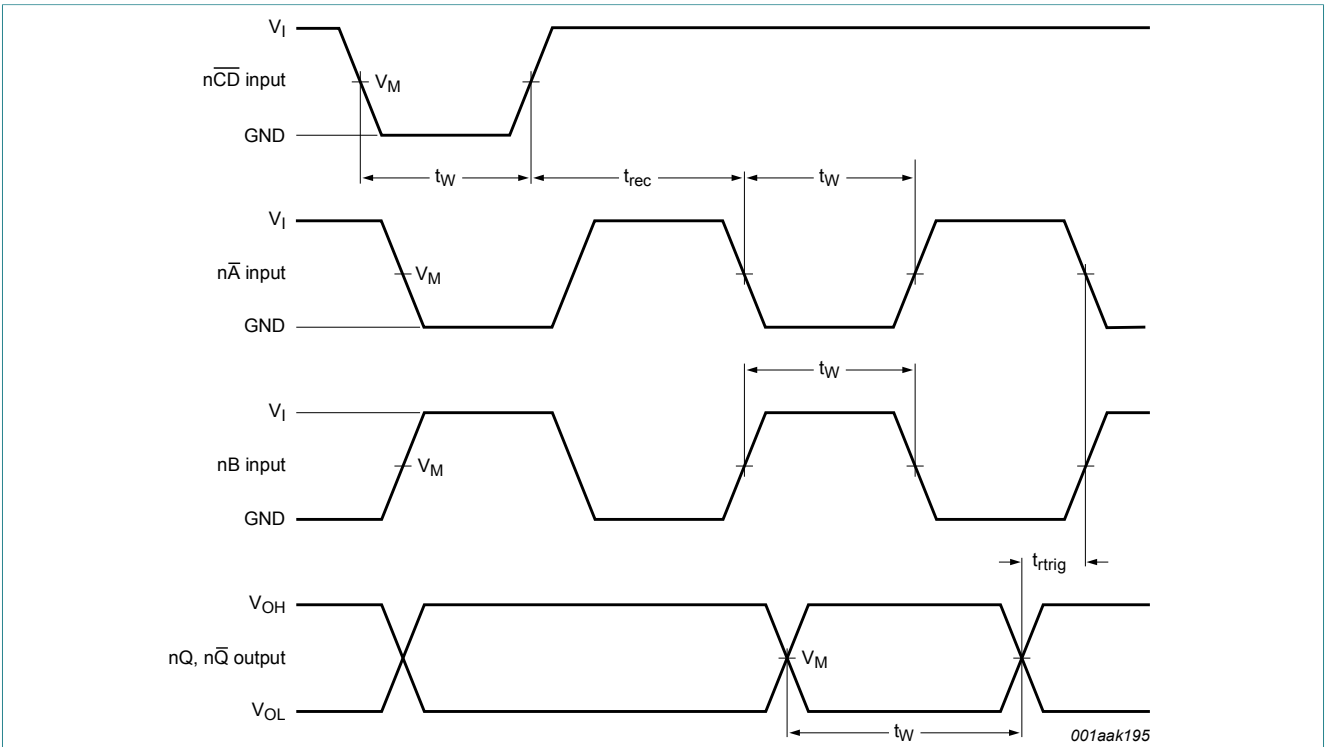
10.1 Waveforms and test circuit



Measurement points are given in [Table 8](#).

Logic levels: V_{OL} and V_{OH} are typical output levels that occur with the output load.

Figure 7. Waveforms showing propagation delays and transition times



Measurement points are given in [Table 8](#).

Logic levels: V_{OL} and V_{OH} are typical output levels that occur with the output load.

Figure 8. Waveforms showing nA, nB, nQ, nQ-bar pulse widths, recovery and retrigger times

Table 8. Measurement points

Input	Output		
V_M	V_M	V_X	V_Y
$0.5V_{CC}$	$0.5V_{CC}$	$0.1V_{CC}$	$0.9V_{CC}$

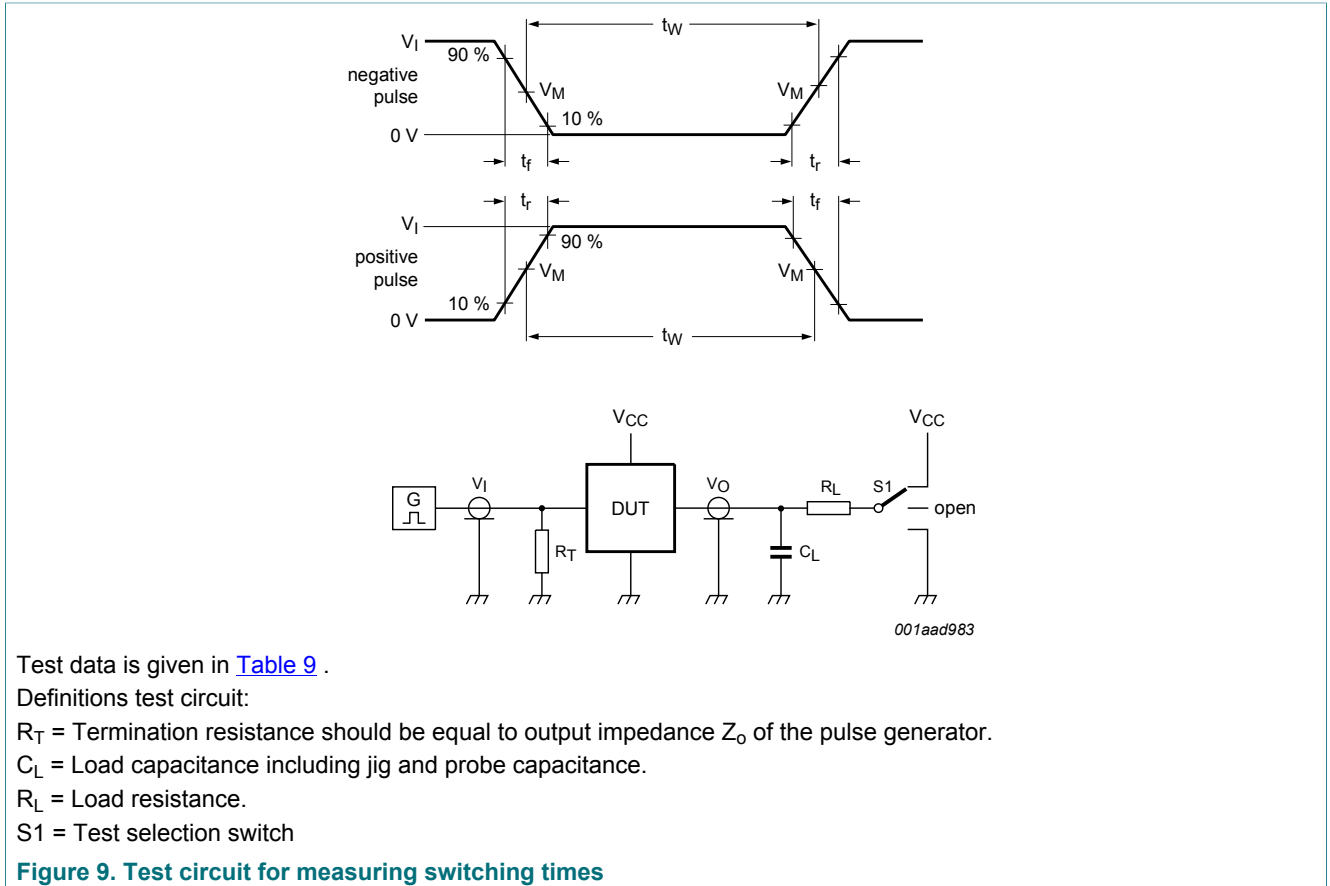


Table 9. Test data

Input		Load		S1 position
V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}
V_{CC}	6 ns	15 pF, 50 pF	1 kΩ	open

11 Application information

11.1 Power-down considerations

A large capacitor (C_{EXT}) may cause problems when powering-down the monostable due to energy stored in this capacitor. When a system containing this device is powered-down or rapid decrease of V_{CC} to zero occurs, the monostable may sustain damage, due to the capacitor discharging through the input protection diodes. To avoid this possibility, use a damping diode (D_{EXT}) preferably a germanium or Schottky type diode able to withstand large current surges and connect as shown in [Figure 10](#)

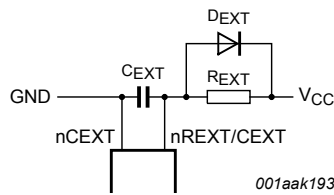
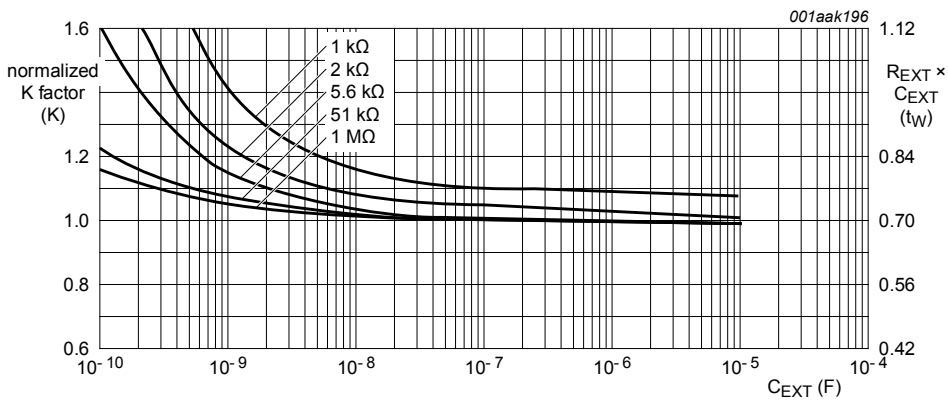


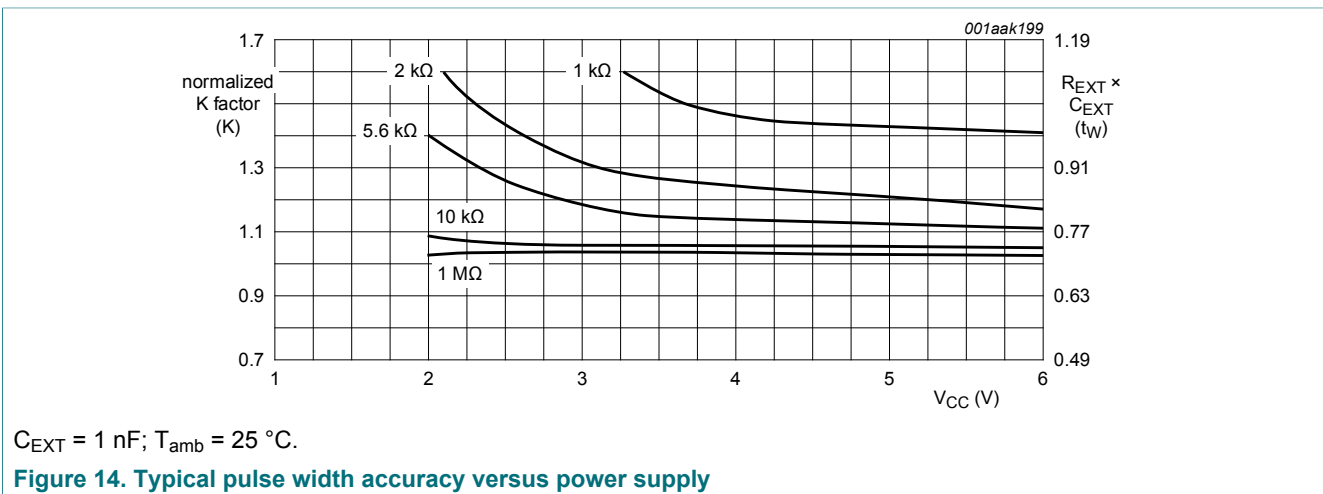
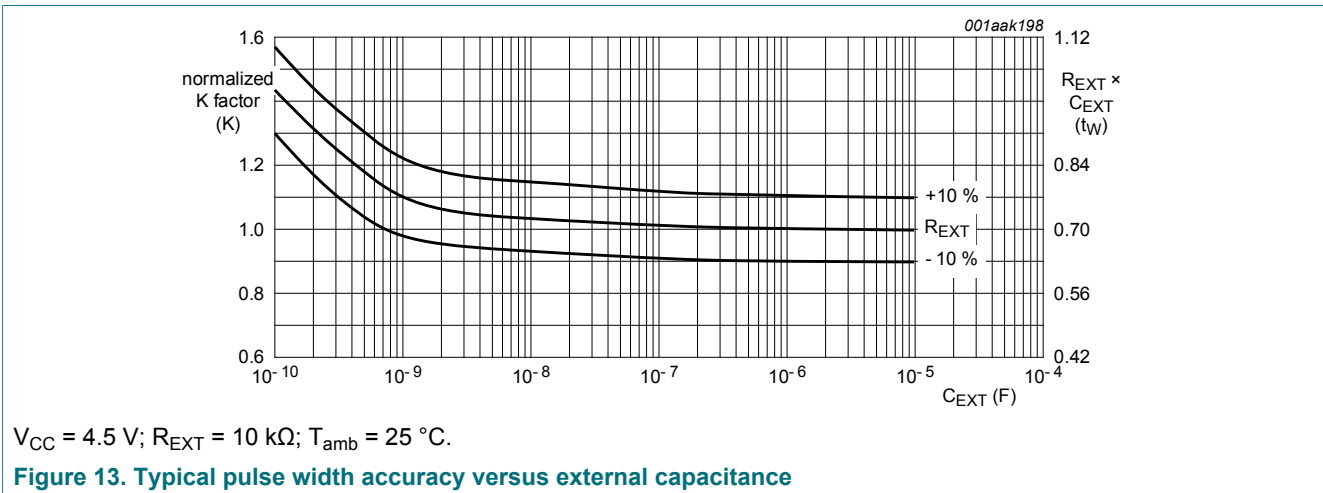
Figure 10. Power-down protection circuit

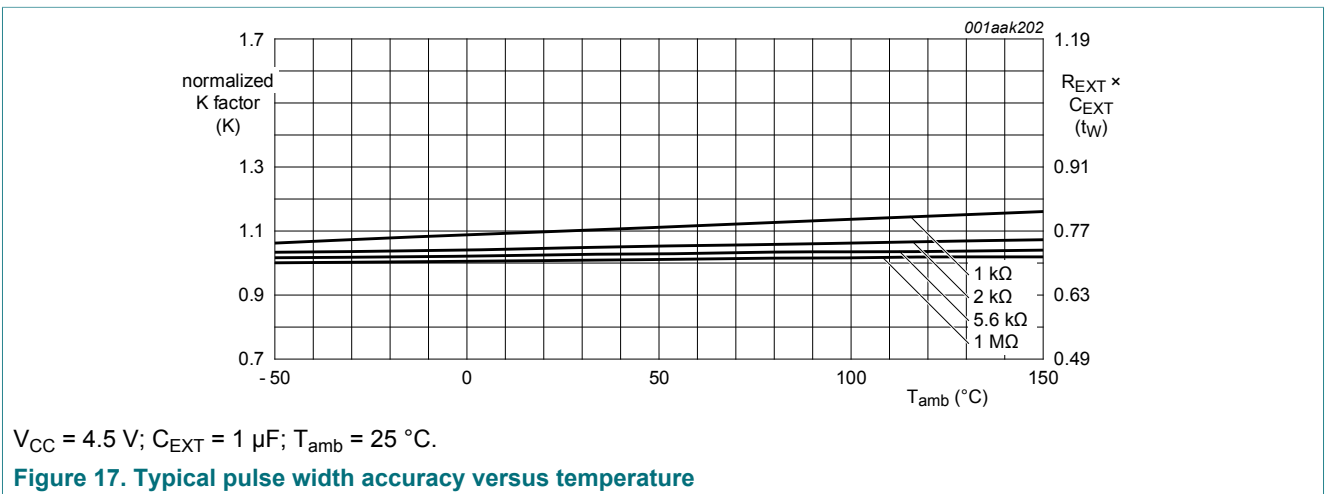
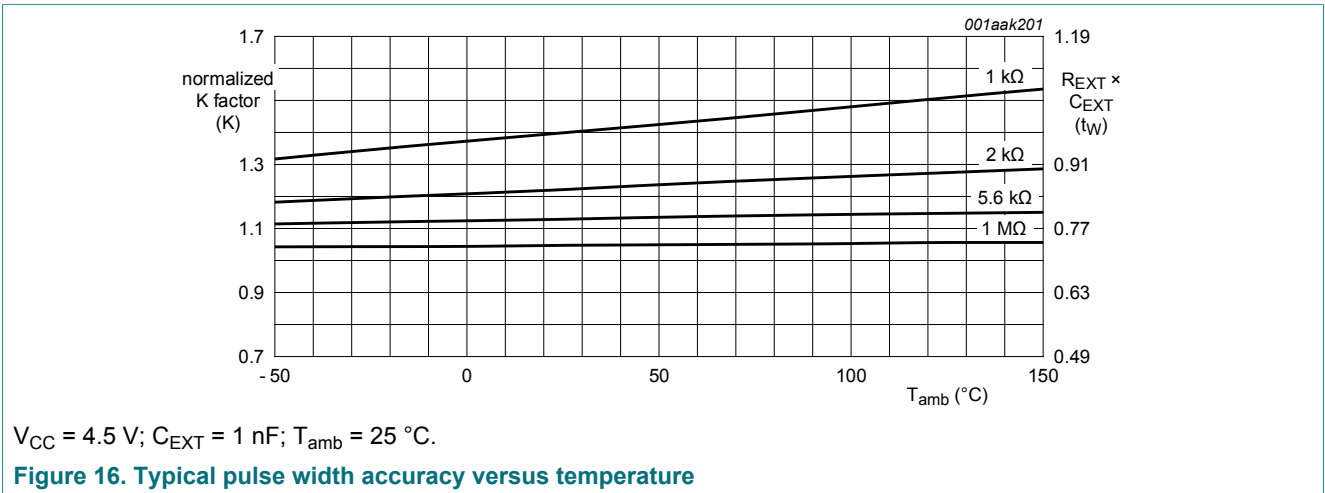
11.2 Graphs



$V_{CC} = 4.5 \text{ V}; T_{amb} = 25 \text{ }^\circ\text{C}.$

Figure 11. Typical pulse width accuracy versus external capacitance

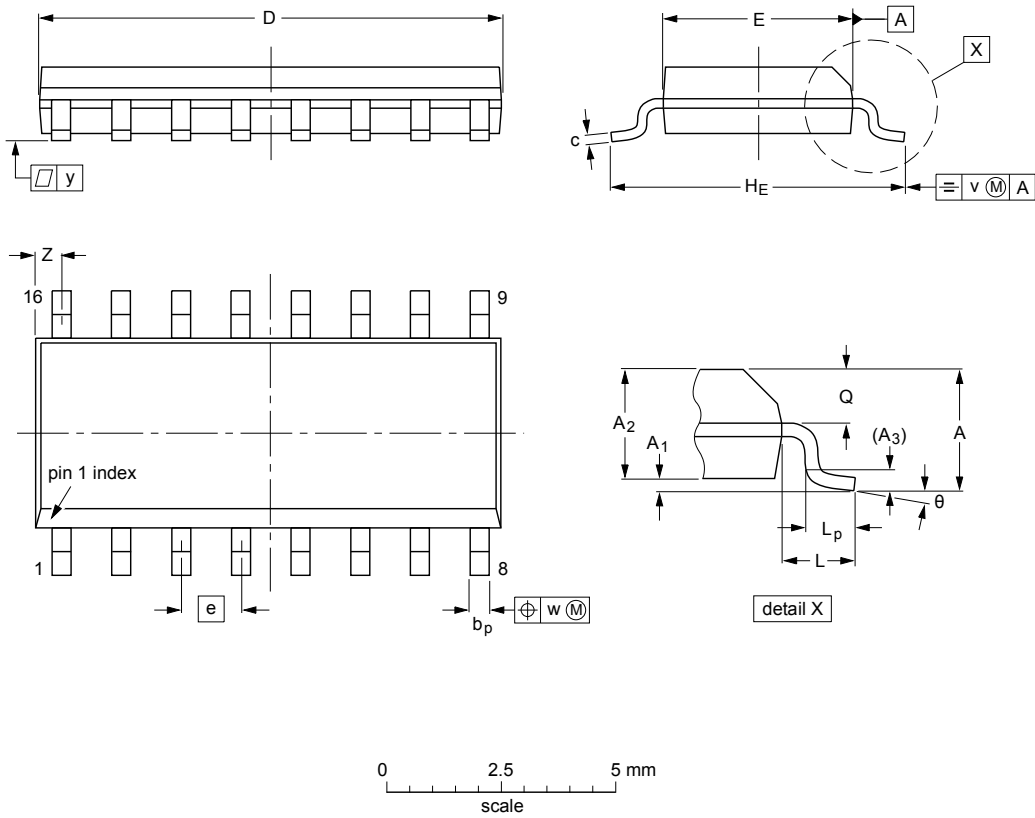




12 Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

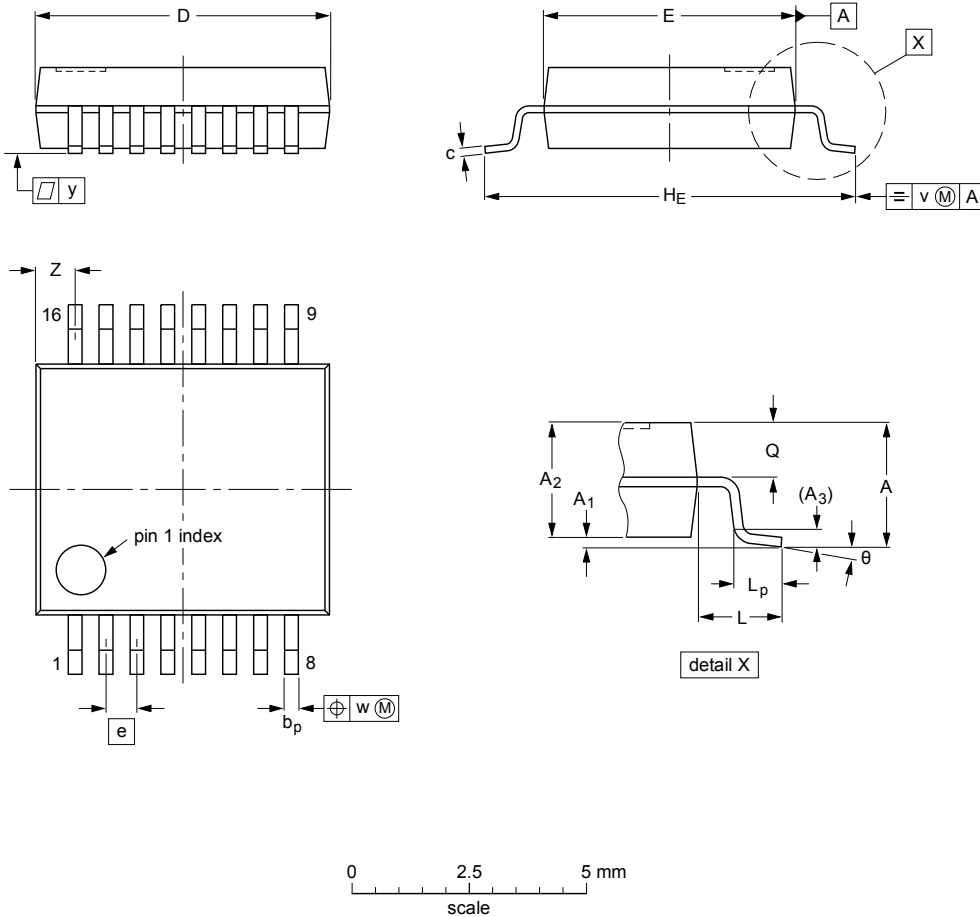
1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT109-1	076E07	MS-012			99-12-27 03-02-19

Figure 18. Package outline SOT109-1 (SO16)

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm

SOT338-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.00 0.55	8° 0°

Note

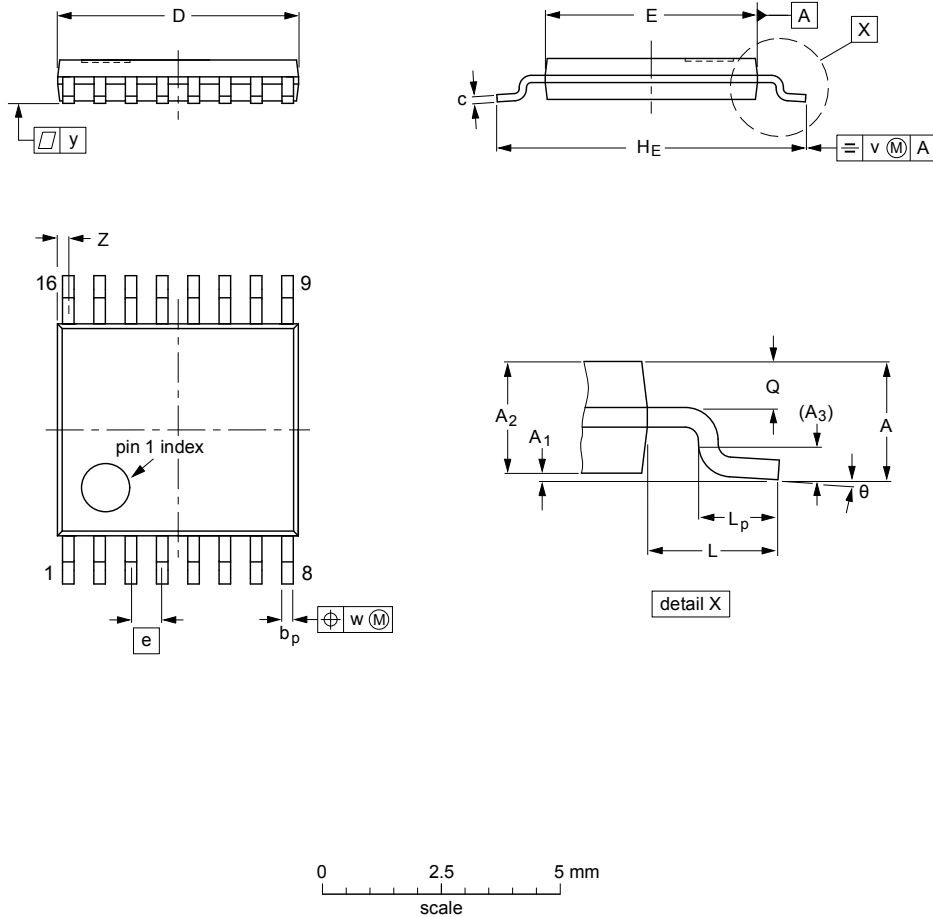
1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT338-1		MO-150				99-12-27 03-02-19

Figure 19. Package outline SOT338-1 (SSOP16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽²⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT403-1		MO-153				99-12-27 03-02-18

Figure 20. Package outline SOT403-1 (TSSOP16)

13 Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model

14 Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC4538 v.5	20170317	Product data sheet	-	74HC_HCT4538 v.4
Modifications:	<ul style="list-style-type: none"> Type numbers 74HCT4538D, 74HCT4538DB, 74HCT4538PW removed. Table 6: Maximum input leakage current for pins 1REXT/CEXT and 2REXT/CEXT changed. 			
74HC_HCT4538 v.4	20160224	Product data sheet	-	74HC_HCT4538 v.3
Modifications:	<ul style="list-style-type: none"> Type numbers 74HC4538N and 74HCT4538N (SOT38-4) removed. 			
74HC_HCT4538 v.3	20090608	Product data sheet	-	74HC_HCT4538_CNV v.2
Modifications:	<ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. Legal texts have been adapted to the new company name where appropriate. Pin names changed throughout. Section Section 7, Section 8 and Section 9 added, taken from the 74HC/T HCMOS Family characteristics/specification (March 1988). Test circuit added: Figure 9. Quick reference data incorporated in to Section 9 and Section 10. Package information added for DIP16, SO16, SSOP16 and TSSOP16 packages. 			
74HC_HCT4538_CNV v.2	19970902	Product specification	-	-

15 Legal information

15.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nexperia.com>.

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Contents

1	General description	1
2	Features and benefits	1
3	Ordering information	2
4	Functional diagram	2
5	Pinning information	4
5.1	Pinning	4
5.2	Pin description	4
6	Functional description	5
7	Limiting values	6
8	Recommended operating conditions	6
9	Static characteristics	7
10	Dynamic characteristics	8
10.1	Waveforms and test circuit	10
11	Application information	12
11.1	Power-down considerations	12
11.2	Graphs	12
12	Package outline	15
13	Abbreviations	18
14	Revision history	18
15	Legal information	19

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