STEREO 2W AUDIO POWER AMPLIFIER AA4002

General Description

The AA4002 is a monolithic stereo audio power amplifier including DC volume control, a selectable gain/bass boost, and stereo bridged audio power amplifiers, with the capability of producing 2W into 4Ω with THD+N less than 1%. The AA4002 is specially designed for Notebook PC, LCD monitor and portable media player.

The AA4002 features low power consumption in shutdown mode, power amplifier and headphone mute for maximum system flexibility and performance. It also provides thermal shutdown protection.

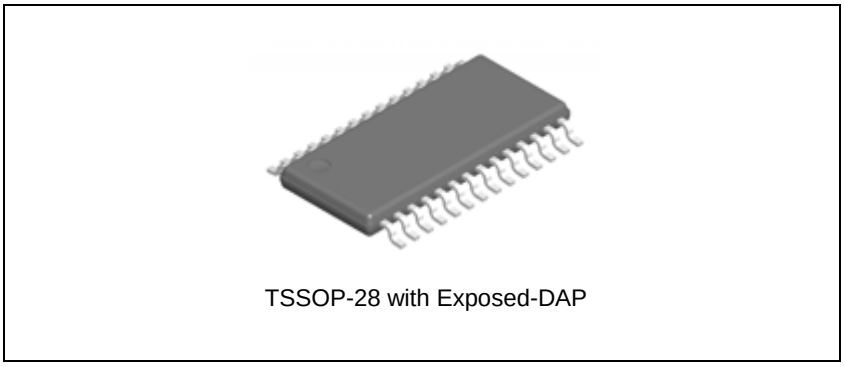
The AA4002 is available in TSSOP-28 with Exposed-DAP package.

Features

- DC Volume Control Interface, 0dB to -78dB, 31 Steps
- System Beep Detect
- Very Low Power Consumption in Shutdown Mode, I_{SD}=0.7μA
- Stereo Power Output for Speakers/Headphones with BTL Mode/SE Mode
- Selectable Internal/External Gain
- Bass Boost
- Pop Noise Suppression Circuit
- Thermal Shutdown Protection

Applications

- Notebook PC
- LCD monitor
- Portable DVD Player
- Portable Media Player
- Digital Photo Frame



TSSOP-28 with Exposed-DAP

Figure 1. Package Type of AA4002

Pin Configuration

G Package
(TSSOP-28 with Exposed-DAP)

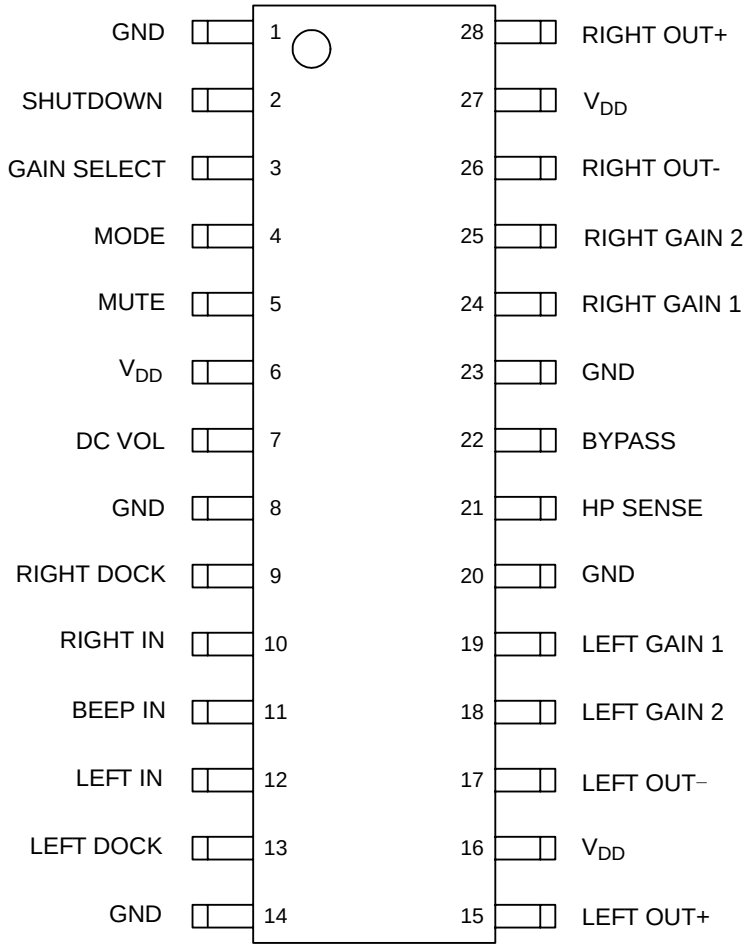


Figure 2. Pin Configuration of AA4002

Pin Description

Pin Number	Pin Name	Function
1, 8, 14, 20, 23	GND	Ground for circuitry.
2	SHUTDOWN	Shutdown mode control signal input, place entire IC in shutdown mode when held high, I_{DD}=0.7μA.
3	GAIN SELECT	Gain select input pin, logic high will switch the amplifier to external gain mode, and logic low will switch to internal unity gain.
4	MODE	Mode select input pin, fixed gain when logic L and gain adjustable mode when logic H.
5	MUTE	Mute control input pin, active H.
6, 16, 27	V_{DD}	Supply voltage input pin.
7	DC VOL	Volume control function input pin.
9	RIGHT DOCK	Right docking output pin.
10	RIGHT IN	Right channel audio input pin.
11	BEEP IN	Beep signal input pin.
12	LEFT IN	Left channel audio input pin.
13	LEFT DOCK	Left docking output pin.
15	LEFT OUT+	Left channel positive output pin.
17	LEFT OUT-	Left channel negative output pin.
18	LEFT GAIN 2	Connect pin 2 of the external gain setting resistor for left channel.
19	LEFT GAIN 1	Connect pin 1 of the external gain setting resistor for left channel.
21	HP SENSE	Headphone sense control pin.
22	BYPASS	Bypass pin.
24	RIGHT GAIN 1	Connect pin 1 of the external gain setting resistor for right channel.
25	RIGHT GAIN 2	Connect pin 2 of the external gain setting resistor for right channel.
26	RIGHT OUT-	Right channel negative output pin.
28	RIGHT OUT+	Right channel positive output pin.

Functional Block Diagram

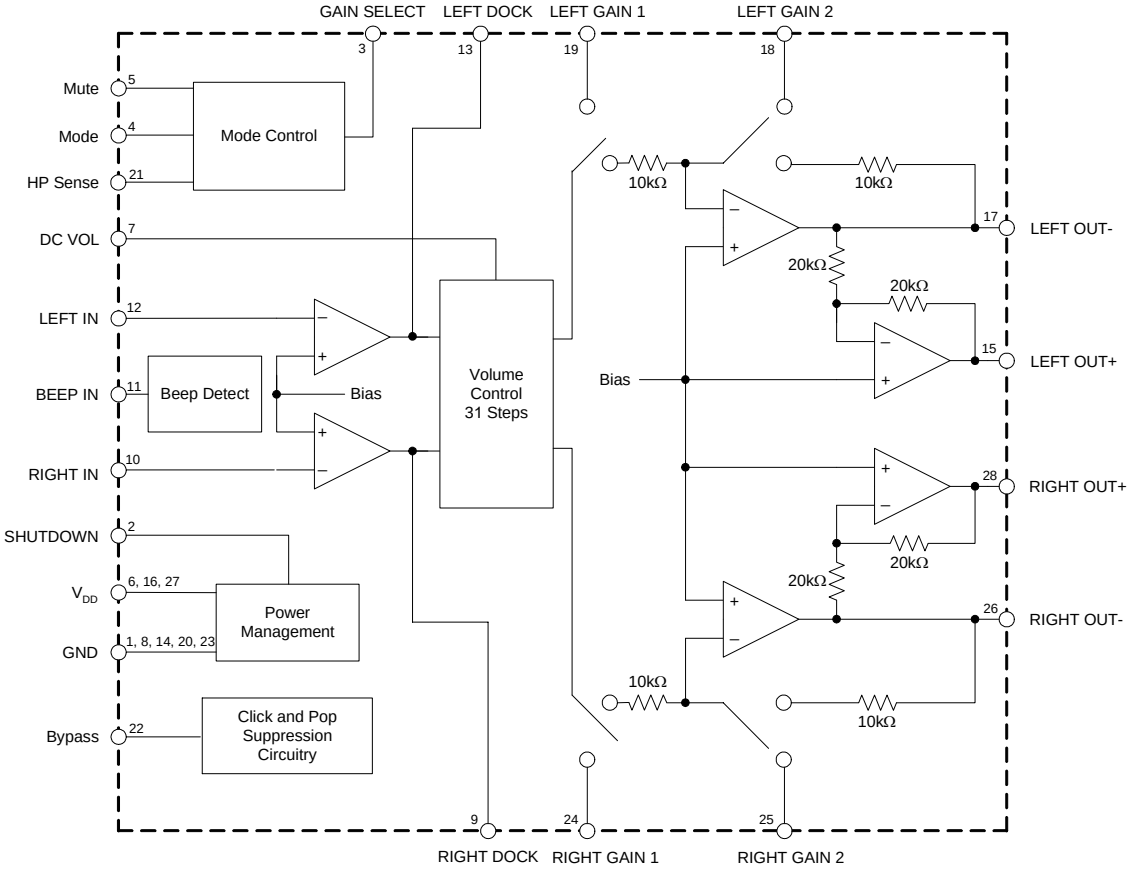


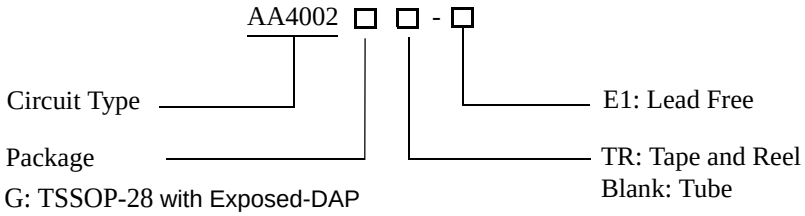
Figure 3. Functional Block Diagram of AA4002

Truth Table for Logic Inputs (Note 1)

Gain Sel	Mode	Headphone Sense	Mute	Shutdown	Output Stage Set To	DC Volume	Output Stage Configuration
0	0	0	0	0	Internal Gain	Fixed	BTL
0	0	1	0	0	Internal Gain	Fixed	SE
0	1	0	0	0	Internal Gain	Adjustable	BTL
0	1	1	0	0	Internal Gain	Adjustable	SE
1	0	0	0	0	External Gain	Fixed	BTL
1	0	1	0	0	External Gain	Fixed	SE
1	1	0	0	0	External Gain	Adjustable	BTL
1	1	1	0	0	External Gain	Adjustable	SE
X	X	X	1	0	Muted	X	Muted
X	X	X	X	1	Shutdown	X	X

Note 1: If system beep is detected on the BEEP IN pin, the system beep will be passed through the bridged amplifier regardless of the logic of the MUTE and HP SENSE pins.

Ordering Information



Package	Temperature Range	Part Number	Marking ID	Packing Type
TSSOP-28 with Exposed-DAP	-40 to 85 ℃	AA4002G-E1	AA4002G-E1	Tube
		AA4002GTR-E1	AA4002G-E1	Tape & Reel

BCD Semiconductor's Pb-free products, as designated with "E1" suffix in the part number, are RoHS compliant.

Absolute Maximum Ratings (Note 2)

Parameter	Symbol	Value	Unit
Supply Voltage	V_{DD}	6.0	V
Input Voltage	V_{IN}	-0.3 to V_{DD} + 0.3	V
Power Dissipation	P_D	Internally limited	
ESD (Machine Model)	ESD	200 (Note 3)	V
Operating Junction Temperature	T_J	150	^oC
Storage Temperature	T_{STG}	-65 to 150	^oC
Lead Temperature (Soldering 10s)	T_L	260	^oC
Package Thermal Resistance	$R_{\theta JA}$ (Note 4)	45	$^oC/W$

Note 2: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operation is not implied. Exposure to "Absolute Maximum Ratings" for extended periods may affect device reliability.
Note 3: This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.
Note 4: The Chip is soldered to 200mm^2 copper of 1oz. with 12x0.5mm vias.

Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{DD}	2.7	5.5	V
Operating Temperature	T_A	-40	85	^oC

Electrical Characteristics

(V_{DD}=5V, T_A=25°C, unless otherwise specified.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Standby and Logical Section						
Supply Voltage	V_{DD}		2.7		5.5	V
Quiescent Power Supply Current	I_{DD}	V_{IN}=0V, I_{OUT}=0A		11	30	mA
Shutdown Current	I_{SD}	$V_{SHUTDOWN}$=V_{DD}		0.7	2.0	μA
Headphone Sense High Input Voltage	V_{IH}		4			V
Headphone Sense Low Input Voltage	V_{IL}				0.8	V
(Mute, Shutdown, Mode, Gain Select) High Input Voltage	V_{IH}		3			V
(Mute, Shutdown, Mode, Gain Select) Low Input Voltage	V_{IL}				1	V
Volume Attenuators Section						
Attenuator Range	C_{RANGE}	V_{VOL}=5V (DC), No load			± 0.75	dB
		V_{VOL}=0V (DC), BTL and SE Mode	-75			dB
Mute Attenuation	A_M	V_{MUTE}=5V, BTL Mode	-78			dB
		V_{MUTE}=5V, SE Mode	-78			dB
Single-ended (SE) Mode Section						
Output Power	P_{OUT}	THD=1%, f=1kHz, R_L=32Ω		85		mW
		THD=10%, f=1kHz, R_L=32Ω		95		
Total Harmonic Distortion + Noise	THD+N	V_{OUT}=1V_{RMS}, f=1kHz, R_L=10KΩ, A_{VD}=1		0.065		%
Power Supply Rejection Ratio	PSRR	C_B=1.0μF, f=120kHz, R_L=32Ω, V_{RIPPLE}=200mV_{RMS}		58		dB
Signal to Noise Ratio	SNR	P_{OUT}=75mW, R_L=32Ω, A-Wtd Filter		102		dB
Channel Separation		f=1kHz, C_B=1.0μF		65		dB
BTL Mode Section						
Output Offset Voltage	V_{OS}	V_{IN}=0V, No load		± 5	± 50	mV
Output Power	P_{OUT}	THD+N=1%, f=1kHz, R_L=4Ω, LPF=22kHz		2		W
		THD+N=1%, f=1kHz, R_L=8Ω,	1.0	1.1		
		THD+N=10%, f=1kHz, R_L=8Ω,		1.5		
Total Harmonic Distortion + Noise	THD+N	P_{OUT}=1.0W, R_L=4Ω, A_{VD}=2 20Hz<f<20kHz		0.3		%
Power Supply Rejection Ratio	PSRR	C_B=1.0μF, f=120Hz, V_{RIPPLE}=200mV_{RMS}, R_L=8Ω		74		dB

Electrical Characteristics (Continued)

(V_{DD}=5V, T_A=25°C, unless otherwise specified.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
BTL Mode Section (Continued)						
Signal to Noise Ratio	SNR	P_{OUT}=1.1W, R_L=8Ω, A-Wtd Filter		93		dB
Channel Separation		C_B=1.0μF, f=1kHz		70		dB

Typical Performance Characteristics

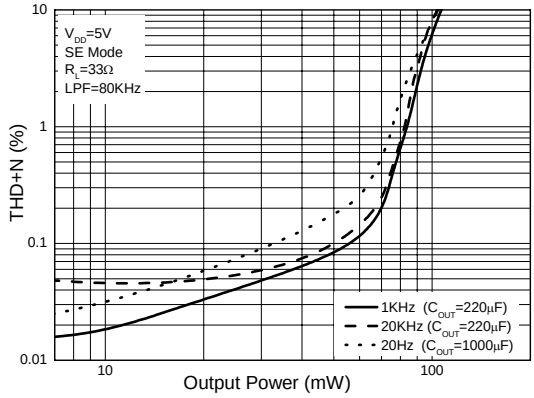


Figure 4. THD+N vs. Output Power

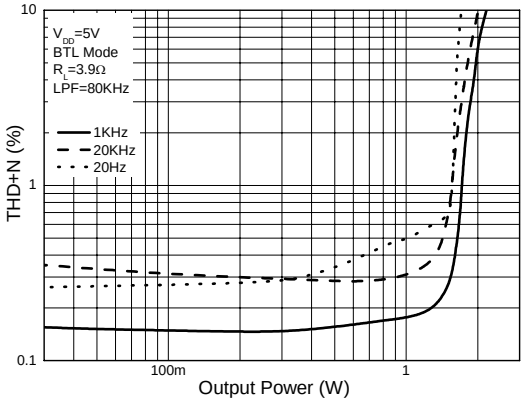


Figure 5. THD+N vs. Output Power

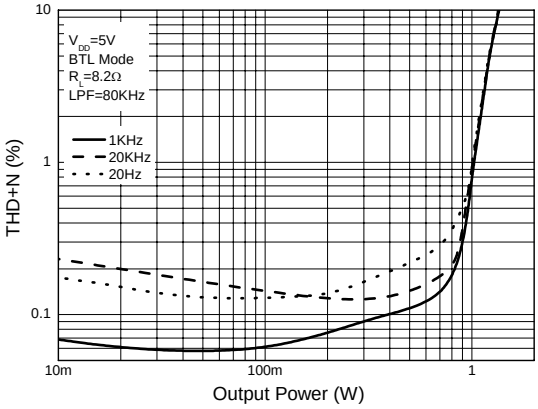


Figure 6. THD+N vs. Output Power

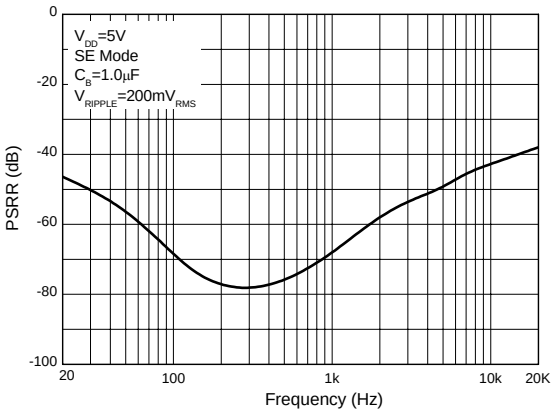


Figure 7. PSRR vs. Frequency

Typical Performance Characteristics (Continued)

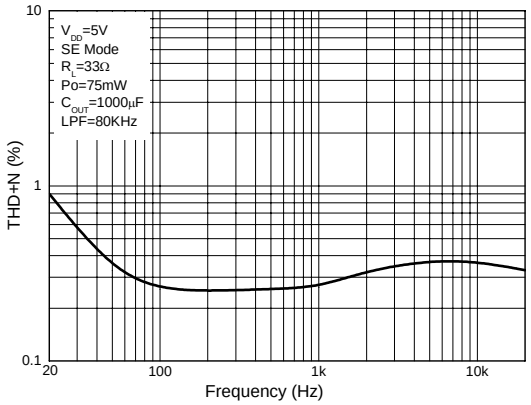


Figure 8. THD+N vs. Frequency

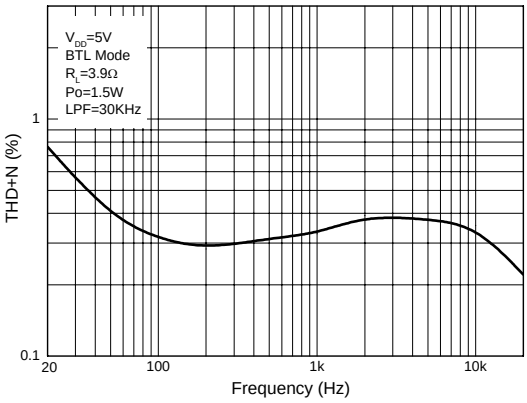


Figure 9. THD+N vs. Frequency

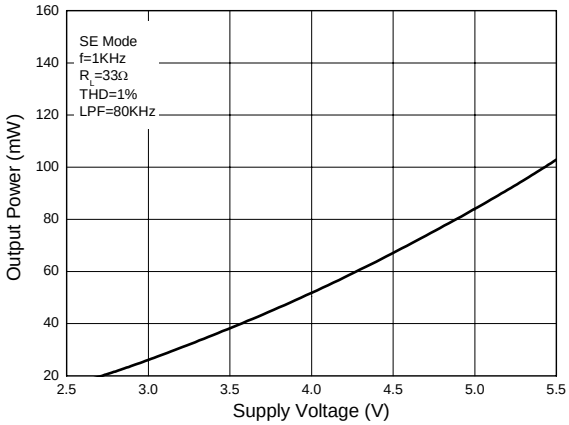


Figure 10. Output Power vs. Supply Voltage

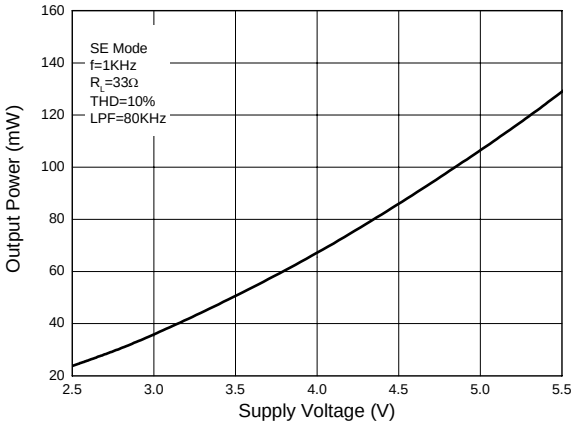


Figure 11. Output Power vs. Supply Voltage

Typical Performance Characteristics (Continued)

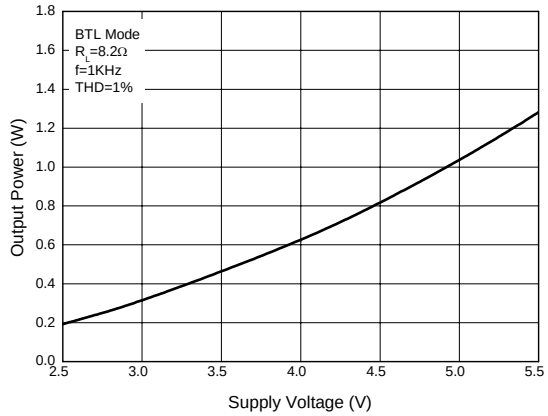


Figure 12. Output Power vs. Supply Voltage

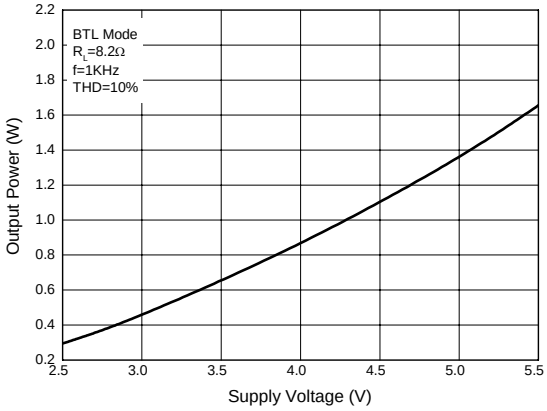


Figure 13. Output Power vs. Power Supply

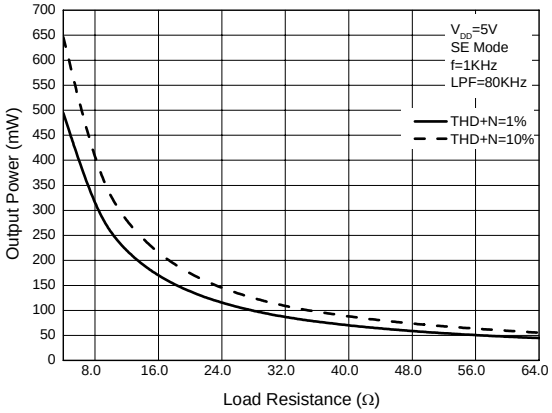


Figure 14. Output Power vs. Load Resistance

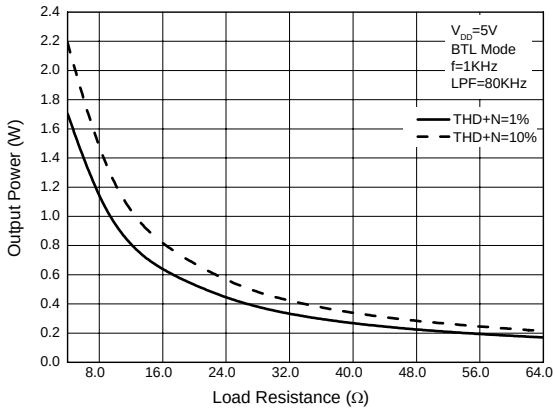


Figure 15. Output Power vs. Load Resistance

Typical Performance Characteristics (Continued)

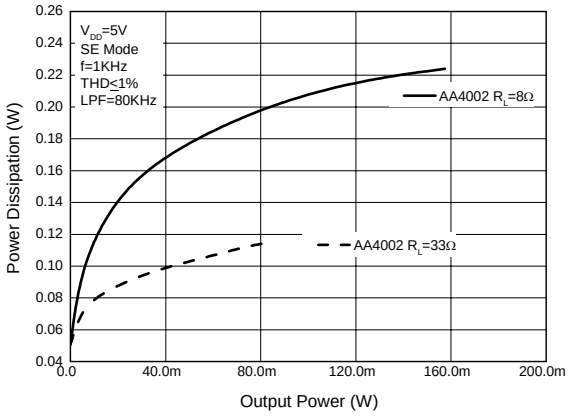


Figure 16. Power Dissipation vs. Output Power

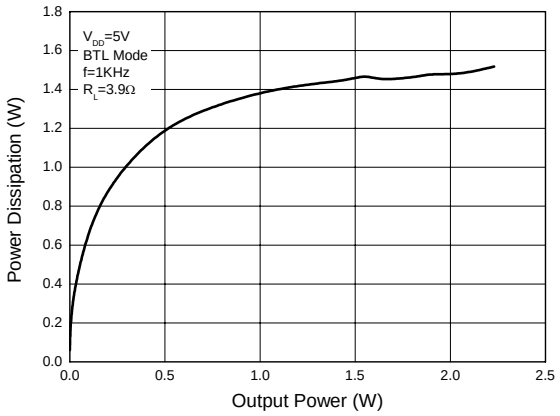


Figure 17. Power Dissipation vs. Output Power

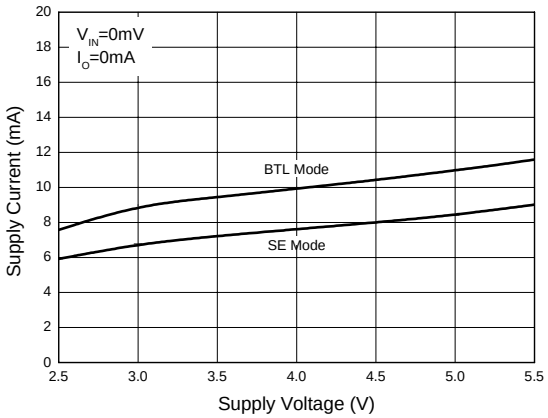


Figure 18. Supply Current vs. Supply Voltage

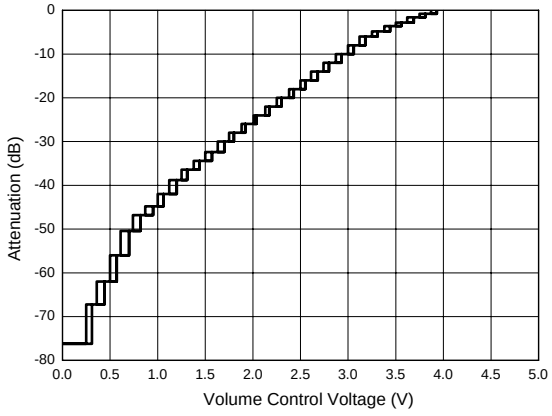


Figure 19. Volume Control Characteristics

Typical Performance Characteristics (Continued)

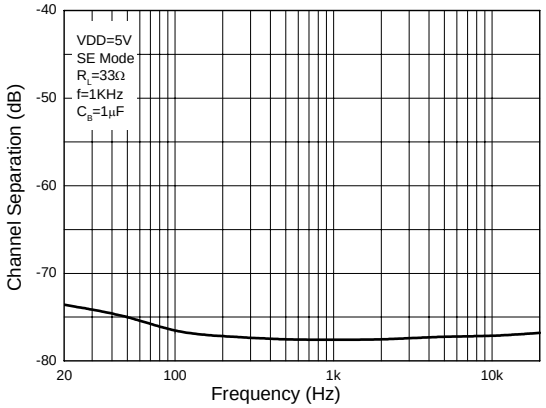


Figure 20. Channel Separation vs. Frequency

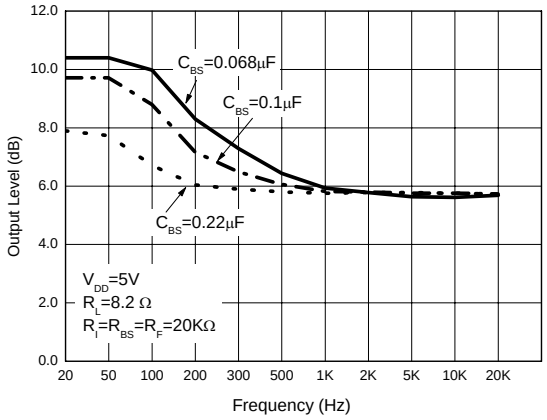


Figure 21. External Gain/Bass Boost Characteristics

Application Information

SE/BTL Mode, HP_SENSE Pin

The AA4002 can be operated in 2 types of output configurations, SE (Single-Ended) mode and BTL (Bridged-Tied-Load) mode, determined by HP_SENSE pin (pin 21) logic level. (Here is the discussion about left channel only, it also applies to right channel.)

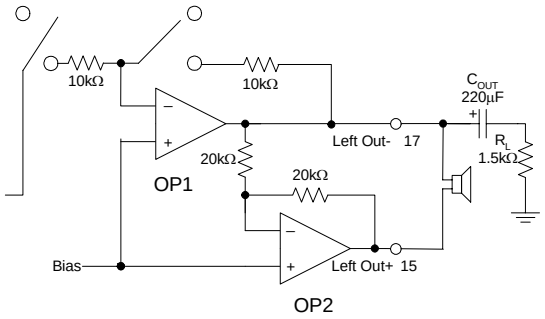


Figure 22. BTL Configuration in Left Channel

If applying high level to pin 21, the output of OP2 unit is in high impedance, the chip operates in SE mode. There is no current loop between OUT+ and OUT-, also no power consumption.

When HP_SENSE pin is held low, OP2 unit is turned on, the chip operates in BTL mode. AC signal at OUT+ is -180^o phase shift of OUT-. OP2 has fixed unity gain internally, so DC components (Bias voltage, approx 1/2 V_{DD}) between OUT+, OUT- is canceled. There is no need for DC block capacitors in system.

In BTL mode, voltage between speaker load is about 2 times that in SE mode, so there is 4 times output power compared to SE mode with same load.

In SE mode, output audio signal rides on Bias voltage at OUT-, so it is necessary to use capacitor to block DC bias and couple AC signal. See Figure 28 typical application circuit.

It is recommended to connect HP_SENSE to the control pin of headphone jack, illustrated in Figure 28. When headphone plug is not inserted, the voltage of HP_SENSE pin is determined by voltage divider formed by R_{PU}, R_L. For given resistors value in Figure 28, R_{PU}=100k, R_L=1.5k, DC voltage at HP_SENSE is about 75mV. AC signal equals output amplitude of OUT- through C_{OUT}, so signal at HP_SENSE node is 75mV DC plus AC signal. The maximum Peak-to-Peak voltage at OUT- is not greater than V_{DD}=5.0V supply voltage, so the positive maximum voltage of HP_SENSE node is not greater than 2.5V+75mV=2.575V, which can not reach HP_SENSE input high level minimum value (4.0V), there is no risk of mode switching between SE and BTL.

HP_SENSE pin can also be connected to MCU I/O port, it is necessary to note that AA4002 still can drive headphone even in BTL mode because OUT- is always active whatever SE or BTL mode.

Internal/External Gain, Gain SELECT Pin

The AA4002 provides 2 selectable feedback loops, Internal and External determined by SELECT pin (pin 3) logic level. Applying low level to SELECT pin, the AA4002 switches to internal feedback loop, OP1 works as unity gain. If applying high level to SELECT pin, external components are used as feedback loop, and the gain is expressed by formula below.

$$A_{VFB} = \frac{(R_{BS} \,//\, ZC_{BS}) + R_F}{R_I} \quad \text{.....(1)}$$

Here ZC_{BS} is the impedance of bass boost capacitor, $ZC_{BS}=1/2\pi*f*C_{BS}$. So A_{VFB} approaches 2 points, A_{VFBLF} at low frequency, A_{VFBHF} at high frequency, expressed by formula 2 and 3.

$$A_{VDLF} = \frac{R_{BS} + R_F}{R_I} \quad \text{.....(2)}$$

$$A_{VFBHF} = \frac{R_F}{R_I} \quad \text{.....(3)}$$

Bass Boost

From above discussion, the AA4002 can improve gain of audio signal at low frequency, which is hard to listening for human ears relative to middle band (2kHz to 3kHz). The boost corner frequency is determined by formula 4.

Application Information (Continued)

$$f_{BS} = 1/2\pi R_{BS} C_{BS} \quad \text{.....(4)}$$

Assuming $R_{BS}=R_F=R_I=20k\Omega$, $C_{BS}=0.068\mu F$ and $f_{BS}=117Hz$, the bass boost characteristic is shown in Figure 21.

Fixed Gain/Adjustable Gain Loop, MODE pin, DC Volume Control

The AA4002 can be set in fixed gain or adjustable gain, according to applying high or low level to MODE pin (pin 4). Low level is for fixed gain, High level is for adjustable gain, which permits to change volume by applying various DC voltages to DC VOL pin (pin7).

Table 1 shows the relationship of Volume Attenuation vs. the voltage of DC VOL pin.

There are 31 steps from 0 to -78dB; step size is different for different volume control voltage,
1dB/step from 0dB to -6dB,
2dB/step from -6dB to -36dB,
3dB/step from -36dB to -47dB,
4dB/step from -47db to -51dB,
5dB/step from -51dB to -66dB,
The last step is 12dB from -66dB to -78dB.

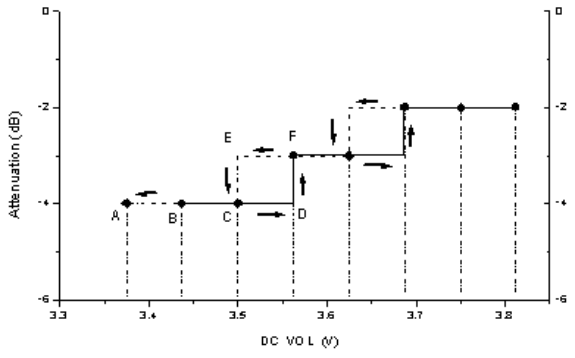


Figure 23. Volume Attenuation vs. DC VOL Pin Voltage

For example, increasing voltage applied to DC VOL pin from 3.437V (point B in Figure 23) to 3.562V (point D), gain will change one step from -4dB to -3dB (point F).

Table 1. Volume Attenuation vs. DC VOL Pin Voltage

V_{DD}=5V		
Attenuation (dB)	**High Level (V)**	**Low Level (V)**
0	5	3.875
-1	3.937	3.750
-2	3.812	3.625
-3	3.687	3.500
-4	3.562	3.375
-5	3.437	3.250
-6	3.312	3.125
-8	3.187	3.000
-10	3.06	2.875
-12	2.937	2.750
-14	2.812	2.625
-16	2.687	2.500
-18	2.562	2.375
-20	2.437	2.250
-22	2.312	2.125
-24	2.187	2.000
-26	2.062	1.875
-28	1.937	1.750
-30	1.812	1.625
-32	1.687	1.500
-34	1.562	1.375
-36	1.437	1.250
-39	1.312	1.125
-42	1.187	1.000
-45	1.062	0.875
-47	0.937	0.750
-51	0.812	0.625
-56	0.687	0.500
-61	0.562	0.375
-66	0.437	0.250
-78	0.312	0

Application Information (Continued)

But, decreasing voltage from 3.562V (point F), gain does not change immediately, the change occurs at 3.5V (point E). There is a hysteresis which guarantees that the volume control is monotonic, with immunity against noise coupled from system. In above Table 1, the column of Low Level means the lower threshold voltage with the voltage of DC VOL varying from high to low, High Level column means the other upper threshold voltage DC VOL voltage varying from low to high.

Mute, Shutdown

When applying high level to MUTE pin (pin 5), the AA4002 will mute output stage stereo dock output-whatever in BTL or SE mode. The AA4002 offers shutdown function which can further reduce power consumption. SHUTDOWN pin (pin 2) should be held low in normal operation. If applying high level to SHUTDOWN pin, the AA4002 will turn off internal bias circuits, enter into shutdown mode with very low quiescent current, 0.7μA Typ. MUTE, SHUTDOWN pin should be tied to high or low level to avoid undesired operation state.

Left/Right Dock Output

There are stereo amplifiers built-in AA4002 front-end input stages. It provide very low distortion audio monitor signal for line out, the pass-band gain is determined by external feedback resistors,

$$A_{VDOCK(L/R)} = \frac{R_{F(L/R)}}{R_{I(L/R)}} \quad \text{.....(5)}$$

The dock output is also used as input source for back-end amplifiers, so the gain of docking output (A_{VDOCK}) will affect total loop gain. The function of $C_{OUT(L/R)}$ (0.1μF) serial in Left/Right dock output is to remove DC bias.

Beep Detect

Beep feature is used in Notebook PC system for alerting. If peak-to-peak voltage of beep signal applied to BEEP DETECT pin (pin 11) exceeds a certain voltage called detect voltage, the feature will be activated, then AA4002 will be forced at BTL mode with internal fixed gain, ignoring MUTE and HP_SENSE pin logic level. For AA4002, V_{DETECT} is about 2.8V. Beep signal passes through Left/Right channel input path, the gain under BTL load is only dependent on the ratio of $R_{F(L/R)}$ to R_{BEEP}.

$$A_{VBEEP(L/R)} = 2 * \frac{R_{F(L/R)}}{R_{BEEP}} \quad \text{.....(6)}$$

For resistors value given in Figure 28, A_{VBEEP} is about 0.2 (-14dB). If this feature is not used, connecting the capacitor (C_{BEEP}) to ground, it is recommended removing two resistors (R_{BEEP}, 200kΩ), to minimize crosstalk between left and right channel.

C_I, C_{OUT}, C_B and C_S (Power Supply Bypassing Capacitor) Selection

For input stages of Left/Right channel, input capacitors (C_{IL}, C_{IR}), are used to accommodate different DC level between input source and AA4002 bias voltage (about 1/2 VDD). Input capacitors (C_{IL}, C_{IR}) and input resistors (R_{IL}, R_{IR}) form first order High Pass Filters, which determine the corner frequency,

$$f_{CI(L/R)} = \frac{1}{2\pi R_{I(L/R)} * C_{I(L/R)}} \quad \text{.....(7)}$$

For given values in Figure 28, R_{IL}=R_{IR}=20kΩ, C_{IL}=C_{IR}=0.33μF, the corner frequency of input stage is about 24Hz.

Similarly, for output stage in SE mode, output capacitor (C_{OUT}), and headphone load also form a first order High Pass Filter, and its cut-off frequency is determined by classic formula below.

$$f_{CO(L/R)} = \frac{1}{2\pi R_{HP(L/R)} * C_{O(L/R)}} \quad \text{.....(8)}$$

For bypass capacitor (C_B), the purpose is to filter internal bias noise, reduce harmonic distortion, and improve power supply rejection ratio performance. Tantalum or ceramic capacitor with low ESR is recommended, and is placed as close as possible to chip bypass pin in PCB layout. Both input and output

Application Information (Continued)

signal ride on such reference voltage, the chip can not work until internal DC bias is set up completely. So the size of C_B can also affect the chip start-up time, which is approx linearly proportional to the value of bypass capacitor. For AA4002, here are the start-up times for several typical capacitor values.

Table 2. C_B vs. Start-up Time

C_B (μF)	Start-up Time (ms)
0.47	300
1.0	600
2.2	1300

For AA4002 power supply, it is better to use individual power source generated from voltage regulators split from video, digital circuit units in system. For bypassing capacitors, it is recommended to use one electrolytic capacitor of 4.7μF to 10μF in parallel with 0.1μF ceramic capacitor which is located close to the part.

Setup Proper Gain, Design Example

The total closed loop gain is determined by three individual units - input stage, feedback network and output stage.

Input stage, pass-band gain

$$A_{VIN} = \frac{R_{F(L/R)}}{R_{I(L/R)}} \quad \text{.....(9)}$$

Feedback network, Internal pass-band gain, A_{VFB}=1, for external gain, see formula 1, 2, 3.

Output stage, for BTL mode, A_{VOUT}=2, for SE mode, A_{VOUT}=1.

So the total pass-band gain of AA4002, A_{VTOTAL} is,

$$A_{VTOTAL} = A_{VIN} * A_{VFB} * A_{VOUT} \quad \text{.....(10)}$$

According to formulas above, it is easy to plot Amplitude-Frequency characteristic curve. The lower corner frequency is dependant on A_{VIN}, A_{VOUT}, Bass Boost feature relies on A_{VOUT}.

Example

V_{DD}=5V, R_L=8Ω, BTL configuration, desired output power each channel, P_O=1.0W, THD+N ≤ 1%.
Input signal, V_{IN}=1.0VRMS from D-A converter.

Step 1,
To check if the chip can deliver 1W to 8Ω load with the limitation of THD+N ≤ 1%, V_{DD}=5V by Figure 6, 15.

Step 2,
If yes, to calculate output voltage, . So total pass-band gain (ignoring Bass boost feature, low frequency attenuation caused by AC coupling capacitors, A_{VFB}=1x.),

$A_{VTOTAL}=V_{OUT}/V_{IN}$=2.83x.

Step 3,
$A_{VIN}=A_{VTOTAL}/(A_{VFB}*A_{VOUT})$=2.83/(1*2)=1.415, $R_{F(L/R)}=A_{VIN}*R_{I(L/R)}$, assuming components values are given in Figure 28, just changing $R_{F(L/R)}$ to 20kΩ*1.415=28.3kΩ. Select the closest standard value 28kΩ.

Optimizing CLICK/POP Noise

The AA4002 includes a circuit to suppress CLICK/POP noise during power up/down transition. In practical application, the chip can effectively suppress common mode signal including CLICK/POP noise in BTL configuration. In SE mode, decreasing the size of output capacitor (C_{OUT}) can minish POP noise, which can also affect low frequency response according to formula 8 above. Increasing bypass capacitor value (C_B) can slower ramp of charge, prolong start-up time, mask most of transient noises before bias voltage is set-up.

Proper power on/off sequence can also optimize CLICK/POP noise. The recommended is shown in Figure 24.

Application Information (Continued)

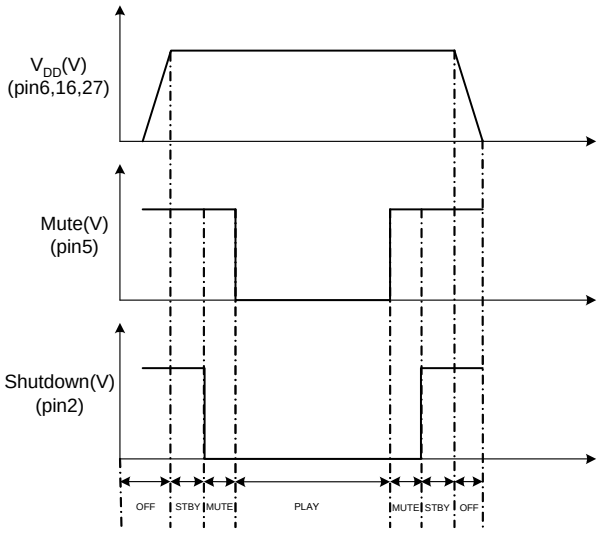


Figure 24. Recommended Sequences for Power ON/OFF

1) Power ON operation, enable mute, then enable shutdown; after V_{DD} is stable, release shutdown first, then mute.

2) Power OFF, enable mute, then enable shutdown; after V_{DD} is discharged completely, release shutdown firstly, then mute.

Efficiency, Power Dissipation and Thermal Consideration in Design

For Class-AB amplifier, Figure 11 is the basic equation of efficiency worked in BTL configuration,

$$\eta = \frac{\pi V_P}{4V_{DD}} \quad \text{.....(11)}$$

Here V_P is peak voltage of output swing.

Thermal dissipation becomes major concern when output power is close to 2W especially in BTL mode. The maximum power dissipation of package for AA4002 can be calculated by following equation.

$$P_{DMAX} = \frac{T_{JMAX} - T_A}{\theta_{JA}} \quad \text{.....(12)}$$

Here T_{JMAX} is maximum operating junction temperature 150°C, T_A is ambient temperature, θ_{JA} is thermal resistance form junction to ambient. For G package (TSSOP-28 with exposed DAP), it is 45°C/W given in datasheet page 6.

Assuming T_A is +25°C, the maximum allowed power dissipation P_{DMAX} is about 2.78W according to formula 12.

There is the other formula about power dissipation drawn from application for each channel which is determined by supply voltage and load resistance.

$$P_{DSEMAX} = \frac{V_{DD}^{\ 2}}{2\pi^2 R_L} \quad \text{(for SE mode).....(13)}$$

$$P_{DBTLMAX} = \frac{2V_{DD}^{\ 2}}{\pi^2 R_L} \quad \text{(for BTL mode).....(14)}$$

If power dissipation calculated by application is larger than permissible by package, it is necessary to assemble additional heat sinking, or keep ambient temperature around the chip very low, or increasing load impedance, or decreasing power supply voltage.

Here is an example, assuming V_{DD}=5.0V, R_L=4Ω, stereo in BTL mode,

$$P_{DBTLMAX} = \frac{2V_{DD}^{\ 2}}{\pi^2 R_L} = \frac{2\times 5^2}{3.14^2 \times 4} = 1.266W$$

, for 2 channels, total power dissipation P_{DTOTAL}=2* $P_{DBTLMAX}$=2*1.266=2.53W, according to formula 13, the maxim ambient temperature is,

$$T_A = T_{JMAX} - \theta_{JA} * P_{DBTLMAX} \quad \text{=150-45*2.53=36.2 °C}$$

That is to say, if user wants AA4002 can delivery maximum output power to 4Ω load, at V_{DD}=5.0V, BTL mode, ambient temperature has to hold less than 36.2°C. When junction temperature exceeds about +165°C, thermal shutdown circuit built-in AA4002

Application Information (Continued)

will turn off output stage to limit total power dissipation.

There is an exposed thermal pad on bottom of the chip to provide the direct thermal path from die to external heat sink. It is recommended to use copper on the surface of PC Board as heat sink for AA4002. To dig some matrix regular holes under chip, set diameter for each hole at 0.8~1.0mm, keep distance around 1.7mm between holes, remove copper solder mask of this area, and make sure to keep them contact well when soldering to PCB. See Figure 24.

Recommended PCB Layout for AA4002

Using wide traces for power supply, output power to reduce losses caused by parasitic resistance is recommended, which can also help to release heat away from the chip. It is recommended to place bypass capacitor, power supply bypassing capacitors as close as possible to the chip. Figure 25, 26 shows the recommended layout of double layer PCB.

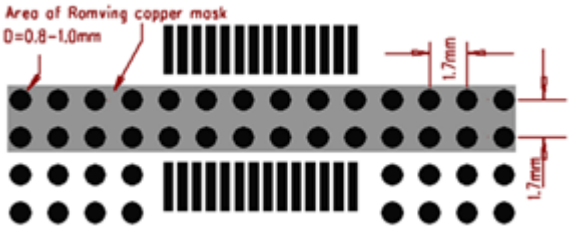


Figure 25. Copper and Holes under the Chip

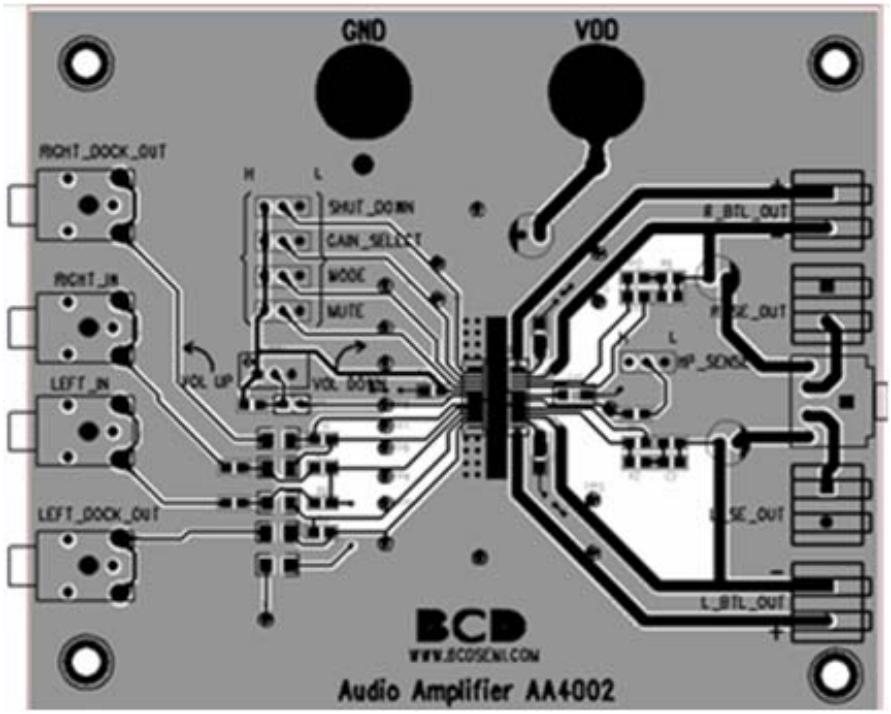


Figure 26. Top Route, Copper and Silkscreen

Application Information (Continued)

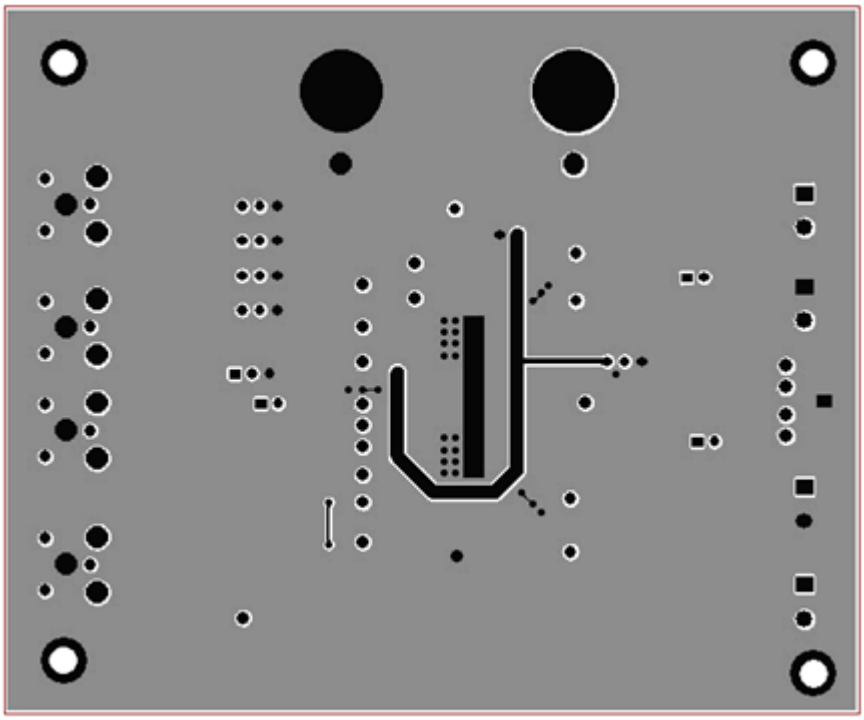


Figure 27. Bottom Route, Copper and Silkscreen

Typical Application

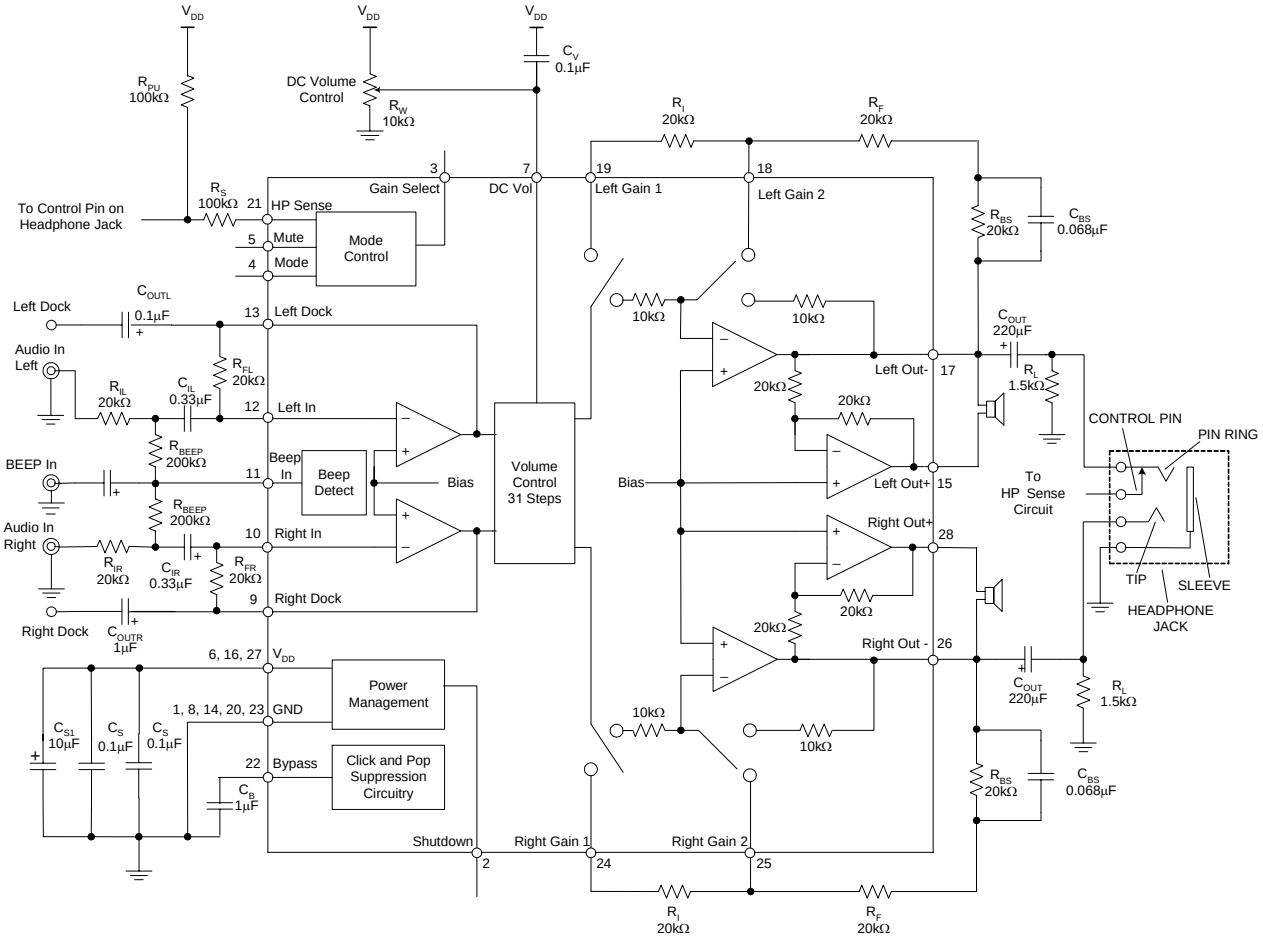
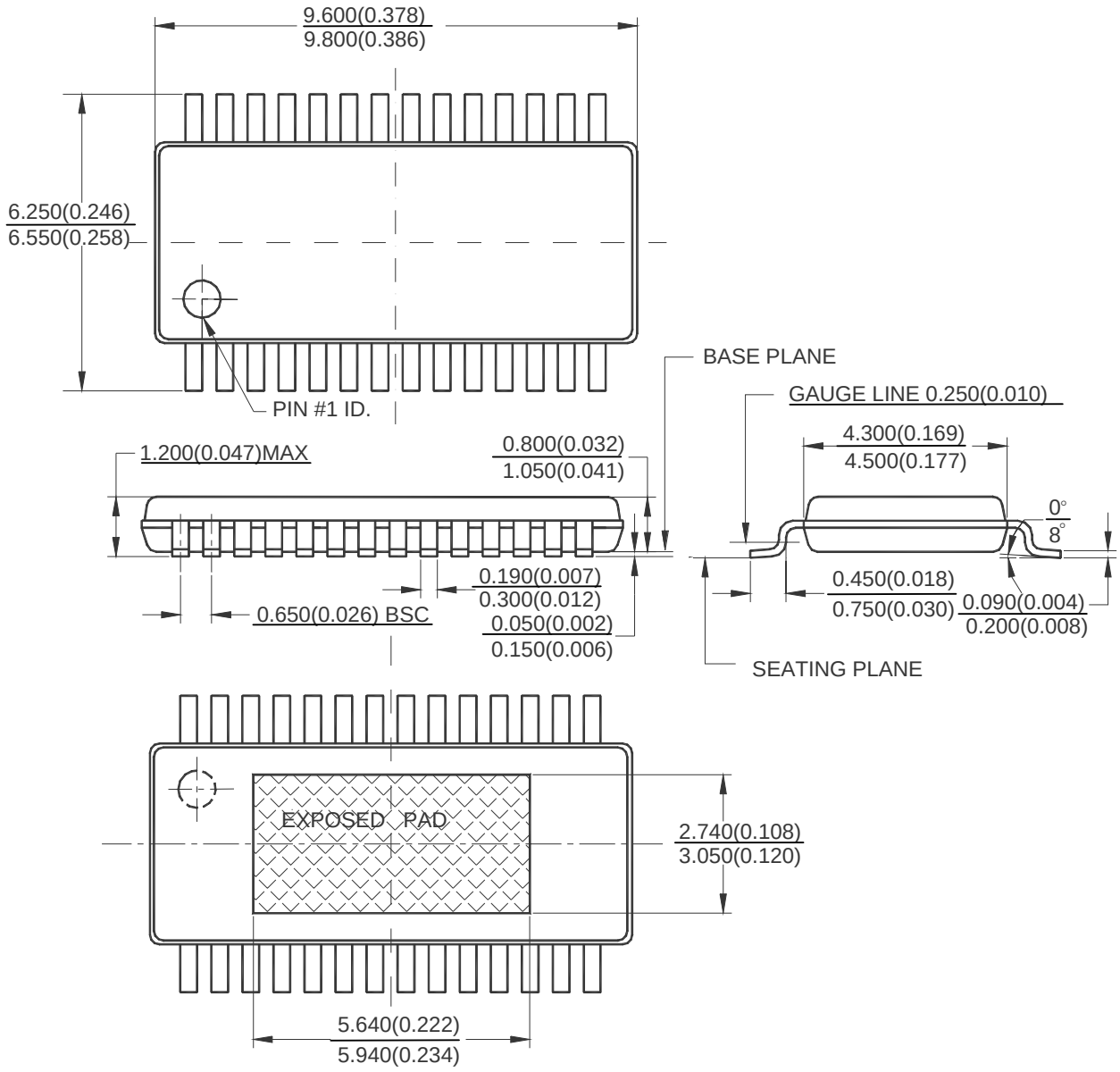


Figure 28. Typical Application of AA4002

Mechanical Dimensions

TSSOP-28 with Exposed-DAP **Unit: mm(inch)**





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MAIN SITE

BCD Semiconductor Manufacturing Limited
- Wafer Fab
Shanghai SIM-BCD Semiconductor Manufacturing Limited
800, Yi Shan Road, Shanghai 200233, China
Tel: +86-21-6485 1491, Fax: +86-21-5450 0008

BCD Semiconductor Manufacturing Limited
- IC Design Group
Advanced Analog Circuits (Shanghai) Corporation
8F, Zone B, 900, Yi Shan Road, Shanghai 200233, China
Tel: +86-21-6495 9539, Fax: +86-21-6485 9673

REGIONAL SALES OFFICE

Shenzhen Office
Shanghai SIM-BCD Semiconductor Manufacturing Co., Ltd. Shenzhen Office
Advanced Analog Circuits (Shanghai) Corporation Shenzhen Office
Room E, 5F, Noble Center, No.1006, 3rd Fuzhong Road, Futian District, Shenzhen 518026, China
Tel: +86-755-8826 7951, Fax: +86-755-8826 7865

Taiwan Office
BCD Semiconductor (Taiwan) Company Limited
4F, 298-1, Rui Guang Road, Nei-Hu District, Taipei, Taiwan
Tel: +886-2-2656 2808, Fax: +886-2-2656 2806

USA Office
BCD Semiconductor Corporation
3170 De La Cruz Blvd., Suite 105, Santa Clara,
CA 95054-2411, U.S.A

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Телефон: 8 (812) 309-75-97 (многоканальный)
Факс: 8 (812) 320-03-32
Электронная почта: ocean@oceanchips.ru
Web: http://oceanchips.ru/
Адрес: 198099, г. Санкт-Петербург, ул. Калинина, д. 2, корп. 4, лит. А