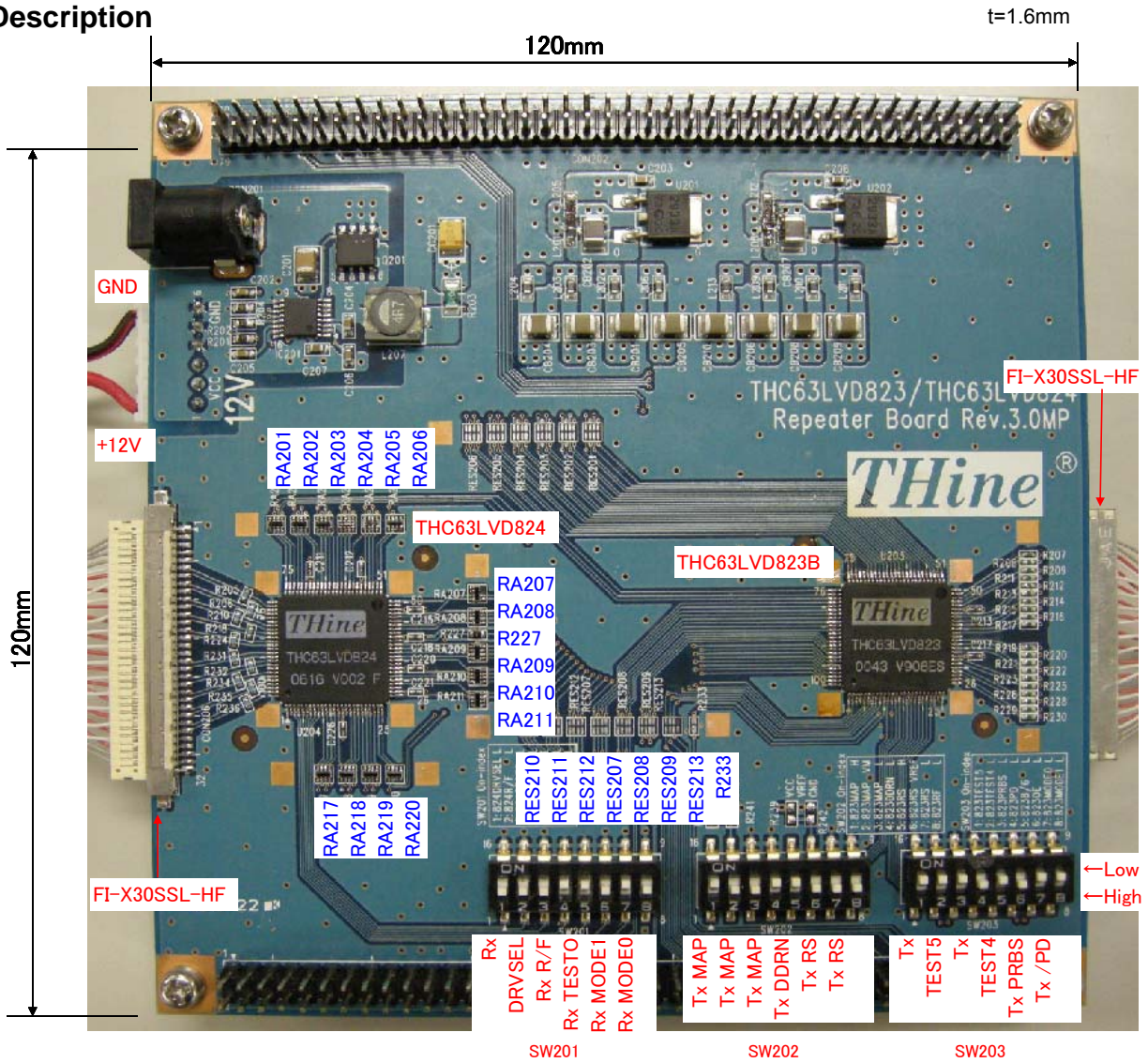
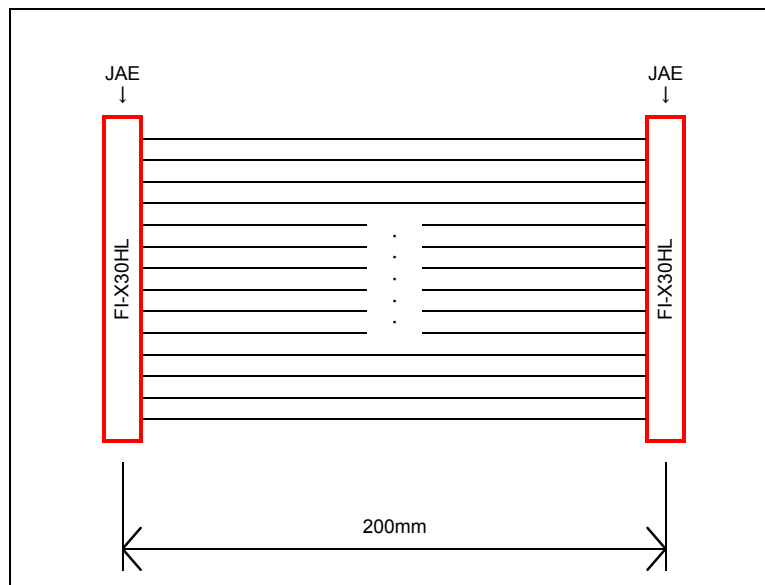


Description



LVDS-Cable Type.



SW201 Setting

* Def. : Default Setting

THC63LVD824														
SW Pin#	* Def.	NodeName	IC Pin#	PinName	Description									
1	H	RX DRVSEL	9	DRVSEL	Output Driverbility Select. H : High power, L : Low power.									
2	H	RX R/F	8	R/F	Output Clock Triggering Edge Select. H : Rising edge, L : Falling edge.									
3	L	RX TEST0	7	GND	Ground Pins for TTL outputs and digital circuitry.									
4	L	RX MODE1	6	MODE1	Pixel Data Mode. <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>MODE1</th> <th>MODE0</th> <th>Mode</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>L</td> <td>Dual Link</td> </tr> <tr> <td>L</td> <td>H</td> <td>Single Link</td> </tr> </tbody> </table>	MODE1	MODE0	Mode	L	L	Dual Link	L	H	Single Link
MODE1	MODE0	Mode												
L	L	Dual Link												
L	H	Single Link												
5	L	RX MODE0	5	MODE0										
6	H	RX /PD	4	/PDWN	H : Normal operation, L : Power down (all outputs are pulled to ground)									
7	L	RX TEST1	3	GND	Ground Pins for TTL outputs and digital circuitry.									
8	H	N/C	-	-	Non Connected.									

SW202 Setting

* Def. : Default Setting

THC63LVD823B																																
SW Pin#	* Def.	Node Name	IC Pin#	PinName	Description																											
1	L	TX MAP	14	MAP	LVDS mapping table select. <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th colspan="3">SW-Pin#</th> <th rowspan="2">RS</th> <th rowspan="2">Mapping Mode</th> </tr> <tr> <th>1</th> <th>2</th> <th>3</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>H(open)</td> <td>H(open)</td> <td>VIHM</td> <td>Mapping MODE1</td> </tr> <tr> <td>H(open)</td> <td>L</td> <td>H(open)</td> <td>VIMM</td> <td>Mapping MODE2</td> </tr> <tr> <td>H(open)</td> <td>H(open)</td> <td>L</td> <td>VILM</td> <td>Reserved</td> </tr> </tbody> </table>	SW-Pin#			RS	Mapping Mode	1	2	3	L	H(open)	H(open)	VIHM	Mapping MODE1	H(open)	L	H(open)	VIMM	Mapping MODE2	H(open)	H(open)	L	VILM	Reserved				
SW-Pin#						RS	Mapping Mode																									
1	2							3																								
L	H(open)	H(open)	VIHM	Mapping MODE1																												
H(open)	L	H(open)	VIMM	Mapping MODE2																												
H(open)	H(open)	L	VILM	Reserved																												
2	H																															
3	H																															
4	L	TX DDRN	13	DDRN	DDR function is active when MODE<1:0> = HL(Single-in/Dual-out mode). Open or H : DDR(Double Edge input) function disable. L : DDR(Double Edge input) function enable.																											
5	L	TX RS	12	RS	LVDS swing mode, VREF select. <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th colspan="3">SW-Pin#</th> <th rowspan="2">RS</th> <th rowspan="2">LVDS Swing</th> <th rowspan="2">Small Swing Input Support</th> </tr> <tr> <th>5</th> <th>6</th> <th>7</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>H(open)</td> <td>H(open)</td> <td>VIHM</td> <td>350mV</td> <td>N/A</td> </tr> <tr> <td>H(open)</td> <td>L</td> <td>H(open)</td> <td>VIMM</td> <td>350mV</td> <td>RS=VREFa</td> </tr> <tr> <td>H(open)</td> <td>H(open)</td> <td>L</td> <td>VILM</td> <td>200mV</td> <td>N/A</td> </tr> </tbody> </table> a. VREF is Input Reference Voltage.	SW-Pin#			RS	LVDS Swing	Small Swing Input Support	5	6	7	L	H(open)	H(open)	VIHM	350mV	N/A	H(open)	L	H(open)	VIMM	350mV	RS=VREFa	H(open)	H(open)	L	VILM	200mV	N/A
SW-Pin#						RS	LVDS Swing	Small Swing Input Support																								
5	6								7																							
L	H(open)	H(open)	VIHM	350mV	N/A																											
H(open)	L	H(open)	VIMM	350mV	RS=VREFa																											
H(open)	H(open)	L	VILM	200mV	N/A																											
6	H																															
7	H																															
8	H	TX RF	11	R/F	Input Clock Triggering Edge Select. H : Rising edge, L : Falling edge																											

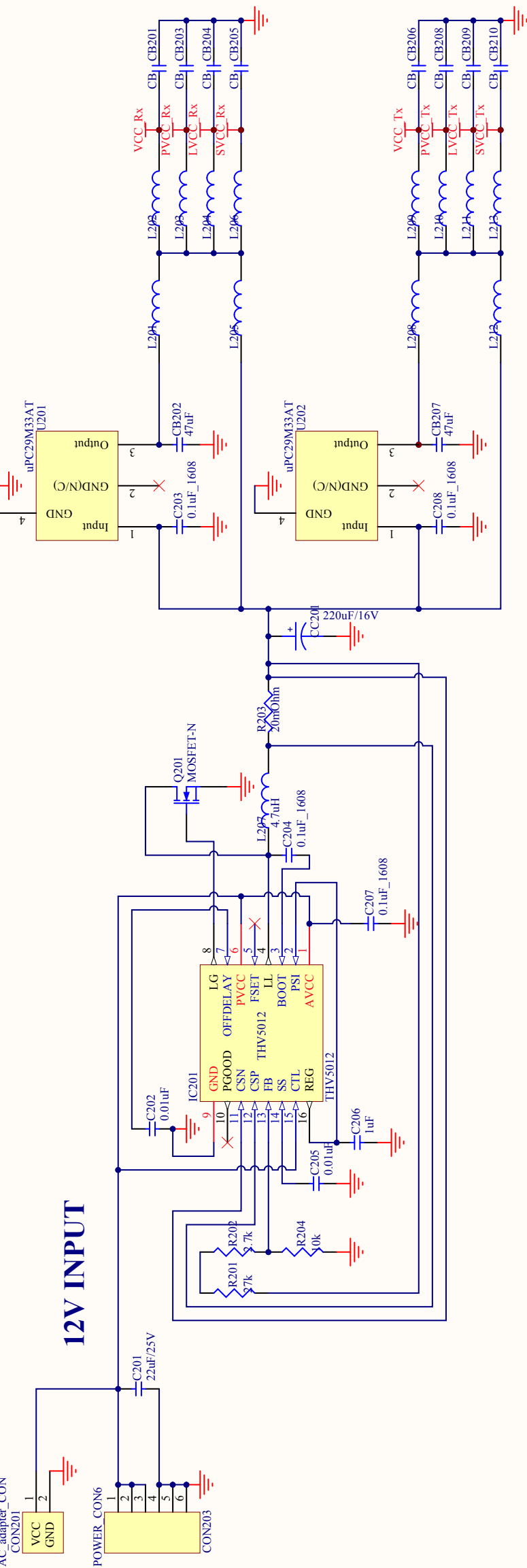
SW203 Setting

* Def. : Default Setting

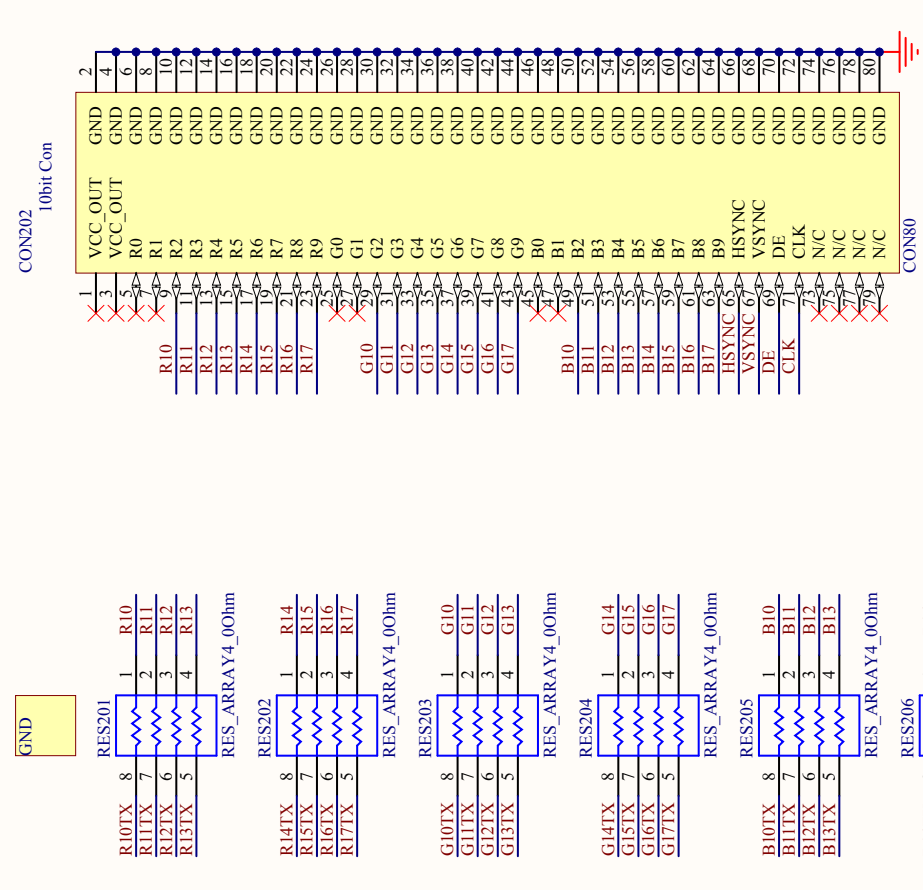
THC63LVD823B																				
SW Pin#	* Def.	NodeName	IC Pin#	PinName	Description															
1	H	TX TEST5	22	N/C	Must be Open.															
2	L	TX TEST4	21	Reserved	Must be tied to GND.															
3	L	TX PRBS	20	PRBS	PRBS(Pseudo-Random Binary Sequence) generator is active in order to evaluate eye patterns when MODE<1:0> = LL(Dual-in/Dual-out mode). H : PRBS generator is enable. L : Normal Operation															
4	H	TX /PD	19	/PDWN	H : Normal operation, L : Power down (all outputs are Hi-Z)															
5	L	TX 8/6	18	GND	Ground Pins for TTL inputs and digital circuitry.															
6	H	TX OE	17	OE	Output enable. H : Output enable, L : Output disable (all outputs are Hi-Z).															
7	L	TX MODE0	16	MODE0	Pixel Data Mode <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>MODE1</th> <th>MODE0</th> <th>Mode</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>L</td> <td>Dual Link(Dual-in/Dual-out)</td> </tr> <tr> <td>H</td> <td>L</td> <td>Dual Link(Single-in/Dual-out)</td> </tr> <tr> <td>L</td> <td>H</td> <td>Single Link(Dual-in/Single-out)</td> </tr> <tr> <td>H</td> <td>H</td> <td>Single Link(Single-in/Single-out)</td> </tr> </tbody> </table>	MODE1	MODE0	Mode	L	L	Dual Link(Dual-in/Dual-out)	H	L	Dual Link(Single-in/Dual-out)	L	H	Single Link(Dual-in/Single-out)	H	H	Single Link(Single-in/Single-out)
MODE1	MODE0	Mode																		
L	L	Dual Link(Dual-in/Dual-out)																		
H	L	Dual Link(Single-in/Dual-out)																		
L	H	Single Link(Dual-in/Single-out)																		
H	H	Single Link(Single-in/Single-out)																		
8	L	TX MODE1	15	MODE1																

Measures Type

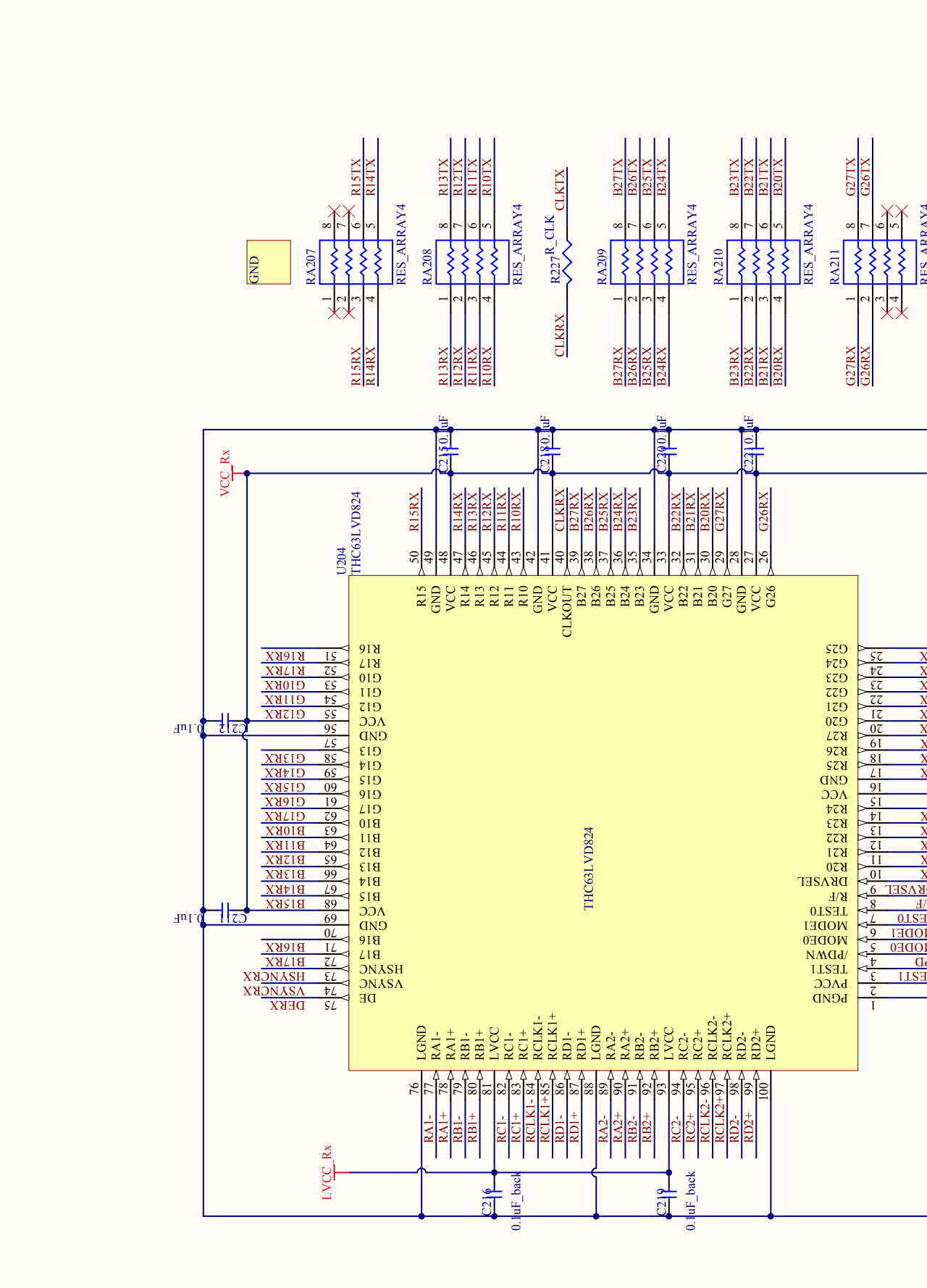
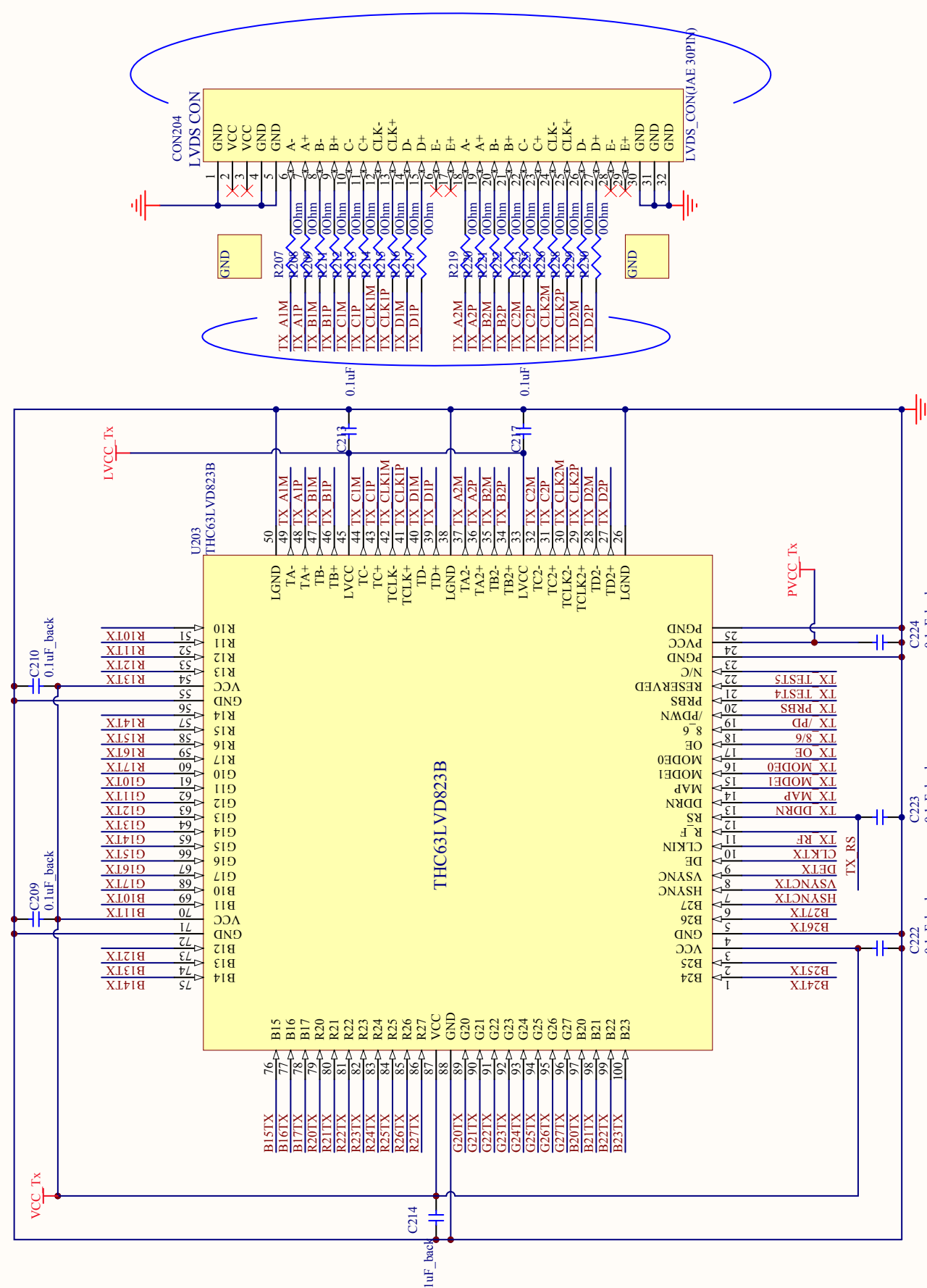
#	Type	Un-Mount	0Ω-Mount	33Ω-Mount
1		RES207 RES208 RES209 RES210 RES211 RES212 RES213 R233		RA201 RA211 RA202 RA217 RA203 RA218 RA204 RA219 RA205 RA220 RA206 R227 RA207 RA208 RA209 RA210
2			RES207 RES208 RES209 RES210 RES211 RES212 RES213 R233	RA201 RA211 RA202 RA217 RA203 RA218 RA204 RA219 RA205 RA220 RA206 R227 RA207 RA208 RA209 RA210
3		THC63LVD823B	RES207 RES208 RES209 RES210 RES211 RES212 RES213 R233	RA201 RA211 RA202 RA217 RA203 RA218 RA204 RA219 RA205 RA220 RA206 R227 RA207 RA208 RA209 RA210
4		RA201 RA211 RA202 RA217 RA203 RA218 RA204 RA219 RA205 RA220 RA206 R227 RA207 RA208 RA209 RA210	RES207 RES208 RES209 RES210 RES211 RES212 RES213 R233	



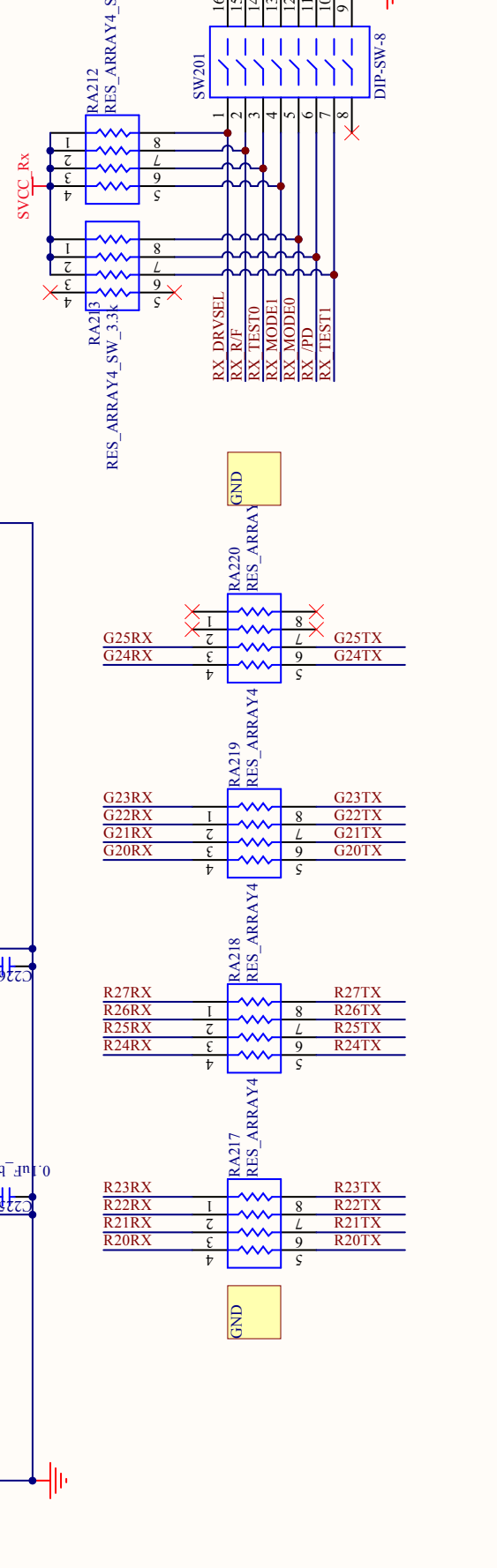
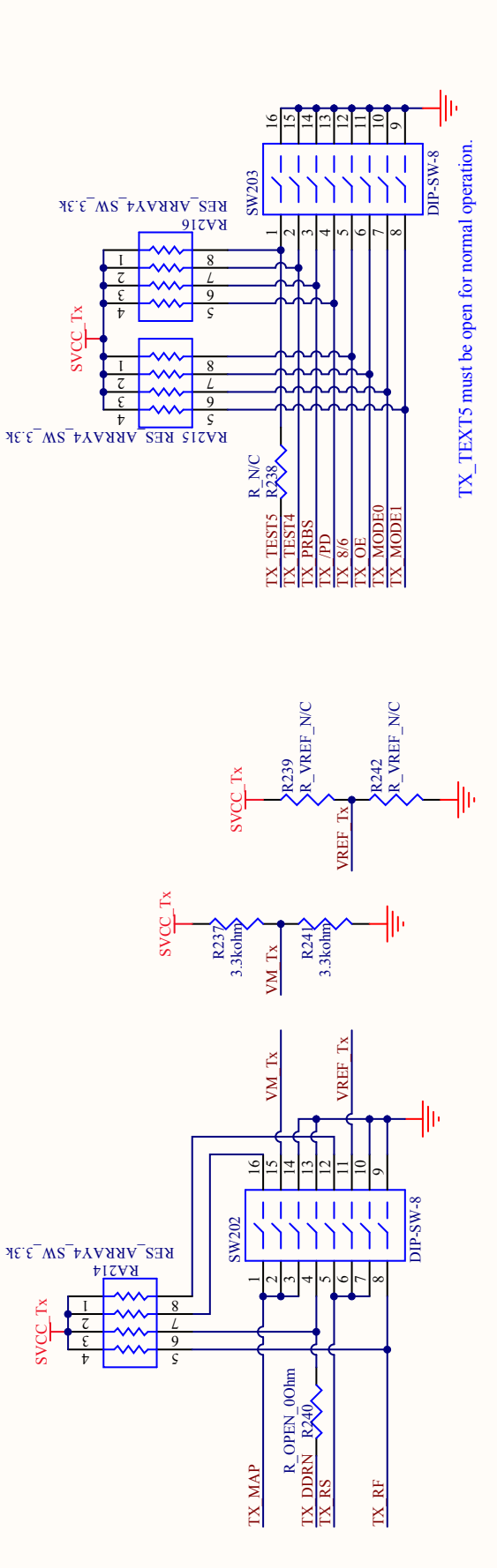
From Pin header



1st Pixel



2nd Pixel



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6. Despite our utmost efforts to improve the quality and reliability of the product, faults will occur with a certain small probability, which is inevitable to a semi-conductor product. Therefore, you are encouraged to have sufficient redundant or error preventive design applied to the use of the product so as not to have our product cause any social or public damage.
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THine Electronics, Inc.

sales@thine.co.jp

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JONHON

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