

Product Summary

BV_{DSS}	$R_{DS(ON)}$ Max	I_D Max $T_A = +25^\circ C$
-20V	45m Ω @ $V_{GS} = -4.5V$	-4.7A
	90m Ω @ $V_{GS} = -1.8V$	-3.3A

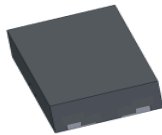
Description and Applications

This MOSFET is designed to minimize the on-state resistance ($R_{DS(ON)}$) and yet maintain superior switching performance, making it ideal for high-efficiency power management applications.

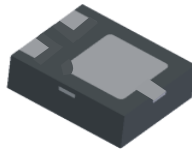
- Backlighting
- Power Management Functions
- DC-DC Converters



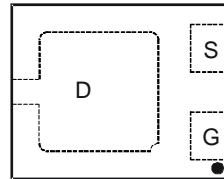
ESD protected Gate



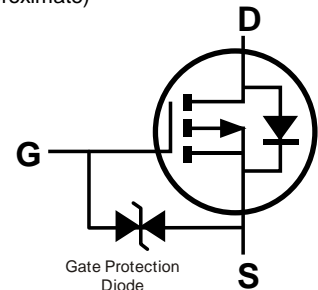
TOP VIEW



BOTTOM VIEW



Internal Schematic
(Top View)



Equivalent Circuit

Features and Benefits

- Low On-Resistance
- Low Input Capacitance
- Fast Switching Speed
- Low Input/Output Leakage
- **ESD Protected**
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**

Mechanical Data

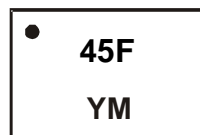
- Case: X2-DFN2015-3
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish — NiPdAu over Copper Leadframe. Solderable per MIL-STD-202, Method 208
- Terminals Connections: See Diagram Below
- Weight: 0.008 grams (Approximate)

Ordering Information (Note 4)

Part Number	Case	Packaging
DMP2045UFY4-7	X2-DFN2015-3	3,000/Tape & Reel

- Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
 2. See http://www.diodes.com/quality/lead_free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
 4. For packaging details, go to our website at <https://www.diodes.com/design/support/packaging/diodes-packaging/>.

Marking Information



45F = Marking Code
 YM = Date Code Marking
 Y = Year (ex: F = 2018)
 M = Month (ex: 9 = September)

Date Code Key

Year	2017	2018	2019	2020	2021	2022	2023	2024	2025
Code	E	F	G	H	I	J	K	L	M

Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	O	N	D

Maximum Ratings (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Characteristic	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	-20	V
Gate-Source Voltage	V_{GSS}	± 8	V
Continuous Drain Current (Note 6) $V_{GS} = -4.5\text{V}$	I_D	$T_A = +25^\circ\text{C}$	-4.7
		$T_A = +70^\circ\text{C}$	-3.8
Maximum Continuous Body Diode Forward Current (Note 6)	I_S	-1	A
Pulsed Drain Current (10 μs Pulse, Duty Cycle = 1%)	I_{DM}	-25	A

Thermal Characteristics

Characteristic	Symbol	Value	Unit
Total Power Dissipation (Note 5)	P_D	0.67	W
Thermal Resistance, Junction to Ambient (Note 5)	$R_{\theta JA}$	Steady State	190
Total Power Dissipation (Note 6)		P_D	1.49
Thermal Resistance, Junction to Ambient (Note 6)	$R_{\theta JA}$	Steady State	84
Thermal Resistance, Junction to Case (Note 6)		$R_{\theta JC}$	14.5
Operating and Storage Temperature Range	T_J, T_{STG}	-55 to +150	$^\circ\text{C}$

Electrical Characteristics (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 7)						
Drain-Source Breakdown Voltage	BV_{DSS}	-20	—	—	V	$V_{GS} = 0\text{V}, I_D = -250\mu\text{A}$
Zero Gate Voltage Drain Current $T_J = +25^\circ\text{C}$	I_{DSS}	—	—	-1	μA	$V_{DS} = -20\text{V}, V_{GS} = 0\text{V}$
Gate-Source Leakage	I_{GSS}	—	—	± 10	μA	$V_{GS} = \pm 8.0\text{V}, V_{DS} = 0\text{V}$
ON CHARACTERISTICS (Note 7)						
Gate Threshold Voltage	$V_{GS(TH)}$	-0.3	—	-1.0	V	$V_{DS} = V_{GS}, I_D = -250\mu\text{A}$
Static Drain-Source On-Resistance	$R_{DS(ON)}$	—	34	45	m Ω	$V_{GS} = -4.5\text{V}, I_D = -4.0\text{A}$
		—	44	58		$V_{GS} = -2.5\text{V}, I_D = -3.5\text{A}$
		—	56	90		$V_{GS} = -1.8\text{V}, I_D = -0.1\text{A}$
		—	80	160		$V_{GS} = -1.5\text{V}, I_D = -0.1\text{A}$
Diode Forward Voltage	V_{SD}	—	-0.6	-1.2	V	$V_{GS} = 0\text{V}, I_S = 1.0\text{A}$
DYNAMIC CHARACTERISTICS (Note 8)						
Input Capacitance	C_{iss}	—	634	—	pF	$V_{DS} = -10\text{V}, V_{GS} = 0\text{V}$ $f = 1.0\text{MHz}$
Output Capacitance	C_{oss}	—	81	—	pF	
Reverse Transfer Capacitance	C_{rss}	—	66	—	pF	
Gate Resistance	R_g	—	20	—	Ω	$V_{DS} = 0\text{V}, V_{GS} = 0\text{V}, f = 1.0\text{MHz}$
Total Gate Charge	Q_g	—	6.8	—	nC	$V_{GS} = -4.5\text{V}, V_{DS} = -10\text{V}$ $I_D = -4\text{A}$
Gate-Source Charge	Q_{gs}	—	0.7	—	nC	
Gate-Drain Charge	Q_{gd}	—	1.6	—	nC	
Turn-On Delay Time	$t_{D(ON)}$	—	4.2	—	ns	$V_{DS} = -10\text{V}, V_{GS} = -4.5\text{V},$ $R_D = 2.5\Omega, R_g = 3.0\Omega, I_D = -1\text{A}$
Turn-On Rise Time	t_R	—	3.4	—	ns	
Turn-Off Delay Time	$t_{D(OFF)}$	—	22.7	—	ns	
Turn-Off Fall Time	t_F	—	9.6	—	ns	
Reverse Recovery Time	t_{RR}	—	1.8	—	ns	$I_F = -1.0\text{A}, di/dt = 100\text{A}/\mu\text{s}$
Reverse Recovery Charge	Q_{RR}	—	9.4	—	nC	$I_F = -1.0\text{A}, di/dt = 100\text{A}/\mu\text{s}$

- Notes: 5. Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.
6. Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.
7. Short duration pulse test used to minimize self-heating effect.
8. Guaranteed by design. Not subject to product testing.

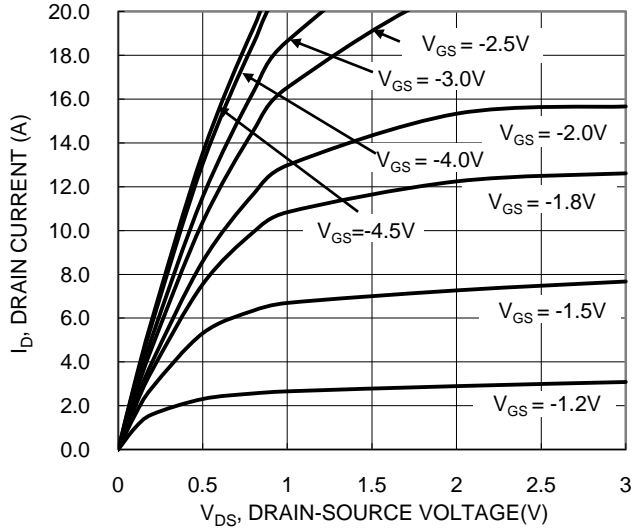


Figure 1. Typical Output Characteristic

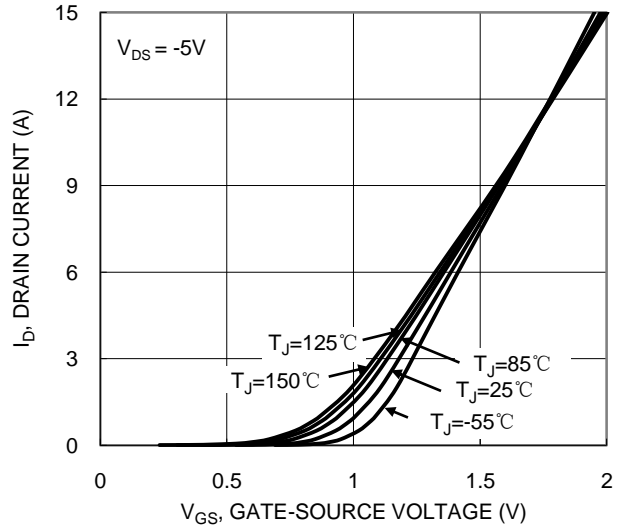


Figure 2. Typical Transfer Characteristic

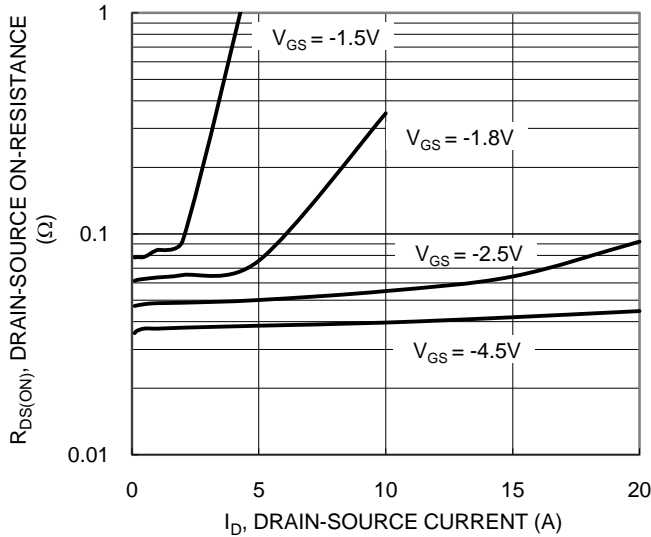


Figure 3. Typical On-Resistance vs. Drain Current and Gate Voltage

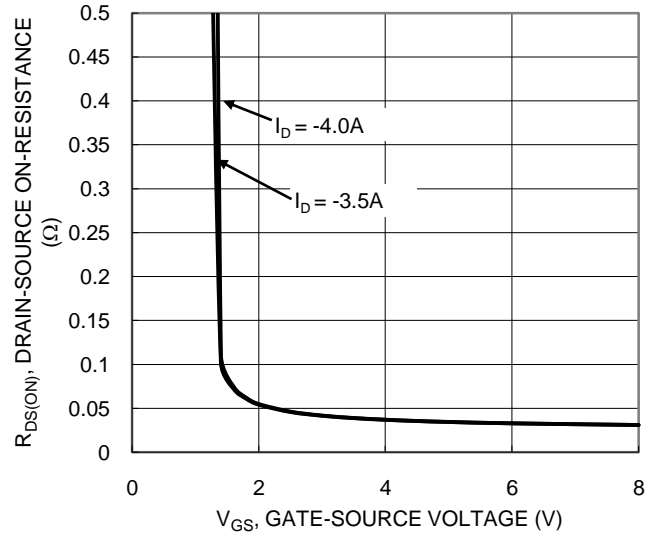


Figure 4. Typical Transfer Characteristic

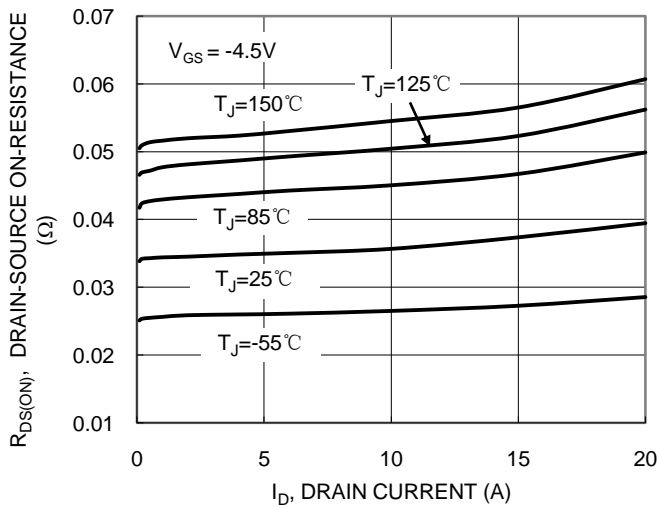


Figure 5. Typical On-Resistance vs. Drain Current and Junction Temperature

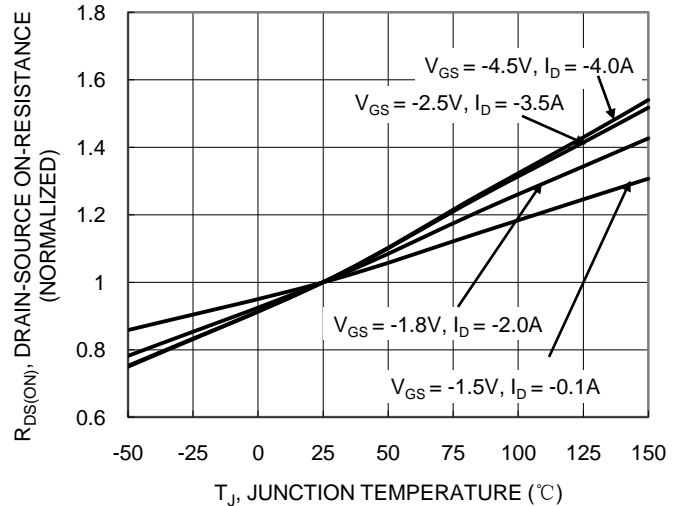


Fig.5 On-Resistance Variation with Junction Temperature

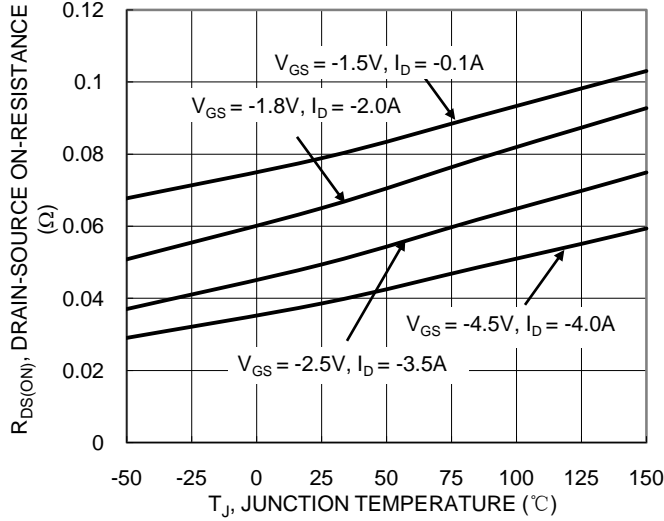


Figure 7. On-Resistance Variation with Junction Temperature

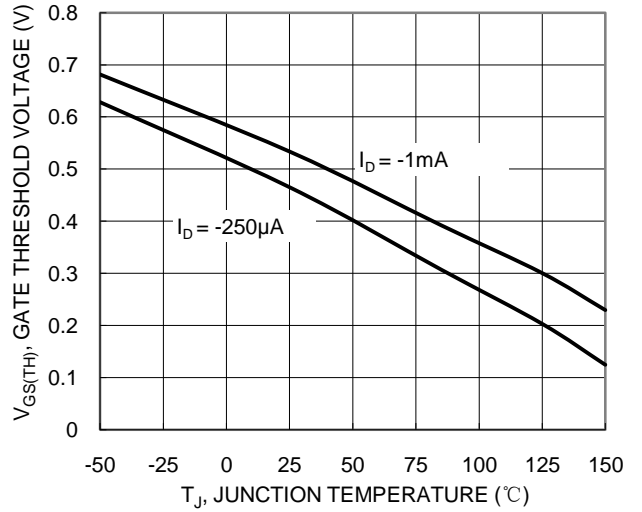


Figure 8. Gate Threshold Variation vs. Junction Temperature

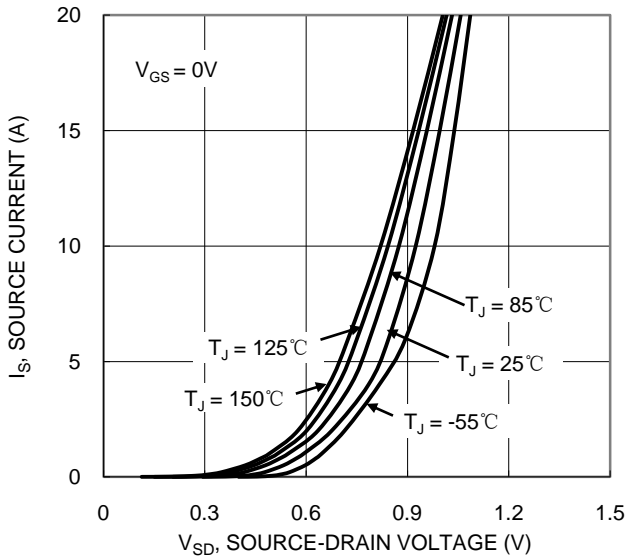


Figure 9. Diode Forward Voltage vs. Current

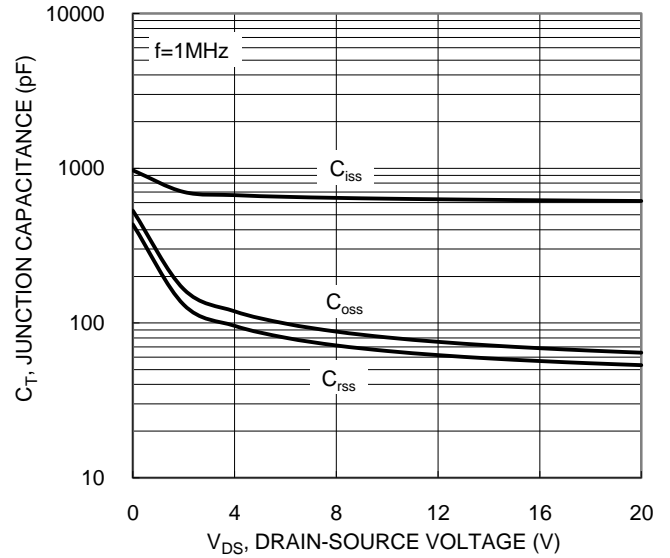


Figure 10. Typical Junction Capacitance

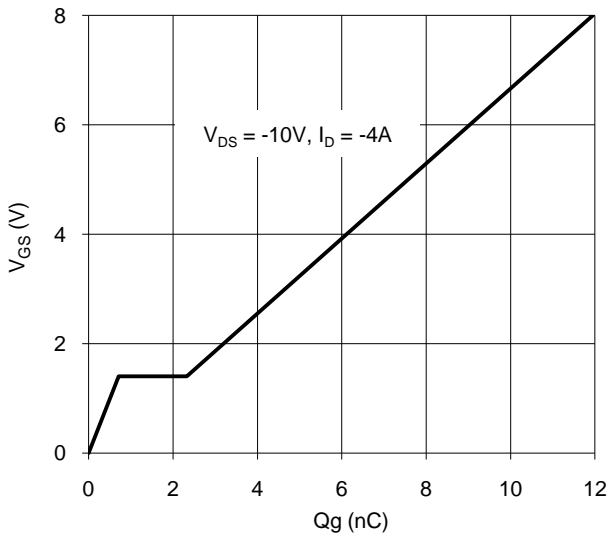


Figure 11. Gate Charge

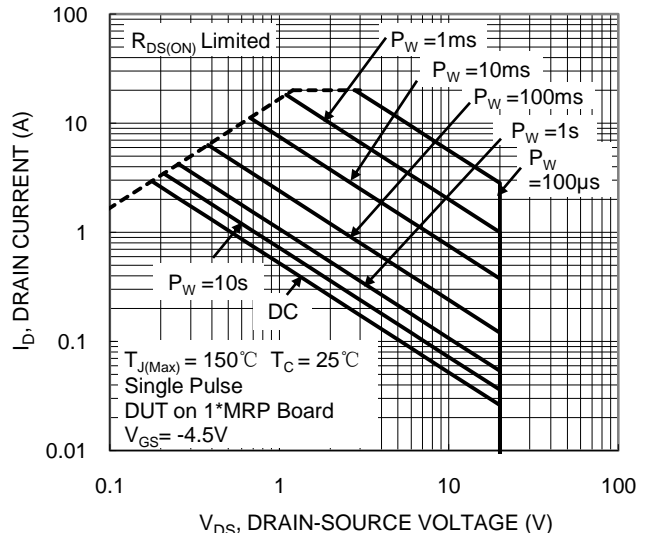


Figure 12. SOA, Safe Operation Area

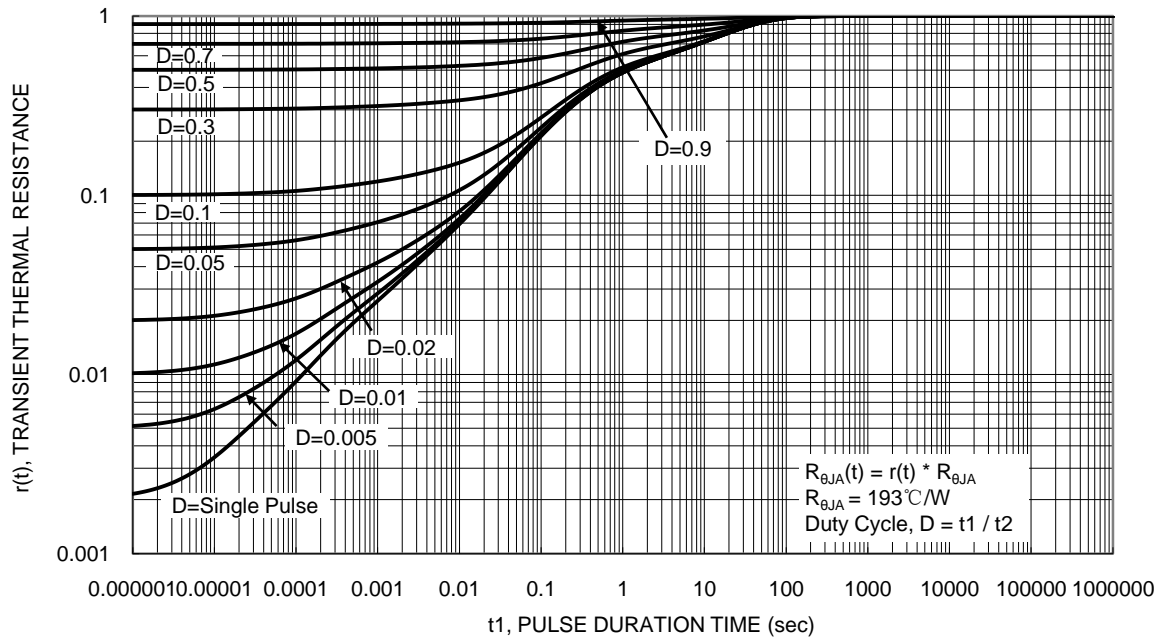
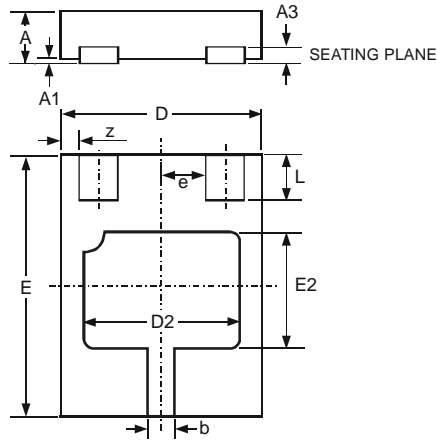


Figure 13. Transient Thermal Resistance

Package Outline Dimensions

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

X2-DFN2015-3

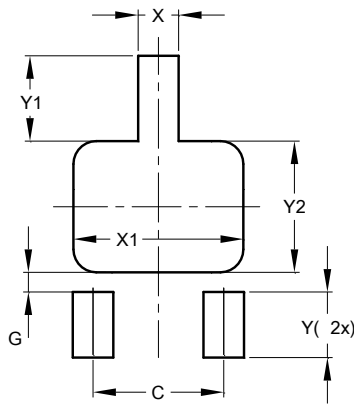


X2-DFN2015-3			
Dim	Min	Max	Typ
A	-	0.40	-
A1	0	0.05	0.02
A3	-	-	0.13
b	0.20	0.30	0.25
D	1.45	1.575	1.5
D2	1.00	1.20	1.10
e	-	-	0.50
E	1.95	2.075	2.00
E2	0.70	0.90	0.80
L	0.25	0.35	0.30
z	-	-	0.125
All Dimensions in mm			

Suggested Pad Layout

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

X2-DFN2015-3



X2-DFN2015-3	
Dimensions	Value (in mm)
C	1.000
G	0.150
X	0.310
X1	1.300
Y	0.500
Y1	0.650
Y2	1.000

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