# PIC18F8723 Family Data Sheet

## 64/80-Pin, 1-Mbit, Enhanced Flash Microcontrollers with 12-Bit A/D and nanoWatt Technology

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# PIC18F8723 FAMILY

## 64/80-Pin, 1-Mbit, Enhanced Flash Microcontrollers with 12-Bit A/D and nanoWatt Technology

### Peripheral Highlights:

- 12-Bit, Up to 16-Channel Analog-to-Digital Converter module (A/D):
  - Auto-acquisition capability
  - Conversion available during Sleep
- Two Master Synchronous Serial Port (MSSP) modules supporting 2/3/4-Wire SPI (all four modes) and $I^2C$™ Master and Slave modes
- Two Capture/Compare/PWM (CCP) modules
- Three Enhanced Capture/Compare/PWM (ECCP) modules:
  - One, two or four PWM outputs
  - Selectable polarity
  - Programmable dead time
  - Auto-shutdown and auto-restart
- Two Enhanced Addressable USART modules:
  - Supports RS-485, RS-232 and LIN 1.2
  - Auto-wake-up on Start bit
  - Auto-Baud Detect
- Dual Analog Comparators with Input Multiplexing
- High-Current Sink/Source 25 mA/25 mA
- Four Programmable External Interrupts
- Four Input Change Interrupts

### External Memory Interface:

- Address Capability of Up to 2 Mbytes
- 8-Bit or 16-Bit Interface
- 8, 12, 16 and 20-Bit Address modes

### Power-Managed Modes:

- Run: CPU on, Peripherals on
- Idle: CPU off, Peripherals on
- Sleep: CPU off, Peripherals off
- Idle mode Currents Down to 15 μA Typical
- Sleep Current Down to 0.2 μA Typical
- Timer1 Oscillator: 1.8 μA, 32 kHz, 2V
- Watchdog Timer: 2.1 μA

### Special Microcontroller Features:

- C Compiler Optimized Architecture:
  - Optional extended instruction set designed to optimize re-entrant code
- 100,000 Erase/Write Cycle Enhanced Flash Program Memory Typical
- 1,000,000 Erase/Write Cycle Data EEPROM Memory Typical
- Flash/Data EEPROM Retention: 100 Years Typical
- Self-Programmable under Software Control
- Priority Levels for Interrupts
- 8 x 8 Single-Cycle Hardware Multiplier
- Extended Watchdog Timer (WDT):
  - Programmable period from 4 ms to 131s
- Single-Supply In-Circuit Serial Programming™ (ICSP™) via Two Pins
- In-Circuit Debug (ICD) via Two Pins
- Wide Operating Voltage Range: 2.0V to 5.5V
- Fail-Safe Clock Monitor
- Two-Speed Oscillator Start-up
- nanoWatt Technology

**Note:** This document is supplemented by the *"PIC18F8722 Family Data Sheet"* (DS39646). See **Section 1.0 "Device Overview"**.

| Device | Program Memory | | Data Memory | | I/O | 12-Bit A/D (ch) | CCP/ ECCP (PWM) | MSSP | | | EUSART | Comparators | Timers 8/16-Bit | External Bus |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Flash (bytes) | # Single-Word Instructions | SRAM (bytes) | EEPROM (bytes) | | | | | SPI | Master $I^2C$™ | | | | |
| PIC18F6628 | 96K | 49152 | 3936 | 1024 | 54 | 12 | 2/3 | 2 | Y | Y | 2 | 2 | 2/3 | N |
| PIC18F6723 | 128K | 65536 | 3936 | 1024 | 54 | 12 | 2/3 | 2 | Y | Y | 2 | 2 | 2/3 | N |
| PIC18F8628 | 96K | 49152 | 3936 | 1024 | 70 | 16 | 2/3 | 2 | Y | Y | 2 | 2 | 2/3 | Y |
| PIC18F8723 | 128K | 65536 | 3936 | 1024 | 70 | 16 | 2/3 | 2 | Y | Y | 2 | 2 | 2/3 | Y |

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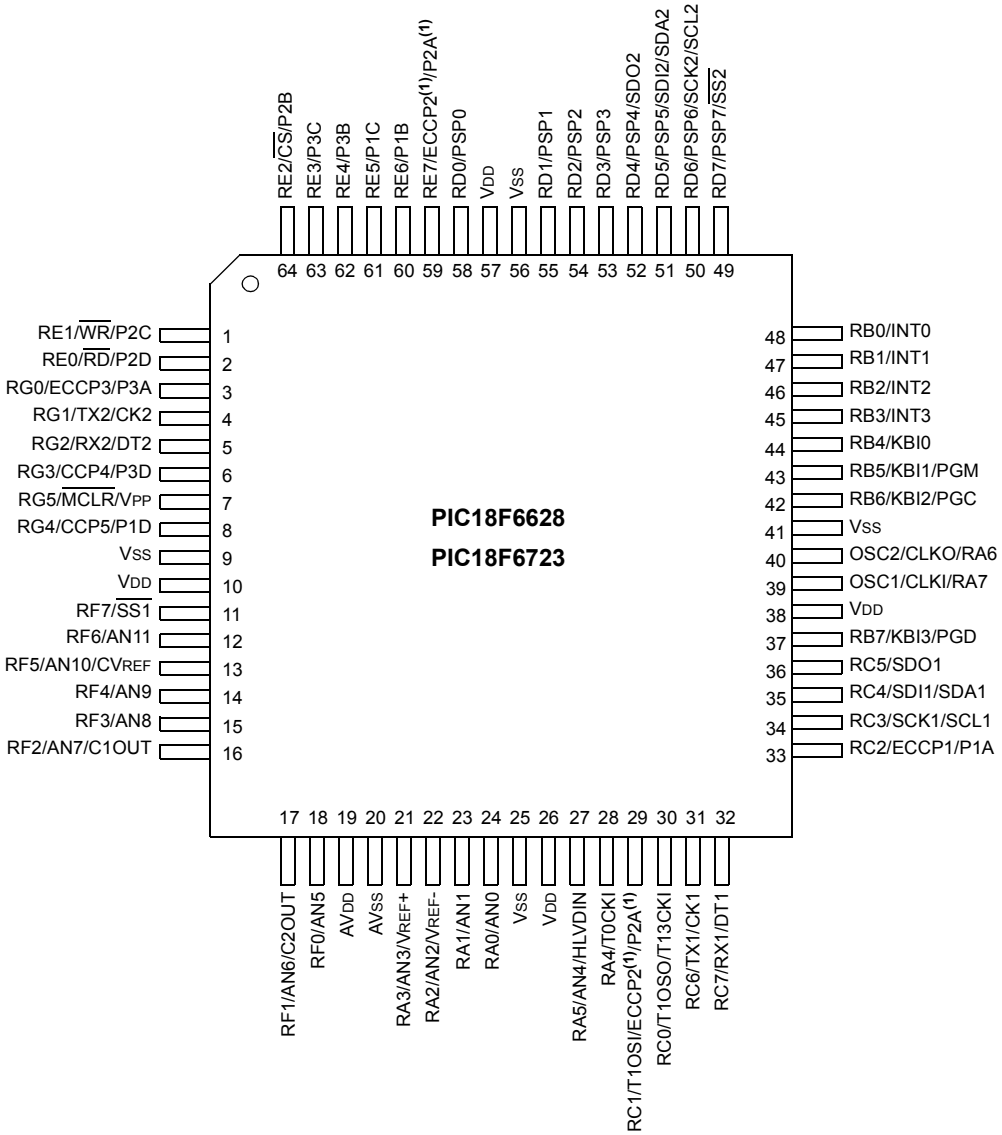
## Pin Diagrams

**64-Pin TQFP**




**Note 1:** The ECCP2/P2A pin placement is determined by the CCP2MX Configuration bit.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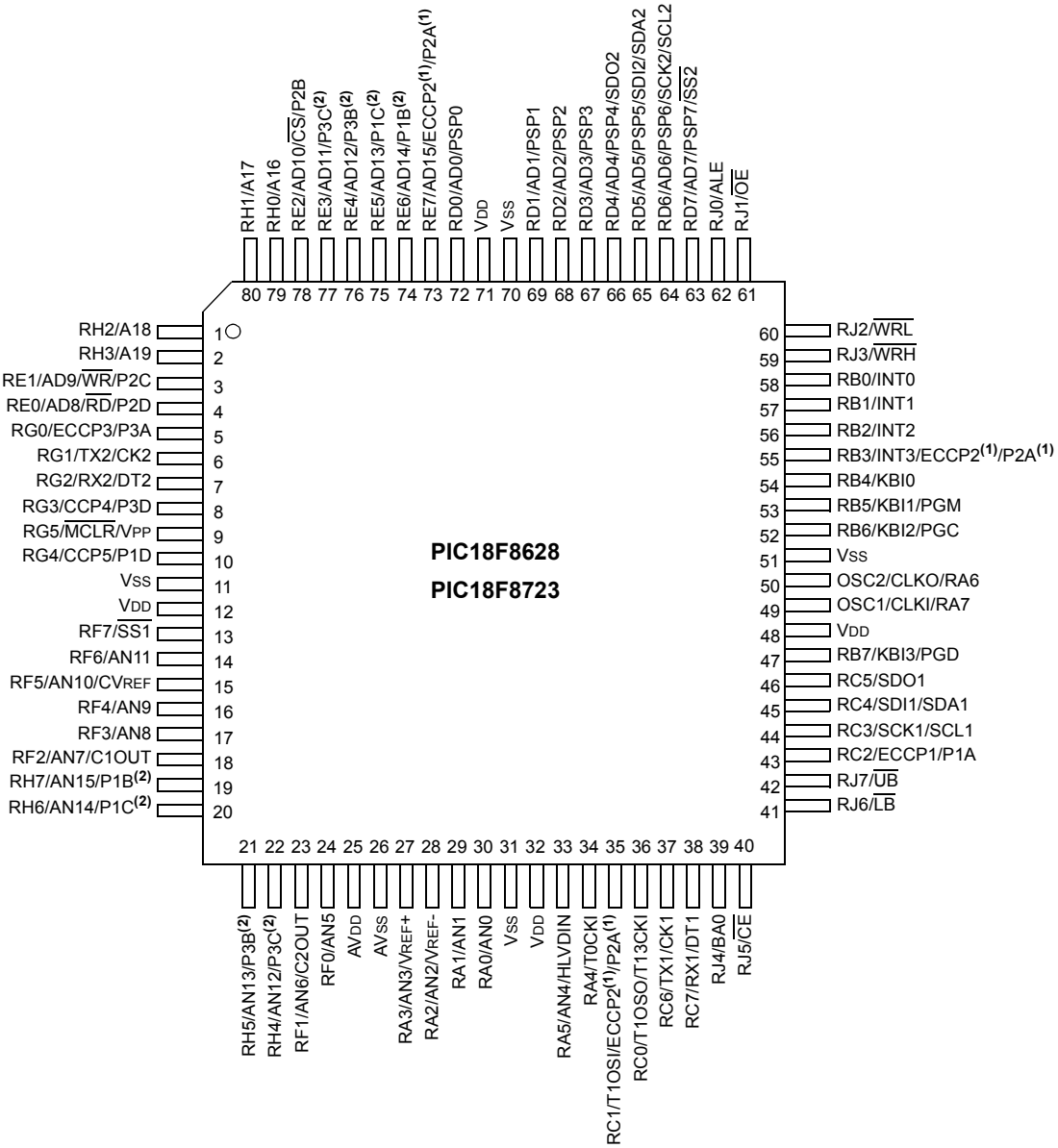
## Pin Diagrams (Continued)

**80-Pin TQFP**




**Note 1:** The ECCP2/P2A pin placement is determined by the CCP2MX Configuration bit and Processor mode settings.
**2:** P1B, P1C, P3B and P3C pin placement is determined by the ECCPMX Configuration bit.

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**NOTES:**


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## 1.0 DEVICE OVERVIEW

This document contains device-specific information for the following devices:

- PIC18F6628
- PIC18F6723
- PIC18F8628
- PIC18F8723
- PIC18LF6628
- PIC18LF6723
- PIC18LF8628
- PIC18LF8723

**Note:** This data sheet documents only the devices' features and specifications that are in addition to the features and specifications of the PIC18F8722 family devices. For information on the features and specifications shared by the PIC18F8723 family and PIC18F8722 family devices, see the *"PIC18F8722 Family Data Sheet"* (DS39646).

The PIC18F8723 family of devices offers the advantages of all PIC18 microcontrollers – namely, high computational performance at an economical price – with the addition of high-endurance, Enhanced Flash program memory. In addition to these features, the PIC18F8723 introduces design enhancements that make these microcontrollers a logical choice for many high-performance, power-sensitive applications.

### 1.1 Special Features

- **12-Bit A/D Converter:** The PIC18F8723 family implements a 12-bit A/D Converter. A/D Converters in both families incorporate programmable acquisition time. This allows for a channel to be selected and a conversion to be initiated, without waiting for a sampling period and thus, reducing code overhead.

### 1.2 Details on Individual Family Members

Devices in the PIC18F8723 family are available in 64-pin and 80-pin packages. Block diagrams for the two groups are shown in Figure 1-1 and Figure 1-2.

The devices are differentiated from each other in the following ways:

- Flash program memory (96 Kbytes for PIC18FX628 devices and 128 Kbytes for PIC18FX723).
- A/D channels (12 for PIC18F6628/6723 devices and 16 for PIC18F8628/8723 devices).
- I/O ports (seven bidirectional ports on PIC18F6628/6723 devices and nine bidirectional ports on PIC18F8628/8723 devices).
- External Memory Bus, configurable for 8 and 16-bit operation

All other features for devices in this family are identical. These are summarized in Table 1-1.

The pinouts for all devices are listed in Table 1-2 and Table 1-3.

Like all Microchip PIC18 devices, members of the PIC18F8723 family are available as both standard and low-voltage devices. Standard devices with Enhanced Flash memory, designated with an "F" in the part number (such as PIC18**F**6628), accommodate an operating VDD range of 4.2V to 5.5V. Low-voltage parts, designated by "LF" (such as PIC18**LF**6628), function over an extended VDD range of 2.0V to 5.5V.

**TABLE 1-1: DEVICE FEATURES**

| Features | PIC18F6628 | PIC18F6723 | PIC18F8628 | PIC18F8723 |
|---|---|---|---|---|
| Operating Frequency | DC – 40 MHz | DC – 40 MHz | DC – 40 MHz | DC – 40 MHz |
| Program Memory (Bytes) | 96K | 128K | 96K | 128K |
| Program Memory (Instructions) | 49152 | 65536 | 49152 | 65536 |
| Data Memory (Bytes) | 3936 | 3936 | 3936 | 3936 |
| Data EEPROM Memory (Bytes) | 1024 | 1024 | 1024 | 1024 |
| Interrupt Sources | 28 | 28 | 29 | 29 |
| I/O Ports | Ports A, B, C, D, E, F, G | Ports A, B, C, D, E, F, G | Ports A, B, C, D, E, F, G, H, J | Ports A, B, C, D, E, F, G, H, J |
| Timers | 5 | 5 | 5 | 5 |
| Capture/Compare/PWM Modules | 2 | 2 | 2 | 2 |
| Enhanced Capture/Compare/ PWM Modules | 3 | 3 | 3 | 3 |
| Enhanced USART | 2 | 2 | 2 | 2 |
| Serial Communications | MSSP, Enhanced USART | MSSP, Enhanced USART | MSSP, Enhanced USART | MSSP, Enhanced USART |
| Parallel Communications (PSP) | Yes | Yes | Yes | Yes |
| 12-Bit Analog-to-Digital Module | 12 Input Channels | 12 Input Channels | 16 Input Channels | 16 Input Channels |
| Resets (and Delays) | POR, BOR, RESET Instruction, Stack Full, Stack Underflow (PWRT, OST), MCLR (optional), WDT | POR, BOR, RESET Instruction, Stack Full, Stack Underflow (PWRT, OST), MCLR (optional), WDT | POR, BOR, RESET Instruction, Stack Full, Stack Underflow (PWRT, OST), MCLR (optional), WDT | POR, BOR, RESET Instruction, Stack Full, Stack Underflow (PWRT, OST), MCLR (optional), WDT |
| Programmable High/Low-Voltage Detect | Yes | Yes | Yes | Yes |
| Programmable Brown-out Reset | Yes | Yes | Yes | Yes |
| Instruction Set | 75 Instructions; 83 with Extended Instruction Set Enabled | 75 Instructions; 83 with Extended Instruction Set Enabled | 75 Instructions; 83 with Extended Instruction Set Enabled | 75 Instructions; 83 with Extended Instruction Set Enabled |
| Packages | 64-Pin TQFP | 64-Pin TQFP | 80-Pin TQFP | 80-Pin TQFP |


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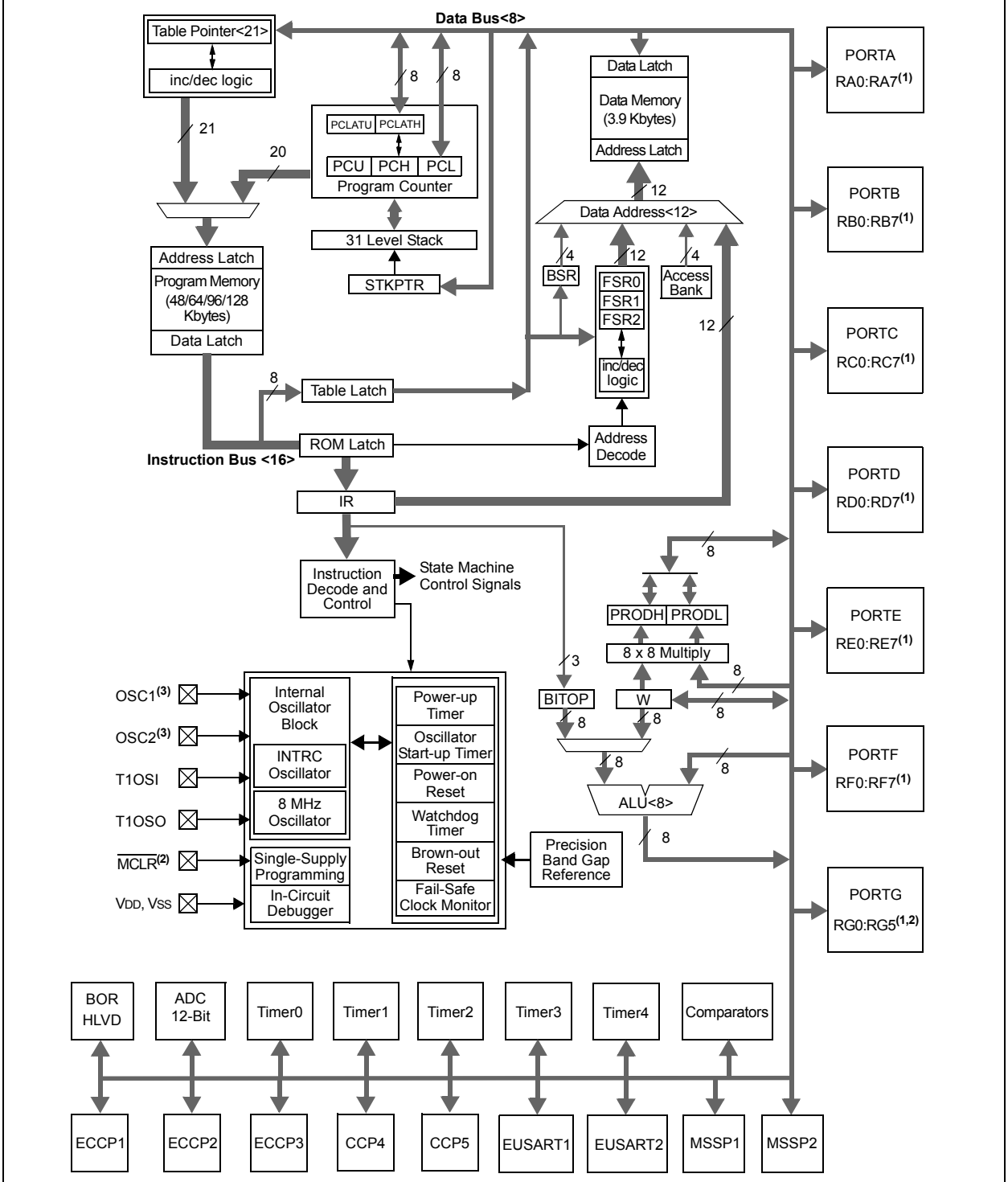
**FIGURE 1-1: PIC18F6628/6723 (64-PIN) BLOCK DIAGRAM**

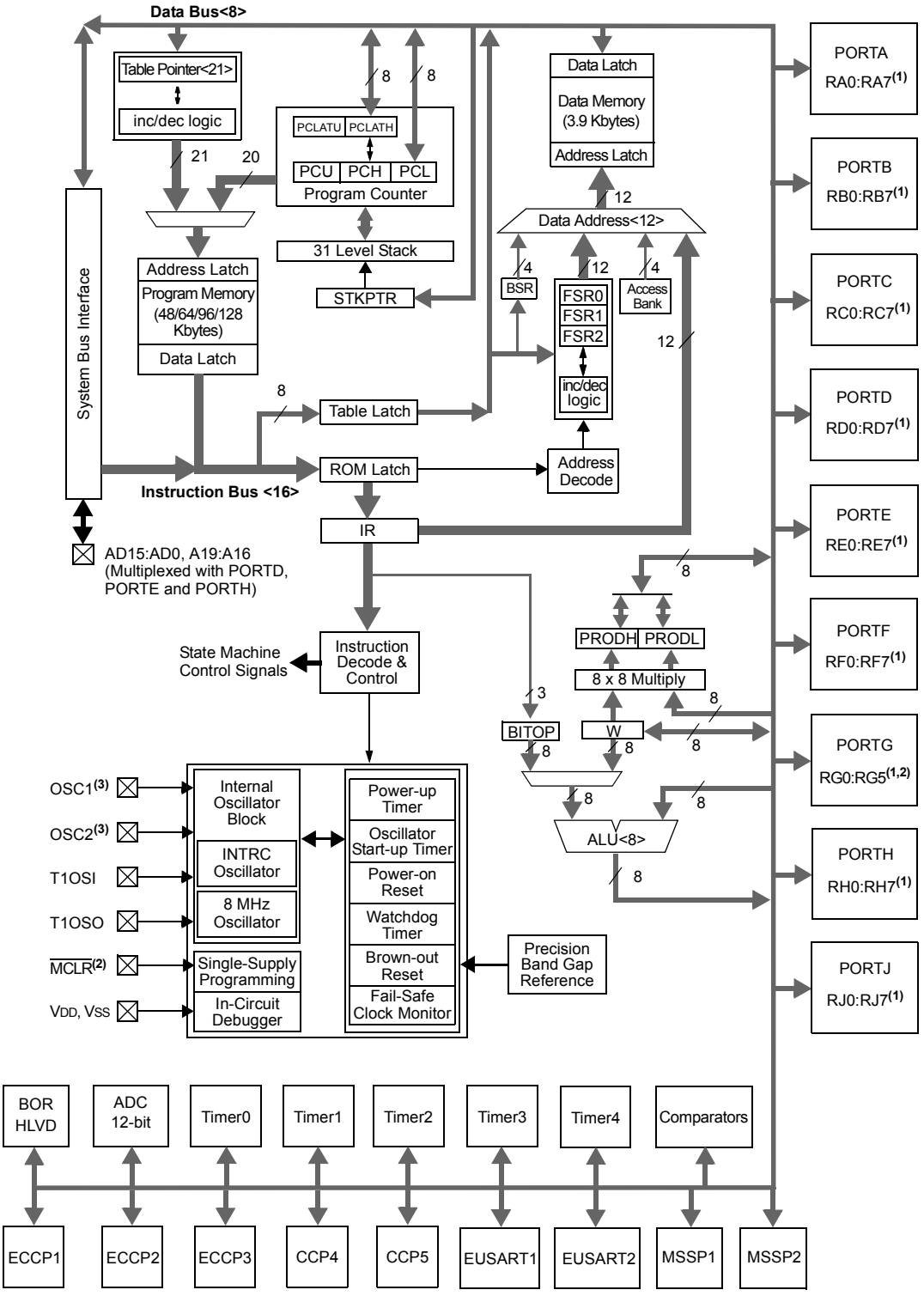



**Note 1:** See Table 1-2 for I/O port pin descriptions.

**2:** RG5 is only available when $\overline{\text{MCLR}}$ functionality is disabled.

**3:** OSC1/CLKI and OSC2/CLKO are only available in select oscillator modes and when these pins are not being used as digital I/O. For additional information, refer to **Section 2.0 "Oscillator Configurations"** of the *"PIC18F8722 Family Data Sheet"* (DS39646).

**FIGURE 1-2: PIC18F8628/8723 (80-PIN) BLOCK DIAGRAM**




**Note 1:** See Table 1-3 for I/O port pin descriptions.

**2:** RG5 is only available when $\overline{\text{MCLR}}$ functionality is disabled.

**3:** OSC1/CLKI and OSC2/CLKO are only available in select oscillator modes and when these pins are not being used as digital I/O. For additional information, refer to **Section 2.0 "Oscillator Configurations"** of the *"PIC18F8722 Family Data Sheet"* (DS39646).


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**TABLE 1-2: PIC18F6628/6723 (64-PIN) PINOUT I/O DESCRIPTIONS**

| Pin Name | Pin Number | Pin Type | Buffer Type | Description |
|---|---|---|---|---|
| | TQFP | | | |
| RG5/$\overline{MCLR}$/$V_{PP}$ | 7 | | | Master Clear (input) or programming voltage (input). |
| RG5 | | I | ST | Digital input. |
| $\overline{MCLR}$ | | I | ST | Master Clear (Reset) input. This pin is an active-low Reset to the device. |
| $V_{PP}$ | | P | | Programming voltage input. |
| OSC1/CLKI/RA7 | 39 | | | Oscillator crystal or external clock input. |
| OSC1 | | I | ST | Oscillator crystal input or external clock source input. ST buffer when configured in RC mode, CMOS otherwise. |
| CLKI | | I | CMOS | External clock source input. Always associated with pin function OSC1. (See related OSC1/CLKI, OSC2/CLKO pins.) |
| RA7 | | I/O | TTL | General purpose I/O pin. |
| OSC2/CLKO/RA6 | 40 | | | Oscillator crystal or clock output. |
| OSC2 | | O | — | Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. |
| CLKO | | O | — | In RC mode, OSC2 pin outputs CLKO, which has 1/4 the frequency of OSC1 and denotes the instruction cycle rate. |
| RA6 | | I/O | TTL | General purpose I/O pin. |

**Legend:** TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; Analog = Analog input; I = Input; O = Output; P = Power; $I^2C$™ = $I^2C$/SMBus input buffer

**Note 1:** Default assignment for ECCP2 when Configuration bit, CCP2MX, is set.

**2:** Alternate assignment for ECCP2 when Configuration bit, CCP2MX, is cleared.

**TABLE 1-2: PIC18F6628/6723 (64-PIN) PINOUT I/O DESCRIPTIONS (CONTINUED)**

| Pin Name | Pin Number | Pin Type | Buffer Type | Description |
|---|---|---|---|---|
| | TQFP | | | |
| | | | | PORTA is a bidirectional I/O port. |
| RA0/AN0 | 24 | | | |
| RA0 | | I/O | TTL | Digital I/O. |
| AN0 | | I | Analog | Analog input 0. |
| RA1/AN1 | 23 | | | |
| RA1 | | I/O | TTL | Digital I/O. |
| AN1 | | I | Analog | Analog input 1. |
| RA2/AN2/VREF- | 22 | | | |
| RA2 | | I/O | TTL | Digital I/O. |
| AN2 | | I | Analog | Analog input 2. |
| VREF- | | I | Analog | A/D reference voltage (low) input. |
| RA3/AN3/VREF+ | 21 | | | |
| RA3 | | I/O | TTL | Digital I/O. |
| AN3 | | I | Analog | Analog input 3. |
| VREF+ | | I | Analog | A/D reference voltage (high) input. |
| RA4/T0CKI | 28 | | | |
| RA4 | | I/O | ST | Digital I/O. |
| T0CKI | | I | ST | Timer0 external clock input. |
| RA5/AN4/HLVDIN | 27 | | | |
| RA5 | | I/O | TTL | Digital I/O. |
| AN4 | | I | Analog | Analog input 4. |
| HLVDIN | | I | Analog | High/Low-Voltage Detect input. |
| RA6 | | | | See the OSC2/CLKO/RA6 pin. |
| RA7 | | | | See the OSC1/CLKI/RA7 pin. |

**Legend:** TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; Analog = Analog input; I = Input; O = Output; P = Power; $I^2C$™ = $I^2C$/SMBus input buffer

**Note 1:** Default assignment for ECCP2 when Configuration bit, CCP2MX, is set.

**2:** Alternate assignment for ECCP2 when Configuration bit, CCP2MX, is cleared.


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**TABLE 1-2: PIC18F6628/6723 (64-PIN) PINOUT I/O DESCRIPTIONS (CONTINUED)**

| Pin Name | Pin Number | Pin Type | Buffer Type | Description |
|---|---|---|---|---|
| | TQFP | | | |
| | | | | PORTB is a bidirectional I/O port. PORTB can be software programmed for internal weak pull-ups on all inputs. |
| RB0/INT0/FLT0 | 48 | | | |
| RB0 | | I/O | TTL | Digital I/O. |
| INT0 | | I | ST | External interrupt 0. |
| FLT0 | | I | ST | PWM Fault input for ECCPx. |
| RB1/INT1 | 47 | | | |
| RB1 | | I/O | TTL | Digital I/O. |
| INT1 | | I | ST | External interrupt 1. |
| RB2/INT2 | 46 | | | |
| RB2 | | I/O | TTL | Digital I/O. |
| INT2 | | I | ST | External interrupt 2. |
| RB3/INT3 | 45 | | | |
| RB3 | | I/O | TTL | Digital I/O. |
| INT3 | | I | ST | External interrupt 3. |
| RB4/KBI0 | 44 | | | |
| RB4 | | I/O | TTL | Digital I/O. |
| KBI0 | | I | TTL | Interrupt-on-change pin. |
| RB5/KBI1/PGM | 43 | | | |
| RB5 | | I/O | TTL | Digital I/O. |
| KBI1 | | I | TTL | Interrupt-on-change pin. |
| PGM | | I/O | ST | Low-Voltage ICSP™ Programming enable pin. |
| RB6/KBI2/PGC | 42 | | | |
| RB6 | | I/O | TTL | Digital I/O. |
| KBI2 | | I | TTL | Interrupt-on-change pin. |
| PGC | | I/O | ST | In-Circuit Debugger and ICSP programming clock pin. |
| RB7/KBI3/PGD | 37 | | | |
| RB7 | | I/O | TTL | Digital I/O. |
| KBI3 | | I | TTL | Interrupt-on-change pin. |
| PGD | | I/O | ST | In-Circuit Debugger and ICSP programming data pin. |

**Legend:** TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; Analog = Analog input; I = Input; O = Output; P = Power; $I^2C$™ = $I^2C$/SMBus input buffer

**Note 1:** Default assignment for ECCP2 when Configuration bit, CCP2MX, is set.

**2:** Alternate assignment for ECCP2 when Configuration bit, CCP2MX, is cleared.

**TABLE 1-2: PIC18F6628/6723 (64-PIN) PINOUT I/O DESCRIPTIONS (CONTINUED)**

| Pin Name | Pin Number | Pin Type | Buffer Type | Description |
|---|---|---|---|---|
| | TQFP | | | |
| | | | | PORTC is a bidirectional I/O port. |
| RC0/T1OSO/T13CKI | 30 | | | |
| RC0 | | I/O | ST | Digital I/O. |
| T1OSO | | O | — | Timer1 oscillator output. |
| T13CKI | | I | ST | Timer1/Timer3 external clock input. |
| RC1/T1OSI/ECCP2/ P2A | 29 | | | |
| RC1 | | I/O | ST | Digital I/O. |
| T1OSI | | I | CMOS | Timer1 oscillator input. |
| ECCP2(1) | | I/O | ST | Enhanced Capture 2 input/Compare 2 output/ PWM2 output. |
| P2A(1) | | O | — | ECCP2 PWM output A. |
| RC2/ECCP1/P1A | 33 | | | |
| RC2 | | I/O | ST | Digital I/O. |
| ECCP1 | | I/O | ST | Enhanced Capture 1 input/Compare 1 output/ PWM1 output. |
| P1A | | O | — | ECCP1 PWM output A. |
| RC3/SCK1/SCL1 | 34 | | | |
| RC3 | | I/O | ST | Digital I/O. |
| SCK1 | | I/O | ST | Synchronous serial clock input/output for SPI mode. |
| SCL1 | | I/O | ST | Synchronous serial clock input/output for $I^2C$™ mode. |
| RC4/SDI1/SDA1 | 35 | | | |
| RC4 | | I/O | ST | Digital I/O. |
| SDI1 | | I | ST | SPI data in. |
| SDA1 | | I/O | ST | $I^2C$ data I/O. |
| RC5/SDO1 | 36 | | | |
| RC5 | | I/O | ST | Digital I/O. |
| SDO1 | | O | — | SPI data out. |
| RC6/TX1/CK1 | 31 | | | |
| RC6 | | I/O | ST | Digital I/O. |
| TX1 | | O | — | EUSART1 asynchronous transmit. |
| CK1 | | I/O | ST | EUSART1 synchronous clock (see related RX1/DT1). |
| RC7/RX1/DT1 | 32 | | | |
| RC7 | | I/O | ST | Digital I/O. |
| RX1 | | I | ST | EUSART1 asynchronous receive. |
| DT1 | | I/O | ST | EUSART1 synchronous data (see related TX1/CK1). |

**Legend:** TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; Analog = Analog input; I = Input; O = Output; P = Power; $I^2C$™ = $I^2C$/SMBus input buffer

**Note 1:** Default assignment for ECCP2 when Configuration bit, CCP2MX, is set.

**2:** Alternate assignment for ECCP2 when Configuration bit, CCP2MX, is cleared.


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**TABLE 1-2: PIC18F6628/6723 (64-PIN) PINOUT I/O DESCRIPTIONS (CONTINUED)**

| Pin Name | Pin Number | Pin Type | Buffer Type | Description |
|---|---|---|---|---|
| | TQFP | | | |
| | | | | PORTD is a bidirectional I/O port. |
| RD0/PSP0 | 58 | | | |
| RD0 | | I/O | ST | Digital I/O. |
| PSP0 | | I/O | TTL | Parallel Slave Port data. |
| RD1/PSP1 | 55 | | | |
| RD1 | | I/O | ST | Digital I/O. |
| PSP1 | | I/O | TTL | Parallel Slave Port data. |
| RD2/PSP2 | 54 | | | |
| RD2 | | I/O | ST | Digital I/O. |
| PSP2 | | I/O | TTL | Parallel Slave Port data. |
| RD3/PSP3 | 53 | | | |
| RD3 | | I/O | ST | Digital I/O. |
| PSP3 | | I/O | TTL | Parallel Slave Port data. |
| RD4/PSP4/SDO2 | 52 | | | |
| RD4 | | I/O | ST | Digital I/O. |
| PSP4 | | I/O | TTL | Parallel Slave Port data. |
| SDO2 | | O | — | SPI data out. |
| RD5/PSP5/SDI2/ SDA2 | 51 | | | |
| RD5 | | I/O | ST | Digital I/O. |
| PSP5 | | I/O | TTL | Parallel Slave Port data. |
| SDI2 | | I | ST | SPI data in. |
| SDA2 | | I/O | $I^2C$/SMB | $I^2C$™ data I/O. |
| RD6/PSP6/SCK2/ SCL2 | 50 | | | |
| RD6 | | I/O | ST | Digital I/O. |
| PSP6 | | I/O | TTL | Parallel Slave Port data. |
| SCK2 | | I/O | ST | Synchronous serial clock input/output for SPI mode. |
| SCL2 | | I/O | $I^2C$/SMB | Synchronous serial clock input/output for $I^2C$ mode. |
| RD7/PSP7/$\overline{SS2}$ | 49 | | | |
| RD7 | | I/O | ST | Digital I/O. |
| PSP7 | | I/O | TTL | Parallel Slave Port data. |
| $\overline{SS2}$ | | I | TTL | SPI slave select input. |

**Legend:** TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; Analog = Analog input; I = Input; O = Output; P = Power; $I^2C$™ = $I^2C$/SMBus input buffer

**Note 1:** Default assignment for ECCP2 when Configuration bit, CCP2MX, is set.

**2:** Alternate assignment for ECCP2 when Configuration bit, CCP2MX, is cleared.

**TABLE 1-2: PIC18F6628/6723 (64-PIN) PINOUT I/O DESCRIPTIONS (CONTINUED)**

| Pin Name | Pin Number | Pin Type | Buffer Type | Description |
|---|---|---|---|---|
| | TQFP | | | |
| | | | | PORTE is a bidirectional I/O port. |
| RE0/$\overline{RD}$/P2D | 2 | | | |
| RE0 | | I/O | ST | Digital I/O. |
| $\overline{RD}$ | | I | TTL | Read control for Parallel Slave Port. |
| P2D | | O | — | ECCP2 PWM output D. |
| RE1/$\overline{WR}$/P2C | 1 | | | |
| RE1 | | I/O | ST | Digital I/O. |
| $\overline{WR}$ | | I | TTL | Write control for Parallel Slave Port. |
| P2C | | O | — | ECCP2 PWM output C. |
| RE2/$\overline{CS}$/P2B | 64 | | | |
| RE2 | | I/O | ST | Digital I/O. |
| $\overline{CS}$ | | I | TTL | Chip select control for Parallel Slave Port. |
| P2B | | O | — | ECCP2 PWM output B. |
| RE3/P3C | 63 | | | |
| RE3 | | I/O | ST | Digital I/O. |
| P3C | | O | — | ECCP3 PWM output C. |
| RE4/P3B | 62 | | | |
| RE4 | | I/O | ST | Digital I/O. |
| P3B | | O | — | ECCP3 PWM output B. |
| RE5/P1C | 61 | | | |
| RE5 | | I/O | ST | Digital I/O. |
| P1C | | O | — | ECCP1 PWM output C. |
| RE6/P1B | 60 | | | |
| RE6 | | I/O | ST | Digital I/O. |
| P1B | | O | — | ECCP1 PWM output B. |
| RE7/ECCP2/P2A | 59 | | | |
| RE7 | | I/O | ST | Digital I/O. |
| ECCP2**(2)** | | I/O | ST | Enhanced Capture 2 input/Compare 2 output/ PWM2 output. |
| P2A**(2)** | | O | — | ECCP2 PWM output A. |

**Legend:** TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; Analog = Analog input; I = Input; O = Output; P = Power; $I^2C$™ = $I^2C$/SMBus input buffer

**Note 1:** Default assignment for ECCP2 when Configuration bit, CCP2MX, is set.

**2:** Alternate assignment for ECCP2 when Configuration bit, CCP2MX, is cleared.


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**TABLE 1-2: PIC18F6628/6723 (64-PIN) PINOUT I/O DESCRIPTIONS (CONTINUED)**

| Pin Name | Pin Number | Pin Type | Buffer Type | Description |
|---|---|---|---|---|
| | TQFP | | | |
| | | | | PORTF is a bidirectional I/O port. |
| RF0/AN5 | 18 | | | |
| RF0 | | I/O | ST | Digital I/O. |
| AN5 | | I | Analog | Analog input 5. |
| RF1/AN6/C2OUT | 17 | | | |
| RF1 | | I/O | ST | Digital I/O. |
| AN6 | | I | Analog | Analog input 6. |
| C2OUT | | O | — | Comparator 2 output. |
| RF2/AN7/C1OUT | 16 | | | |
| RF2 | | I/O | ST | Digital I/O. |
| AN7 | | I | Analog | Analog input 7. |
| C1OUT | | O | — | Comparator 1 output. |
| RF3/AN8 | 15 | | | |
| RF3 | | I/O | ST | Digital I/O. |
| AN8 | | I | Analog | Analog input 8. |
| RF4/AN9 | 14 | | | |
| RF4 | | I/O | ST | Digital I/O. |
| AN9 | | I | Analog | Analog input 9. |
| RF5/AN10/CVREF | 13 | | | |
| RF5 | | I/O | ST | Digital I/O. |
| AN10 | | I | Analog | Analog input 10. |
| CVREF | | O | Analog | Comparator reference voltage output. |
| RF6/AN11 | 12 | | | |
| RF6 | | I/O | ST | Digital I/O. |
| AN11 | | I | Analog | Analog input 11. |
| RF7/$\overline{SS1}$ | 11 | | | |
| RF7 | | I/O | ST | Digital I/O. |
| $\overline{SS1}$ | | I | TTL | SPI slave select input. |

**Legend:** TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; Analog = Analog input; I = Input; O = Output; P = Power; $I^2C$™ = $I^2C$/SMBus input buffer

**Note 1:** Default assignment for ECCP2 when Configuration bit, CCP2MX, is set.

**2:** Alternate assignment for ECCP2 when Configuration bit, CCP2MX, is cleared.

**TABLE 1-2: PIC18F6628/6723 (64-PIN) PINOUT I/O DESCRIPTIONS (CONTINUED)**

| Pin Name | Pin Number | Pin Type | Buffer Type | Description |
|---|---|---|---|---|
| | TQFP | | | |
| | | | | PORTG is a bidirectional I/O port. |
| RG0/ECCP3/P3A | 3 | | | |
| RG0 | | I/O | ST | Digital I/O. |
| ECCP3 | | I/O | ST | Enhanced Capture 3 input/Compare 3 output/ PWM3 output. |
| P3A | | O | — | ECCP3 PWM output A. |
| RG1/TX2/CK2 | 4 | | | |
| RG1 | | I/O | ST | Digital I/O. |
| TX2 | | O | — | EUSART2 asynchronous transmit. |
| CK2 | | I/O | ST | EUSART2 synchronous clock (see related RX2/DT2). |
| RG2/RX2/DT2 | 5 | | | |
| RG2 | | I/O | ST | Digital I/O. |
| RX2 | | I | ST | EUSART2 asynchronous receive. |
| DT2 | | I/O | ST | EUSART2 synchronous data (see related TX2/CK2). |
| RG3/CCP4/P3D | 6 | | | |
| RG3 | | I/O | ST | Digital I/O. |
| CCP4 | | I/O | ST | Capture 4 input/Compare 4 output/PWM4 output. |
| P3D | | O | — | ECCP3 PWM output D. |
| RG4/CCP5/P1D | 8 | | | |
| RG4 | | I/O | ST | Digital I/O. |
| CCP5 | | I/O | ST | Capture 5 input/Compare 5 output/PWM5 output. |
| P1D | | O | — | ECCP1 PWM output D. |
| RG5 | | | | See RG5/$\overline{\text{MCLR}}$/VPP pin. |
| VSS | 9, 25, 41, 56 | P | — | Ground reference for logic and I/O pins. |
| VDD | 10, 26, 38, 57 | P | — | Positive supply for logic and I/O pins. |
| AVSS | 20 | P | — | Ground reference for analog modules. |
| AVDD | 19 | P | — | Positive supply for analog modules. |

**Legend:** TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; Analog = Analog input; I = Input; O = Output; P = Power; $I^2C$™ = $I^2C$/SMBus input buffer

**Note 1:** Default assignment for ECCP2 when Configuration bit, CCP2MX, is set.

**2:** Alternate assignment for ECCP2 when Configuration bit, CCP2MX, is cleared.


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**TABLE 1-3: PIC18F8628/8723 (80-PIN) PINOUT I/O DESCRIPTIONS**

| Pin Name | Pin Number | Pin Type | Buffer Type | Description |
|---|---|---|---|---|
| | TQFP | | | |
| RG5/$\overline{MCLR}$/VPP | 9 | | | Master Clear (input) or programming voltage (input). |
| RG5 | | I | ST | Digital input. |
| $\overline{MCLR}$ | | I | ST | Master Clear (Reset) input. This pin is an active-low Reset to the device. |
| VPP | | P | | Programming voltage input. |
| OSC1/CLKI/RA7 | 49 | | | Oscillator crystal or external clock input. |
| OSC1 | | I | ST | Oscillator crystal input or external clock source input. ST buffer when configured in RC mode, CMOS otherwise. |
| CLKI | | I | CMOS | External clock source input. Always associated with pin function OSC1. (See related OSC1/CLKI, OSC2/CLKO pins.) |
| RA7 | | I/O | TTL | General purpose I/O pin. |
| OSC2/CLKO/RA6 | 50 | | | Oscillator crystal or clock output. |
| OSC2 | | O | — | Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. |
| CLKO | | O | — | In RC mode, OSC2 pin outputs CLKO, which has 1/4 the frequency of OSC1 and denotes the instruction cycle rate. |
| RA6 | | I/O | TTL | General purpose I/O pin. |

**Legend:** TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; Analog = Analog input; I = Input; O = Output; P = Power; $I^2C$™/SMB = $I^2C$/SMBus input buffer

**Note 1:** Alternate assignment for ECCP2 when Configuration bit, CCP2MX, is cleared (all operating modes except Microcontroller mode).

**2:** Default assignment for ECCP2 in all operating modes (CCP2MX is set).

**3:** Alternate assignment for ECCP2 when CCP2MX is cleared (Microcontroller mode only).

**4:** Default assignment for P1B/P1C/P3B/P3C (ECCPMX is set).

**5:** Alternate assignment for P1B/P1C/P3B/P3C (ECCPMX is clear).

**TABLE 1-3: PIC18F8628/8723 (80-PIN) PINOUT I/O DESCRIPTIONS (CONTINUED)**

| Pin Name | Pin Number | Pin Type | Buffer Type | Description |
|---|---|---|---|---|
| | TQFP | | | |
| | | | | PORTA is a bidirectional I/O port. |
| RA0/AN0 | 30 | | | |
| RA0 | | I/O | TTL | Digital I/O. |
| AN0 | | I | Analog | Analog input 0. |
| RA1/AN1 | 29 | | | |
| RA1 | | I/O | TTL | Digital I/O. |
| AN1 | | I | Analog | Analog input 1. |
| RA2/AN2/VREF- | 28 | | | |
| RA2 | | I/O | TTL | Digital I/O. |
| AN2 | | I | Analog | Analog input 2. |
| VREF- | | I | Analog | A/D reference voltage (low) input. |
| RA3/AN3/VREF+ | 27 | | | |
| RA3 | | I/O | TTL | Digital I/O. |
| AN3 | | I | Analog | Analog input 3. |
| VREF+ | | I | Analog | A/D reference voltage (high) input. |
| RA4/T0CKI | 34 | | | |
| RA4 | | I/O | ST | Digital I/O. |
| T0CKI | | I | ST | Timer0 external clock input. |
| RA5/AN4/HLVDIN | 33 | | | |
| RA5 | | I/O | TTL | Digital I/O. |
| AN4 | | I | Analog | Analog input 4. |
| HLVDIN | | I | Analog | High/Low-Voltage Detect input. |
| RA6 | | | | See the OSC2/CLKO/RA6 pin. |
| RA7 | | | | See the OSC1/CLKI/RA7 pin. |

**Legend:** TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; Analog = Analog input; I = Input; O = Output; P = Power; $I^2C$™/SMB = $I^2C$/SMBus input buffer

**Note 1:** Alternate assignment for ECCP2 when Configuration bit, CCP2MX, is cleared (all operating modes except Microcontroller mode).

**2:** Default assignment for ECCP2 in all operating modes (CCP2MX is set).

**3:** Alternate assignment for ECCP2 when CCP2MX is cleared (Microcontroller mode only).

**4:** Default assignment for P1B/P1C/P3B/P3C (ECCPMX is set).

**5:** Alternate assignment for P1B/P1C/P3B/P3C (ECCPMX is clear).


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**TABLE 1-3: PIC18F8628/8723 (80-PIN) PINOUT I/O DESCRIPTIONS (CONTINUED)**

| Pin Name | Pin Number | Pin Type | Buffer Type | Description |
|---|---|---|---|---|
| | TQFP | | | |
| | | | | PORTB is a bidirectional I/O port. PORTB can be software programmed for internal weak pull-ups on all inputs. |
| RB0/INT0/FLT0 | 58 | | | |
| RB0 | | I/O | TTL | Digital I/O. |
| INT0 | | I | ST | External interrupt 0. |
| FLT0 | | I | ST | PWM Fault input for ECCPx. |
| RB1/INT1 | 57 | | | |
| RB1 | | I/O | TTL | Digital I/O. |
| INT1 | | I | ST | External interrupt 1. |
| RB2/INT2 | 56 | | | |
| RB2 | | I/O | TTL | Digital I/O. |
| INT2 | | I | ST | External interrupt 2. |
| RB3/INT3/ECCP2/P2A | 55 | | | |
| RB3 | | I/O | TTL | Digital I/O. |
| INT3 | | I | ST | External interrupt 3. |
| ECCP2(1) | | O | — | Enhanced Capture 2 input/Compare 2 output/ PWM2 output. |
| P2A(1) | | O | — | ECCP2 PWM output A. |
| RB4/KBI0 | 54 | | | |
| RB4 | | I/O | TTL | Digital I/O. |
| KBI0 | | I | TTL | Interrupt-on-change pin. |
| RB5/KBI1/PGM | 53 | | | |
| RB5 | | I/O | TTL | Digital I/O. |
| KBI1 | | I | TTL | Interrupt-on-change pin. |
| PGM | | I/O | ST | Low-Voltage ICSP™ Programming enable pin. |
| RB6/KBI2/PGC | 52 | | | |
| RB6 | | I/O | TTL | Digital I/O. |
| KBI2 | | I | TTL | Interrupt-on-change pin. |
| PGC | | I/O | ST | In-Circuit Debugger and ICSP™ programming clock pin. |
| RB7/KBI3/PGD | 47 | | | |
| RB7 | | I/O | TTL | Digital I/O. |
| KBI3 | | I | TTL | Interrupt-on-change pin. |
| PGD | | I/O | ST | In-Circuit Debugger and ICSP programming data pin. |

**Legend:** TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; Analog = Analog input; I = Input; O = Output; P = Power; $I^2C$™/SMB = $I^2C$/SMBus input buffer

**Note 1:** Alternate assignment for ECCP2 when Configuration bit, CCP2MX, is cleared (all operating modes except Microcontroller mode).

**2:** Default assignment for ECCP2 in all operating modes (CCP2MX is set).

**3:** Alternate assignment for ECCP2 when CCP2MX is cleared (Microcontroller mode only).

**4:** Default assignment for P1B/P1C/P3B/P3C (ECCPMX is set).

**5:** Alternate assignment for P1B/P1C/P3B/P3C (ECCPMX is clear).

**TABLE 1-3: PIC18F8628/8723 (80-PIN) PINOUT I/O DESCRIPTIONS (CONTINUED)**

| Pin Name | Pin Number | Pin Type | Buffer Type | Description |
|---|---|---|---|---|
| | TQFP | | | |
| | | | | PORTC is a bidirectional I/O port. |
| RC0/T1OSO/T13CKI | 36 | | | |
| RC0 | | I/O | ST | Digital I/O. |
| T1OSO | | O | — | Timer1 oscillator output. |
| T13CKI | | I | ST | Timer1/Timer3 external clock input. |
| RC1/T1OSI/ECCP2/ P2A | 35 | | | |
| RC1 | | I/O | ST | Digital I/O. |
| T1OSI | | I | CMOS | Timer1 oscillator input. |
| ECCP2(2) | | I/O | ST | Enhanced Capture 2 input/Compare 2 output/ PWM2 output. |
| P2A(2) | | O | — | ECCP2 PWM output A. |
| RC2/ECCP1/P1A | 43 | | | |
| RC2 | | I/O | ST | Digital I/O. |
| ECCP1 | | I/O | ST | Enhanced Capture 1 input/Compare 1 output/ PWM1 output. |
| P1A | | O | — | ECCP1 PWM output A. |
| RC3/SCK1/SCL1 | 44 | | | |
| RC3 | | I/O | ST | Digital I/O. |
| SCK1 | | I/O | ST | Synchronous serial clock input/output for SPI mode. |
| SCL1 | | I/O | ST | Synchronous serial clock input/output for $I^2C$™ mode. |
| RC4/SDI1/SDA1 | 45 | | | |
| RC4 | | I/O | ST | Digital I/O. |
| SDI1 | | I | ST | SPI data in. |
| SDA1 | | I/O | ST | $I^2C$ data I/O. |
| RC5/SDO1 | 46 | | | |
| RC5 | | I/O | ST | Digital I/O. |
| SDO1 | | O | — | SPI data out. |
| RC6/TX1/CK1 | 37 | | | |
| RC6 | | I/O | ST | Digital I/O. |
| TX1 | | O | — | EUSART1 asynchronous transmit. |
| CK1 | | I/O | ST | EUSART1 synchronous clock (see related RX1/DT1). |
| RC7/RX1/DT1 | 38 | | | |
| RC7 | | I/O | ST | Digital I/O. |
| RX1 | | I | ST | EUSART1 asynchronous receive. |
| DT1 | | I/O | ST | EUSART1 synchronous data (see related TX1/CK1). |

**Legend:** TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; Analog = Analog input; I = Input; O = Output; P = Power; $I^2C$™/SMB = $I^2C$/SMBus input buffer

**Note 1:** Alternate assignment for ECCP2 when Configuration bit, CCP2MX, is cleared (all operating modes except Microcontroller mode).

**2:** Default assignment for ECCP2 in all operating modes (CCP2MX is set).

**3:** Alternate assignment for ECCP2 when CCP2MX is cleared (Microcontroller mode only).

**4:** Default assignment for P1B/P1C/P3B/P3C (ECCPMX is set).

**5:** Alternate assignment for P1B/P1C/P3B/P3C (ECCPMX is clear).


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**TABLE 1-3: PIC18F8628/8723 (80-PIN) PINOUT I/O DESCRIPTIONS (CONTINUED)**

| Pin Name | Pin Number | Pin Type | Buffer Type | Description |
|---|---|---|---|---|
| | TQFP | | | |
| | | | | PORTD is a bidirectional I/O port. |
| RD0/AD0/PSP0 | 72 | | | |
| RD0 | | I/O | ST | Digital I/O. |
| AD0 | | I/O | TTL | External memory address/data 0. |
| PSP0 | | I/O | TTL | Parallel Slave Port data. |
| RD1/AD1/PSP1 | 69 | | | |
| RD1 | | I/O | ST | Digital I/O. |
| AD1 | | I/O | TTL | External memory address/data 1. |
| PSP1 | | I/O | TTL | Parallel Slave Port data. |
| RD2/AD2/PSP2 | 68 | | | |
| RD2 | | I/O | ST | Digital I/O. |
| AD2 | | I/O | TTL | External memory address/data 2. |
| PSP2 | | I/O | TTL | Parallel Slave Port data. |
| RD3/AD3/PSP3 | 67 | | | |
| RD3 | | I/O | ST | Digital I/O. |
| AD3 | | I/O | TTL | External memory address/data 3. |
| PSP3 | | I/O | TTL | Parallel Slave Port data. |
| RD4/AD4/PSP4/SDO2 | 66 | | | |
| RD4 | | I/O | ST | Digital I/O. |
| AD4 | | I/O | TTL | External memory address/data 4. |
| PSP4 | | I/O | TTL | Parallel Slave Port data. |
| SDO2 | | O | — | SPI data out. |
| RD5/AD5/PSP5/ SDI2/SDA2 | 65 | | | |
| RD5 | | I/O | ST | Digital I/O. |
| AD5 | | I/O | TTL | External memory address/data 5. |
| PSP5 | | I/O | TTL | Parallel Slave Port data. |
| SDI2 | | I | ST | SPI data in. |
| SDA2 | | I/O | $I^2C$/SMB | $I^2C$™ data I/O. |
| RD6/AD6/PSP6/ SCK2/SCL2 | 64 | | | |
| RD6 | | I/O | ST | Digital I/O. |
| AD6 | | I/O | TTL | External memory address/data 6. |
| PSP6 | | I/O | TTL | Parallel Slave Port data. |
| SCK2 | | I/O | ST | Synchronous serial clock input/output for SPI mode. |
| SCL2 | | I/O | $I^2C$/SMB | Synchronous serial clock input/output for $I^2C$ mode. |
| RD7/AD7/PSP7/$\overline{SS2}$ | 63 | | | |
| RD7 | | I/O | ST | Digital I/O. |
| AD7 | | I/O | TTL | External memory address/data 7. |
| PSP7 | | I/O | TTL | Parallel Slave Port data. |
| $\overline{SS2}$ | | I | TTL | SPI slave select input. |

**Legend:** TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; Analog = Analog input; I = Input; O = Output; P = Power; $I^2C$™/SMB = $I^2C$/SMBus input buffer

**Note 1:** Alternate assignment for ECCP2 when Configuration bit, CCP2MX, is cleared (all operating modes except Microcontroller mode).

**2:** Default assignment for ECCP2 in all operating modes (CCP2MX is set).

**3:** Alternate assignment for ECCP2 when CCP2MX is cleared (Microcontroller mode only).

**4:** Default assignment for P1B/P1C/P3B/P3C (ECCPMX is set).

**5:** Alternate assignment for P1B/P1C/P3B/P3C (ECCPMX is clear).

**TABLE 1-3: PIC18F8628/8723 (80-PIN) PINOUT I/O DESCRIPTIONS (CONTINUED)**

| Pin Name | Pin Number | Pin Type | Buffer Type | Description |
|---|---|---|---|---|
| | TQFP | | | |
| | | | | PORTE is a bidirectional I/O port. |
| RE0/AD8/$\overline{RD}$/P2D | 4 | | | |
| RE0 | | I/O | ST | Digital I/O. |
| AD8 | | I/O | TTL | External memory address/data 8. |
| $\overline{RD}$ | | I | TTL | Read control for Parallel Slave Port. |
| P2D | | O | — | ECCP2 PWM output D. |
| RE1/AD9/$\overline{WR}$/P2C | 3 | | | |
| RE1 | | I/O | ST | Digital I/O. |
| AD9 | | I/O | TTL | External memory address/data 9. |
| $\overline{WR}$ | | I | TTL | Write control for Parallel Slave Port. |
| P2C | | O | — | ECCP2 PWM output C. |
| RE2/AD10/$\overline{CS}$/P2B | 78 | | | |
| RE2 | | I/O | ST | Digital I/O. |
| AD10 | | I/O | TTL | External memory address/data 10. |
| $\overline{CS}$ | | I | TTL | Chip select control for Parallel Slave Port. |
| P2B | | O | — | ECCP2 PWM output B. |
| RE3/AD11/P3C | 77 | | | |
| RE3 | | I/O | ST | Digital I/O. |
| AD11 | | I/O | TTL | External memory address/data 11. |
| P3C(4) | | O | — | ECCP3 PWM output C. |
| RE4/AD12/P3B | 76 | | | |
| RE4 | | I/O | ST | Digital I/O. |
| AD12 | | I/O | TTL | External memory address/data 12. |
| P3B(4) | | O | — | ECCP3 PWM output B. |
| RE5/AD13/P1C | 75 | | | |
| RE5 | | I/O | ST | Digital I/O. |
| AD13 | | I/O | TTL | External memory address/data 13. |
| P1C(4) | | O | — | ECCP1 PWM output C. |
| RE6/AD14/P1B | 74 | | | |
| RE6 | | I/O | ST | Digital I/O. |
| AD14 | | I/O | TTL | External memory address/data 14. |
| P1B(4) | | O | — | ECCP1 PWM output B. |
| RE7/AD15/ECCP2/ P2A | 73 | | | |
| RE7 | | I/O | ST | Digital I/O. |
| AD15 | | I/O | TTL | External memory address/data 15. |
| ECCP2(3) | | I/O | ST | Enhanced Capture 2 input/Compare 2 output/ PWM2 output. |
| P2A(3) | | O | — | ECCP2 PWM output A. |

**Legend:** TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; Analog = Analog input; I = Input; O = Output; P = Power; $I^2C$™/SMB = $I^2C$/SMBus input buffer

**Note 1:** Alternate assignment for ECCP2 when Configuration bit, CCP2MX, is cleared (all operating modes except Microcontroller mode).

**2:** Default assignment for ECCP2 in all operating modes (CCP2MX is set).

**3:** Alternate assignment for ECCP2 when CCP2MX is cleared (Microcontroller mode only).

**4:** Default assignment for P1B/P1C/P3B/P3C (ECCPMX is set).

**5:** Alternate assignment for P1B/P1C/P3B/P3C (ECCPMX is clear).


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**TABLE 1-3: PIC18F8628/8723 (80-PIN) PINOUT I/O DESCRIPTIONS (CONTINUED)**

| Pin Name | Pin Number | Pin Type | Buffer Type | Description |
|---|---|---|---|---|
| | TQFP | | | |
| | | | | PORTF is a bidirectional I/O port. |
| RF0/AN5 | 24 | | | |
| RF0 | | I/O | ST | Digital I/O. |
| AN5 | | I | Analog | Analog input 5. |
| RF1/AN6/C2OUT | 23 | | | |
| RF1 | | I/O | ST | Digital I/O. |
| AN6 | | I | Analog | Analog input 6. |
| C2OUT | | O | — | Comparator 2 output. |
| RF2/AN7/C1OUT | 18 | | | |
| RF2 | | I/O | ST | Digital I/O. |
| AN7 | | I | Analog | Analog input 7. |
| C1OUT | | O | — | Comparator 1 output. |
| RF3/AN8 | 17 | | | |
| RF3 | | I/O | ST | Digital I/O. |
| AN8 | | I | Analog | Analog input 8. |
| RF4/AN9 | 16 | | | |
| RF4 | | I/O | ST | Digital I/O. |
| AN9 | | I | Analog | Analog input 9. |
| RF5/AN10/CVREF | 15 | | | |
| RF5 | | I/O | ST | Digital I/O. |
| AN10 | | I | Analog | Analog input 10. |
| CVREF | | O | Analog | Comparator reference voltage output. |
| RF6/AN11 | 14 | | | |
| RF6 | | I/O | ST | Digital I/O. |
| AN11 | | I | Analog | Analog input 11. |
| RF7/$\overline{SS1}$ | 13 | | | |
| RF7 | | I/O | ST | Digital I/O. |
| $\overline{SS1}$ | | I | TTL | SPI slave select input. |

**Legend:** TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; Analog = Analog input; I = Input; O = Output; P = Power; $I^2C$™/SMB = $I^2C$/SMBus input buffer

**Note 1:** Alternate assignment for ECCP2 when Configuration bit, CCP2MX, is cleared (all operating modes except Microcontroller mode).

**2:** Default assignment for ECCP2 in all operating modes (CCP2MX is set).

**3:** Alternate assignment for ECCP2 when CCP2MX is cleared (Microcontroller mode only).

**4:** Default assignment for P1B/P1C/P3B/P3C (ECCPMX is set).

**5:** Alternate assignment for P1B/P1C/P3B/P3C (ECCPMX is clear).

**TABLE 1-3: PIC18F8628/8723 (80-PIN) PINOUT I/O DESCRIPTIONS (CONTINUED)**

| Pin Name | Pin Number | Pin Type | Buffer Type | Description |
|---|---|---|---|---|
| | TQFP | | | |
| | | | | PORTG is a bidirectional I/O port. |
| RG0/ECCP3/P3A | 5 | | | |
| RG0 | | I/O | ST | Digital I/O. |
| ECCP3 | | I/O | ST | Enhanced Capture 3 input/Compare 3 output/ PWM3 output. |
| P3A | | O | — | ECCP3 PWM output A. |
| RG1/TX2/CK2 | 6 | | | |
| RG1 | | I/O | ST | Digital I/O. |
| TX2 | | O | — | EUSART2 asynchronous transmit. |
| CK2 | | I/O | ST | EUSART2 synchronous clock (see related RX2/DT2). |
| RG2/RX2/DT2 | 7 | | | |
| RG2 | | I/O | ST | Digital I/O. |
| RX2 | | I | ST | EUSART2 asynchronous receive. |
| DT2 | | I/O | ST | EUSART2 synchronous data (see related TX2/CK2). |
| RG3/CCP4/P3D | 8 | | | |
| RG3 | | I/O | ST | Digital I/O. |
| CCP4 | | I/O | ST | Capture 4 input/Compare 4 output/PWM4 output. |
| P3D | | O | — | ECCP3 PWM output D. |
| RG4/CCP5/P1D | 10 | | | |
| RG4 | | I/O | ST | Digital I/O. |
| CCP5 | | I/O | ST | Capture 5 input/Compare 5 output/PWM5 output. |
| P1D | | O | — | ECCP1 PWM output D. |
| RG5 | | | | See RG5/$\overline{\text{MCLR}}$/$V_{PP}$ pin. |

**Legend:** TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; Analog = Analog input; I = Input; O = Output; P = Power; $I^2C$™/SMB = $I^2C$/SMBus input buffer

**Note 1:** Alternate assignment for ECCP2 when Configuration bit, CCP2MX, is cleared (all operating modes except Microcontroller mode).

**2:** Default assignment for ECCP2 in all operating modes (CCP2MX is set).

**3:** Alternate assignment for ECCP2 when CCP2MX is cleared (Microcontroller mode only).

**4:** Default assignment for P1B/P1C/P3B/P3C (ECCPMX is set).

**5:** Alternate assignment for P1B/P1C/P3B/P3C (ECCPMX is clear).


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**TABLE 1-3: PIC18F8628/8723 (80-PIN) PINOUT I/O DESCRIPTIONS (CONTINUED)**

| Pin Name | Pin Number | Pin Type | Buffer Type | Description |
|---|---|---|---|---|
| | TQFP | | | |
| | | | | PORTH is a bidirectional I/O port. |
| RH0/A16 | 79 | | | |
| RH0 | | I/O | ST | Digital I/O. |
| A16 | | I/O | TTL | External memory address/data 16. |
| RH1/A17 | 80 | | | |
| RH1 | | I/O | ST | Digital I/O. |
| A17 | | I/O | TTL | External memory address/data 17. |
| RH2/A18 | 1 | | | |
| RH2 | | I/O | ST | Digital I/O. |
| A18 | | I/O | TTL | External memory address/data 18. |
| RH3/A19 | 2 | | | |
| RH3 | | I/O | ST | Digital I/O. |
| A19 | | I/O | TTL | External memory address/data 19. |
| RH4/AN12/P3C | 22 | | | |
| RH4 | | I/O | ST | Digital I/O. |
| AN12 | | I | Analog | Analog input 12. |
| P3C(5) | | O | — | ECCP3 PWM output C. |
| RH5/AN13/P3B | 21 | | | |
| RH5 | | I/O | ST | Digital I/O. |
| AN13 | | I | Analog | Analog input 13. |
| P3B(5) | | O | — | ECCP3 PWM output B. |
| RH6/AN14/P1C | 20 | | | |
| RH6 | | I/O | ST | Digital I/O. |
| AN14 | | I | Analog | Analog input 14. |
| P1C(5) | | O | — | ECCP1 PWM output C. |
| RH7/AN15/P1B | 19 | | | |
| RH7 | | I/O | ST | Digital I/O. |
| AN15 | | I | Analog | Analog input 15. |
| P1B(5) | | O | — | ECCP1 PWM output B. |

**Legend:** TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; Analog = Analog input; I = Input; O = Output; P = Power; $I^2C$™/SMB = $I^2C$/SMBus input buffer

**Note 1:** Alternate assignment for ECCP2 when Configuration bit, CCP2MX, is cleared (all operating modes except Microcontroller mode).

**2:** Default assignment for ECCP2 in all operating modes (CCP2MX is set).

**3:** Alternate assignment for ECCP2 when CCP2MX is cleared (Microcontroller mode only).

**4:** Default assignment for P1B/P1C/P3B/P3C (ECCPMX is set).

**5:** Alternate assignment for P1B/P1C/P3B/P3C (ECCPMX is clear).

**TABLE 1-3: PIC18F8628/8723 (80-PIN) PINOUT I/O DESCRIPTIONS (CONTINUED)**

| Pin Name | Pin Number | Pin Type | Buffer Type | Description |
|---|---|---|---|---|
| | TQFP | | | |
| | | | | PORTJ is a bidirectional I/O port. |
| RJ0/ALE | 62 | | | |
| RJ0 | | I/O | ST | Digital I/O. |
| ALE | | O | — | External memory address latch enable. |
| RJ1/$\overline{OE}$ | 61 | | | |
| RJ1 | | I/O | ST | Digital I/O. |
| $\overline{OE}$ | | O | — | External memory output enable. |
| RJ2/$\overline{WRL}$ | 60 | | | |
| RJ2 | | I/O | ST | Digital I/O. |
| $\overline{WRL}$ | | O | — | External memory write low control. |
| RJ3/$\overline{WRH}$ | 59 | | | |
| RJ3 | | I/O | ST | Digital I/O. |
| $\overline{WRH}$ | | O | — | External memory write high control. |
| RJ4/BA0 | 39 | | | |
| RJ4 | | I/O | ST | Digital I/O. |
| BA0 | | O | — | External memory byte address 0 control. |
| RJ5/$\overline{CE}$ | 40 | | | |
| RJ4 | | I/O | ST | Digital I/O |
| $\overline{CE}$ | | O | — | External memory chip enable control. |
| RJ6/$\overline{LB}$ | 41 | | | |
| RJ6 | | I/O | ST | Digital I/O. |
| $\overline{LB}$ | | O | — | External memory low byte control. |
| RJ7/$\overline{UB}$ | 42 | | | |
| RJ7 | | I/O | ST | Digital I/O. |
| $\overline{UB}$ | | O | — | External memory high byte control. |
| VSS | 11, 31, 51, 70 | P | — | Ground reference for logic and I/O pins. |
| VDD | 12, 32, 48, 71 | P | — | Positive supply for logic and I/O pins. |
| AVSS | 26 | P | — | Ground reference for analog modules. |
| AVDD | 25 | P | — | Positive supply for analog modules. |

**Legend:** TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; Analog = Analog input; I = Input; O = Output; P = Power; $I^2C$™/SMB = $I^2C$/SMBus input buffer

**Note 1:** Alternate assignment for ECCP2 when Configuration bit, CCP2MX, is cleared (all operating modes except Microcontroller mode).

**2:** Default assignment for ECCP2 in all operating modes (CCP2MX is set).

**3:** Alternate assignment for ECCP2 when CCP2MX is cleared (Microcontroller mode only).

**4:** Default assignment for P1B/P1C/P3B/P3C (ECCPMX is set).

**5:** Alternate assignment for P1B/P1C/P3B/P3C (ECCPMX is clear).


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## 2.0 12-BIT ANALOG-TO-DIGITAL CONVERTER (A/D) MODULE

The Analog-to-Digital (A/D) Converter module has 12 inputs for the 64-pin devices (PIC18F6628/6723) and 16 for the 80-pin devices (PIC18F8628/8723). This module allows conversion of an analog input signal to a corresponding 12-bit digital number.

The module has five registers:

- A/D Result High Register (ADRESH)
- A/D Result Low Register (ADRESL)
- A/D Control Register 0 (ADCON0)
- A/D Control Register 1 (ADCON1)
- A/D Control Register 2 (ADCON2)

The ADCON0 register, shown in Register 2-1, controls the operation of the A/D module. The ADCON1 register, shown in Register 2-2, configures the functions of the port pins. The ADCON2 register, shown in Register 2-3, configures the A/D clock source, programmed acquisition time and justification.

**REGISTER 2-1: ADCON0: A/D CONTROL REGISTER 0**

| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | CHS3 | CHS2 | CHS1 | CHS0 | GO/$\overline{\text{DONE}}$ | ADON |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 7-6 **Unimplemented:** Read as '0'

bit 5-2 **CHS3:CHS0:** Analog Channel Select bits
0000 = Channel 0 (AN0)
0001 = Channel 1 (AN1)
0010 = Channel 2 (AN2)
0011 = Channel 3 (AN3)
0100 = Channel 4 (AN4)
0101 = Channel 5 (AN5)
0110 = Channel 6 (AN6)
0111 = Channel 7 (AN7)
1000 = Channel 8 (AN8)
1001 = Channel 9 (AN9)
1010 = Channel 10 (AN10)
1011 = Channel 11 (AN11)
1100 = Channel 12 (AN12)**(1,2)**
1101 = Channel 13 (AN13)**(1,2)**
1110 = Channel 14 (AN14)**(1,2)**
1111 = Channel 15 (AN15)**(1,2)**

bit 1 **GO/$\overline{\text{DONE}}$:** A/D Conversion Status bit
When ADON = 1:
1 = A/D conversion in progress
0 = A/D Idle

bit 0 **ADON:** A/D On bit
1 = A/D Converter module is enabled
0 = A/D Converter module is disabled

**Note 1:** These channels are not implemented on PIC18F6628/6723 devices.
**2:** Performing a conversion on unimplemented channels will return a floating input measurement.

**REGISTER 2-2: ADCON1: A/D CONTROL REGISTER 1**

| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | VCFG1 | VCFG0 | PCFG3 | PCFG2 | PCFG1 | PCFG0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 7-6 **Unimplemented:** Read as '0'

bit 5-4 **VCFG1:VCFG0:** Voltage Reference Configuration bits

| | **A/D VREF+** | **A/D VREF-** |
|---|---|---|
| 00 | AVDD | AVSS |
| 01 | External VREF+ | AVSS |
| 10 | AVDD | External VREF- |
| 11 | External VREF+ | External VREF- |

bit 3-0 **PCFG3:PCFG0:** A/D Port Configuration Control bits:

| **PCFG<3:0>** | **AN15(1)** | **AN14(1)** | **AN13(1)** | **AN12(1)** | **AN11** | **AN10** | **AN9** | **AN8** | **AN7** | **AN6** | **AN5** | **AN4** | **AN3** | **AN2** | **AN1** | **AN0** |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0000 | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| 0001 | D | D | A | A | A | A | A | A | A | A | A | A | A | A | A | A |
| 0010 | D | D | D | A | A | A | A | A | A | A | A | A | A | A | A | A |
| 0011 | D | D | D | D | A | A | A | A | A | A | A | A | A | A | A | A |
| 0100 | D | D | D | D | D | A | A | A | A | A | A | A | A | A | A | A |
| 0101 | D | D | D | D | D | D | A | A | A | A | A | A | A | A | A | A |
| 0110 | D | D | D | D | D | D | D | A | A | A | A | A | A | A | A | A |
| 0111 | D | D | D | D | D | D | D | D | A | A | A | A | A | A | A | A |
| 1000 | D | D | D | D | D | D | D | D | D | A | A | A | A | A | A | A |
| 1001 | D | D | D | D | D | D | D | D | D | D | A | A | A | A | A | A |
| 1010 | D | D | D | D | D | D | D | D | D | D | D | A | A | A | A | A |
| 1011 | D | D | D | D | D | D | D | D | D | D | D | D | A | A | A | A |
| 1100 | D | D | D | D | D | D | D | D | D | D | D | D | D | A | A | A |
| 1101 | D | D | D | D | D | D | D | D | D | D | D | D | D | D | A | A |
| 1110 | D | D | D | D | D | D | D | D | D | D | D | D | D | D | D | A |
| 1111 | D | D | D | D | D | D | D | D | D | D | D | D | D | D | D | D |

A = Analog input D = Digital I/O

**Note 1:** AN15 through AN12 are available only on PIC18F8628/8723 devices.


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**REGISTER 2-3: ADCON2: A/D CONTROL REGISTER 2**

| R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| ADFM | — | ACQT2 | ACQT1 | ACQT0 | ADCS2 | ADCS1 | ADCS0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 7 **ADFM:** A/D Result Format Select bit
1 = Right justified
0 = Left justified

bit 6 **Unimplemented:** Read as '0'

bit 5-3 **ACQT2:ACQT0:** A/D Acquisition Time Select bits
111 = 20 TAD
110 = 16 TAD
101 = 12 TAD
100 = 8 TAD
011 = 6 TAD
010 = 4 TAD
001 = 2 TAD
000 = 0 TAD(1)

bit 2-0 **ADCS2:ADCS0:** A/D Conversion Clock Select bits
111 = FRC (clock derived from A/D RC oscillator)(1)
110 = FOSC/64
101 = FOSC/16
100 = FOSC/4
011 = FRC (clock derived from A/D RC oscillator)(1)
010 = FOSC/32
001 = FOSC/8
000 = FOSC/2

**Note 1:** If the A/D FRC clock source is selected, a delay of one TCY (instruction cycle) is added before the A/D clock starts. This allows the SLEEP instruction to be executed before starting a conversion.

The analog reference voltage is software selectable to either the device's positive and negative supply voltage ($V_{DD}$ and $V_{SS}$), or the voltage level on the RA3/AN3/$V_{REF+}$ and RA2/AN2/$V_{REF-}$/$CV_{REF}$ pins.

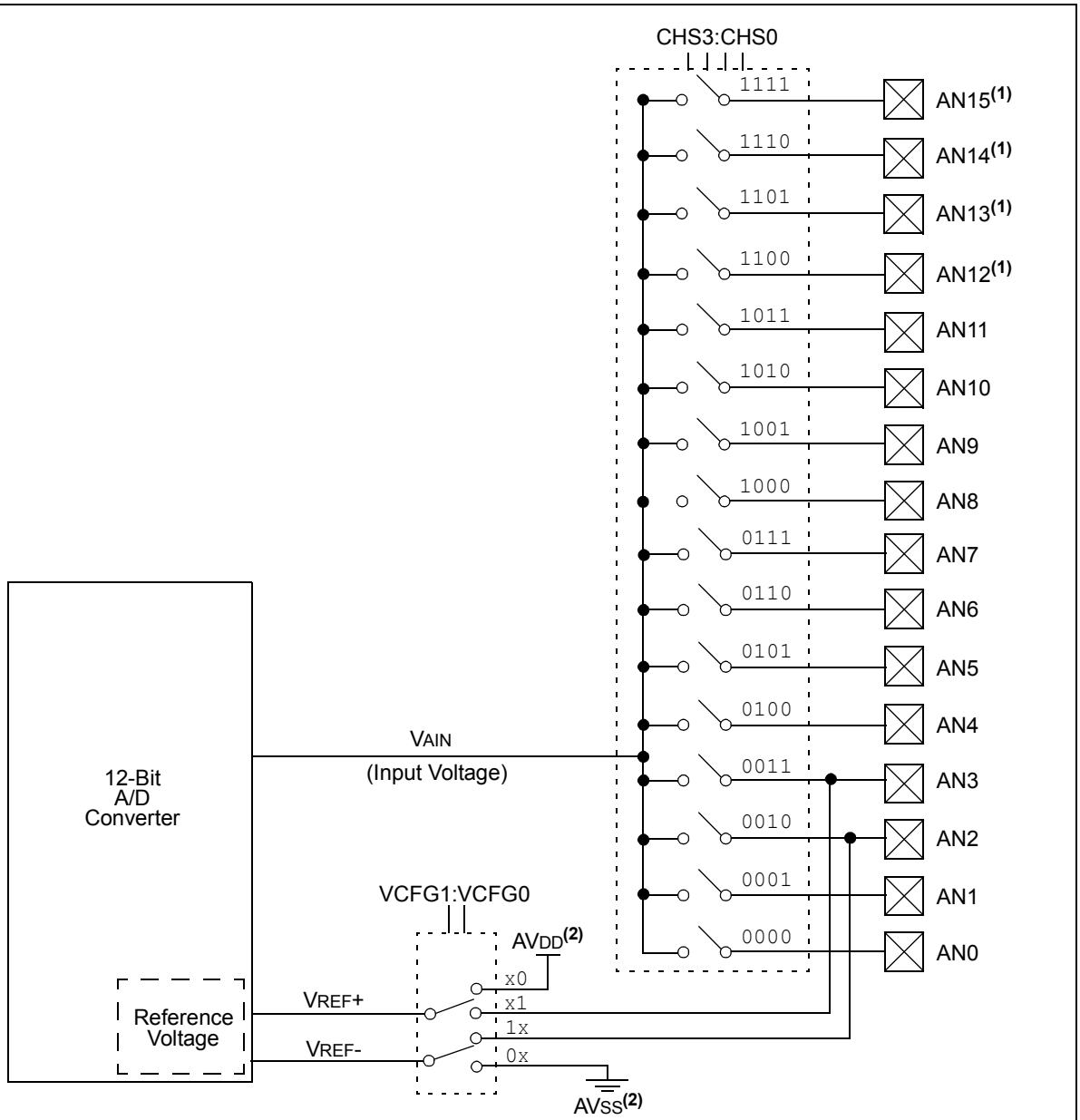
The A/D Converter has a unique feature of being able to operate while the device is in Sleep mode. To operate in Sleep, the A/D conversion clock must be derived from the A/D's internal RC oscillator.

The output of the sample and hold is the input into the converter, which generates the result via successive approximation.

A device Reset forces all registers to their Reset state. This forces the A/D module to be turned off and any conversion in progress is aborted.

Each port pin associated with the A/D Converter can be configured as an analog input or a digital I/O. The ADRESH and ADRESL registers contain the result of the A/D conversion. When the A/D conversion is complete, the result is loaded into the ADRESH:ADRESL register pair, the GO/$\overline{DONE}$ bit (ADCON0<1>) is cleared and the A/D Interrupt Flag bit, ADIF, is set. The block diagram of the A/D module is shown in Figure 2-1.

**FIGURE 2-1: A/D BLOCK DIAGRAM**




**Note 1:** Channels AN12 through AN15 are not available on PIC18F6628/6723 devices.

**2:** I/O pins have diode protection to $V_{DD}$ and $V_{SS}$.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The value in the ADRESH:ADRESL registers is unknown following Power-on and Brown-out Resets and is not affected by any other Reset.

After the A/D module has been configured as desired, the selected channel must be acquired before the conversion is started. The analog input channels must have their corresponding TRIS bits selected as an input. To determine acquisition time, see **Section 2.1 "A/D Acquisition Requirements"**. After this acquisition time has elapsed, the A/D conversion can be started. An acquisition time can be programmed to occur between setting the GO/$\overline{\text{DONE}}$ bit and the actual start of the conversion.

The following steps should be followed to perform an A/D conversion:

1. Configure the A/D module:
   - Configure analog pins, voltage reference and digital I/O (ADCON1)
   - Select A/D input channel (ADCON0)
   - Select A/D acquisition time (ADCON2)
   - Select A/D conversion clock (ADCON2)
   - Turn on A/D module (ADCON0)
2. Configure A/D interrupt (if desired):
   - Clear ADIF bit
   - Set ADIE bit
   - Set GIE bit
3. Wait the required acquisition time (if required).
4. Start conversion:
   - Set GO/$\overline{\text{DONE}}$ bit (ADCON0<1>)
5. Wait for A/D conversion to complete by either:
   - Polling for the GO/$\overline{\text{DONE}}$ bit to be cleared

   OR
   - Waiting for the A/D interrupt
6. Read A/D Result registers (ADRESH:ADRESL); clear bit, ADIF, if required.
7. For next conversion, go to step 1 or step 2, as required. The A/D conversion time per bit is defined as TAD. A minimum wait of 2 TAD is required before the next acquisition starts.

**FIGURE 2-2: A/D TRANSFER FUNCTION**

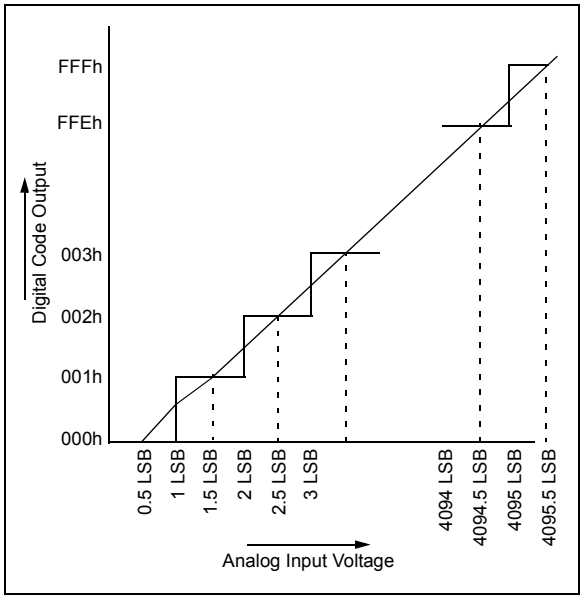
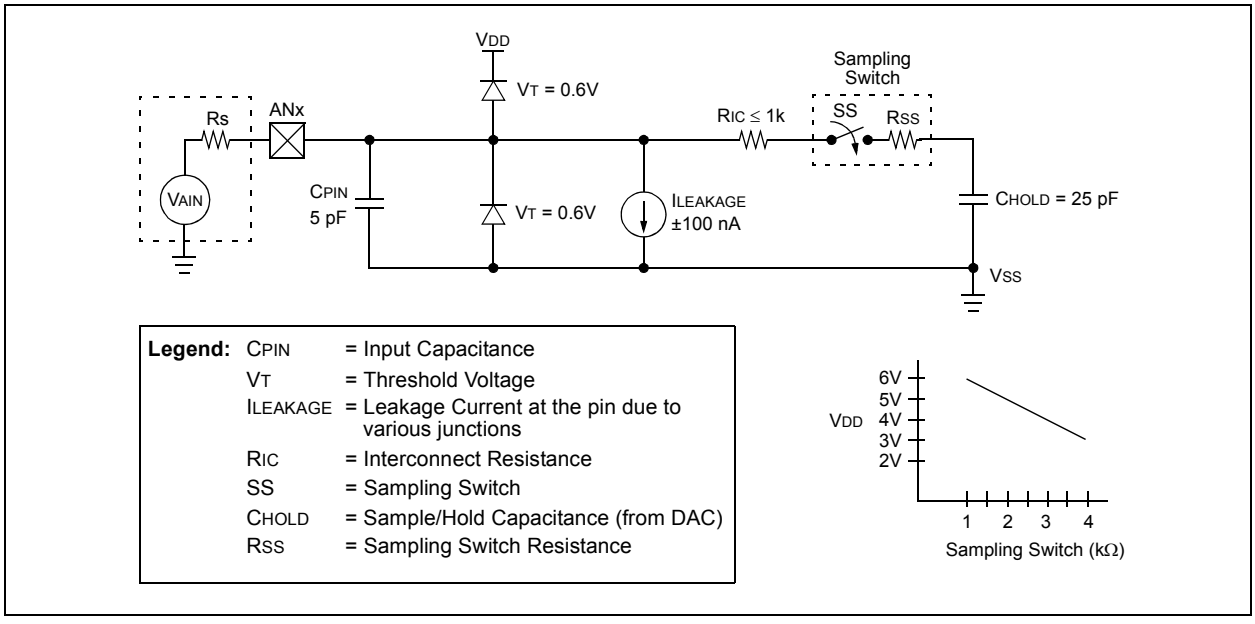



**FIGURE 2-3: ANALOG INPUT MODEL**



## 2.1 A/D Acquisition Requirements

For the A/D Converter to meet its specified accuracy, the charge holding capacitor (CHOLD) must be allowed to fully charge to the input channel voltage level. The analog input model is shown in Figure 2-3. The source impedance (RS) and the internal sampling switch (RSS) impedance directly affect the time required to charge the capacitor, CHOLD. The sampling switch (RSS) impedance varies over the device voltage (VDD). The source impedance affects the offset voltage at the analog input (due to pin leakage current). **The maximum recommended impedance for analog sources is 2.5 kΩ**. After the analog input channel is selected (changed), the channel must be sampled for at least the minimum acquisition time before starting a conversion.

| **Note:** | When the conversion is started, the holding capacitor is disconnected from the input pin. |
|---|---|

To calculate the minimum acquisition time, Equation 2-1 may be used. This equation assumes that 1/2 LSb error is used (4096 steps for the 12-bit A/D). The 1/2 LSb error is the maximum error allowed for the A/D to meet its specified resolution.

Example 2-3 shows the calculation of the minimum required acquisition time, TACQ. This calculation is based on the following application system assumptions:

| | | |
|---|---|---|
| CHOLD | = | 25 pF |
| Rs | = | 2.5 kΩ |
| Conversion Error | ≤ | 1/2 LSb |
| VDD | = | 3V → Rss = 4 kΩ |
| Temperature | = | 85°C (system max.) |

**EQUATION 2-1: ACQUISITION TIME**

$$T_{ACQ} = \text{Amplifier Settling Time} + \text{Holding Capacitor Charging Time} + \text{Temperature Coefficient}$$
$$= T_{AMP} + T_C + T_{COFF}$$

**EQUATION 2-2: A/D MINIMUM CHARGING TIME**

$$V_{HOLD} = (V_{REF} - (V_{REF}/4096)) \cdot (1 - e^{(-T_C/C_{HOLD}(R_{IC} + R_{SS} + R_S))})$$
or
$$T_C = -(C_{HOLD})(R_{IC} + R_{SS} + R_S) \ln(1/4096)$$

**EQUATION 2-3: CALCULATING THE MINIMUM REQUIRED ACQUISITION TIME**

$$T_{ACQ} = T_{AMP} + T_C + T_{COFF}$$
$$T_{AMP} = 0.2\ \mu s$$
$$T_{COFF} = (\text{Temp} - 25°C)(0.02\ \mu s/°C)$$
$$(85°C - 25°C)(0.02\ \mu s/°C)$$
$$1.2\ \mu s$$

Temperature coefficient is only required for temperatures > 25°C. Below 25°C, $T_{COFF} = 0\ \mu s$.

$$T_C = -(C_{HOLD})(R_{IC} + R_{SS} + R_S) \ln(1/4096)\ \mu s$$
$$-(25\ pF)\ (1\ k\Omega + 4\ k\Omega + 2.5\ k\Omega) \ln(0.0002441)\ \mu s$$
$$1.56\ \mu s$$

$$T_{ACQ} = 0.2\ \mu s + 1.56\ \mu s + 1.2\ \mu s$$
$$2.96\ \mu s$$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## 2.2 Selecting and Configuring Acquisition Time

The ADCON2 register allows the user to select an acquisition time that occurs each time the GO/DONE bit is set. It also gives users the option to use an automatically determined acquisition time.

Acquisition time may be set with the ACQT2:ACQT0 bits (ADCON2<5:3>), which provide a range of 2 to 20 TAD. When the GO/DONE bit is set, the A/D module continues to sample the input for the selected acquisition time, then automatically begins a conversion. Since the acquisition time is programmed, there may be no need to wait for an acquisition time between selecting a channel and setting the GO/DONE bit.

Manual acquisition is selected when ACQT2:ACQT0 = 000. When the GO/DONE bit is set, sampling is stopped and a conversion begins. The user is responsible for ensuring the required acquisition time has passed between selecting the desired input channel and setting the GO/DONE bit. This option is also the default Reset state of the ACQT2:ACQT0 bits and is compatible with devices that do not offer programmable acquisition times.

In either case, when the conversion is completed, the GO/DONE bit is cleared, the ADIF flag is set and the A/D begins sampling the currently selected channel again. If an acquisition time is programmed, there is nothing to indicate if the acquisition time has ended or if the conversion has begun.

## 2.3 Selecting the A/D Conversion Clock

The A/D conversion time per bit is defined as TAD. The A/D conversion requires 13 TAD per 12-bit conversion. The source of the A/D conversion clock is software selectable. There are seven possible options for TAD:

- 2 TOSC
- 4 TOSC
- 8 TOSC
- 16 TOSC
- 32 TOSC
- 64 TOSC
- Internal RC Oscillator

For correct A/D conversions, the A/D conversion clock (TAD) must be as short as possible, but greater than the minimum TAD (see parameter 130 for more information).

Table 2-1 shows the resultant TAD times derived from the device operating frequencies and the A/D clock source selected.

**TABLE 2-1: TAD vs. DEVICE OPERATING FREQUENCIES**

| A/D Clock Source (TAD) | | Assumes TAD Min. = 0.8 μs |
|---|---|---|
| **Operation** | **ADCS2:ADCS0** | **Maximum FOSC** |
| 2 TOSC | 000 | 2.50 MHz |
| 4 TOSC | 100 | 5.00 MHz |
| 8 TOSC | 001 | 10.00 MHz |
| 16 TOSC | 101 | 20.00 MHz |
| 32 TOSC | 010 | 40.00 MHz |
| 64 TOSC | 110 | 40.00 MHz |
| RC(1) | x11 | 1.00 MHz(2) |

**Note 1:** The RC source has a typical TAD time of 2.5 μs.

**2:** For device frequencies above 1 MHz, the device must be in Sleep for the entire conversion or a FOSC divider should be used instead; otherwise, the A/D accuracy specification may not be met.

## 2.4 Operation in Power-Managed Modes

The selection of the automatic acquisition time and A/D conversion clock is determined in part by the clock source and frequency while in a power-managed mode.

If the A/D is expected to operate while the device is in a power-managed mode, the ADCS2:ADCS0 bits in ADCON2 should be updated in accordance with the clock source to be used. The ACQT2:ACQT0 bits do not need to be adjusted as the ADCS2:ADCS0 bits adjust the TAD time for the new clock speed. After entering the mode, an A/D acquisition or conversion may be started. Once started, the device should continue to be clocked by the same clock source until the conversion has been completed.

If desired, the device may be placed into the corresponding Idle mode during the conversion. If the device clock frequency is less than 1 MHz, the A/D RC clock source should be selected.

Operation in Sleep mode requires the A/D FRC clock to be selected. If the ACQT2:ACQT0 bits are set to '000' and a conversion is started, the conversion will be delayed one instruction cycle to allow execution of the SLEEP instruction and entry to Sleep mode. The IDLEN bit (OSCCON<7>) must have already been cleared prior to starting the conversion.

## 2.5 Configuring Analog Port Pins

The ADCON1, TRISA, TRISF and TRISH registers all configure the A/D port pins. The port pins needed as analog inputs must have their corresponding TRIS bits set (input). If the TRIS bit is cleared (output), the digital output level (VOH or VOL) will be converted.

The A/D operation is independent of the state of the CHS3:CHS0 bits and the TRIS bits.

| | |
|---|---|
| **Note 1:** | When reading the PORT register, all pins configured as analog input channels will read as cleared (a low level). Analog conversion on pins configured as digital pins can be performed. The voltage on the pin will be accurately converted. |
| **2:** | Analog levels on any pin defined as a digital input may cause the digital input buffer to consume current out of the device's specification limits. |


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## 2.6 A/D Conversions

Figure 2-4 shows the operation of the A/D Converter after the GO/$\overline{\text{DONE}}$ bit has been set and the ACQT2:ACQT0 bits are cleared. A conversion is started after the following instruction to allow entry into Sleep mode before the conversion begins.

Figure 2-5 shows the operation of the A/D Converter after the GO/$\overline{\text{DONE}}$ bit has been set, the ACQT2:ACQT0 bits are set to '010' and a 4 TAD acquisition time has been selected before the conversion starts.

Clearing the GO/$\overline{\text{DONE}}$ bit during a conversion will abort the current conversion. The A/D Result register pair will NOT be updated with the partially completed A/D conversion sample. This means the ADRESH:ADRESL registers will continue to contain the value of the last completed conversion (or the last value written to the ADRESH:ADRESL registers).

After the A/D conversion is completed or aborted, a 2 TCY wait is required before the next acquisition can be started. After this wait, acquisition on the selected channel is automatically started.

**Note:** The GO/$\overline{\text{DONE}}$ bit should **NOT** be set in the same instruction that turns on the A/D. Code should wait at least 2 μs after enabling the A/D before beginning an acquisition and conversion cycle.

## 2.7 Discharge

The discharge phase is used to initialize the value of the holding capacitor. The array is discharged before every sample. This feature helps to optimize the unity gain amplifier, as the circuit always needs to charge the capacitor array, rather than charge/discharge based on previous measure values.

**FIGURE 2-4: A/D CONVERSION TAD CYCLES (ACQT<2:0> = 000, TACQ = 0)**

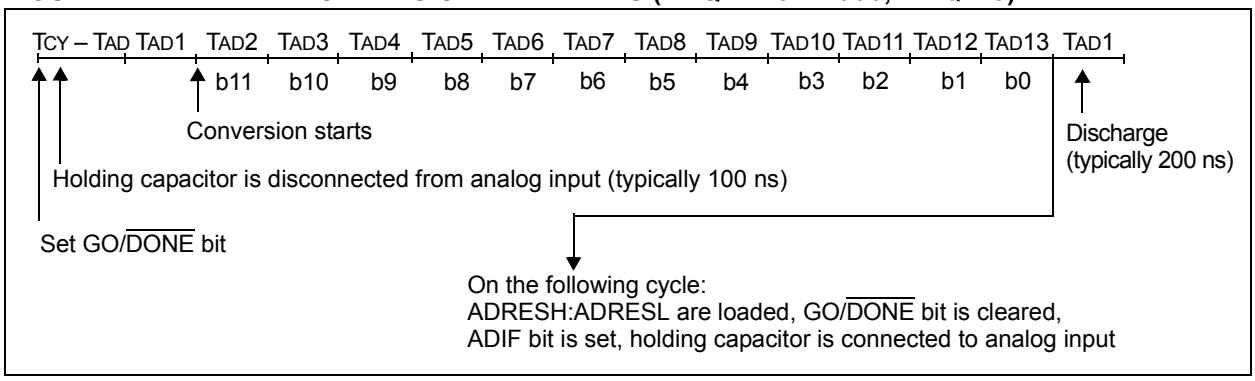
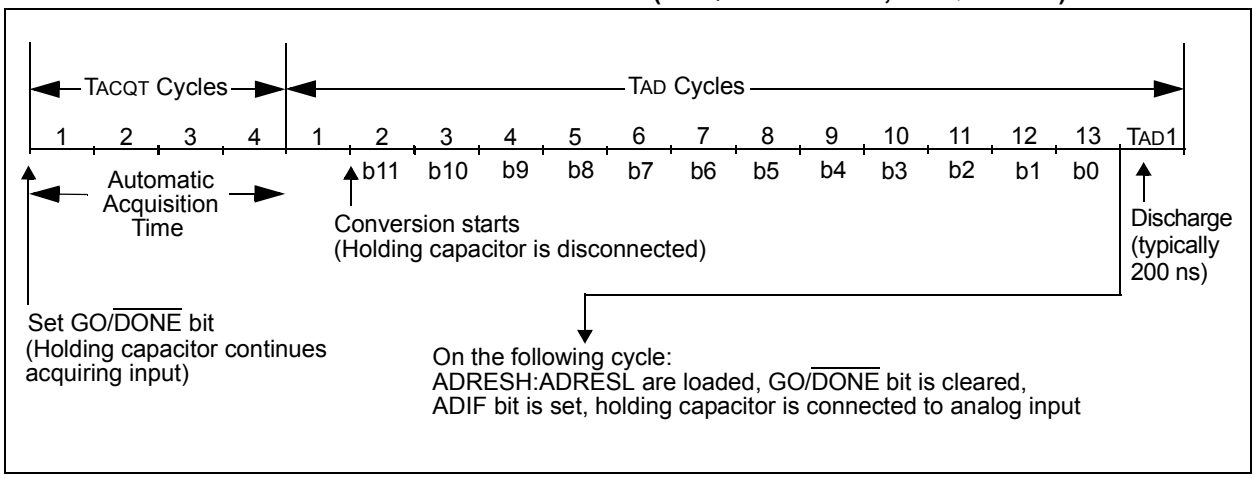



**FIGURE 2-5: A/D CONVERSION TAD CYCLES (ACQT<2:0> = 010, TACQ = 4 TAD)**



## 2.8 Use of the ECCP2 Trigger

An A/D conversion can be started by the Special Event Trigger of the ECCP2 module. This requires that the CCP2M3:CCP2M0 bits (CCP2CON<3:0>) be programmed as '1011' and that the A/D module is enabled (ADON bit is set). When the trigger occurs, the GO/$\overline{\text{DONE}}$ bit will be set, starting the A/D acquisition and conversion, and the Timer1 (or Timer3) counter will be reset to zero. Timer1 (or Timer3) is reset to automatically repeat the A/D acquisition period with minimal software overhead (moving ADRESH:ADRESL to the desired location). The appropriate analog input channel must be selected and the minimum acquisition period is either timed by the user, or an appropriate TACQ time selected before the Special Event Trigger sets the GO/$\overline{\text{DONE}}$ bit (starts a conversion).

If the A/D module is not enabled (ADON is cleared), the Special Event Trigger will be ignored by the A/D module but will still reset the Timer1 (or Timer3) counter.

**TABLE 2-2: REGISTERS ASSOCIATED WITH A/D OPERATION**

| Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Reset Values |
|---|---|---|---|---|---|---|---|---|---|
| INTCON | GIE/GIEH | PEIE/GIEL | TMR0IE | INT0IE | RBIE | TMR0IF | INT0IF | RBIF | (3) |
| PIR1 | PSPIF | ADIF | RC1IF | TX1IF | SSP1IF | CCP1IF | TMR2IF | TMR1IF | (3) |
| PIE1 | PSPIE | ADIE | RC1IE | TX1IE | SSP1IE | CCP1IE | TMR2IE | TMR1IE | (3) |
| IPR1 | PSPIP | ADIP | RC1IP | TX1IP | SSP1IP | CCP1IP | TMR2IP | TMR1IP | (3) |
| PIR2 | OSCFIF | CMIF | — | EEIF | BCL1IF | HLVDIF | TMR3IF | CCP2IF | (3) |
| PIE2 | OSCFIE | CMIE | — | EEIE | BCL1IE | HLVDIE | TMR3IE | CCP2IE | (3) |
| IPR2 | OSCFIP | CMIP | — | EEIP | BCL1IP | HLVDIP | TMR3IP | CCP2IP | (3) |
| ADRESH | A/D Result Register High Byte | | | | | | | | (3) |
| ADRESL | A/D Result Register Low Byte | | | | | | | | (3) |
| ADCON0 | — | — | CHS3 | CHS2 | CHS1 | CHS0 | GO/$\overline{\text{DONE}}$ | ADON | (3) |
| ADCON1 | — | — | VCFG1 | VCFG0 | PCFG3 | PCFG2 | PCFG1 | PCFG0 | (3) |
| ADCON2 | ADFM | — | ACQT2 | ACQT1 | ACQT0 | ADCS2 | ADCS1 | ADCS0 | (3) |
| TRISA | TRISA7(1) | TRISA6(1) | TRISA5 | TRISA4 | TRISA3 | TRISA2 | TRISA1 | TRISA0 | (3) |
| TRISF | TRISF7 | TRISF6 | TRISF5 | TRISF4 | TRISF3 | TRISF2 | TRISF1 | TRISF0 | (3) |
| TRISH(2) | TRISH7 | TRISH6 | TRISH5 | TRISH4 | TRISH3 | TRISH2 | TRISH1 | TRISH0 | (3) |

**Legend:** — = unimplemented, read as '0'. Shaded cells are not used for A/D conversion.

**Note 1:** PORTA<7:6> and their direction bits are individually configured as port pins based on various primary oscillator modes. When disabled, these bits read as '0'.

**2:** These registers are not implemented on PIC18F6628/6723 devices.

**3:** For these Reset values, see the *"PIC18F8722 Family Data Sheet"* (DS39646).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## 3.0 SPECIAL FEATURES OF THE CPU

**Note:** For additional details on the Configuration bits, refer to **Section 25.1 "Configuration Bits" in** the *"PIC18F8722 Family Data Sheet"* (DS39646). Device ID information presented in this section is for the PIC18F8723 family only.

PIC18F8723 family devices include several features intended to maximize reliability and minimize cost through elimination of external components. These include:

- Device ID Registers

### 3.1 Device ID Registers

The Device ID registers are "read-only" registers. They identify the device type and revision to device programmers and can be read by firmware using table reads.

**TABLE 3-1: DEVICE IDs**

| File Name | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default/ Unprogrammed Value |
|---|---|---|---|---|---|---|---|---|---|---|
| 3FFFFEh | DEVID1 | DEV2 | DEV1 | DEV0 | REV4 | REV3 | REV2 | REV1 | REV0 | xxxx xxxx(1) |
| 3FFFFFh | DEVID2 | DEV10 | DEV9 | DEV8 | DEV7 | DEV6 | DEV5 | DEV4 | DEV3 | xxxx xxxx(1) |

**Legend:** x = unknown

**Note 1:** See Register 3-1 and Register 3-2 for DEVID values. DEVID registers are read-only and cannot be programmed by the user.

**REGISTER 3-1: DEVID1: DEVICE ID REGISTER 1 FOR PIC18F8723 FAMILY DEVICES**

| R | R | R | R | R | R | R | R |
|---|---|---|---|---|---|---|---|
| DEV2 | DEV1 | DEV0 | REV4 | REV3 | REV2 | REV1 | REV0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | |
|---|---|---|
| R = Read-only bit | P = Programmable bit | U = Unimplemented bit, read as '0' |
| -n = Value when device is unprogrammed | | u = Unchanged from programmed state |

bit 7-5 **DEV2:DEV0:** Device ID bits
See Register 3-2 for a complete listing.

bit 4-0 **REV4:REV0:** Revision ID bits
These bits are used to indicate the device revision.

**REGISTER 3-2: DEVID2: DEVICE ID REGISTER 2 FOR PIC18F8723 FAMILY DEVICES**

| R | R | R | R | R | R | R | R |
|---|---|---|---|---|---|---|---|
| DEV10 | DEV9 | DEV8 | DEV7 | DEV6 | DEV5 | DEV4 | DEV3 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | |
|---|---|---|
| R = Read-only bit | P = Programmable bit | U = Unimplemented bit, read as '0' |
| -n = Value when device is unprogrammed | | u = Unchanged from programmed state |

bit 7-0 **DEV10:DEV3:** Device ID bits

| DEV10:DEV3 (DEVID2<7:0>) | DEV2:DEV0 (DEVID1<7:5>) | Device |
|---|---|---|
| 0100 1001 | 110 | PIC18F6628 |
| 0100 1010 | 000 | PIC18F6723 |
| 0100 1001 | 111 | PIC18F8628 |
| 0100 1010 | 001 | PIC18F8723 |


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## 4.0 ELECTRICAL CHARACTERISTICS

**Note:** Other than some basic data, this section documents only the PIC18F8723 family's specifications that differ from those of the PIC18F8722 family devices. For detailed information on the electrical specifications shared by the PIC18F8723 family and PIC18F8722 family devices, see the *"PIC18F8722 Family Data Sheet"* (DS39646).

### Absolute Maximum Ratings(†)

Ambient temperature under bias ..... -40°C to +125°C

Storage temperature ..... -65°C to +150°C

Voltage on any pin with respect to $V_{SS}$ (except $V_{DD}$ and $\overline{MCLR}$) ..... -0.3V to ($V_{DD}$ + 0.3V)

Voltage on $V_{DD}$ with respect to $V_{SS}$ ..... -0.3V to +7.5V

Voltage on $\overline{MCLR}$ with respect to $V_{SS}$ **(Note 2)** ..... 0V to +13.25V

Total power dissipation **(Note 1)** ..... 1.0W

Maximum current out of $V_{SS}$ pin ..... 300 mA

Maximum current into $V_{DD}$ pin ..... 250 mA

Input clamp current, $I_{IK}$ ($V_I$ < 0 or $V_I$ > $V_{DD}$) ..... ±20 mA

Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{DD}$) ..... ±20 mA

Maximum output current sunk by any I/O pin ..... 25 mA

Maximum output current sourced by any I/O pin ..... 25 mA

Maximum current sunk by all ports ..... 200 mA

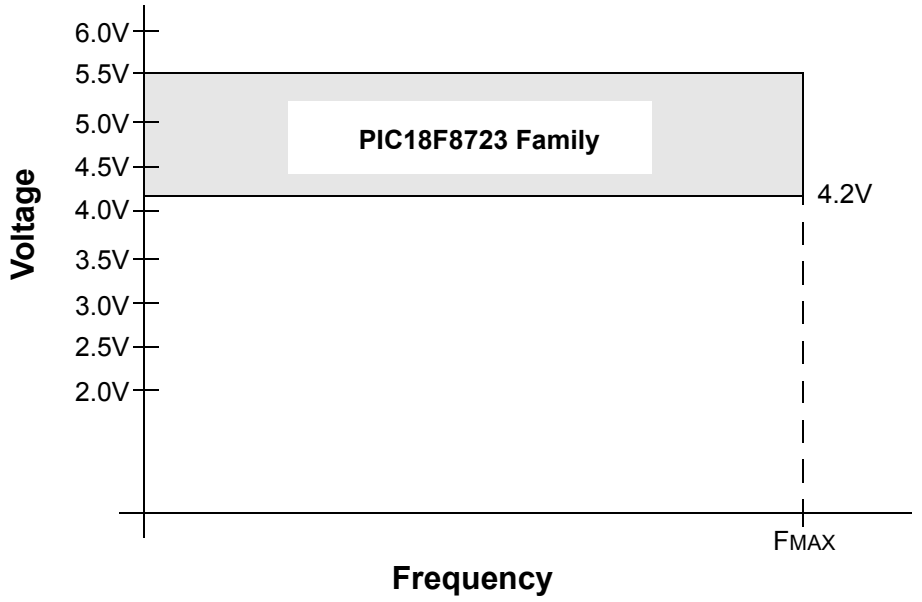
Maximum current sourced by all ports ..... 200 mA

**Note 1:** Power dissipation is calculated as follows:
$P_{dis} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD} - V_{OH}) \times I_{OH}\} + \sum(V_{OL} \times I_{OL})$

**2:** Voltage spikes below $V_{SS}$ at the RG5/$\overline{MCLR}$/$V_{PP}$ pin, inducing currents greater than 80 mA, may cause latch-up. Thus, a series resistor of 50-100Ω should be used when applying a "low" level to the RG5/$\overline{MCLR}$/$V_{PP}$ pin, rather than pulling this pin directly to $V_{SS}$.

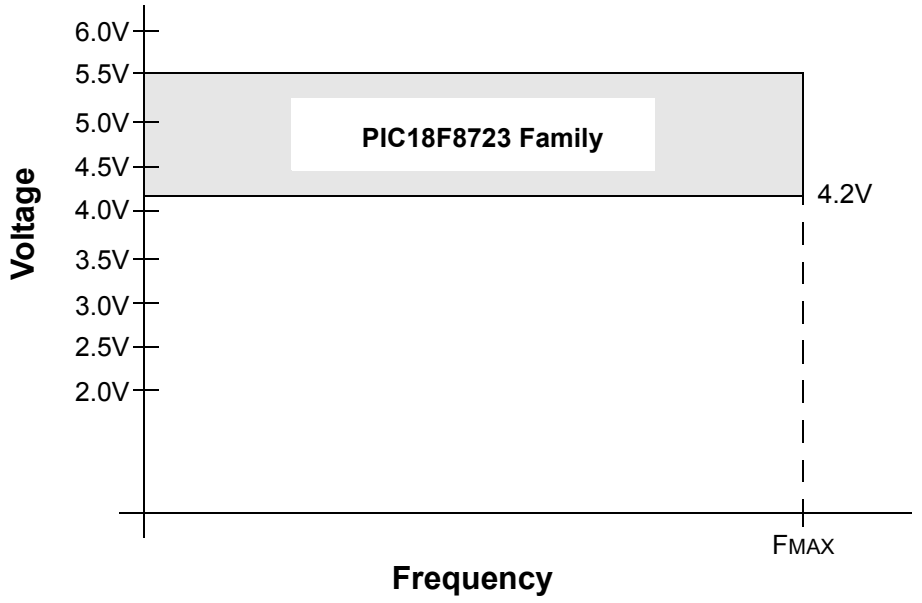
† **NOTICE:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

**FIGURE 4-1: PIC18F8723 FAMILY VOLTAGE-FREQUENCY GRAPH (INDUSTRIAL)**




FMAX = 20 MHz in 8-Bit External Memory mode.
FMAX = 40 MHz in all other modes.

**FIGURE 4-2: PIC18F8723 FAMILY VOLTAGE-FREQUENCY GRAPH (EXTENDED)**




FMAX = 20 MHz in 8-Bit External Memory mode.
FMAX = 25 MHz in all other modes.


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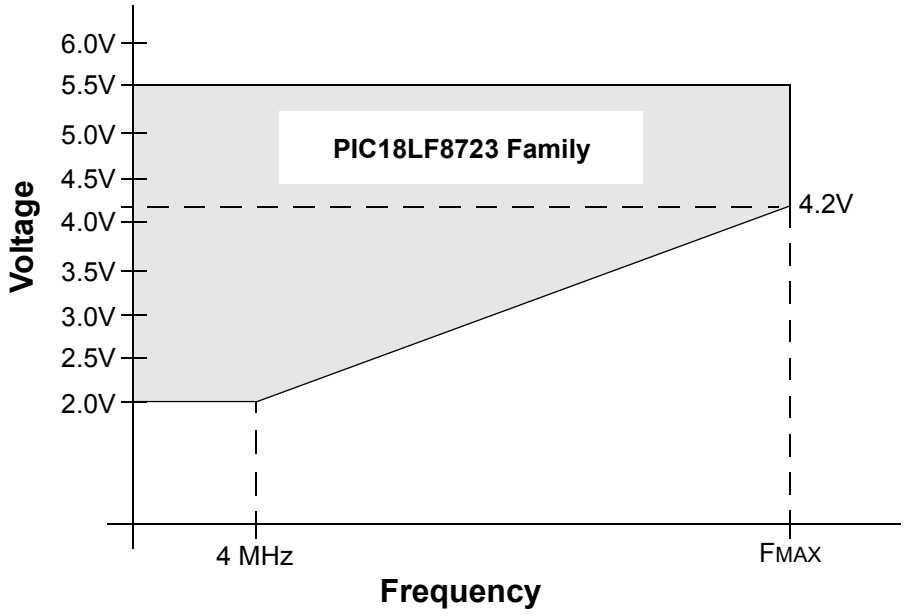
**FIGURE 4-3: PIC18LF8723 FAMILY VOLTAGE-FREQUENCY GRAPH (INDUSTRIAL)**




In 8-Bit External Memory mode:
$F_{MAX}$ = (9.55 MHz/V) ($V_{DDAPPMIN}$ – 2.0V) + 4 MHz, if $V_{DDAPPMIN} \leq$ 4.2V;
$F_{MAX}$ = 25 MHz, if $V_{DDAPPMIN}$ > 4.2V.

In all other modes:
$F_{MAX}$ = (16.36 MHz/V) ($V_{DDAPPMIN}$ – 2.0V) + 4 MHz;
$F_{MAX}$ = 40 MHz, if $V_{DDAPPMIN}$ > 4.2V.

**Note:** $V_{DDAPPMIN}$ is the minimum voltage of the PIC® device in the application.

**TABLE 4-1: A/D CONVERTER CHARACTERISTICS: PIC18F8723 FAMILY (INDUSTRIAL)**

| Param No. | Sym | Characteristic | Min | Typ | Max | Units | Conditions | |
|---|---|---|---|---|---|---|---|---|
| A01 | NR | Resolution | — | — | 12 | bit | | ΔVREF ≥ 3.0V |
| A03 | EIL | Integral Linearity Error | — | <±1 | ±2.0 | LSB | VDD = 3.0V | ΔVREF ≥ 3.0V |
| | | | — | — | ±2.0 | LSB | VDD = 5.0V | |
| A04 | EDL | Differential Linearity Error | — | <±1 | +1.5/-1.0 | LSB | VDD = 3.0V | ΔVREF ≥ 3.0V |
| | | | — | — | +1.5/-1.0 | LSB | VDD = 5.0V | |
| A06 | EOFF | Offset Error | — | <±1 | ±5 | LSB | VDD = 3.0V | ΔVREF ≥ 3.0V |
| | | | — | — | ±3 | LSB | VDD = 5.0V | |
| A07 | EGN | Gain Error | — | <±1 | ±1.25 | LSB | VDD = 3.0V | ΔVREF ≥ 3.0V |
| | | | — | — | ±2.00 | LSB | VDD = 5.0V | |
| A10 | — | Monotonicity | Guaranteed(1) | | | — | | VSS ≤ VAIN ≤ VREF |
| A20 | ΔVREF | Reference Voltage Range (VREFH – VREFL) | 3 | — | VDD – VSS | V | | For 12-bit resolution |
| A21 | VREFH | Reference Voltage High | VSS + 3.0V | — | VDD + 0.3V | V | | For 12-bit resolution |
| A22 | VREFL | Reference Voltage Low | VSS – 0.3V | — | VDD – 3.0V | V | | For 12-bit resolution |
| A25 | VAIN | Analog Input Voltage | VREFL | — | VREFH | V | | |
| A30 | ZAIN | Recommended Impedance of Analog Voltage Source | — | — | 2.5 | kΩ | | |
| A50 | IREF | VREF Input Current(2) | —<br>— | —<br>— | 5<br>150 | μA<br>μA | | During VAIN acquisition.<br>During A/D conversion cycle. |

**Note 1:** The A/D conversion result never decreases with an increase in the input voltage and has no missing codes.

**2:** VREFH current is from the RA3/AN3/VREF+ pin or VDD, whichever is selected as the VREFH source. VREFL current is from the RA2/AN2/VREF-/CVREF pin or VSS, whichever is selected as the VREFL source.


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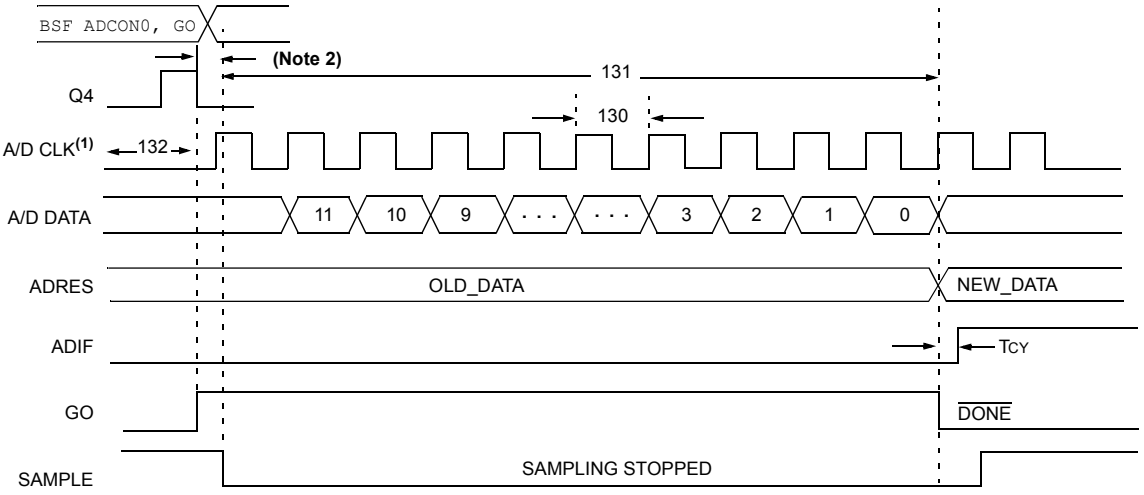
**FIGURE 4-4: A/D CONVERSION TIMING**




**Note 1:** If the A/D clock source is selected as RC, a time of TCY is added before the A/D clock starts. This allows the SLEEP instruction to be executed.

**2:** This is a minimal RC delay (typically 100 ns), which also disconnects the holding capacitor from the analog input.

**TABLE 4-2: A/D CONVERSION REQUIREMENTS**

| Param No. | Symbol | Characteristic | | Min | Max | Units | Conditions |
|---|---|---|---|---|---|---|---|
| 130 | TAD | A/D Clock Period | PIC18**F**XXXX | 0.8 | 12.5(1) | µs | TOSC based, VREF ≥ 3.0V |
| | | | PIC18**LF**XXXX | 1.4 | 25.0(1) | µs | VDD = 3.0V; TOSC based, VREF full range |
| | | | PIC18**F**XXXX | — | 1 | µs | A/D RC mode |
| | | | PIC18**LF**XXXX | — | 3 | µs | VDD = 3.0V; A/D RC mode |
| 131 | TCNV | Conversion Time (not including acquisition time)(2) | | 13 | 14 | TAD | |
| 132 | TACQ | Acquisition Time(3) | | 1.4 | — | µs | |
| 135 | TSWC | Switching Time from Convert → Sample | | — | **(Note 4)** | | |
| 137 | TDIS | Discharge Time | | 0.2 | — | µs | |

**Note 1:** The time of the A/D clock period is dependent on the device frequency and the TAD clock divider.

**2:** ADRES registers may be read on the following TCY cycle.

**3:** The time for the holding capacitor to acquire the "New" input voltage when the voltage changes full scale after the conversion (VDD to VSS or VSS to VDD). The source impedance (RS) on the input channels is 50Ω.

**4:** On the following cycle of the device clock.

**NOTES:**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## 5.0 PACKAGING INFORMATION

For packaging information, see the *"PIC18F8722 Family Data Sheet"* (DS39646).

**NOTES:**


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## APPENDIX A: REVISION HISTORY

### Revision A (August 2007)

Original data sheet for the PIC18F8723 family of devices.

### Revision B (October 2009)

Updated to remove Preliminary status.

## APPENDIX B: DEVICE DIFFERENCES

The differences between the devices listed in this data sheet are shown in Table B-1.

**TABLE B-1: PIC18F8723 FAMILY DEVICE DIFFERENCES**

| Features | PIC18F6628 | PIC18F6723 | PIC18F8628 | PIC18F8723 |
|---|---|---|---|---|
| Program Memory (Bytes) | 96K | 128K | 96K | 128K |
| Program Memory (Instructions) | 49152 | 65536 | 49152 | 65536 |
| Interrupt Sources | 28 | 28 | 29 | 29 |
| I/O Ports | Ports A, B, C, D, E, F, G | Ports A, B, C, D, E, F, G | Ports A, B, C, D, E, F, G, H, J | Ports A, B, C, D, E, F, G, H, J |
| Capture/Compare/PWM Modules | 2 | 2 | 2 | 2 |
| Enhanced Capture/Compare/PWM Modules | 3 | 3 | 3 | 3 |
| Parallel Communications (PSP) | Yes | Yes | Yes | Yes |
| External Memory Bus | No | No | Yes | Yes |
| 12-Bit Analog-to-Digital Module | 12 Input Channels | 12 Input Channels | 16 Input Channels | 16 Input Channels |
| Packages | 64-Pin TQFP | 64-Pin TQFP | 80-Pin TQFP | 80-Pin TQFP |

## APPENDIX C: CONVERSION CONSIDERATIONS

This appendix discusses the considerations for converting from previous versions of a device to the ones listed in this data sheet. Typically, these changes are due to the differences in the process technology used. An example of this type of conversion is from a PIC16C74A to a PIC16C74B.

**Not Applicable**

## APPENDIX D: MIGRATION FROM BASELINE TO ENHANCED DEVICES

This section discusses how to migrate from a Baseline device (i.e., PIC16C5X) to an Enhanced MCU device (i.e., PIC18FXXX).

The following are the list of modifications over the PIC16C5X microcontroller family:

**Not Currently Available**


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## APPENDIX E: MIGRATION FROM MID-RANGE TO ENHANCED DEVICES

A detailed discussion of the differences between the mid-range MCU devices (i.e., PIC16CXXX) and the enhanced devices (i.e., PIC18FXXX) is provided in *AN716, "Migrating Designs from PIC16C74A/74B to PIC18C442*". The changes discussed, while device specific, are generally applicable to all mid-range to enhanced device migrations.

This Application Note is available on our web site, www.microchip.com, as Literature Number DS00716.

## APPENDIX F: MIGRATION FROM HIGH-END TO ENHANCED DEVICES

A detailed discussion of the migration pathway and differences between the high-end MCU devices (i.e., PIC17CXXX) and the enhanced devices (i.e., PIC18FXXX) is provided in *AN726, "PIC17CXXX to PIC18CXXX Migration*".

This Application Note is available on our web site, www.microchip.com, as Literature Number DS00726.

**NOTES:**


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## INDEX



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## R



## S



## T



## V



## W




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- Development Systems Information Line

Customers should contact their distributor, representative or field application engineer (FAE) for support. Local sales offices are also available to help customers. A listing of sales offices and locations is included in the back of this document.

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Device: PIC18F8723 Family Literature Number: DS39894B

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## PIC18F8723 FAMILY PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

| PART NO. | X | /XX | XXX |
|---|---|---|---|
| Device | Temperature Range | Package | Pattern |

| | |
|---|---|
| Device[1) (2)] | PIC18F6628/6723, PIC18F8628/8723, VDD range 4.2V to 5.5V<br>PIC18LF6628/6723, PIC18LF6628/6723( VDD range 2.0V to 5.5V |
| Temperature Range | I = -40°C to +85°C (Industrial)<br>E = -40°C to +125°C (Extended) |
| Package | PT = TQFP (Thin Quad Flatpack) |
| Pattern | QTP, SQTP, Code or Special Requirements (blank otherwise) |

**Examples:**

a) PIC18LF6723-I/PT 301 = Industrial temp., TQFP package, Extended VDD limits, QTP pattern #301.

b) PIC18F6723-E/PT = Extended temp., TQFP package, standard VDD limits.

**Note 1:** F = Standard Voltage Range
LF = Wide Voltage Range
**2:** T = in tape and reel TQFP packages only.

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