

# MC74HC08A

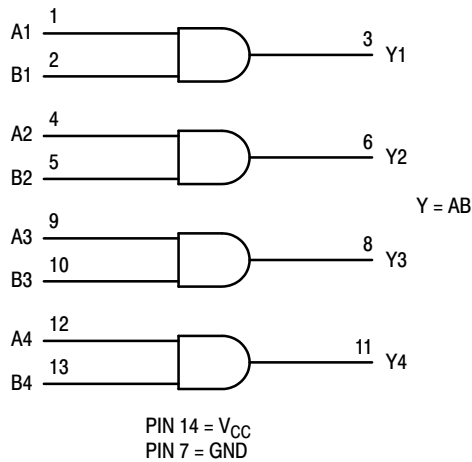
## Quad 2-Input AND Gate High-Performance Silicon-Gate CMOS

The MC74HC08A is identical in pinout to the LS08. The device inputs are compatible with Standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

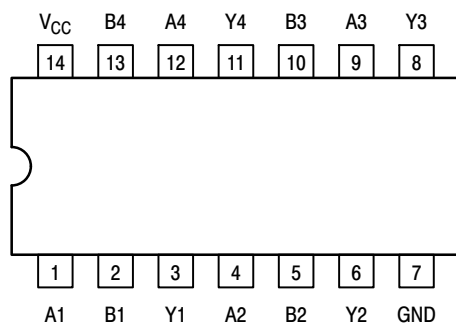
### Features

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance With the JEDEC Standard No. 7A Requirements
- Chip Complexity: 24 FETs or 6 Equivalent Gates
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free and are RoHS Compliant

### LOGIC DIAGRAM



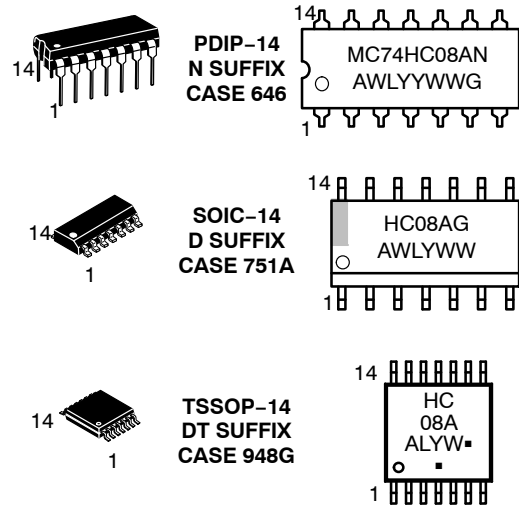
### Pinout: 14-Lead Packages (Top View)



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### MARKING DIAGRAMS



A = Assembly Location  
L, WL = Wafer Lot  
Y, YY = Year  
W, WW = Work Week  
G or ■ = Pb-Free Package

(Note: Microdot may be in either location)

### FUNCTION TABLE

| Inputs |   | Output |
|--------|---|--------|
| A      | B | Y      |
| L      | L | L      |
| L      | H | L      |
| H      | L | L      |
| H      | H | H      |

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

# MC74HC08A

## MAXIMUM RATINGS

| Symbol    | Parameter   | Value                   | Unit |
|-----------|---|-------------------------|------|
| $V_{CC}$  | DC Supply Voltage (Referenced to GND)   | - 0.5 to + 7.0          | V    |
| $V_{in}$  | DC Input Voltage (Referenced to GND)  | - 0.5 to $V_{CC} + 0.5$ | V    |
| $V_{out}$ | DC Output Voltage (Referenced to GND)   | - 0.5 to $V_{CC} + 0.5$ | V    |
| $I_{in}$  | DC Input Current, per Pin   | $\pm 20$                | mA   |
| $I_{out}$ | DC Output Current, per Pin  | $\pm 25$                | mA   |
| $I_{CC}$  | DC Supply Current, $V_{CC}$ and GND Pins  | $\pm 50$                | mA   |
| $P_D$     | Power Dissipation in Still Air,<br>Plastic DIP†<br>SOIC Package†<br>TSSOP Package†    | 750<br>500<br>450       | mW   |
| $T_{stg}$ | Storage Temperature   | - 65 to + 150           | °C   |
| $T_L$     | Lead Temperature, 1 mm from Case for 10 Seconds<br>Plastic DIP, SOIC or TSSOP Package | 260                     | °C   |

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$ . Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or  $V_{CC}$ ). Unused outputs must be left open.

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

†Derating — Plastic DIP: - 10 mW/°C from 65° to 125°C  
SOIC Package: - 7 mW/°C from 65° to 125°C  
TSSOP Package: - 6.1 mW/°C from 65° to 125°C

## RECOMMENDED OPERATING CONDITIONS

| Symbol            | Parameter  | Min   | Max                     | Unit |
|-------------------|--|---|-------------------------|------|
| $V_{CC}$          | DC Supply Voltage (Referenced to GND)                | 2.0   | 6.0                     | V    |
| $V_{in}, V_{out}$ | DC Input Voltage, Output Voltage (Referenced to GND) | 0   | $V_{CC}$                | V    |
| $T_A$             | Operating Temperature, All Package Types             | - 55  | + 125                   | °C   |
| $t_r, t_f$        | Input Rise and Fall Time (Figure 1)                  | $V_{CC} = 2.0\text{ V}$<br>$V_{CC} = 4.5\text{ V}$<br>$V_{CC} = 6.0\text{ V}$ | 0<br>1000<br>500<br>400 | ns   |

## ORDERING INFORMATION

| Device           | Package            | Shipping†          |
|------------------|--------------------|--------------------|
| MC74HC08ANG      | PDIP-14 (Pb-Free)  | 25 Units / Rail    |
| MC74HC08ADG      | SOIC-14 (Pb-Free)  | 55 Units / Rail    |
| MC74HC08ADR2G    | SOIC-14 (Pb-Free)  | 2500 / Tape & Reel |
| MC74HC08ADTR2G   | TSSOP-14 (Pb-Free) | 2500 / Tape & Reel |
| NLV74HC08ADG*    | SOIC-14 (Pb-Free)  | 55 Units / Rail    |
| NLV74HC08ADR2G*  | SOIC-14 (Pb-Free)  | 2500 / Tape & Reel |
| NLV74HC08ADTR2G* | TSSOP-14 (Pb-Free) | 2500 / Tape & Reel |
| NLV74HC08ANG*    | PDIP-14 (Pb-Free)  | 25 Units / Rail    |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

\*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable

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## DC CHARACTERISTICS (Voltages Referenced to GND)

| Symbol          | Parameter                                      | Condition   | V <sub>CC</sub><br>V | Guaranteed Limit |       |        | Unit |
|-----------------|--|---|----------------------|------------------|-------|--------|------|
|                 |  |   |                      | -55 to 25°C      | ≤85°C | ≤125°C |      |
| V <sub>IH</sub> | Minimum High-Level Input Voltage               | V <sub>out</sub> = 0.1V or V <sub>CC</sub> - 0.1V<br> I <sub>out</sub>   ≤ 20μA   | 2.0                  | 1.50             | 1.50  | 1.50   | V    |
|                 |  |   | 3.0                  | 2.10             | 2.10  | 2.10   |      |
|                 |  |   | 4.5                  | 3.15             | 3.15  | 3.15   |      |
|                 |  |   | 6.0                  | 4.20             | 4.20  | 4.20   |      |
| V <sub>IL</sub> | Maximum Low-Level Input Voltage                | V <sub>out</sub> = 0.1V or V <sub>CC</sub> - 0.1V<br> I <sub>out</sub>   ≤ 20μA   | 2.0                  | 0.50             | 0.50  | 0.50   | V    |
|                 |  |   | 3.0                  | 0.90             | 0.90  | 0.90   |      |
|                 |  |   | 4.5                  | 1.35             | 1.35  | 1.35   |      |
|                 |  |   | 6.0                  | 1.80             | 1.80  | 1.80   |      |
| V <sub>OH</sub> | Minimum High-Level Output Voltage              | V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub><br> I <sub>out</sub>   ≤ 20μA  | 2.0                  | 1.9              | 1.9   | 1.9    | V    |
|                 |  |   | 4.5                  | 4.4              | 4.4   | 4.4    |      |
|                 |  |   | 6.0                  | 5.9              | 5.9   | 5.9    |      |
|                 |  | V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub><br> I <sub>out</sub>   ≤ 2.4mA<br> I <sub>out</sub>   ≤ 4.0mA<br> I <sub>out</sub>   ≤ 5.2mA | 3.0                  | 2.48             | 2.34  | 2.20   |      |
|                 |  |   | 4.5                  | 3.98             | 3.84  | 3.70   |      |
|                 |  |   | 6.0                  | 5.48             | 5.34  | 5.20   |      |
| V <sub>OL</sub> | Maximum Low-Level Output Voltage               | V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub><br> I <sub>out</sub>   ≤ 20μA  | 2.0                  | 0.1              | 0.1   | 0.1    | V    |
|                 |  |   | 4.5                  | 0.1              | 0.1   | 0.1    |      |
|                 |  |   | 6.0                  | 0.1              | 0.1   | 0.1    |      |
|                 |  | V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub><br> I <sub>out</sub>   ≤ 2.4mA<br> I <sub>out</sub>   ≤ 4.0mA<br> I <sub>out</sub>   ≤ 5.2mA | 3.0                  | 0.26             | 0.33  | 0.40   |      |
|                 |  |   | 4.5                  | 0.26             | 0.33  | 0.40   |      |
|                 |  |   | 6.0                  | 0.26             | 0.33  | 0.40   |      |
| I <sub>in</sub> | Maximum Input Leakage Current                  | V <sub>in</sub> = V <sub>CC</sub> or GND  | 6.0                  | ±0.1             | ±1.0  | ±1.0   | μA   |
| I <sub>CC</sub> | Maximum Quiescent Supply Current (per Package) | V <sub>in</sub> = V <sub>CC</sub> or GND<br>I <sub>out</sub> = 0μA  | 6.0                  | 1.0              | 10    | 40     | μA   |

## AC CHARACTERISTICS (C<sub>L</sub> = 50pF, Input t<sub>r</sub> = t<sub>f</sub> = 6ns)

| Symbol                                 | Parameter  | V <sub>CC</sub><br>V   | Guaranteed Limit |       |        | Unit |
|--|--|--|------------------|-------|--------|------|
|  |  |  | -55 to 25°C      | ≤85°C | ≤125°C |      |
| t <sub>PLH</sub> ,<br>t <sub>PHL</sub> | Maximum Propagation Delay, Input A or B to Output Y<br>(Figures 1 and 2) | 2.0  | 75               | 95    | 110    | ns   |
|  |  | 3.0  | 30               | 40    | 55     |      |
|  |  | 4.5  | 15               | 19    | 22     |      |
|  |  | 6.0  | 13               | 16    | 19     |      |
| t <sub>TLH</sub> ,<br>t <sub>THL</sub> | Maximum Output Transition Time, Any Output<br>(Figures 1 and 2)          | 2.0  | 75               | 95    | 110    | ns   |
|  |  | 3.0  | 27               | 32    | 36     |      |
|  |  | 4.5  | 15               | 19    | 22     |      |
|  |  | 6.0  | 13               | 16    | 19     |      |
| C <sub>in</sub>                        | Maximum Input Capacitance  |  | 10               | 10    | 10     | pF   |
| C <sub>PD</sub>                        | Power Dissipation Capacitance (Per Buffer)*                              | Typical @ 25°C, V <sub>CC</sub> = 5.0 V, V <sub>EE</sub> = 0 V |                  |       | pF     |      |
|  |  | 20   |                  |       |        |      |

\* Used to determine the no-load dynamic power consumption: P<sub>D</sub> = C<sub>PD</sub> V<sub>CC</sub><sup>2</sup>f + I<sub>CC</sub> V<sub>CC</sub>.

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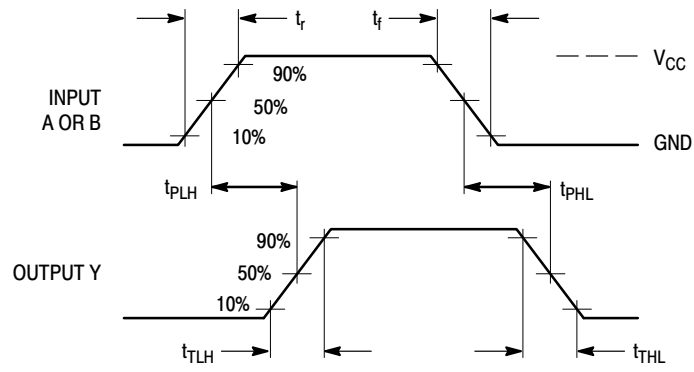
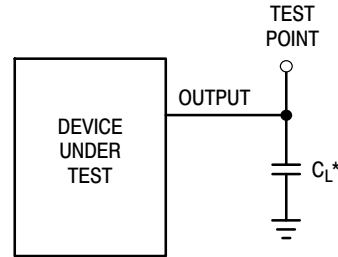


Figure 1. Switching Waveforms



\*Includes all probe and jig capacitance

Figure 2. Test Circuit

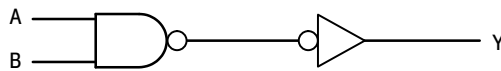
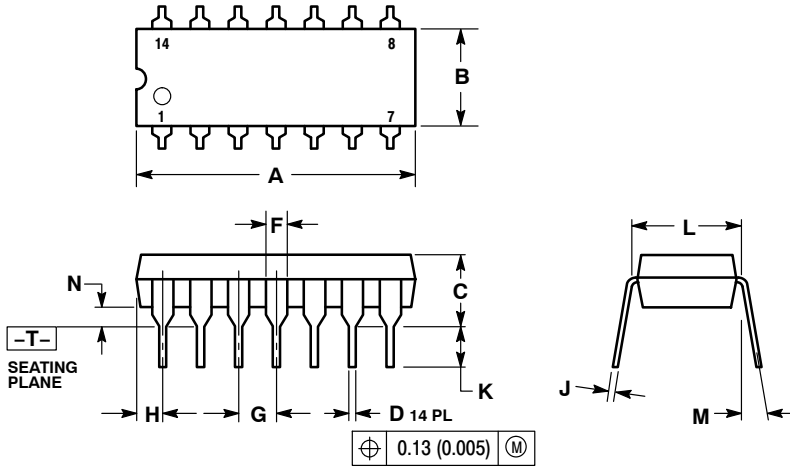


Figure 3. Expanded Logic Diagram  
(1/4 of the Device)

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## PACKAGE DIMENSIONS

PDIP-14  
N SUFFIX  
CASE 646-06  
ISSUE P



### NOTES:

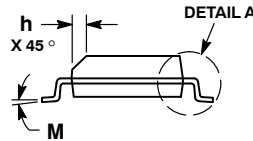
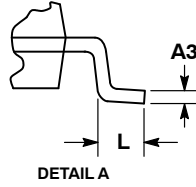
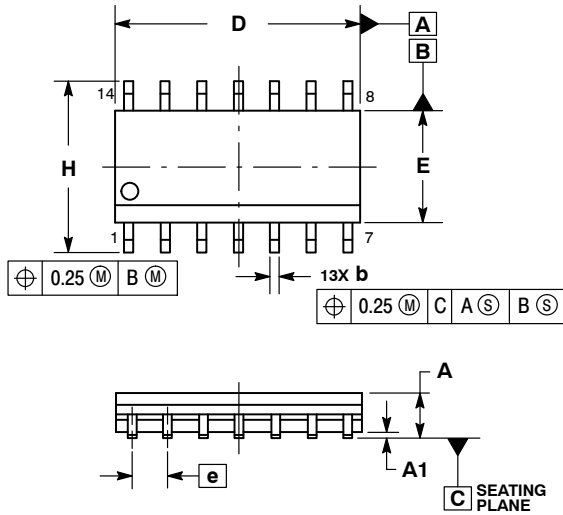
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

| DIM | INCHES    |                 | MILLIMETERS |                 |
|-----|-----------|-----------------|-------------|-----------------|
|     | MIN       | MAX             | MIN         | MAX             |
| A   | 0.715     | 0.770           | 18.16       | 19.56           |
| B   | 0.240     | 0.260           | 6.10        | 6.60            |
| C   | 0.145     | 0.185           | 3.69        | 4.69            |
| D   | 0.015     | 0.021           | 0.38        | 0.53            |
| F   | 0.040     | 0.070           | 1.02        | 1.78            |
| G   | 0.100 BSC |                 | 2.54 BSC    |                 |
| H   | 0.052     | 0.095           | 1.32        | 2.41            |
| J   | 0.008     | 0.015           | 0.20        | 0.38            |
| K   | 0.115     | 0.135           | 2.92        | 3.43            |
| L   | 0.290     | 0.310           | 7.37        | 7.87            |
| M   | ---       | 10 <sup>°</sup> | ---         | 10 <sup>°</sup> |
| N   | 0.015     | 0.039           | 0.38        | 1.01            |

# MC74HC08A

## PACKAGE DIMENSIONS

SOIC-14 NB  
CASE 751A-03  
ISSUE K

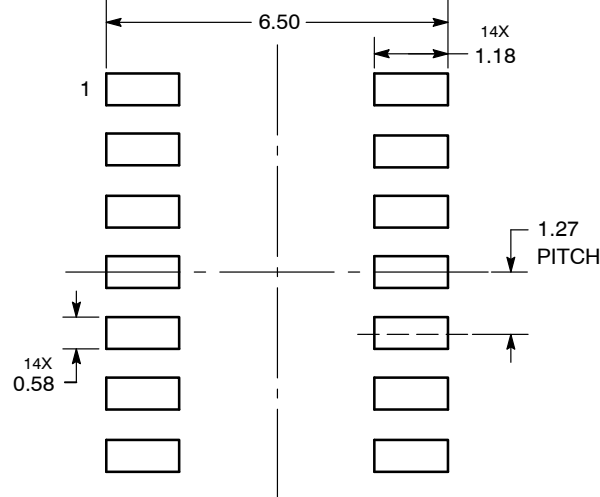


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

| DIM | MILLIMETERS |      | INCHES    |       |
|-----|-------------|------|-----------|-------|
|     | MIN         | MAX  | MIN       | MAX   |
| A   | 1.35        | 1.75 | 0.054     | 0.068 |
| A1  | 0.10        | 0.25 | 0.004     | 0.010 |
| A3  | 0.19        | 0.25 | 0.008     | 0.010 |
| b   | 0.35        | 0.49 | 0.014     | 0.019 |
| D   | 8.55        | 8.75 | 0.337     | 0.344 |
| E   | 3.80        | 4.00 | 0.150     | 0.157 |
| e   | 1.27 BSC    |      | 0.050 BSC |       |
| H   | 5.80        | 6.20 | 0.228     | 0.244 |
| h   | 0.25        | 0.50 | 0.010     | 0.019 |
| L   | 0.40        | 1.25 | 0.016     | 0.049 |
| M   | 0°          | 7°   | 0°        | 7°    |

### SOLDERING FOOTPRINT\*



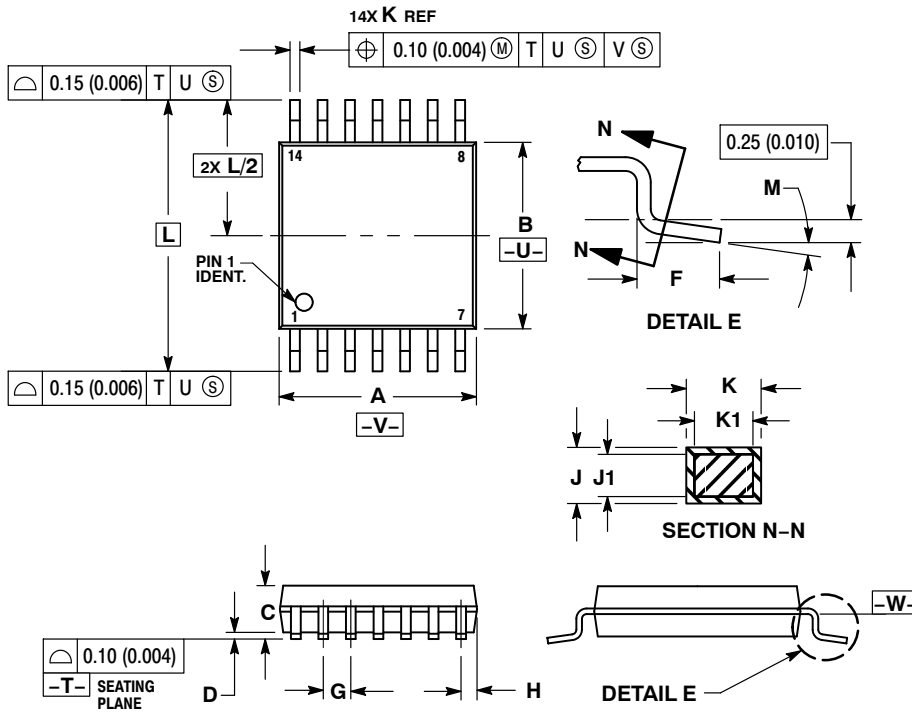
DIMENSIONS: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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## PACKAGE DIMENSIONS

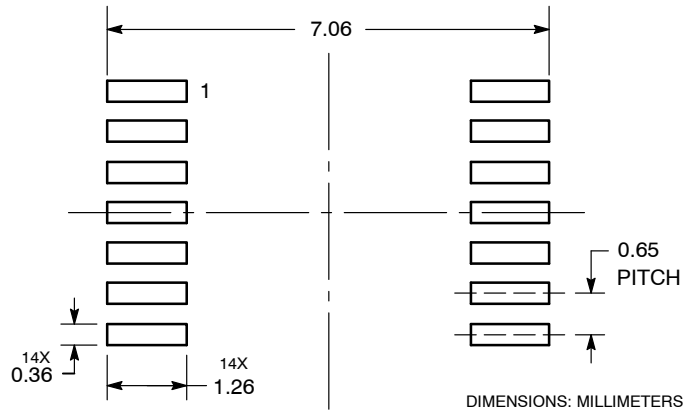
TSSOP-14  
DT SUFFIX  
CASE 948G-01  
ISSUE B



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
  4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
  5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
  6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
  7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -V-.

| DIM | MILLIMETERS |      | INCHES    |       |
|-----|-------------|------|-----------|-------|
|     | MIN         | MAX  | MIN       | MAX   |
| A   | 4.90        | 5.10 | 0.193     | 0.200 |
| B   | 4.30        | 4.50 | 0.169     | 0.177 |
| C   | ---         | 1.20 | ---       | 0.047 |
| D   | 0.05        | 0.15 | 0.002     | 0.006 |
| F   | 0.50        | 0.75 | 0.020     | 0.030 |
| G   | 0.65 BSC    |      | 0.026 BSC |       |
| H   | 0.50        | 0.60 | 0.020     | 0.024 |
| J   | 0.09        | 0.20 | 0.004     | 0.008 |
| J1  | 0.09        | 0.16 | 0.004     | 0.006 |
| K   | 0.19        | 0.30 | 0.007     | 0.012 |
| K1  | 0.19        | 0.25 | 0.007     | 0.010 |
| L   | 6.40 BSC    |      | 0.252 BSC |       |
| M   | 0°          | 8°   | 0°        | 8°    |

### SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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- При необходимости вся продукция военного и аэрокосмического назначения проходит испытания и сертификацию в лаборатории (по согласованию с заказчиком);
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«FORSTAR» (основан в 1998 г.)

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Телефон: 8 (812) 309-75-97 (многоканальный)

Факс: 8 (812) 320-03-32

Электронная почта: [ocean@oceanchips.ru](mailto:ocean@oceanchips.ru)

Web: <http://oceanchips.ru/>

Адрес: 198099, г. Санкт-Петербург, ул. Калинина, д. 2, корп. 4, лит. А