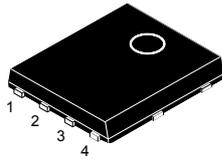
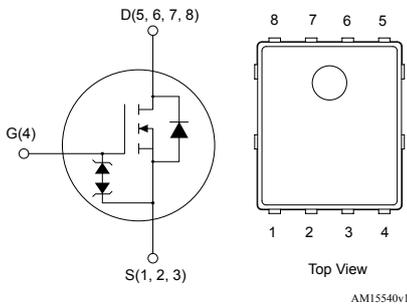


## N-channel 650 V, 0.62 $\Omega$ typ., 5 A MDmesh™ M2 Power MOSFET in a PowerFLAT™ 5x6 HV package


**PowerFLAT 5x6 HV**


AM15540v1

### Features

Order code	$V_{DS}$	$R_{DS(on)}$ max.	$I_D$	$P_{TOT}$
STL12N65M2	650 V	0.75 $\Omega$	5 A	48 W

- Extremely low gate charge
- Excellent output capacitance ( $C_{OSS}$ ) profile
- 100% avalanche tested
- Zener-protected

### Applications

- Switching applications

### Description

This device is an N-channel Power MOSFET developed using MDmesh M2 technology. Thanks to its strip layout and an improved vertical structure, the device exhibits low on-resistance and optimized switching characteristics, rendering it suitable for the most demanding high efficiency converters.



#### Product status link

[STL12N65M2](#)

#### Product summary

<b>Order code</b>	STL12N65M2
<b>Marking</b>	12N65M2
<b>Package</b>	PowerFLAT™ 5x6 HV
<b>Packing</b>	Tape and reel

# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{GS}$	Gate-source voltage	$\pm 25$	V
$I_D$	Drain current (continuous) at $T_{case} = 25\text{ }^\circ\text{C}$	5	A
	Drain current (continuous) at $T_{case} = 100\text{ }^\circ\text{C}$	3.2	
$I_{DM}^{(1)}$	Drain current (pulsed)	20	A
$P_{TOT}$	Total power dissipation at $T_{case} = 25\text{ }^\circ\text{C}$	48	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	15	V/ns
$dv/dt^{(3)}$	MOSFET $dv/dt$ ruggedness	50	
$T_{stg}$	Storage temperature range	-55 to 150	$^\circ\text{C}$
$T_j$	Operating junction temperature range		

1. Pulse width is limited by safe operating area.
2.  $I_{SD} \leq 5\text{ A}$ ,  $di/dt \leq 400\text{ A}/\mu\text{s}$ ;  $V_{DS}(\text{peak}) \leq V_{(BR)DSS}$ ,  $V_{DD} = 400\text{ V}$ .
3.  $V_{DS} \leq 520\text{ V}$ .

**Table 2. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	2.6	$^\circ\text{C}/\text{W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	50	

1. When mounted on a 1-inch<sup>2</sup> FR-4, 2 Oz copper board.

**Table 3. Avalanche characteristics**

Symbol	Parameter	Value	Unit
$I_{AR}^{(1)}$	Avalanche current, repetitive or not repetitive	1.2	A
$E_{AS}^{(2)}$	Single pulse avalanche energy	105	mJ

1. Pulse width limited by  $T_{jmax}$ .
2. starting  $T_j = 25\text{ }^\circ\text{C}$ ,  $I_D = I_{AR}$ ,  $V_{DD} = 50\text{ V}$ .

## 2 Electrical characteristics

( $T_{\text{case}} = 25\text{ °C}$  unless otherwise specified)

**Table 4. Static**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(\text{BR})\text{DSS}}$	Drain-source breakdown voltage	$V_{\text{GS}} = 0\text{ V}$ , $I_{\text{D}} = 1\text{ mA}$	650			V
$I_{\text{DSS}}$	Zero gate voltage drain current	$V_{\text{GS}} = 0\text{ V}$ , $V_{\text{DS}} = 650\text{ V}$			1	$\mu\text{A}$
		$V_{\text{GS}} = 0\text{ V}$ , $V_{\text{DS}} = 650\text{ V}$ , $T_{\text{case}} = 125\text{ °C}^{(1)}$			100	
$I_{\text{GSS}}$	Gate-body leakage current	$V_{\text{DS}} = 0\text{ V}$ , $V_{\text{GS}} = 25\text{ V}$			$\pm 10$	$\mu\text{A}$
$V_{\text{GS}(\text{th})}$	Gate threshold voltage	$V_{\text{DS}} = V_{\text{GS}}$ , $I_{\text{D}} = 250\text{ }\mu\text{A}$	2	3	4	V
$R_{\text{DS}(\text{on})}$	Static drain-source on-resistance	$V_{\text{GS}} = 10\text{ V}$ , $I_{\text{D}} = 3\text{ A}$		0.62	0.75	$\Omega$

1. Defined by design, not subject to production test.

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{\text{iss}}$	Input capacitance	$V_{\text{DS}} = 100\text{ V}$ , $f = 1\text{ MHz}$ , $V_{\text{GS}} = 0\text{ V}$	-	410	-	$\mu\text{F}$
$C_{\text{oss}}$	Output capacitance		-	20	-	
$C_{\text{riss}}$	Reverse transfer capacitance		-	0.9	-	
$C_{\text{oss eq.}}^{(1)}$	Equivalent output capacitance	$V_{\text{DS}} = 0\text{ to }520\text{ V}$ , $V_{\text{GS}} = 0\text{ V}$	-	43	-	$\mu\text{F}$
$R_{\text{G}}$	Intrinsic gate resistance	$f = 1\text{ MHz}$ open drain	-	6.4	-	$\Omega$
$Q_{\text{g}}$	Total gate charge	$V_{\text{DD}} = 520\text{ V}$ , $I_{\text{D}} = 7\text{ A}$ , $V_{\text{GS}} = 0\text{ to }10\text{ V}$ (see Figure 14 )	-	12.5	-	nC
$Q_{\text{gs}}$	Gate-source charge		-	3.2	-	
$Q_{\text{gd}}$	Gate-drain charge		-	5.8	-	

1.  $C_{\text{oss eq.}}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{\text{oss}}$  when  $V_{\text{DS}}$  increases from 0 to 80%  $V_{\text{DSS}}$ .

**Table 6. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{\text{d}(\text{on})}$	Turn-on delay time	$V_{\text{DD}} = 325\text{ V}$ , $I_{\text{D}} = 3.5\text{ A}$ , $R_{\text{G}} = 4.7\text{ }\Omega$ , $V_{\text{GS}} = 10\text{ V}$ (see Figure 13 and Figure 18)	-	9.5	-	ns
$t_{\text{r}}$	Rise time		-	7.5	-	
$t_{\text{d}(\text{off})}$	Turn-off delay time		-	26	-	
$t_{\text{f}}$	Fall time		-	15	-	

**Table 7. Source-drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		5	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		20	A
$V_{SD}^{(2)}$	Forward on voltage	$V_{GS} = 0\text{ V}, I_{SD} = 5\text{ A}$	-		1.6	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 7\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, V_{DD} = 60\text{ V}$ (see <a href="#">Figure 15</a> )	-	318		ns
$Q_{rr}$	Reverse recovery charge		-	2.5		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	15.5		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 7\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, V_{DD} = 60\text{ V}, T_j = 150\text{ }^\circ\text{C}$ (see <a href="#">Figure 15</a> )	-	437		ns
$Q_{rr}$	Reverse recovery charge		-	3.2		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	15		A

1. Pulse width is limited by safe operating area.

2. Pulse test: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%.

## 2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

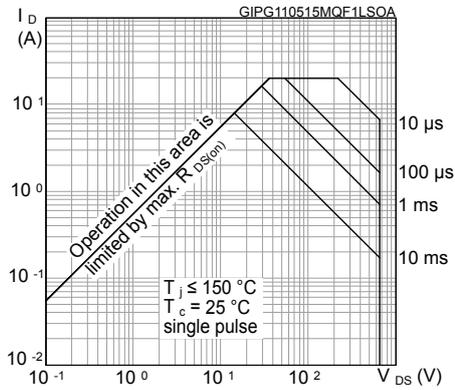


Figure 2. Thermal impedance

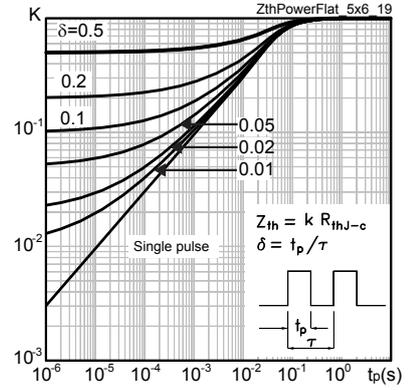


Figure 3. Output characteristics

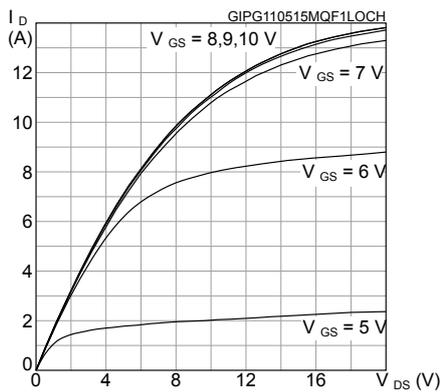


Figure 4. Transfer characteristics

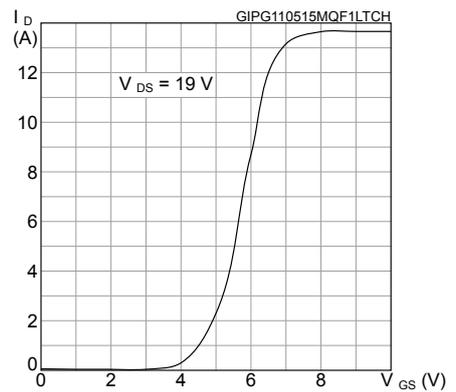


Figure 5. Gate charge vs gate-source voltage

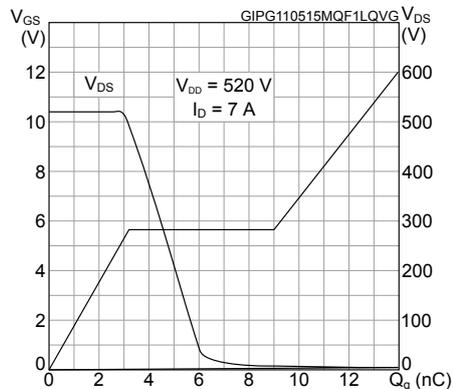


Figure 6. Static drain-source on-resistance

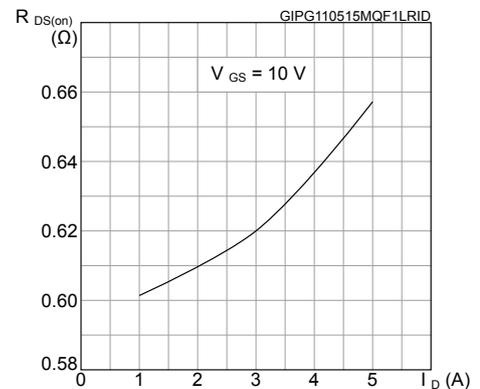


Figure 7. Capacitance variations

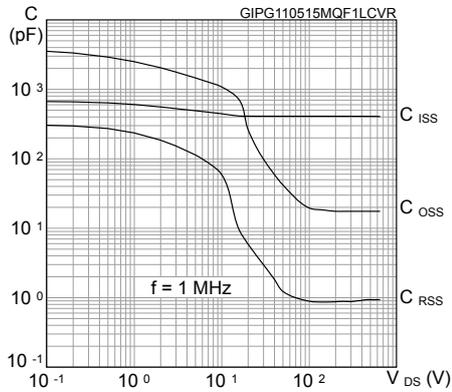


Figure 8. Normalized gate threshold voltage vs temperature

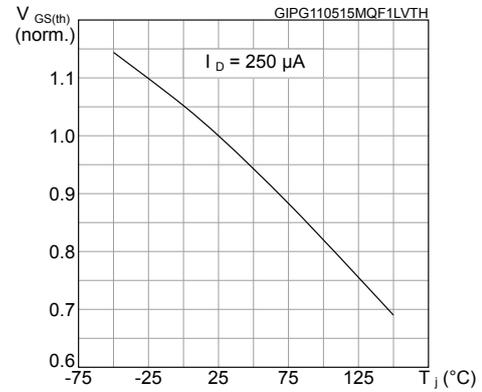


Figure 9. Normalized on-resistance vs temperature

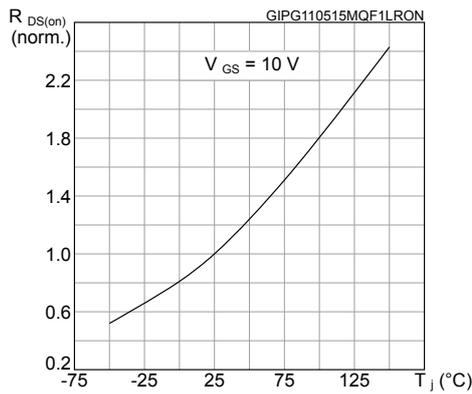


Figure 10. Normalized  $V_{(BR)DSS}$  vs temperature

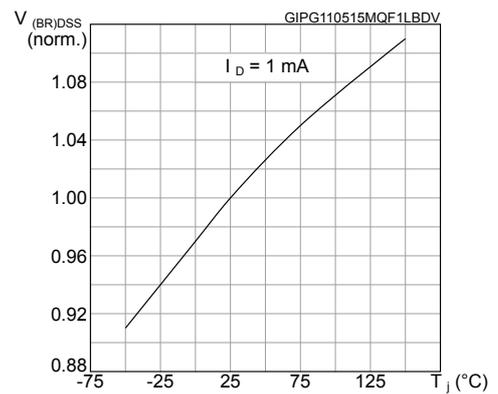


Figure 11. Output capacitance stored energy

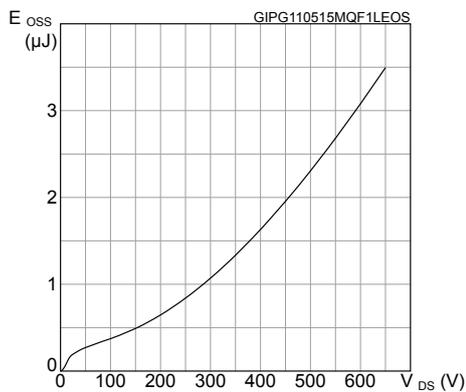
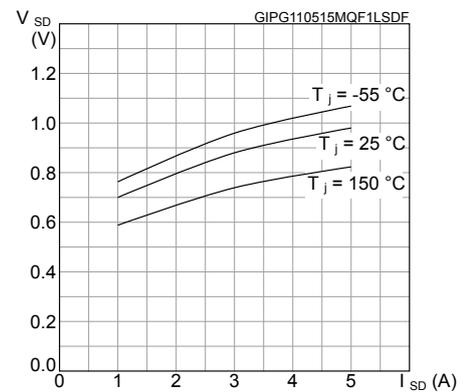
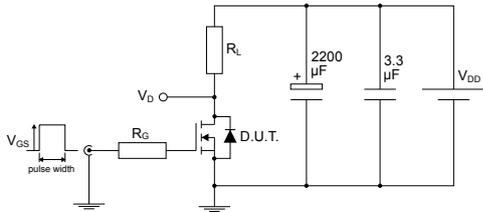


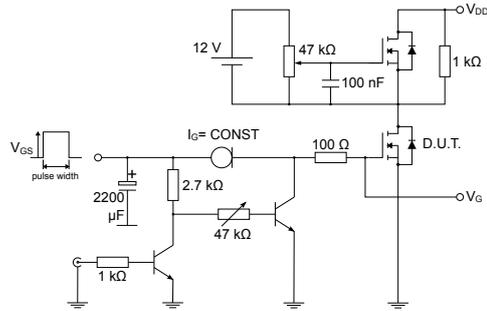
Figure 12. Source-drain diode forward characteristics



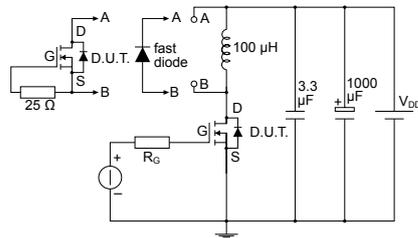
### 3 Test circuits

**Figure 13. Test circuit for resistive load switching times**


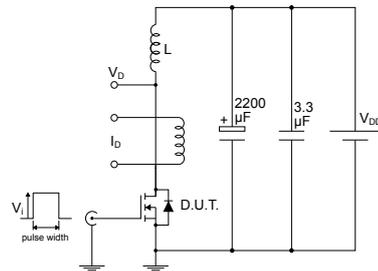
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**Figure 14. Test circuit for gate charge behavior**


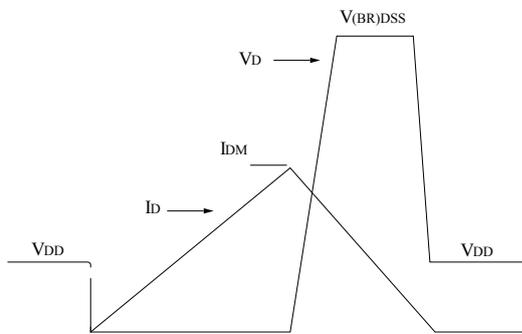
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**Figure 15. Test circuit for inductive load switching and diode recovery times**


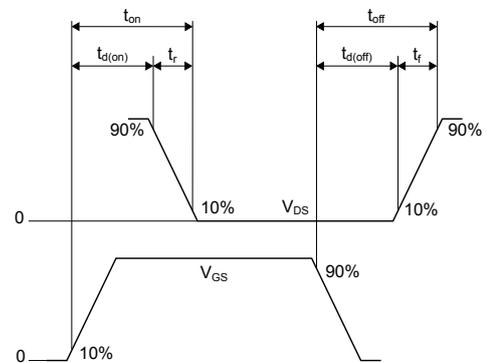
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**Figure 16. Unclamped inductive load test circuit**


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**Figure 17. Unclamped inductive waveform**


AM01472v1

**Figure 18. Switching time waveform**


AM01473v1

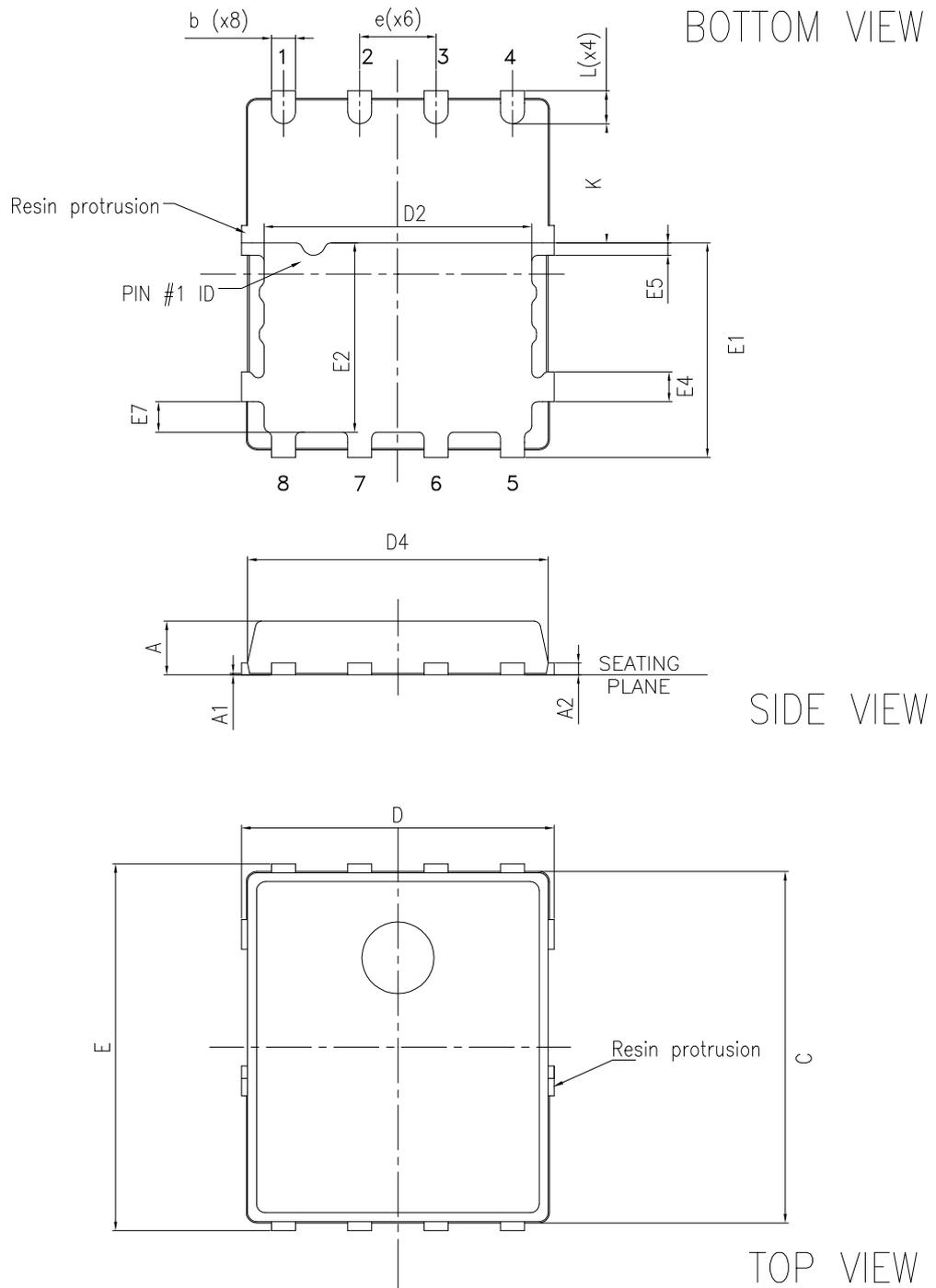
## 4 Package information

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In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

### 4.1 PowerFLAT 5x6 HV package information

Figure 19. PowerFLAT 5x6 HV package outline

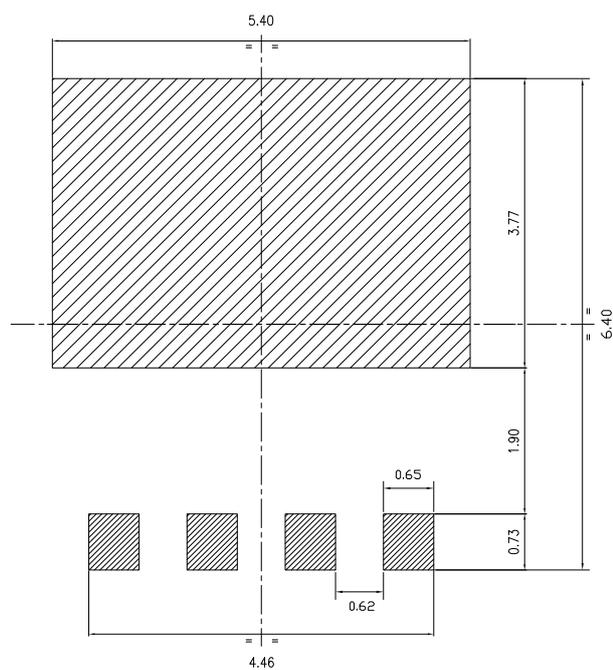


8368143\_Rev\_4

Table 8. PowerFLAT 5x6 HV mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
C	5.60	5.80	6.00
D	5.10	5.20	5.30
D2	4.30	4.40	4.50
D4	4.60	4.80	5.00
E	6.05	6.15	6.25
E1	3.50	3.60	3.70
E2	3.10	3.20	3.30
E4	0.40	0.50	0.60
E5	0.10	0.20	0.30
E7	0.40	0.50	0.60
e		1.27	
L	0.50	0.55	0.60
K	1.90	2.00	2.10

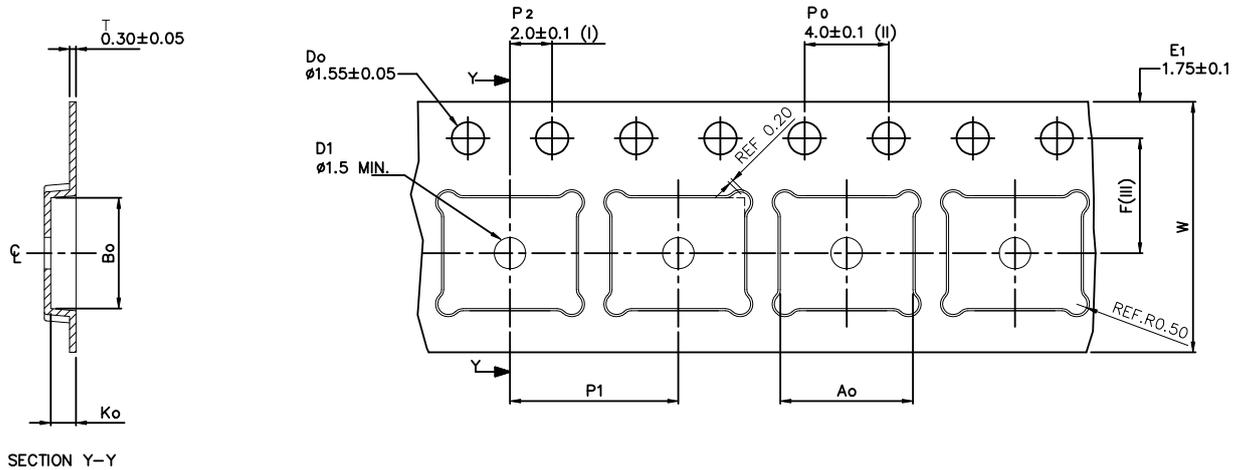
Figure 20. PowerFLAT™ 5x6 HV recommended footprint (dimensions are in mm)



8368143\_Rev\_4\_footprint

## 4.2 PowerFLAT 5x6 packing information

Figure 21. PowerFLAT 5x6 tape (dimensions are in mm)



Ao	6.30 +/- 0.1
Bo	5.30 +/- 0.1
Ko	1.20 +/- 0.1
F	5.50 +/- 0.1
P1	8.00 +/- 0.1
W	12.00 +/- 0.3

(I) Measured from centreline of sprocket hole to centreline of pocket.

(II) Cumulative tolerance of 10 sprocket holes is  $\pm 0.20$ .

(III) Measured from centreline of sprocket hole to centreline of pocket

Base and bulk quantity 3000 pcs  
All dimensions are in millimeters

8234350\_Tape\_rev\_C

Figure 22. PowerFLAT 5x6 package orientation in carrier tape

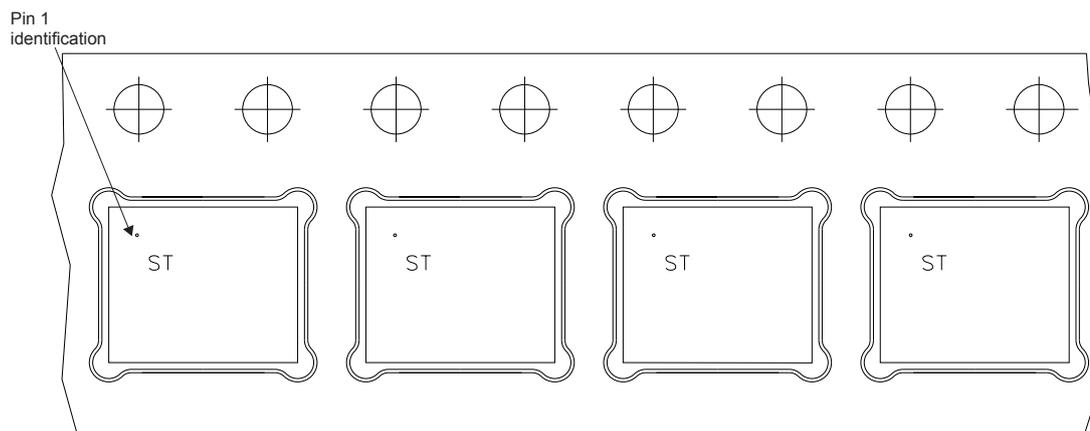
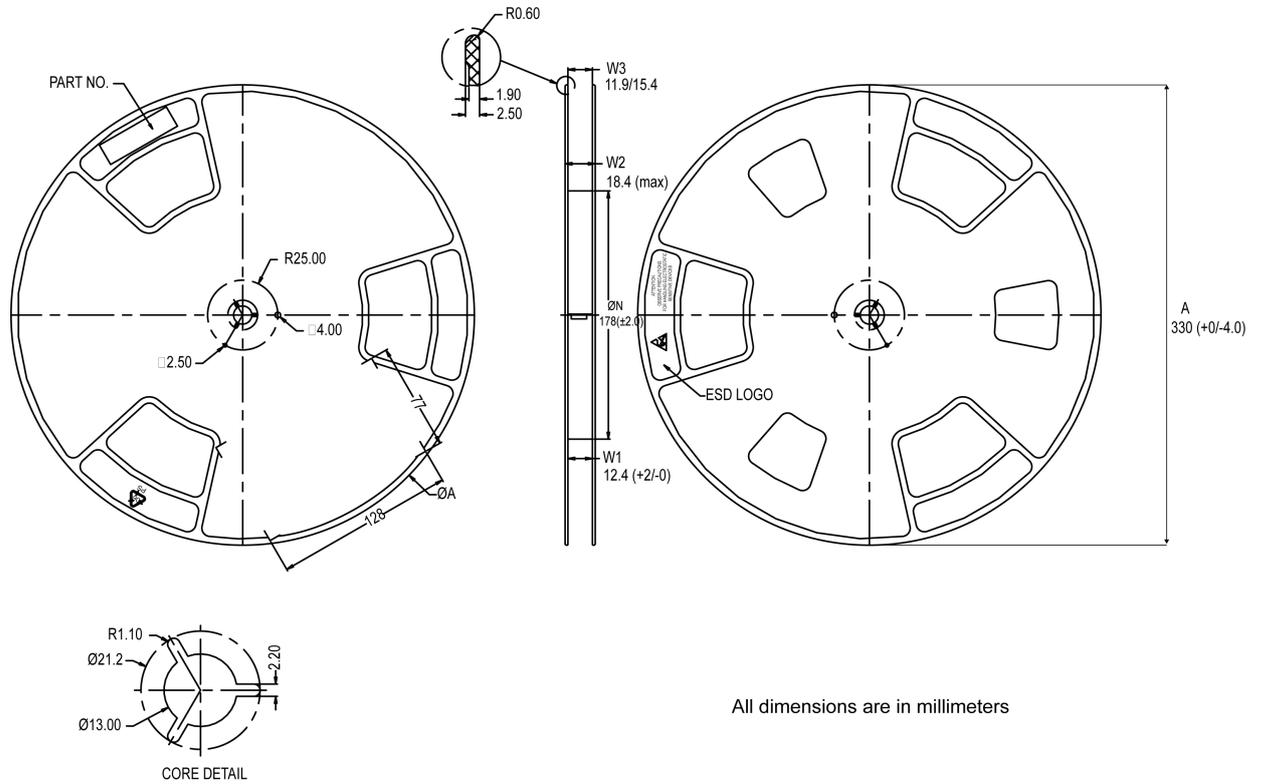


Figure 23. PowerFLAT 5x6 reel



All dimensions are in millimeters

8234350\_Reel\_rev\_C

## Revision history

**Table 9. Document revision history**

Date	Revision	Changes
11-May-2015	1	First release.
20-Jun-2019	2	Updated <a href="#">Section 1</a> and <a href="#">Section 2</a>

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