## Controller ICs <br> for High Side NMOSFET

## BD2270HFV-LB

## General Description

This is the product guarantees long time support in Industrial market.
BD2270HFV is an IC with a built-in external N -channel MOSFET driver circuit. This IC has a built-in charge pump circuit for gate drive and output discharge circuit, enabling configuration of a high side load switch for N-channel MOSFET drive without using any external parts.
In addition, the control input terminal has a built-in comparator with hysteresis function, facilitating control of the power up sequence. The space saving type of HVSOF5 package is used.

## Features

- Long time support a product for Industrial applications.
- Built-in charge pump
- Built-in discharge circuit for output charge
- Soft start circuit
- Built-in comparator with hysteresis function at control input terminal
- Possible to drive N -channel power MOSFET


## Key Specifications

- Input voltage range:
2.7 V to 5.5 V
- GATE rise time ( $\left.\mathrm{C}_{\mathrm{GATE}}=500 \mathrm{pF}\right)$ :

130 $\mu \mathrm{s}$ (Typ.)

- GATE output voltage $\left(\mathrm{V}_{\mathrm{cc}}=5 \mathrm{~V}\right)$ :
13.5V(Typ.)
$50 \mu \mathrm{~A}($ Тур.)
$5 \mu \mathrm{~A}$ (Typ.)
- Standby current:
$-25^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$
Package
W(Typ.) D(Typ.) H (Max.) $1.60 \mathrm{~mm} \times 1.60 \mathrm{~mm} \times 0.60 \mathrm{~mm}$


HVSOF5

## Applications

Industrial Equipment, PCs, PC peripheral devices, digital consumer electronics, etc.

## Typical Application Circuit



Lineup

| GATE output voltage( $\left.\mathrm{V}_{\mathrm{cc}}=5 \mathrm{~V}\right)$ |  |  | Package |  | Orderable Part Number |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Min. | Typ. | Max. |  |  |  |
| 10V | 13.5 V | 15V | HVSOF5 | Reel of 3000 | BD2270HFV - LBTR |

## Block Diagram



## Pin Configuration



Pin Description

| PIN No. | PIN name | I/O | Function |
| :---: | :---: | :---: | :--- |
| 1 | VCC | - | Power input terminal |
| 2 | GND | - | Ground terminal |
| 3 | AEN | I | Control input terminal <br> Turn ON the external MOSFET switch with high level input. <br> High level input $>2.0 \mathrm{~V}$, Low level input $<0.8 \mathrm{~V}$ |
| 4 | DISC | O | Switch output discharge terminal |
| 5 | GATE | O | GATE drive output terminal <br> Used to connect the gate of the external N-channel MOSFET. |

## Absolute Maximum Ratings

| Parameter | Symbol | Ratings | Unit |
| :--- | :---: | :---: | :---: |
| Supply voltage | Vcc | -0.3 to 6.0 | V |
| AEN voltage | VAEN | -0.3 to 6.0 | V |
| DISC voltage | VDISC | -0.3 to 6.0 | V |
| GATE voltage | VGATE | -0.3 to 15.0 | V |
| Storage temperature range | TSTG | -55 to 150 | ${ }^{\circ} \mathrm{C}$ |
| Power dissipation | Pd | $669^{\star 1}$ | mW |

*1 When mounted on a $70 \mathrm{~mm} \times 70 \mathrm{~mm} \times 1.6 \mathrm{~mm}$ glass epoxy PCB, derate by $5.352 \mathrm{~mW} /{ }^{\circ} \mathrm{C}$ above $\mathrm{Ta}=25^{\circ} \mathrm{C}$

## Recommended Operating Conditions

| Parameter | Symbol | Ratings | Unit |
| :--- | :---: | :---: | :---: |
| Operating voltage range | $\mathrm{V}_{\mathrm{CC}}$ | 2.7 to 5.5 | V |
| Operating temperature range | $\mathrm{T}_{\mathrm{OPR}}$ | -25 to 85 | ${ }^{\circ} \mathrm{C}$ |

Electrical Characteristics (Vcc $=3.0 \mathrm{~V}, \mathrm{Ta}=25^{\circ} \mathrm{C}$ unless otherwise specified)

| Parameter | Symbol | Limits |  |  | Unit | Condition |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min. | Typ. | Max. |  |  |
| Operating current | Icc | - | 50 | 75 | $\mu \mathrm{A}$ | $\mathrm{V}_{\text {AEN }}=2.5 \mathrm{~V}$ |
| Standby current | $\mathrm{I}_{\text {StB }}$ | - | 5 | 10 | $\mu \mathrm{A}$ | $\mathrm{V}_{\text {AEN }}=0 \mathrm{~V}$ |
| AEN input voltage | $\mathrm{V}_{\text {AENH }}$ | 1.55 | 2 | 2.45 | V | High level input |
|  | $\mathrm{V}_{\text {AENL }}$ | 1.35 | 1.9 | 2.35 | V | Low level input |
| AEN input current | $\mathrm{I}_{\text {AEN }}$ | - | 3 | 5 | $\mu \mathrm{A}$ | $\mathrm{V}_{\text {AEN }}=3 \mathrm{~V}$ |
| GATE output voltage | $V_{\text {GATE }}$ | 10 | 13.5 | 15 | V | $\mathrm{V}_{\mathrm{cc}}=5 \mathrm{~V}$ |
|  |  | 6.6 | 9.5 | 9.9 | V | $\mathrm{V}_{\mathrm{cc}}=3.3 \mathrm{~V}$ |
|  |  | 6 | 8.5 | 9 | V | $\mathrm{V}_{\mathrm{cc}}=3 \mathrm{~V}$ |
| GATE rise time | Ton | - | 130 | 750 | $\mu \mathrm{s}$ | $\begin{aligned} & \mathrm{C}_{\mathrm{GATE}}=500 \mathrm{pF} \mathrm{~V}_{\mathrm{CC}}=3 \mathrm{~V} \\ & \mathrm{~V}_{\text {GATE }}>4 \mathrm{~V} \end{aligned}$ |
| GATE fall time | Toff | - | 18 | 60 | $\mu \mathrm{s}$ | $\begin{aligned} & \mathrm{C}_{\mathrm{GATE}}=500 \mathrm{pF} \mathrm{~V}_{\mathrm{CC}}=3 \mathrm{~V} \\ & \mathrm{~V}_{\mathrm{GATE}}<0.5 \mathrm{~V} \end{aligned}$ |
| DISC discharge resistance | $\mathrm{R}_{\text {DISC }}$ | - | 200 | 300 | $\Omega$ | $\mathrm{V}_{\text {AEN }}=0 \mathrm{~V}$ |

## Measurement Circuit



## Timing Diagram



## Typical Performance Curves



Figure 1. Operating Current
AEN Enable


Figure 3. Standby Current AEN Disable


Figure 2. Operating Current AEN Enable


Figure 4. Standby Current AEN Disable

Typical Performance Curves - continued


Figure 5. AEN Input Voltage


Figure 7. AEN Input Current


Figure 6. AEN Input Voltage


Figure 8. AEN Input Current


Figure 9. GATE Output Voltage


Figure 11. DISC ON Resistance


Figure 10. GATE Output Voltage


Figure 12. DISC ON Resistance

Typical Performance Curves - continued


Figure 13. GATE Rise Time 1


Figure 15. GATE Rise Time 2


Figure 14. GATE Rise Time 1


Figure 16. GATE Rise Time 2

Typical Performance Curves - continued


Figure 17. GATE Fall Time


Figure 19. GATE Drive Current


Figure 18. GATE Fall Time


Figure 20. GATE Drive Current

## Typical Wave Forms



Figure 21. GATE Rise / Fall Characteristics


Figure 23. GATE Fall Characteristics


Figure 22. GATE Rise Characteristics


Figure 24. GATE Switch Rise Characteristics

Typical Wave Forms - continued


Figure 25. GATE Switch Fall Characteristics


Figure 27. GATE Switch Rise Characteristics

Figure 26. GATE Switch Fall Characteristics


Figure 28. GATE Switch Fall Characteristics


Figure 29. Switch Rise / Fall Characteristics Measurement Circuit Diagram

## Application Circuit

1. Configuration of 3.3 V load switch


Figure 30. Configuration of 3.3V Load Switch
2. Configuration of 5 V load switch


Figure 31. Configuration of 5 V Load Switch
A 5 V load switch can be configured like the 3.3 V load switch. However, if the external N -channel MOSFET has low VGSS, clamp it with Zener diode and the like.
3. Configuration of low-voltage load switch


Figure 32. Configuration of Low-voltage Load Switch
Providing BD2270HFV drive power supply enables configuration of a low-voltage load switch.
4. Soft start configuration


Figure 33. Soft Start Configuration
Connecting an external capacitor to the GATE terminal of the BD2270HFV makes it possible to lengthen the rise time of the N -channel MOSFET, thus achieving reduction of the inrush current to the large-capacity capacitor mounted on the load side.

## Application Information

The system connection diagram shown here gives no guarantee to the operation of the application circuit.
When the recommended external circuit components are changed, be sure to consider adequate margins by taking into account external parts and/or IC's dispersion including not only static characteristics, but also transient characteristics.

## Functional Description

The BD2270HVF is a driver IC that uses an N-channel MOSFET as a high side load switch. This IC incorporates the following functions.

1. GATE drive

The gate drive voltage of an N-channel MOSFET is generated by a built-in charge pump in the BD2270HFV. The built-in charge pump in the BD2270HFV generates a voltage three times as high as the power supply voltage at the GATE terminal. In addition, since this IC has a built-in capacitor for the charge pump, it needs no external parts.

The charge pump operates when the AEN is set to High. When the AEN is set to Low, the GATE terminal voltage is fixed to the GND level.
2. Output discharge circuit

The output discharge circuit is enabled when the AEN is set to Low. When the discharge circuit is activated, the $200 \Omega$ (Typ.) MOSFET switch located between the DISC terminal and the GND terminal turns ON. Connecting the DISC terminal and the source side (load side) of the N-channel MOSFET makes it possible to immediately discharge capacitive load.
3. Soft start function

When the AEN terminal input voltage reaches the High level, the built-in charge pump in the BD2270HFV charges the gate of the N-channel MOSFET. The turn-on time of the N-channel MOSFET is determined by the GATE capacity. In addition, connecting a capacitor to the GATE terminal makes it possible to lengthen the rise of turn-on time of the N -channel MOSFET, thus achieving reduction of the inrush current to a large capacitive load.
4. Analog control input terminal

The AEN input of the BD2270HFV is connected to the built-in hysteresis comparator. Consequently, even analog signals can control the BD2270HFV, thus facilitating the control of the switch ON-OFF sequence.


Figure 34. Operation Timing

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## Power Dissipation

(HVSOF5)


Mounted on a $70 \mathrm{~mm} \times 70 \mathrm{~mm} \times 1.6 \mathrm{~mm}$ glass epoxy PCB
Figure 35. Power dissipation curve (Pd-Ta Curve)
I/O Equivalent Circuit

| Pin name | Pin No. | Equivalent circuit |
| :---: | :---: | :---: |
| AEN | 3 |  |

## Operational Notes

(1) Absolute Maximum Ratings

Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings
(2) Recommended operating conditions

These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.
(3) Reverse connection of power supply

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply terminals.
(4) Power supply line

Design the PCB layout pattern to provide low impedance ground and supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.
(5) Ground Voltage

The voltage of the ground pin must be the lowest voltage of all pins of the IC at all operating conditions. Ensure that no pins are at a voltage below the ground pin at any time, even during transient condition.
(6) Short between pins and mounting errors

Be careful when mounting the IC on printed circuit boards. The IC may be damaged if it is mounted in a wrong orientation or if pins are shorted together. Short circuit may be caused by conductive particles caught between the pins.
(7) Operation under strong electromagnetic field

Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.
(8) Testing on application boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.
(9) Regarding input pins of the IC

This monolithic IC contains $\mathrm{P}+$ isolation and P substrate layers between adjacent elements in order to keep them isolated. $P-N$ junctions are formed at the intersection of the $P$ layers with the $N$ layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.
Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the $P$ substrate) should be avoided.

## Resistor



Transistor (NPN)


Pin B


Other adjacent elements
Example of monolithic IC structure
(10) GND wiring pattern

When using both small-signal and large-current GND traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the GND traces of external components do not cause variations on the GND voltage. The power supply and ground lines must be as short and thick as possible to reduce line impedance.
(11) External Capacitor

When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.
(12) Thermal consideration

Use a thermal design that allows for a sufficient margin by taking into account the permissible power dissipation (Pd) in actual operating conditions. Consider Pc that does not exceed Pd in actual operating conditions ( $\mathrm{Pc} \geq \mathrm{Pd}$ ).

```
Package Power dissipation
Power dissipation
\[
\begin{aligned}
& : \mathrm{Pd}(\mathrm{~W})=(\mathrm{Tjmax}-\mathrm{Ta}) / \theta \text { ja } \\
& : \mathrm{Pc}(\mathrm{~W})=(\mathrm{Vcc}-\mathrm{Vo}) \times \mathrm{lo}+\mathrm{Vcc} \times \mathrm{lb}
\end{aligned}
\]
```

(Tjmax : Maximum junction temperature $=150^{\circ} \mathrm{C}, \mathrm{Ta}$ : Peripheral temperature $\left[^{\circ} \mathrm{C}\right]$, $\theta$ ja : Thermal resistance of package-ambience $\left[{ }^{\circ} \mathrm{C} / \mathrm{W}\right], \mathrm{Pd}:$ Package Power dissipation [W], Pc : Power dissipation [W], Vcc : Input Voltage, Vo : Output Voltage, Io : Load, Ib : Bias Current

## Ordering Information



## Marking Diagram

HVSOF5(TOP VIEW)


| Part Number | Part Number Marking |
| :---: | :---: |
| BD2270HFV | AA |

Physical Dimension Tape and Reel Information


## Revision History

| Date | Revision | Changes |
| :---: | :---: | :--- |
| 13.Mar.2013 | 001 | New Release |
| 21.Feb.2014 | 002 | Delete sentence "and log life cycle" in General Description and Futures (page 1). <br> Change "Industrial Applications" to "Industrial Equipment" in Applications (page 1). <br> Applied new style ("title", "Ordering Information" and "Physical Dimension Tape and Reel <br> Information"). |

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(Note1) Medical Equipment Classification of the Specific Applications

| JAPAN | USA | EU | CHINA |
| :---: | :---: | :---: | :---: |
| CLASSIII | CLASSIII | CLASS II b | CLASSIII |
|  |  | CLASSIII |  |

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[^0]:    * To turn ON the power supply ( $\mathrm{V}_{\mathrm{cc}}, \mathrm{VIN}$ _switch $)$, set the AEN to Low.

