Over-Sampling ADC Multi-Application

DESCRIPTION

Demonstration circuit 2390A is a general-purpose test platform for prototyping and evaluating some of the key applications for the LTC2500 family of high resolution, oversampling ADCs. Assembly type A includes two LTC®2500-32, 32-bit oversampling ADCs with configurable digital filters, two LTC1668 16-bit, 50Msps DACs, analog signal conditioning, and clock generation. (Other dash options are reserved for future use). All power for basic experiments is taken from the host FPGA board. The digital interface is an HSMC (high speed mezzanine connector), which is compatible with the Altera Cyclone 5 SoCkit and other Altera FPGA evaluation boards that support 3.3V CMOS I/O.

This demo manual covers the basic functionality of DC2390. Additional experiments and applications are documented elsewhere.

Design files for this circuit board are available at http://www.linear.com/demo/DC2390A

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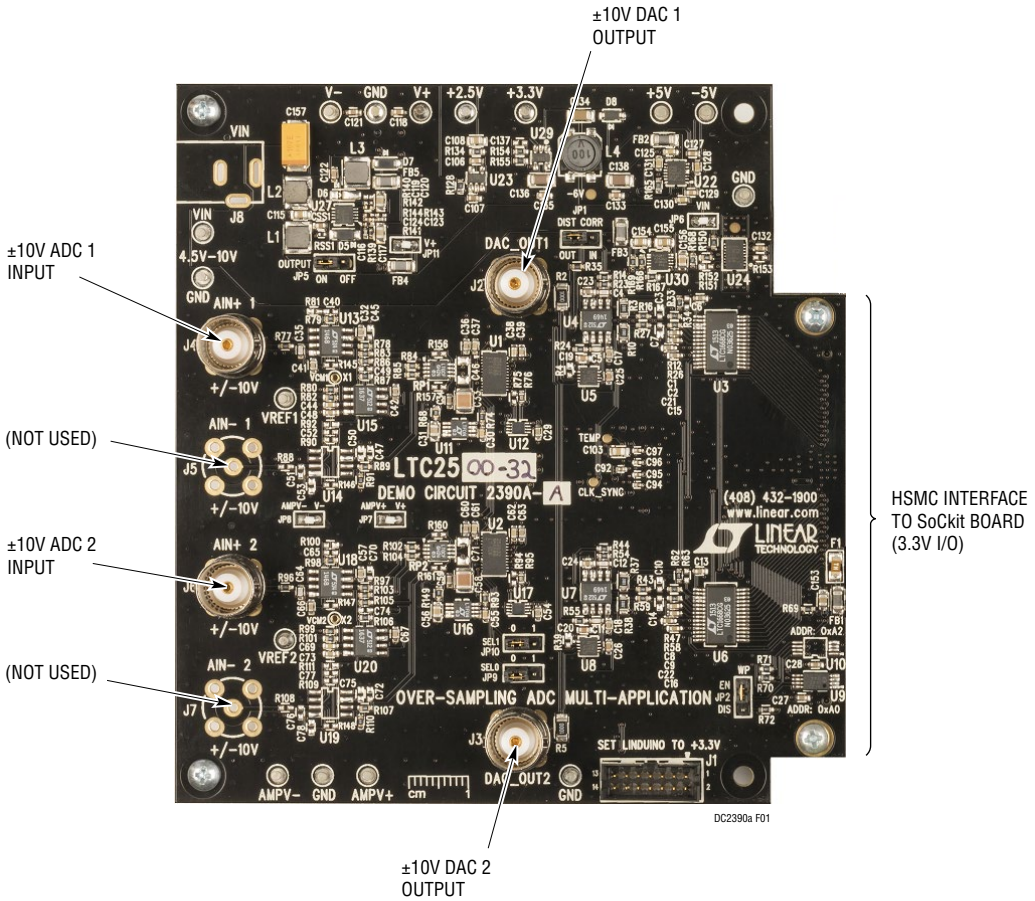

Figure 1. Basic Connections

QUICK START PROCEDURE

1) Prepare the SoCkit board and SD card image as described here:

   http://www.linear.com/solutions/7704

2) Install the LinearLabTools software package from:

   http://www.linear.com/linearlabtools

3) Follow the procedure for installing Python, and verify that the check_linear_lab_tools_python_install.py script executes properly.

4) Carefully mount the DC2390 to the SoCkit board via the HSMC connector, using 5mm standoffs between boards. Tighten mounting screws.

5) Connect the SoCkit board to a network with a DHCP server, or connect directly to host computer's Ethernet jack or USB-Ethernet adapter.

6) Connect DAC_OUT1 BNC jack to the AIN+ 1 BNC and the DAC_OUT2 to AIN+ 2 using short (30cm max) cables.

7) Power up the SoCkit board using the 12V adapter. The DC2390 is powered by the HSMC connector by default, no other power is necessary. After approximately 30 seconds, the FPGA_CONF_D LED will illuminate, and the board's IP address will show in the LCD display.

8) Open Spyder (the Anaconda Python Debugger) click file -> open, and navigate to the location where LinearLabTools is installed. Open this script:

   \python\llt\app_examples\ltc2500_family\ and open DC2390_full_datapath_test.py.

9) Click Run -> Configure, and enter the IP address from the SoCkit LCD screen in the command line argument box. Click Run.

10) If running the script from the command line, append the IP address to the command:

    python DC2390_full_datapath_test.py 10.54.6.123

    (Replace the 10.54.6.123 with the actual IP address shown on the LCD screen.)

11) If the script reports an incorrect FPGA bitfile, log into the SoCkit board using an SSH client such as Putty on Windows, or directly from a terminal in Mac or Linux. User name is "sockit", password is "sockit". Run these commands:

    cd fpga_bitfiles

    rm default.rbf

    ln --symbolic DC2390_ABCD_XXXX.rbf default.rbf

    (where XXXX is the highest number present in the directory, 1240 as of this publication)

    sudo program_fpga.sh default.rbf

    (enter "sockit" for the password)

    This only needs to be done once, the correct FPGA bitfile will be loaded automatically the next time the board boots.

The script will run through a set of diagnostic tests:

1) A basic sinewave capture, using a digital sinewave generator as the data source to the LTC1668.

2) A test of the arbitrary waveform generator, using a counter as the address to a lookup table as the data source to the LTC1668.

3) A single-shot run through the lookup table, triggered by the start of data capture.

4) NCO data as the address to the lookup table (distortion correction mode).

5) A test of the PID controller, with two different sets of PID constants.

These tests are described in more detail in the Python script comments. Typical plots are shown in Figures 2, 3, 4, 5, and 6.

QUICK START PROCEDURE

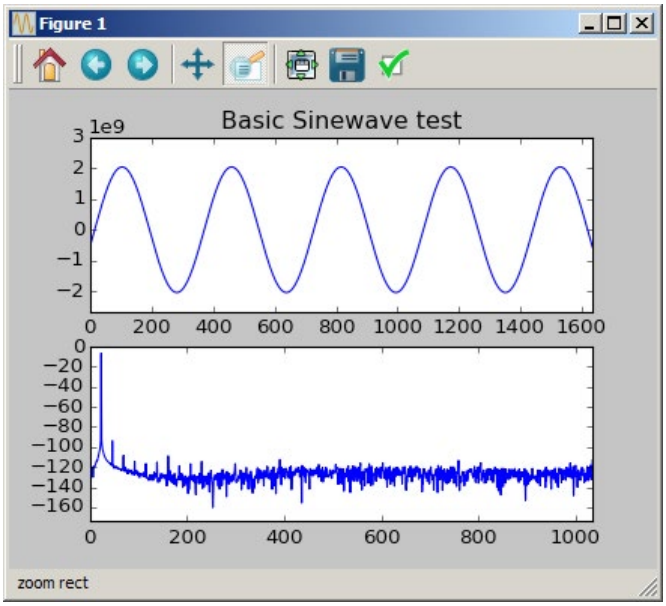

Figure 2

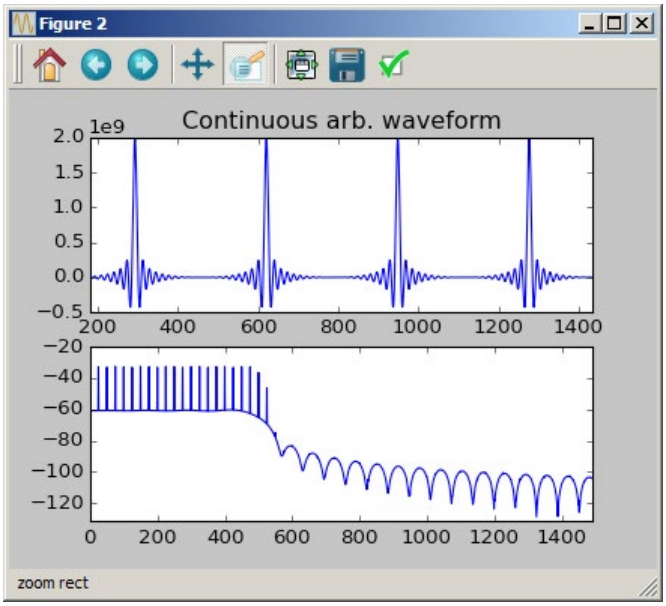

Figure 3

QUICK START PROCEDURE

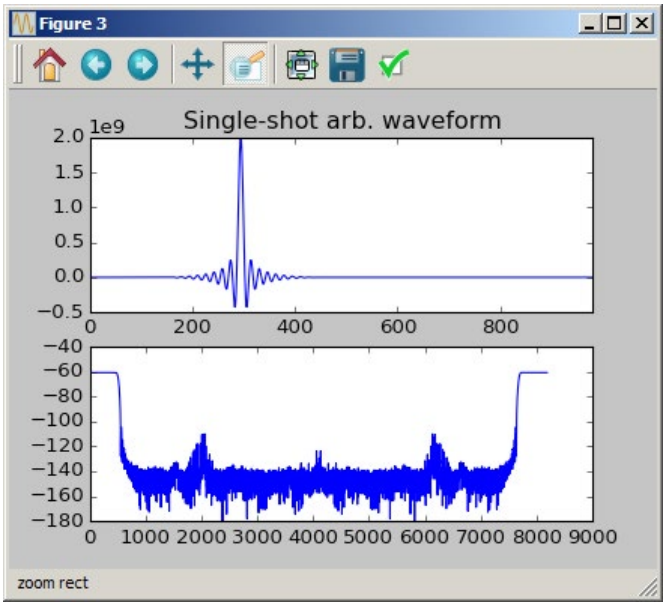

Figure 4

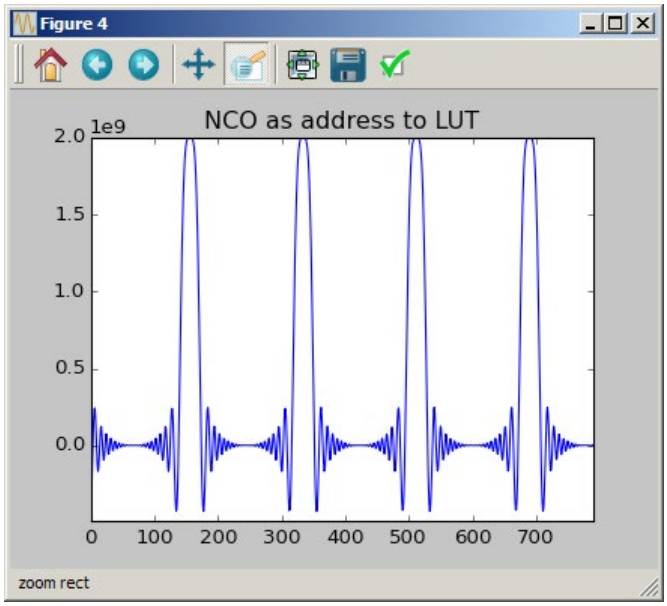

Figure 5

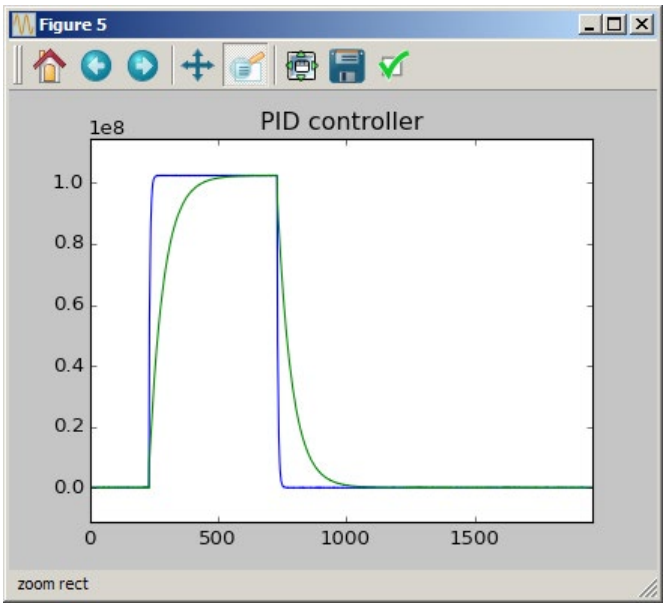

Figure 6

EXTERNAL CONNECTIONS

Connections

P1: (Reverse side of board) - HSMC digital interface. 3.3V CMOS digital signals to and from the DACs and ADCs, as well as auxiliary signals. Also provides 3.3V and 12V power from the FPGA board to the DC2390.

J4, J6 : AIN+1, AIN+2. ±10V analog inputs. Onboard signal conditioning converts the ±10V, single-ended input to a ±5V, fully-differential signal at the ADC inputs.

J2, J3: DAC_OUT1, DAC_OUT2. ±10V analog outputs from the onboard DACs.

J1: QuikEval™ master port with 3.3V logic levels. Allows control of auxiliary QuikEval compatible demo boards for various experiments by emulating a Linduino (DC2026) controller.

Jumpers

JP5: Boost / Inverting regulator control. Enables / disables the onboard ±15V supplies. Default: ON

JP9, JP10: SEL0, SEL1 - configures downsample factor (DF) of certain LTC2500 family devices that are not configured serially (such as LTC2508, LTC2512) which may be included on future assembly types. Must be set to 0, 0 for DC2390A-A, which is populated with the LTC2500-32.

JP2: EEPROM write protection for onboard ID / general-purpose EEPROMs. Default: EN

JP1: Distortion Correction. Sums 1/128 of the output from DAC_OUT2 into DAC_OUT1. For experiments involving correction of DAC_OUT1's distortion or increasing resolution. Default: OUT

JP11: V^+ Connection. Allows the boost output from the boost / inverting converter to be disconnected from the circuit if V^+ is driven from an external supply. Default: Jumper soldered in.

JP6: V_{IN} Connection. Allows the 12V supply from the HSMC connector to be disconnected such that V_{IN} can be supplied externally. Default: Jumper soldered in.

JP7, JP8: $AMPV^+$, $AMPV^-$ connections. Allows the supply for the ADC signal conditioning amplifiers to be supplied externally. Default: Jumpers soldered in.

Turrets

V^+, GND, V^-: ±15V supply. Measure the output of the onboard boost/ inverting converters at these points. May be powered externally by setting JP5 to OFF and removing JP11.

$AMPV^+$, GND, $AMPV^-$: Supply voltages for ADC front-end amplifiers. May be powered externally by removing JP7, JP8.

V_{IN}, GND: Main 12V supply, switched output from onboard hot swap controller. May be supplied externally by removing JP6.

+2.5V: Regulated 2.5V supply for ADCs. Measure only, do not apply power.

+3.3V: Supply for onboard clock circuitry and ADC logic. Normally supplied from the FPGA board via P1. May be powered externally by removing F1.

+5V, –5V: Regulated supplies for DAC circuitry. Measure only, do not apply power.

GND: Two extra ground turrets can be used for power or measurement connections.

VREF1, VREF2: Onboard 5V reference outputs. Measure only, do not apply power.

MODIFICATION GUIDELINES

DC2390 is designed to be easily modified to test various application circuits. This section details the operation of several of the board's subcircuits, with guidelines on possible modifications. Figure 7 shows a simplified block diagram of the subcircuits for reference.

ADC SIGNAL CONDITIONING

The default ADC signal conditioning circuit accepts a ±10V, single-ended input. Refer to Design Note 1032 for details on the operation of this circuit.

Differential ±10V inputs

This circuit can be converted to a differential ±10V input by making the following modifications:

Remove R91, R110

Install zero Ω in R90, R109

Install LT1468CS8 in U14, U19

Install 49.9Ω in R88, R108

Install 3300pF in C51, C76

Basic Buffered Inputs

Another useful configuration is a basic buffer. This allows the testing of external signal conditioning circuits (gain stages, level-shifting, filtering, etc.) without considering their ability to drive the switched-capacitor inputs of the ADC. Make the following modifications:

Disconnect AMPV$^+$, AMPV$^-$ supplies by removing JP7, JP8.

Remove U18, U13.

Install LT6202CS8 in U13, U14, U18, U19.

Install 0.1µF, 50V in C50, C53, C75, C78

Remove R91, R110

Install zero Ω in R90, R109

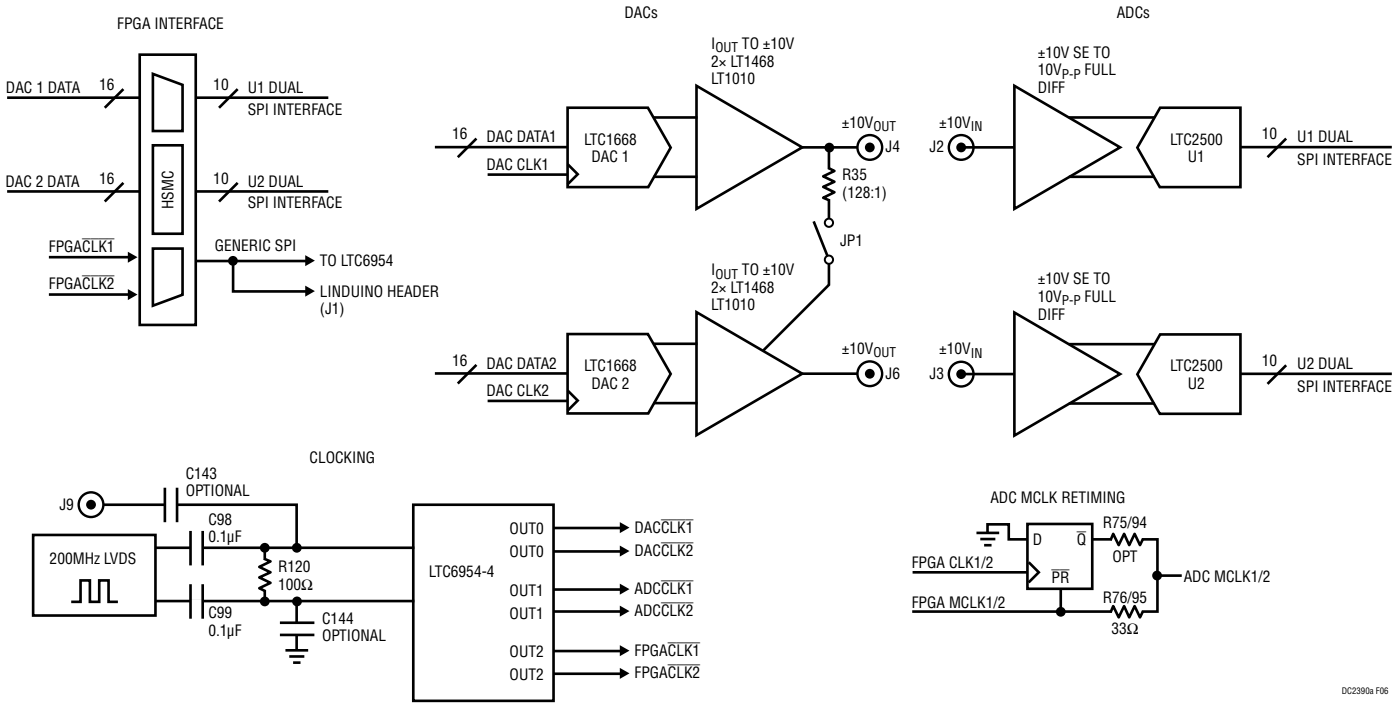

Figure 7. DC2390 Circuit Block Diagram

MODIFICATION GUIDELINES

Install 49.9Ω in R88, R108

Install 3300pF in C51, C76

Remove R84, R85, R102, R104

Install zero Ω in R156, R157, R160, R161

Install 6800pF, NPO type, in C139, C140, C141, C142

CLOCKING

An onboard 200MHz clock feeds an LTC6954 low phase noise, triple output clock distribution divider/driver. The default test script sets the output frequencies to 50MHz, with a three cycle delay on the DAC clock in order to meet the hold time requirement.

An external clock may be provided to J9 (SMA, not installed) by removing C98, C99 and installing 0.1µF capacitors in C143, C144 positions. The externally applied clock must have a signal level of 0.2 to 1.5V_{P-P}. Refer to the LTC6954 data sheet for details on setting divide ratios and delays.

By default, the ADC MCLK signals originate from the FPGA. These may be retimed by the LTC6954 by removing R76, R95 and installing R75, R94. (This requires modification of the FPGA code.)

POWER

The default power configuration is to draw 3.3V and 12V power from the host FPGA board through the HSMC connector. Onboard regulators provide +15V, –15V, +5V, –5V and 2.5V for the various subcircuits.

Power for the front end amplifiers (U13, U14, U18, U19) can be disconnected from the ±15V supplies by removing JP7, JP8. Power can then be connected to the $AMPV^+$, GND, $AMPV^-$ turret posts at the lower edge of the board.

An external, low noise ±15V supply may be connected by removing JP11 and setting JP5 to the OFF position.

An external 12V V_{IN} supply may be applied to J8 (not installed) by removing JP6 (which disconnects the 12V supply from the HSMC connector.)

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