



PMCM6501UPE

20 V, P-channel Trench MOSFET

3 July 2017

Product data sheet

1. General description

P-channel enhancement mode Field-Effect Transistor (FET) in a 6 bumps Wafer Level Chip-Size Package (WLCSP) using Trench MOSFET technology.

2. Features and benefits

- Low threshold voltage
- Ultra small package: 0.98 x 1.48 x 0.35 mm
- Trench MOSFET technology
- ElectroStatic Discharge (ESD) protection > 2 kV HBM

3. Applications

- Battery switch
- High-speed line driver
- High-side loadswitch
- Switching circuits

4. Quick reference data

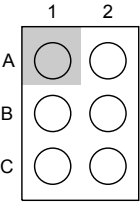
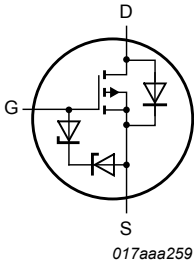
Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j = 25\text{ °C}$		-	-	-20	V
V_{GS}	gate-source voltage			-8	-	8	V
I_D	drain current	$V_{GS} = -4.5\text{ V}; T_{amb} = 25\text{ °C}; t \leq 5\text{ s}$	[1]	-	-	-7.3	A
Static characteristics							
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = -4.5\text{ V}; I_D = -3\text{ A}; T_j = 25\text{ °C}$		-	22	30	mΩ

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and mounting pad for drain 6 cm²

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
A1	G	gate	 Transparent top view WLCSP6 (WLCSP6_3-2)	 017aaa259
A2	S	source		
B1	S	source		
B2	S	source		
C1	D	drain		
C2	D	drain		

6. Ordering information

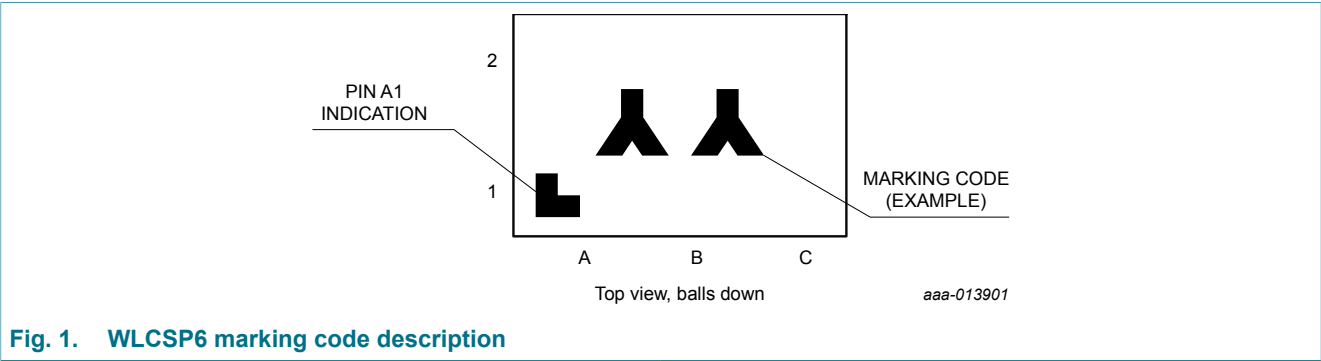
Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PMCM6501UPE	WLCSP6	wafer level chip-size package; 6 bumps (3 x 2)	WLCSP6_3-2

7. Marking

Table 4. Marking codes

Type number	Marking code
PMCM6501UPE	AF



8. Limiting values

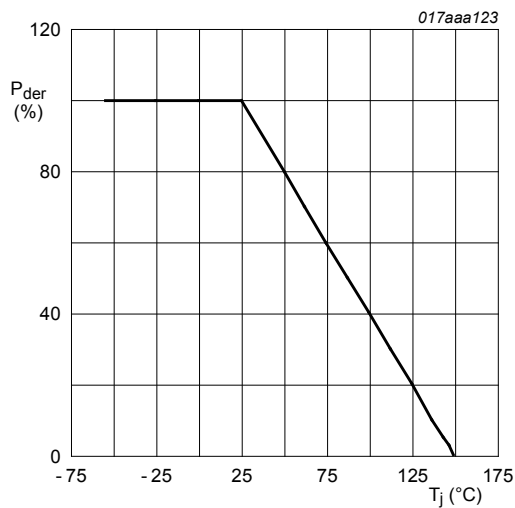
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	$T_j = 25\text{ }^{\circ}\text{C}$		-	-20	V
V_{GS}	gate-source voltage			-8	8	V
I_D	drain current	$V_{GS} = -4.5\text{ V}; T_{amb} = 25\text{ }^{\circ}\text{C}; t \leq 5\text{ s}$	[1]	-	-7.3	A
		$V_{GS} = -4.5\text{ V}; T_{amb} = 25\text{ }^{\circ}\text{C}$	[1]	-	-5.6	A
		$V_{GS} = -4.5\text{ V}; T_{amb} = 100\text{ }^{\circ}\text{C}$	[1]	-	-3.5	A
I_{DM}	peak drain current	$T_{amb} = 25\text{ }^{\circ}\text{C}$; single pulse; $t_p \leq 10\text{ }\mu\text{s}$		-	-22	A
P_{tot}	total power dissipation	$T_{amb} = 25\text{ }^{\circ}\text{C}$	[2]	-	556	mW
			[1]	-	1.3	W
		$T_{sp} = 25\text{ }^{\circ}\text{C}$		-	12.5	W
T_j	junction temperature			-55	150	$^{\circ}\text{C}$
T_{amb}	ambient temperature			-55	150	$^{\circ}\text{C}$
T_{stg}	storage temperature			-65	150	$^{\circ}\text{C}$
I_S	source current	$T_{amb} = 25\text{ }^{\circ}\text{C}$	[1]	-	-1.3	A

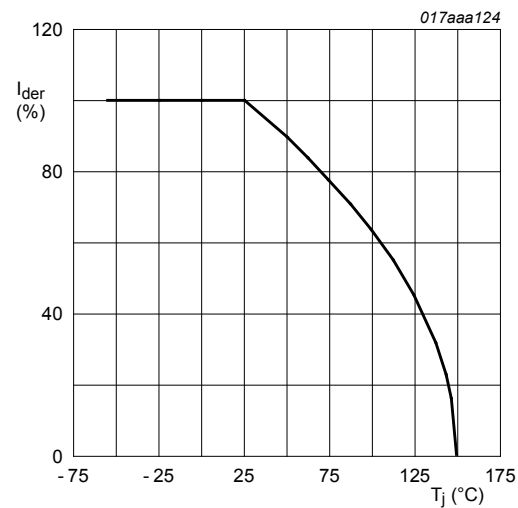
[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and mounting pad for drain 6 cm^2

[2] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper; tin-plated and standard footprint.



$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}\text{C})}} \times 100\%$$

Fig. 2. Normalized total power dissipation as a function of junction temperature



$$I_{der} = \frac{I_D}{I_{D(25^{\circ}\text{C})}} \times 100\%$$

Fig. 3. Normalized continuous drain current as a function of junction temperature

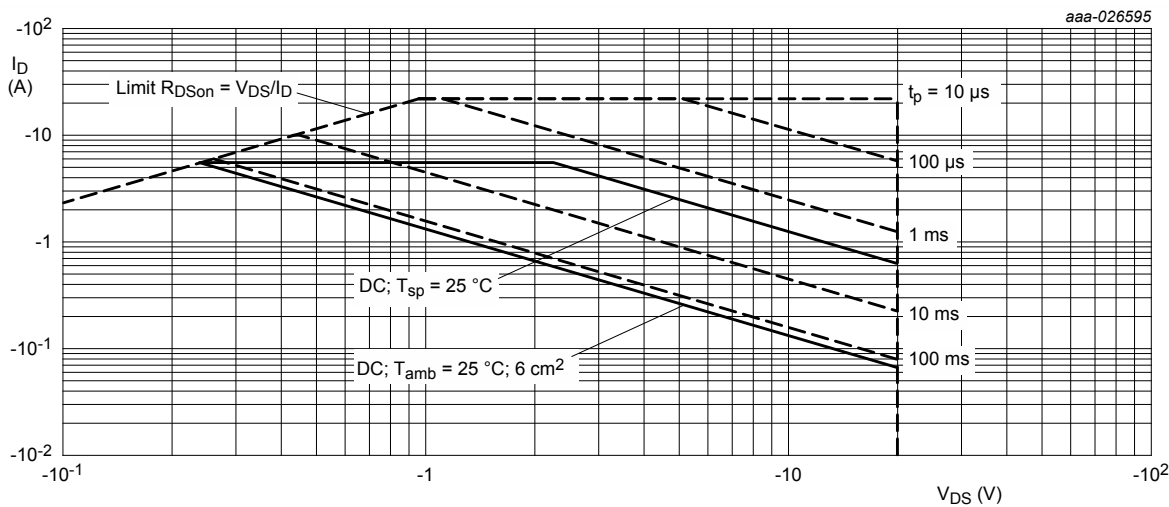


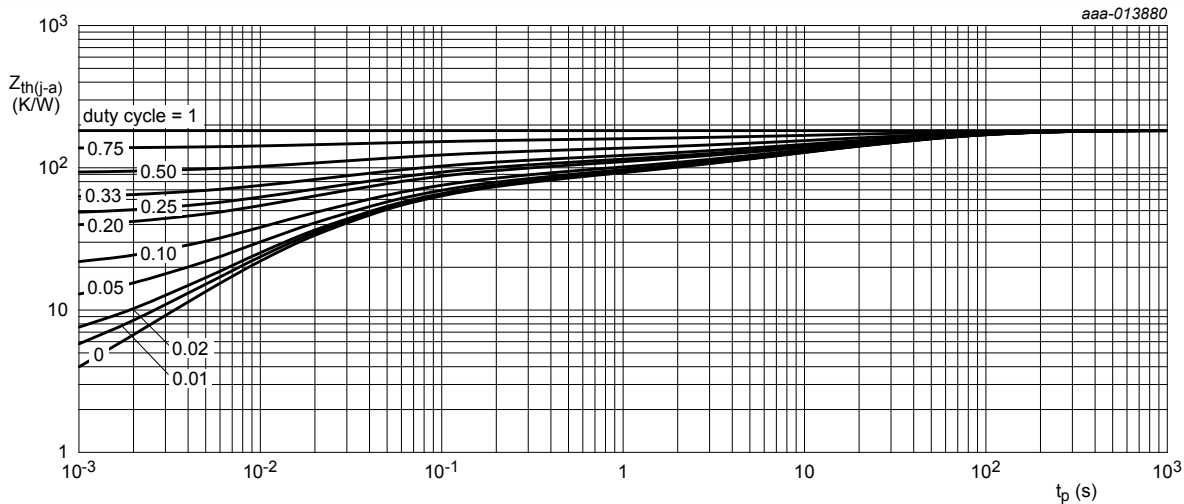
Fig. 4. Safe operating area; junction to ambient; continuous and peak drain currents as a function of drain-source voltage

9. Thermal characteristics

Table 6. Thermal characteristics

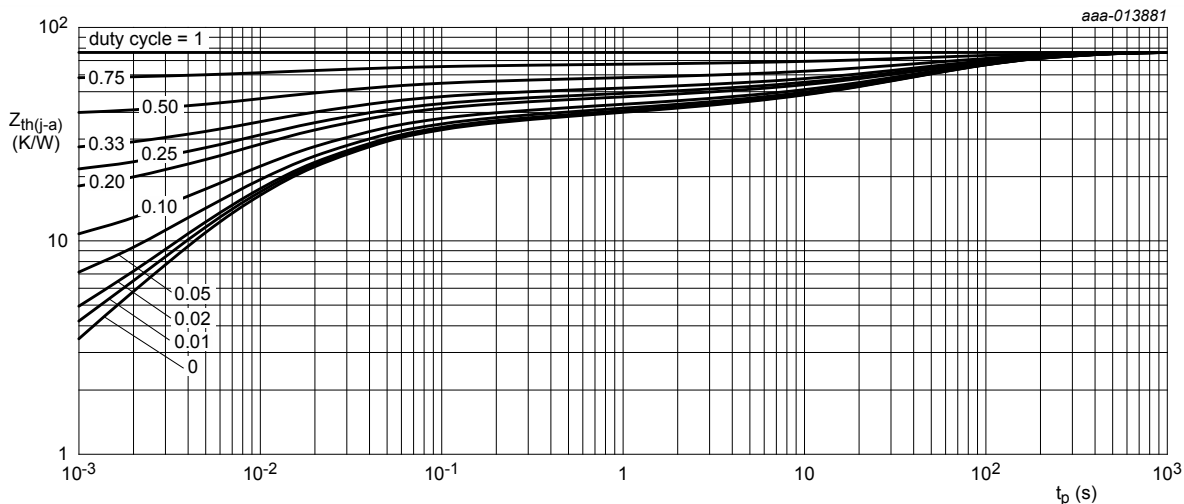
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
R _{th(j-a)}	thermal resistance from junction to ambient	in free air	[1]	-	180	225	K/W
			[2]	-	65	85	K/W
			[3]	-	75	95	K/W
		t ≤ 5 s	[3]	-	45	55	K/W
R _{th(j-sp)}	thermal resistance from junction to solder point			-	5	10	K/W

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single sided-copper; tin-plated and standard footprint.
[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated and mounting pad for drain, 4 layer, 1 cm²
[3] Device mounted on an FR4 PCB, single-sided copper, tin-plated and mounting pad for drain 6 cm².



FR4 PCB, standard footprint

Fig. 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values



FR4 PCB, mounting pad for drain 6 cm²

Fig. 6. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
V _{(BR)DSS}	drain-source breakdown voltage	I _D = -250 μA; V _{GS} = 0 V; T _j = 25 °C		-20	-	-	V
V _{GSth}	gate-source threshold voltage	I _D = -250 μA; V _{DS} = V _{GS} ; T _j = 25 °C		-0.4	-0.6	-0.9	V
I _{DSS}	drain leakage current	V _{DS} = -20 V; V _{GS} = 0 V; T _j = 25 °C		-	-	-1	μA
I _{GSS}	gate leakage current	V _{GS} = 8 V; V _{DS} = 0 V; T _j = 25 °C		-	-	10	μA
		V _{GS} = -8 V; V _{DS} = 0 V; T _j = 25 °C		-	-	-10	μA
		V _{GS} = 4.5 V; V _{DS} = 0 V; T _j = 25 °C		-	-	1	μA
		V _{GS} = -4.5 V; V _{DS} = 0 V; T _j = 25 °C		-	-	-1	μA
		V _{GS} = 2.5 V; V _{DS} = 0 V; T _j = 25 °C		-	-	200	nA
		V _{GS} = -2.5 V; V _{DS} = 0 V; T _j = 25 °C		-	-	-200	nA
R _{DSon}	drain-source on-state resistance	V _{GS} = -4.5 V; I _D = -3 A; T _j = 25 °C		-	22	30	mΩ
		V _{GS} = -4.5 V; I _D = -3 A; T _j = 150 °C		-	30	43	mΩ
		V _{GS} = -2.5 V; I _D = -3 A; T _j = 25 °C		-	28	44	mΩ
		V _{GS} = -1.8 V; I _D = -1 A; T _j = 25 °C		-	38	79	mΩ
g _{fs}	forward transconductance	V _{DS} = -6 V; I _D = -3 A; T _j = 25 °C		-	22	-	S
R _G	gate resistance	f = 1 MHz		-	15	-	Ω
Dynamic characteristics							
Q _{G(tot)}	total gate charge	V _{DS} = -10 V; I _D = -3 A; V _{GS} = -4.5 V; T _j = 25 °C		-	19.1	29	nC
Q _{GS}	gate-source charge			-	1.9	-	nC
Q _{GD}	gate-drain charge			-	5.4	-	nC
C _{iss}	input capacitance	V _{DS} = -10 V; f = 1 MHz; V _{GS} = 0 V; T _j = 25 °C		-	1420	-	pF
C _{oss}	output capacitance			-	210	-	pF
C _{rss}	reverse transfer capacitance			-	190	-	pF
t _{d(on)}	turn-on delay time	V _{DS} = -10 V; I _D = -5.6 A; V _{GS} = -4.5 V; R _{G(ext)} = 6 Ω; T _j = 25 °C		-	6	-	ns
t _r	rise time			-	35	-	ns
t _{d(off)}	turn-off delay time			-	105	-	ns
t _f	fall time			-	55	-	ns
Source-drain diode							
V _{SD}	source-drain voltage	I _S = -1.2 A; V _{GS} = 0 V; T _j = 25 °C		-	-0.7	-1.2	V

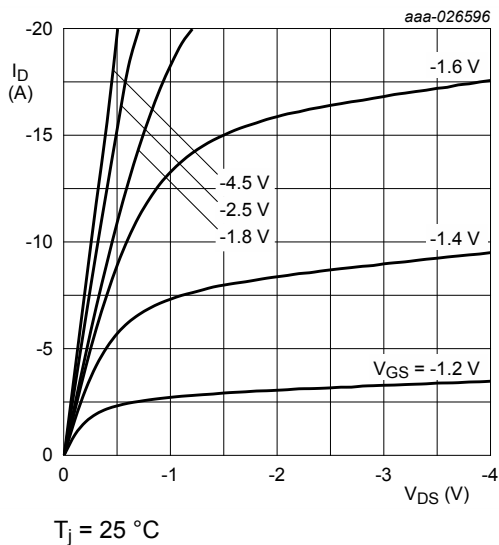


Fig. 7. Output characteristics: drain current as a function of drain-source voltage; typical values

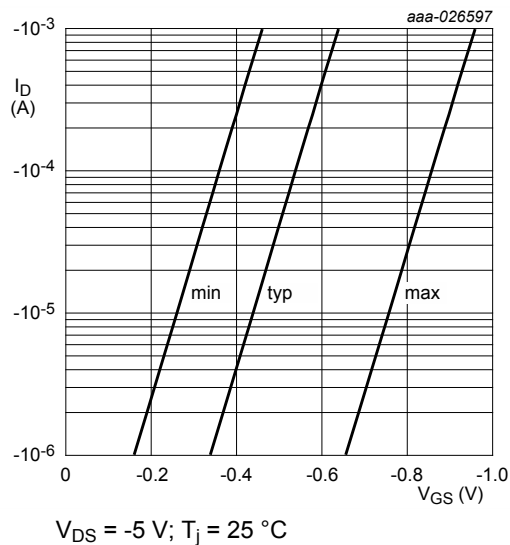


Fig. 8. Sub-threshold drain current as a function of gate-source voltage

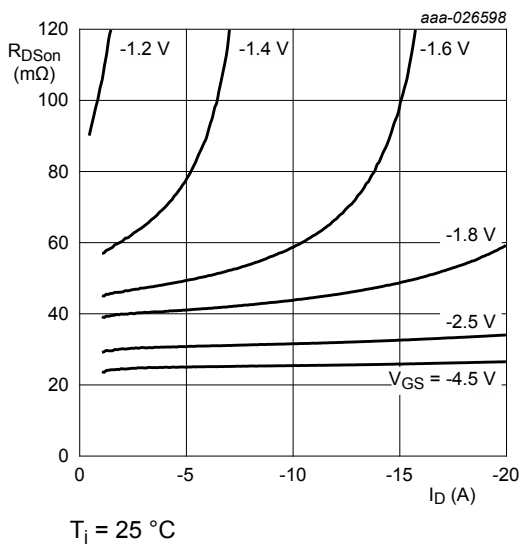


Fig. 9. Drain-source on-state resistance as a function of drain current; typical values

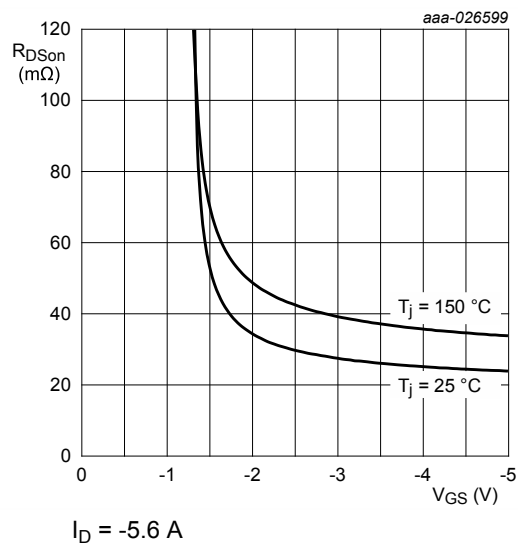


Fig. 10. Drain-source on-state resistance as a function of gate-source voltage; typical values

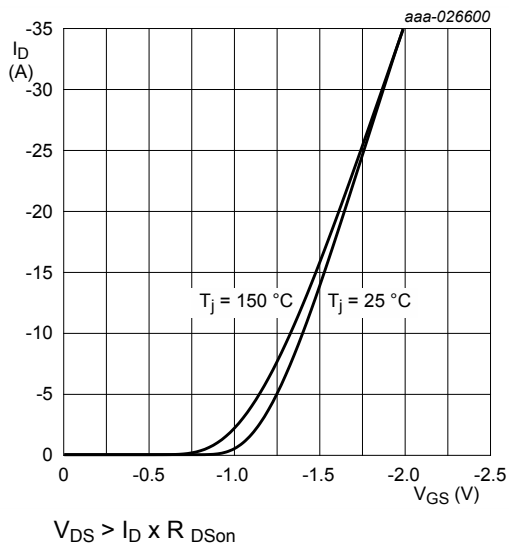


Fig. 11. Transfer characteristics: drain current as a function of gate-source voltage; typical values

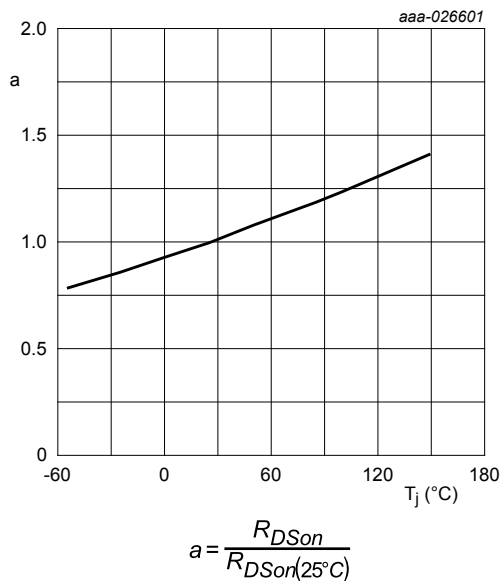


Fig. 12. Normalized drain-source on-state resistance as a function of junction temperature; typical values

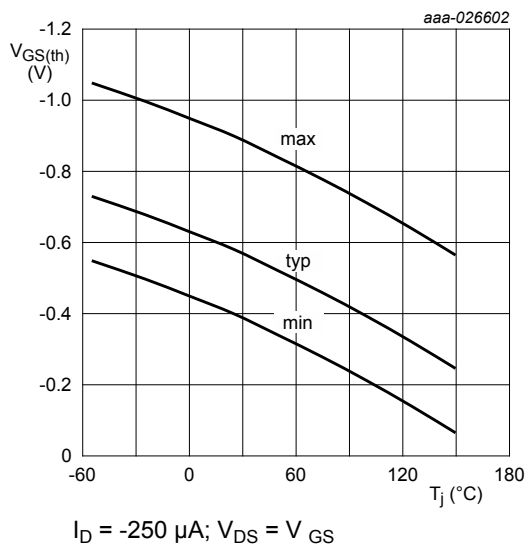


Fig. 13. Gate-source threshold voltage as a function of junction temperature

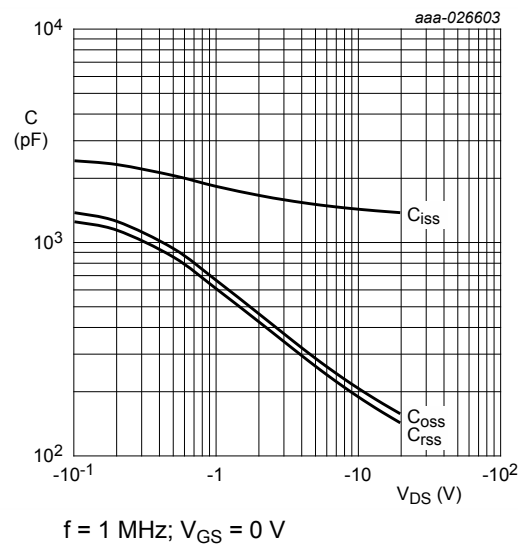


Fig. 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

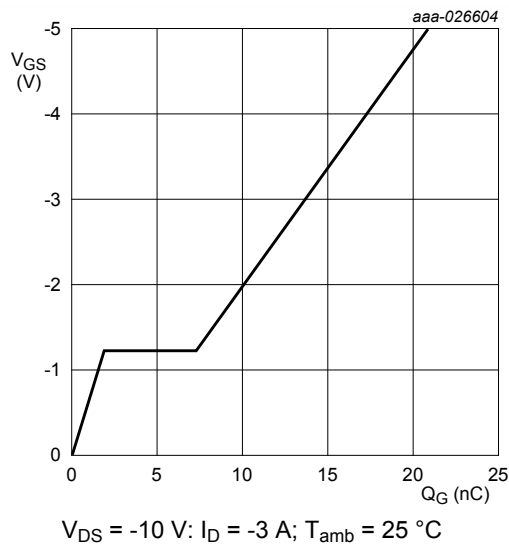


Fig. 15. Gate-source voltage as a function of gate charge; typical values

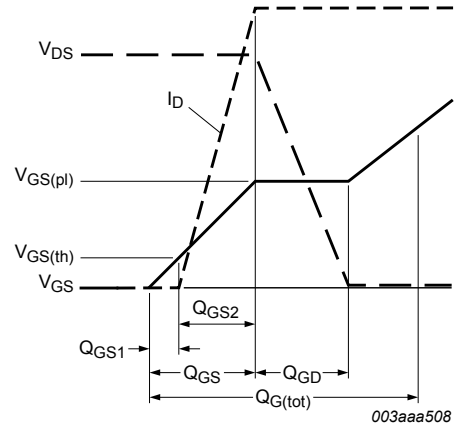


Fig. 16. Gate charge waveform definitions

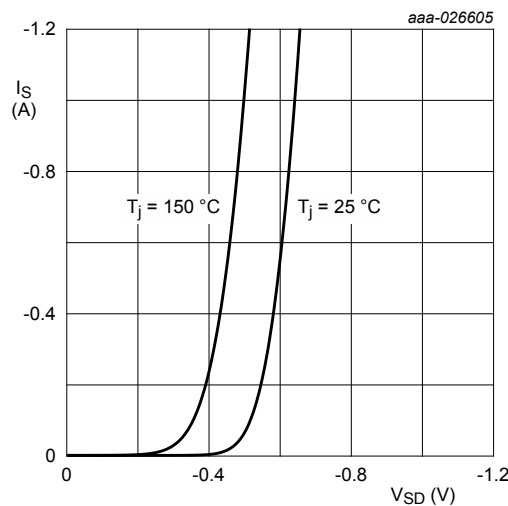


Fig. 17. Source current as a function of source-drain voltage; typical values

11. Test information

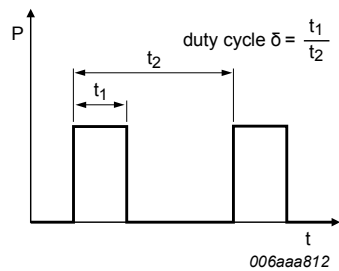


Fig. 18. Duty cycle definition

12. Package outline

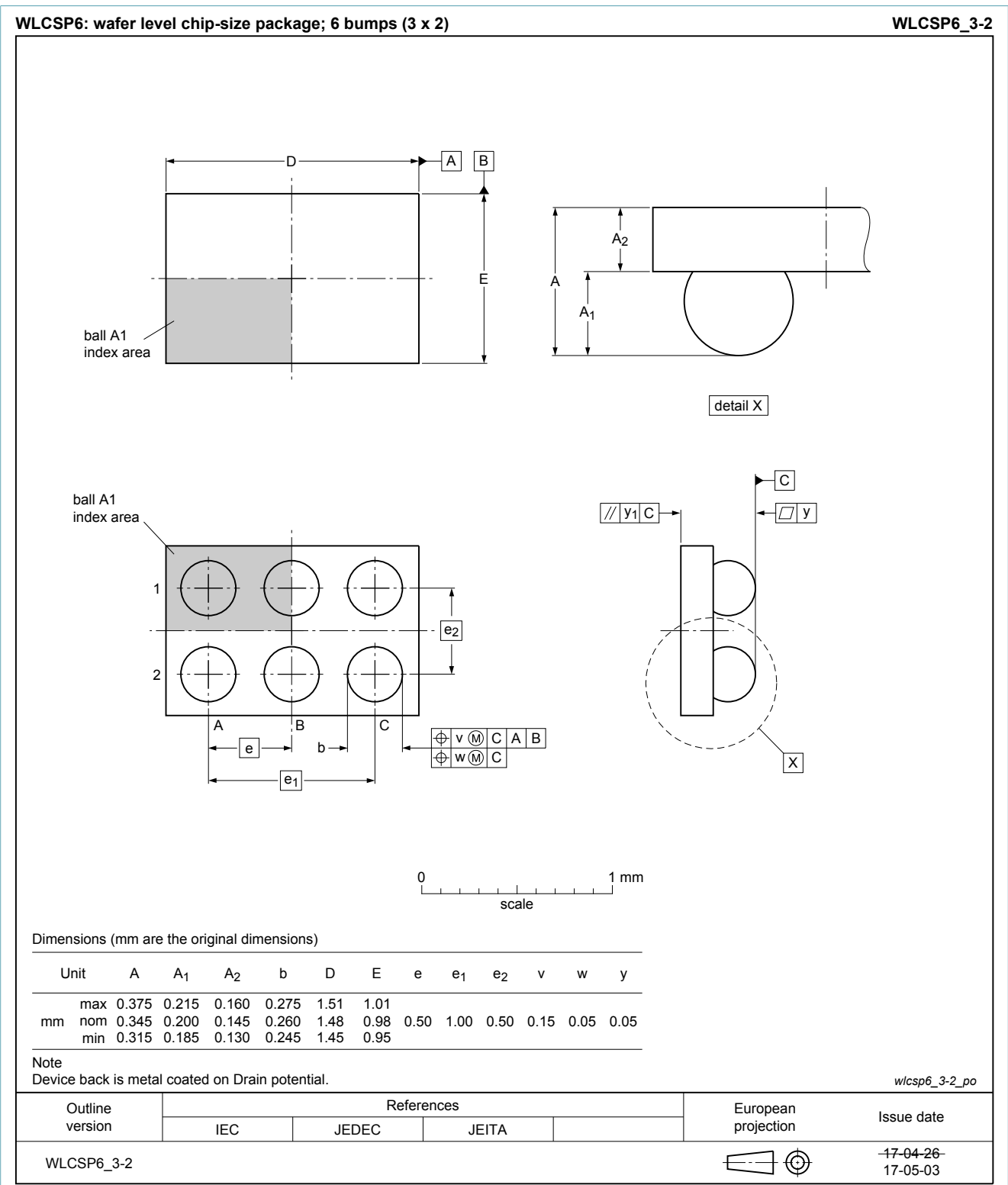
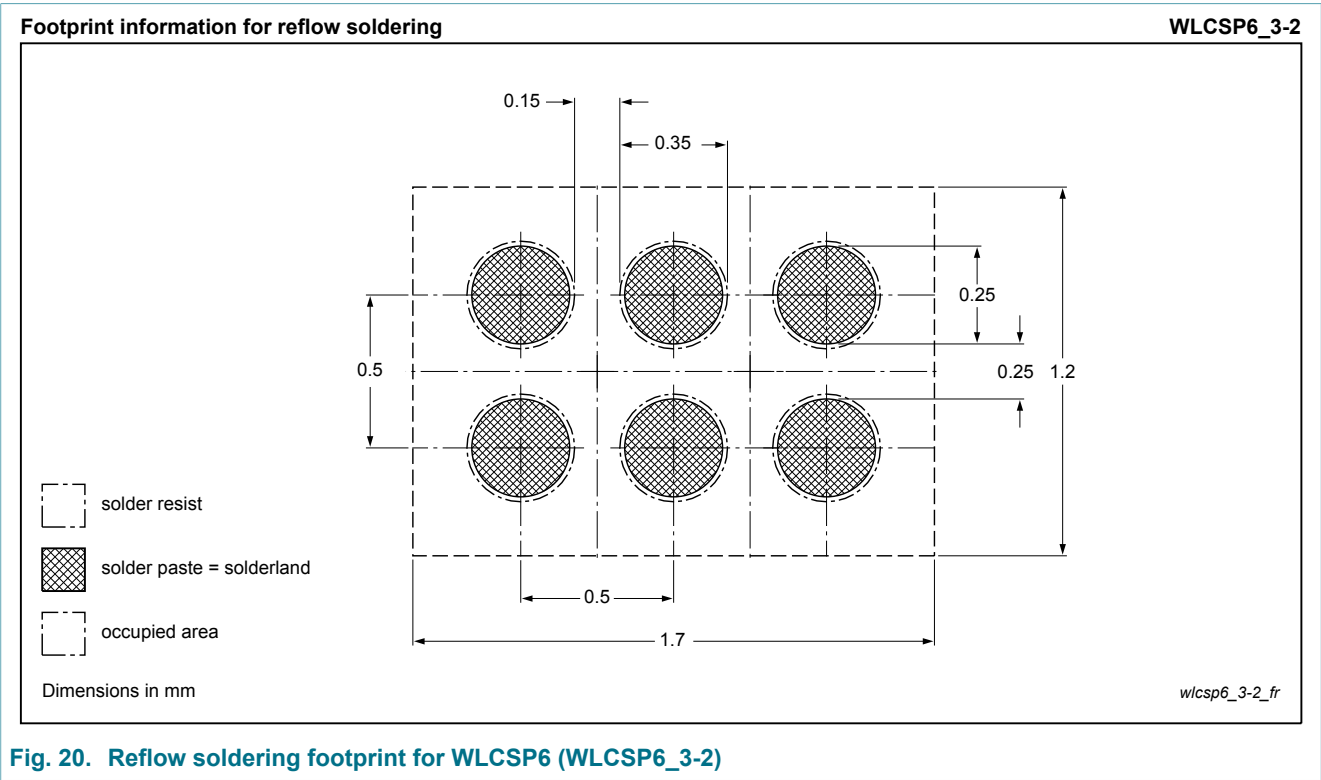


Fig. 19. Package outline WLCSP6 (WLCSP6_3-2)

13. Soldering



14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PMCM6501UPE v.1	20170703	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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16. Contents

1. General description..... 1

2. Features and benefits..... 1

3. Applications..... 1

4. Quick reference data..... 1

5. Pinning information.....2

6. Ordering information.....2

7. Marking.....2

8. Limiting values..... 3

9. Thermal characteristics..... 4

10. Characteristics.....6

11. Test information..... 9

12. Package outline..... 10

13. Soldering..... 11

14. Revision history.....12

15. Legal information..... 13

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Date of release: 3 July 2017

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Web: <http://oceanchips.ru/>

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