AS1117

64 LED Driver for Mobile Applications with Error Detection

1 General Description

The AS1117 is a compact LED driver for 64 single LEDs or 8 digits of 7-segments. The devices can be programmed via an I²C compatible 2-wire interface. Every segment can be individually addressed and updated separately. Only one external resistor (R_{SET}) is required to set the current. LED brightness can be controlled by analog or digital means.

The devices include an integrated BCD code-B/HEX decoder, multiplex scan circuitry, segment and display drivers, and a 64-bit memory. Internal memory stores the shift register settings, eliminating the need for continuous device reprogramming.

Table 1. Available Products

Devices	RESET Input	Interfaces
AS1115	no	I²C
AS1116	no	SPI
AS1117	yes	I²C
AS1118	yes	SPI

Additionally the AS1117 offers a detailed error diagnostic mode for easy and fast production testing in critical applications. The AS1117 features a low shutdown current of typically 200nA, and an operational current of typically 350µA. The number of digits can be programmed, the devices can be reset by software, and an external clock is also supported.

The device is available in a TQFN(4x4)-24 package.

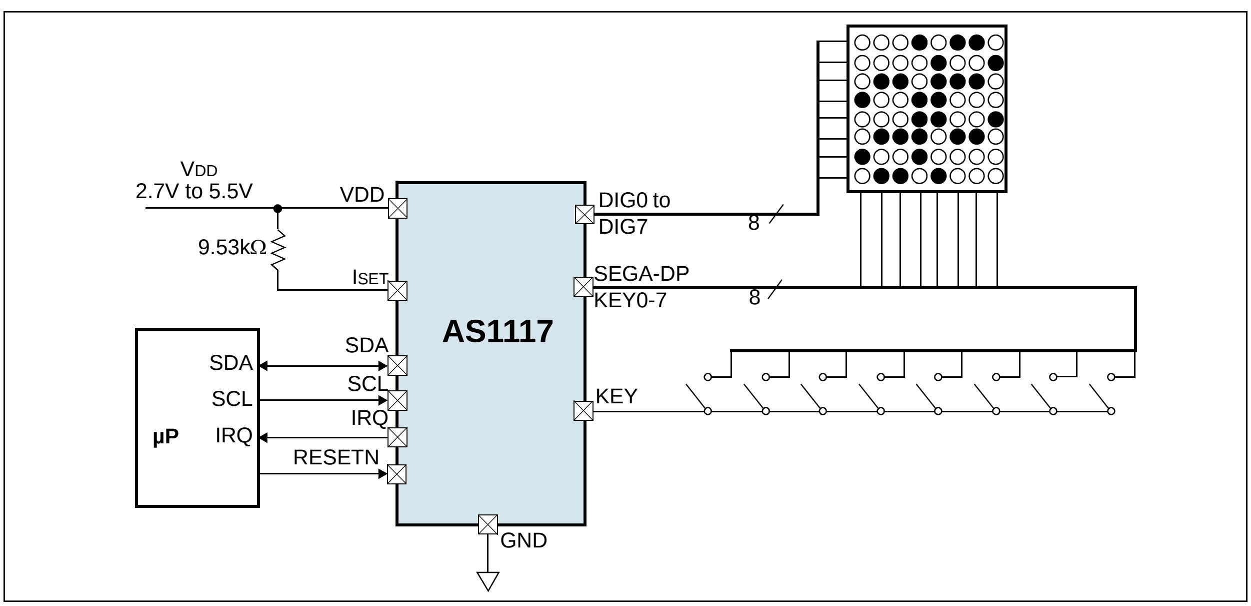
2 Key Features

- 3.4MHz I²C-Compatible Interface
- Individual LED Segment Control
- Readback for 8 Keys plus Interrupt
- Open and Shorted LED Error Detection
  - Global or Individual Error Detection
- Hexadecimal- or BCD-Code for 7-Segment Displays
- 200nA Low-Power Shutdown Current (typ; data retained)
- Digital and Analog Brightness Control
- Display Blanked on Power-Up
- Drive Common-Cathode LED Displays
- Supply Voltage Range: 2.7V to 5.5V
- Software and Hardware Reset
- Up to 4 devices cascadable
- Optional External Clock
- Package: TQFN(4x4)-24

3 Applications

The AS1117 is ideal for seven-segment or dot matrix user interface displays of mobile applications, set-top boxes, VCRs, DVD-players, washing machines, micro wave ovens, refrigerators and other white good or personal electronic applications.

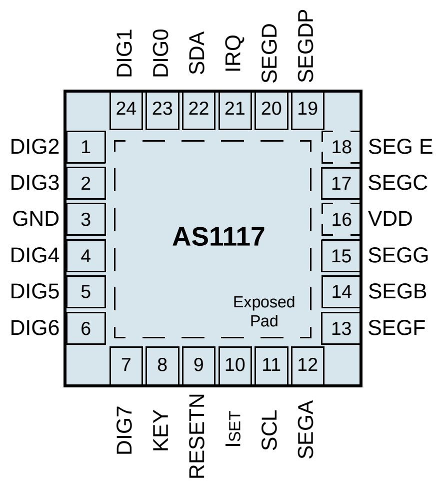
Figure 1. AS1117 - Typical Application Diagram



4 Pinout

Pin Assignments

Figure 2. Pin Assignments (Top View)



Pin Descriptions

Table 2. Pin Descriptions

Pin Name	Pin Number	Description
SDA	22	**Serial-Data I/O**. Open drain digital I/O I²C data pin.
DIG0:DIG7	1, 2, 4, 5, 6, 7, 23, 24	**Digit Drive Lines**. Eight digit drive lines that sink current from the display common cathode. Keyscan detection optional, but must be polled by the µProzessor.
GND	3	**Ground**.
KEY	8	**Keyscan Input.** Keyscan lines for key readback. Can be used for self-adressing.
RESETN	9	**Reset Input.** Pull this pin to low to resest all registers (set to default values) and to put the device into shutdown. Connect this pin via a pull-up resistor to VDD for normal operation.
ISET	10	**Set Segment Current**. Connect to VDD or a reference voltage through RSET to set the peak segment current (see Selecting RSET Resistor Value and Using External Drivers on page 19).
SCL	11	**Serial-Clock Input**. 3.4MHz maximum rate.
IRQ	21	**Interupt Request Output**. Open drain pin.
SEGA:SEGG, SEGDP	12-15, 17-20	**Seven Segment and Decimal Point Drive Lines**. 8 seven-segment drives and decimal point drive that source current to the display.
VDD	16	**Positive Supply Voltage**. Connect to +2.7V to +5.5V supply. Bypass this pin to GND with a 0.1µF capacitor to avoid power supply ripple.
	Exposed Pad	**Exposed Pad.** This pin also functions as a heat sink. Solder it to a large pad or to the circuit-board ground plane to maximize power dissipation.

5 Absolute Maximum Ratings

Stresses beyond those listed in Table 3 may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Section 6 Electrical Characteristics on page 4 is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 3. Absolute Maximum Ratings

<table>
<tr><th colspan="2">Parameter</th><th>Min</th><th>Max</th><th>Units</th><th>Notes</th></tr>
<tr><td rowspan="2">Input Voltage Range</td><td>V_{DD} to GND</td><td>-0.3</td><td>7</td><td>V</td><td></td></tr>
<tr><td>All other pins to GND</td><td>-0.3</td><td>7 or
V_{DD} + 0.3</td><td>V</td><td></td></tr>
<tr><td rowspan="2">Current</td><td>DIG0:DIG7 Sink Current</td><td></td><td>500</td><td>mA</td><td></td></tr>
<tr><td>SEGA:SEGG, SEGDP</td><td></td><td>100</td><td>mA</td><td></td></tr>
<tr><td colspan="2">Humidity</td><td>5</td><td>85</td><td>%</td><td>Non-condensing</td></tr>
<tr><td rowspan="2">ESD</td><td>Digital outputs</td><td colspan="2" rowspan="2">1</td><td rowspan="2">kV</td><td rowspan="2">Norm: MIL 833 E method 3015</td></tr>
<tr><td>All other pins</td></tr>
<tr><td colspan="2">Latch-Up Immunity</td><td colspan="2">±100</td><td>mA</td><td>EIA/JESD78</td></tr>
<tr><td colspan="2">Thermal Resistance Θ_{JA}</td><td></td><td>30.5</td><td>ºC/W</td><td>on PCB</td></tr>
<tr><td colspan="2">Ambient Temperature</td><td>-40</td><td>+85</td><td>ºC</td><td></td></tr>
<tr><td colspan="2">Storage Temperature</td><td>-55</td><td>150</td><td>ºC</td><td></td></tr>
<tr><td colspan="2">Package Body Temperature</td><td></td><td>+260</td><td>ºC</td><td>The reflow peak soldering temperature (body temperature) specified is in accordance with IPC/JEDEC J-STD-020D “Moisture/Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices”.
The lead finish for Pb-free leaded packages is matte tin (100% Sn).</td></tr>
</table>

6 Electrical Characteristics

V_{DD} = 2.7V to 5.5V, R_{SET} = 9.53kΩ, T_{AMB} = -40°C to +85°C, typ. values @ T_{AMB} = +25ºC and V_{DD} = 5.0V (unless otherwise specified).

Table 4. Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	Operating Supply Voltage		2.7		5.5	V
I_{DDSD}	Shutdown Supply Current	All digital inputs at V_{DD} or GND, T_{AMB} = +25ºC		0.2	2	µA
I_{DD}	Operating Supply Current	R_{SET} = open circuit.		0.35	0.6	mA
		All segments and decimal point on; I_{SEG} = -40mA.		335		mA
f_{OSC}	Display Scan Rate	8 digits scanned	0.48		0.96	kHz
I_{DIGIT}	Digit Drive Sink Current	V_{OUT} = 0.65V	320			mA
I_{SEG}	Segment Drive Source Current	V_{DD} = 5.0V, V_{OUT} = (V_{DD} -1V)	-35	-41	-47	mA
ΔI_{SEG}	Segment Drive Current Matching			3		%
I_{SEG}	Segment Drive Source Current	Average Current			47	mA

Table 5. Logic Inputs/Outputs Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{IH}, I_{IL}	Input Current SDA, SCL	V_{IN} = 0V or V_{DD}	-1		1	µA
V_{IH}	Logic High Input Voltage SDA, SCL, RESETN		1.26			V
V_{IL}	Logic Low Input Voltage SDA, SCL, RESETN				0.54	V
$V_{OL(SDA)}$	SDA Output Low Voltage	I_{SINK} = 3mA			0.4	V
$V_{KEYopen}$	Keyscan Open Input Voltage		0.8xV_{DD}			V
$V_{KEYshort}$	Keyscan Short Input Voltage				0.7x V_{DD}	V
$V_{OL(IRQ)}$	Interrupt Output Low Voltage	I_{SINK} = 3mA			0.4	V
ΔV_I	Hysteresis Voltage	DIN, CLK, LD/CS		1		V
	Capacitive Load for Each Bus Line			400		pF
	Open Detection Level Threshold		0.7x V_{DD}	0.75x V_{DD}	0.8x V_{DD}	V
	Short Detection Level Threshold		0.05x V_{DD}	0.1x V_{DD}	0.15x V_{DD}	V

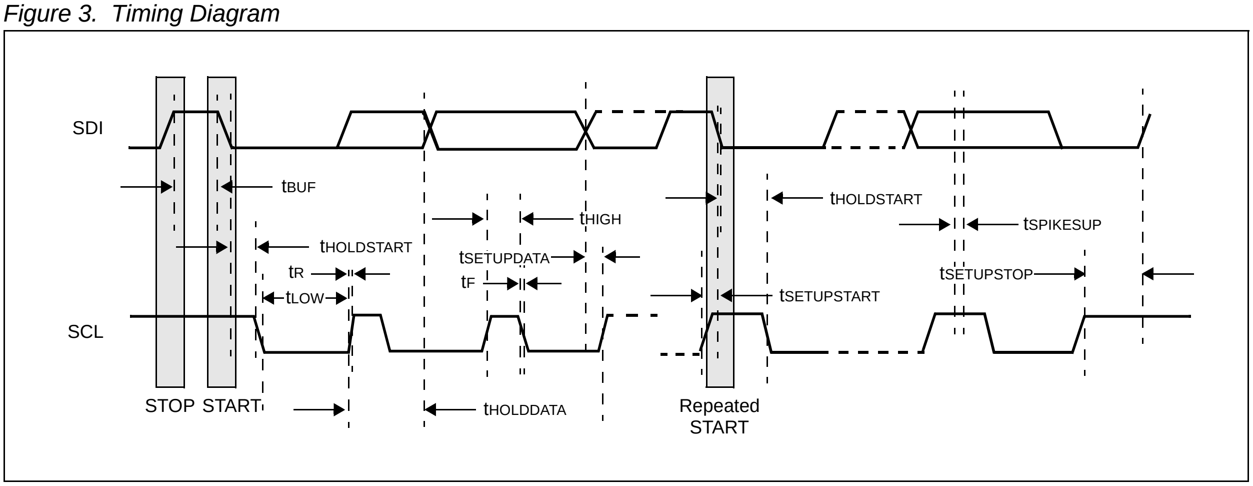
Table 6. Timing Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCL}	SCL Frequency		0.1		3.4	MHz
t_{BUF}	Bus Free Time Between STOP and START Conditions		1.3			µs
$t_{HOLDSTART}$	Hold Time for Repeated START Condition		160			ns
t_{LOW}	SCL Low Period		50		75	ns
t_{HIGH}	SCL High Period		50		75	ns
$t_{SETUPSTART}$	Setup Time for Repeated START Condition		100			ns
$t_{SETUPDATA}$	Data Setup Time		10			ns
$t_{HOLDDATA}$	Data Hold Time				70	ns
$t_{RISE(SCL)}$	SCL Rise Time		10		40	ns
$t_{RISE(SCL1)}$	SCL Rise Time after Repeated START Condition and After an ACK Bit		10		80	ns
$t_{FALL(SCL)}$	SCL Fall Time		10		40	ns
$t_{RISE(SDA)}$	SDA Rise Time		20		80	ns
$t_{FALL(SDA)}$	SDA Fall Time		20		80	ns
$t_{SETUPSTOP}$	STOP Condition Setup Time		160			ns
$t_{SPIKESUP}$	Pulse Width of Spike Suppressed			50		ns
Key Readback						
	Debounce Time			20		ms

Notes:

1. The Min / Max values of the Timing Characteristics are guaranteed by design.
2. All limits are guaranteed. The parameters with min and max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

Figure 3. Timing Diagram



7 Typical Operating Characteristics

RSET = 9.53kΩ, VRset = VDD;

Figure 4. Display Scan Rate vs. Supply Voltage;

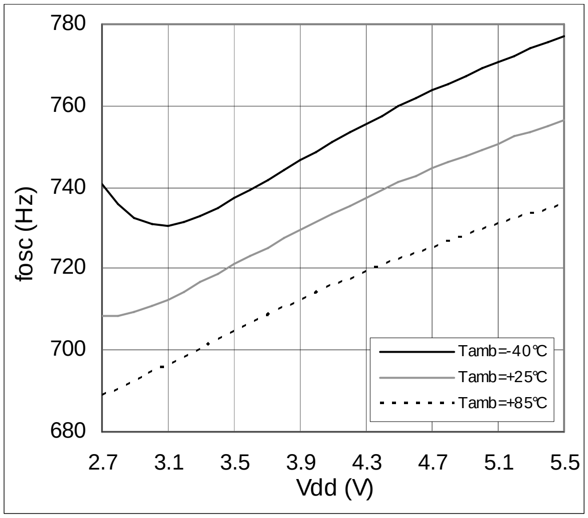


Figure 5. Display Scan Rate vs. Temperature;

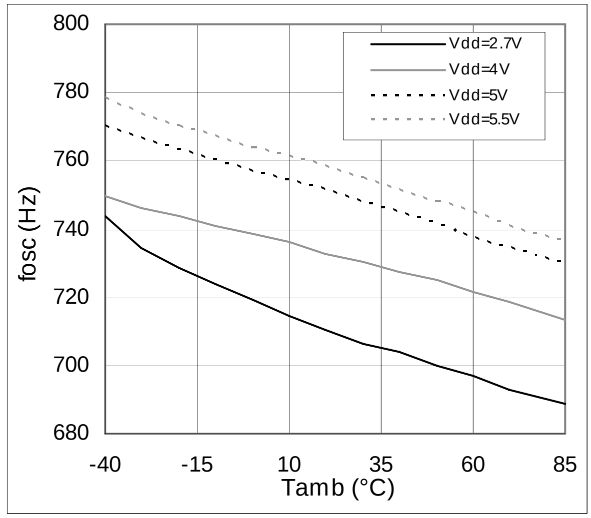


Figure 6. Segment Current vs. Temperature;

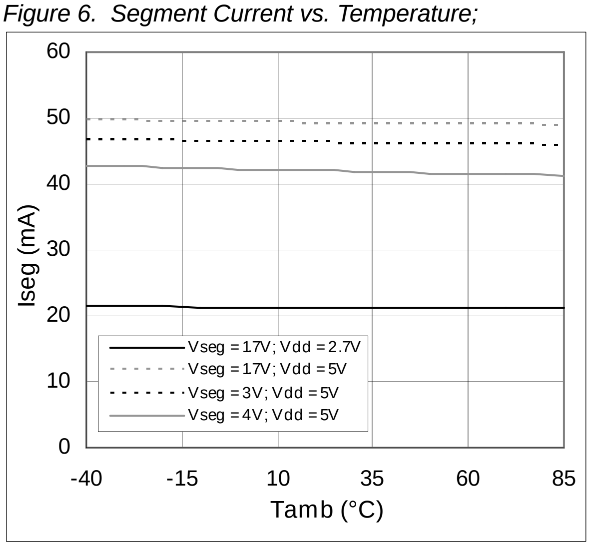


Figure 7. Segment Current vs. RSET;

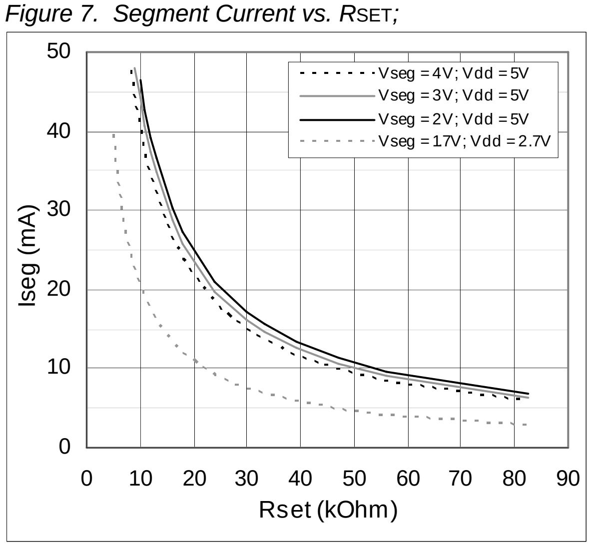


Figure 8. Segment Current vs. Supply Voltage;

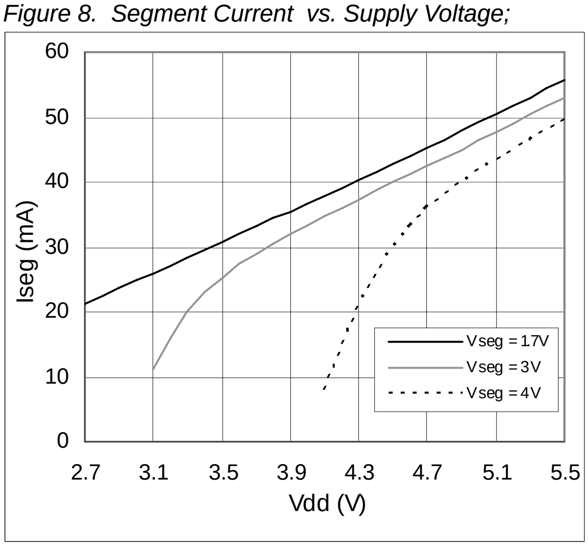


Figure 9. Segment Current vs. VDD; VRset = 2.8V

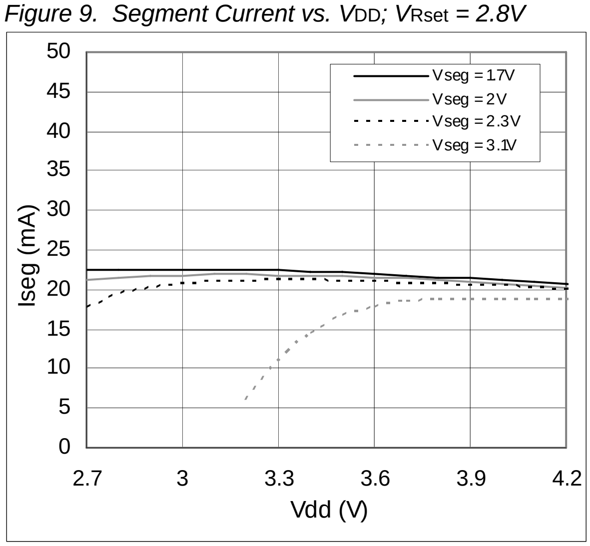


Figure 10. VDIGIT vs. IDIGIT

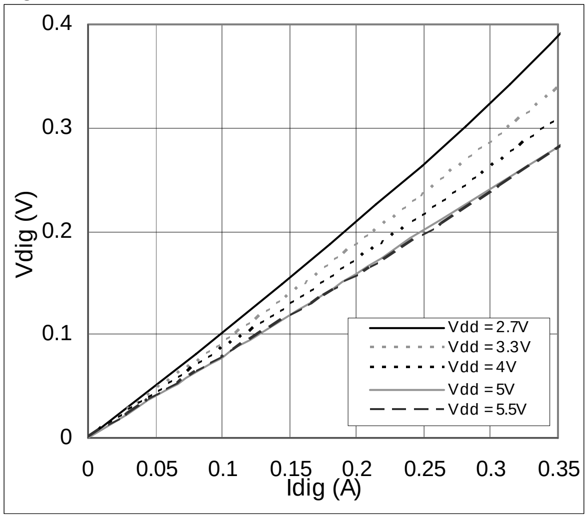


Figure 11. Input High Level vs. Supply Voltage

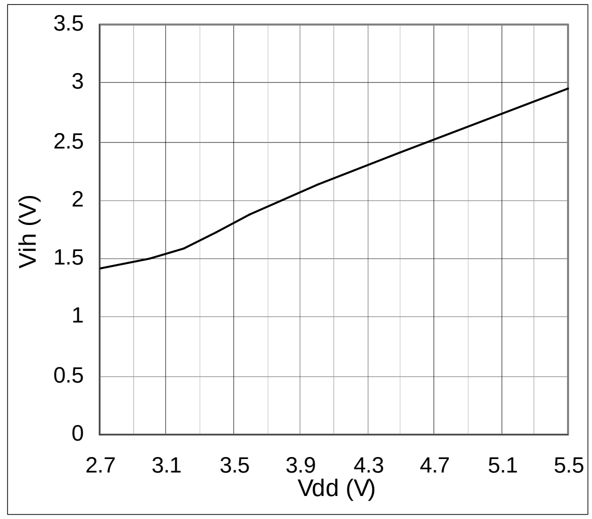


Figure 12. ISEG vs. VSEG; VDD = 5V

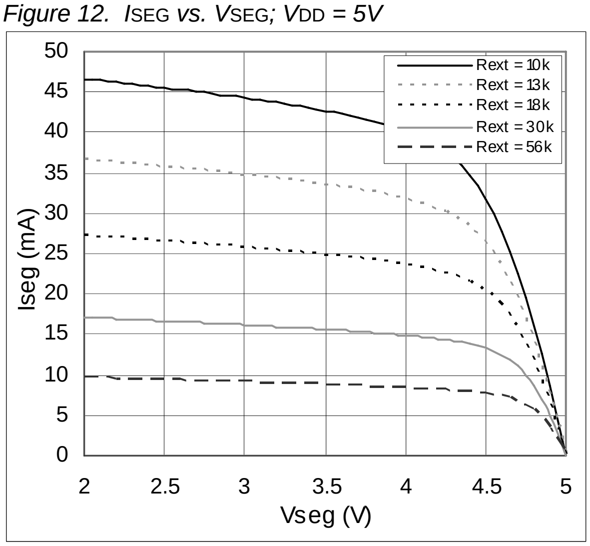


Figure 13. ISEG vs. VSEG; VDD = 4V

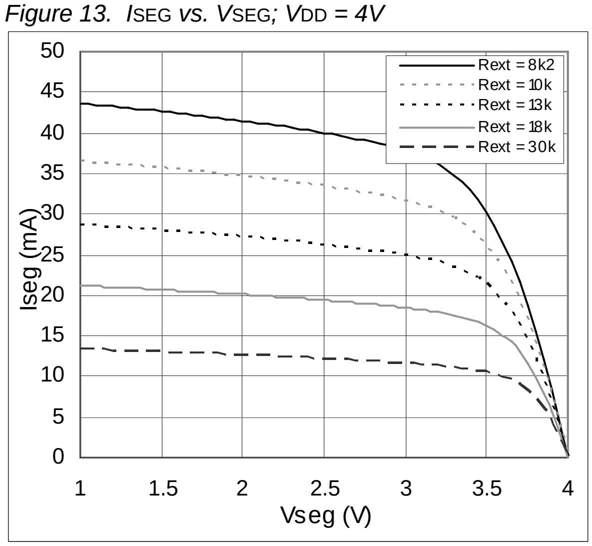


Figure 14. ISEG vs. VSEG; VDD = 3.3V

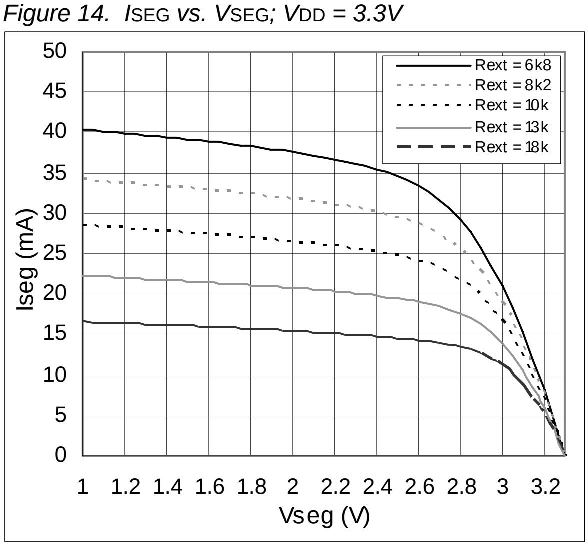
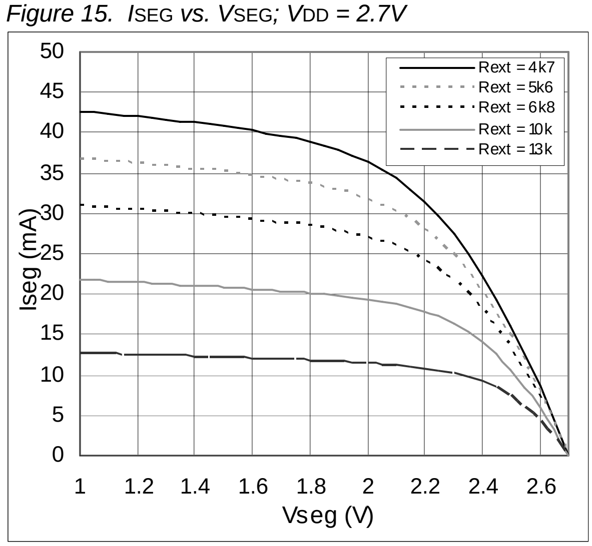


Figure 15. ISEG vs. VSEG; VDD = 2.7V



8 Detailed Description

Block Diagram

Figure 16. AS1117 - Block Diagram

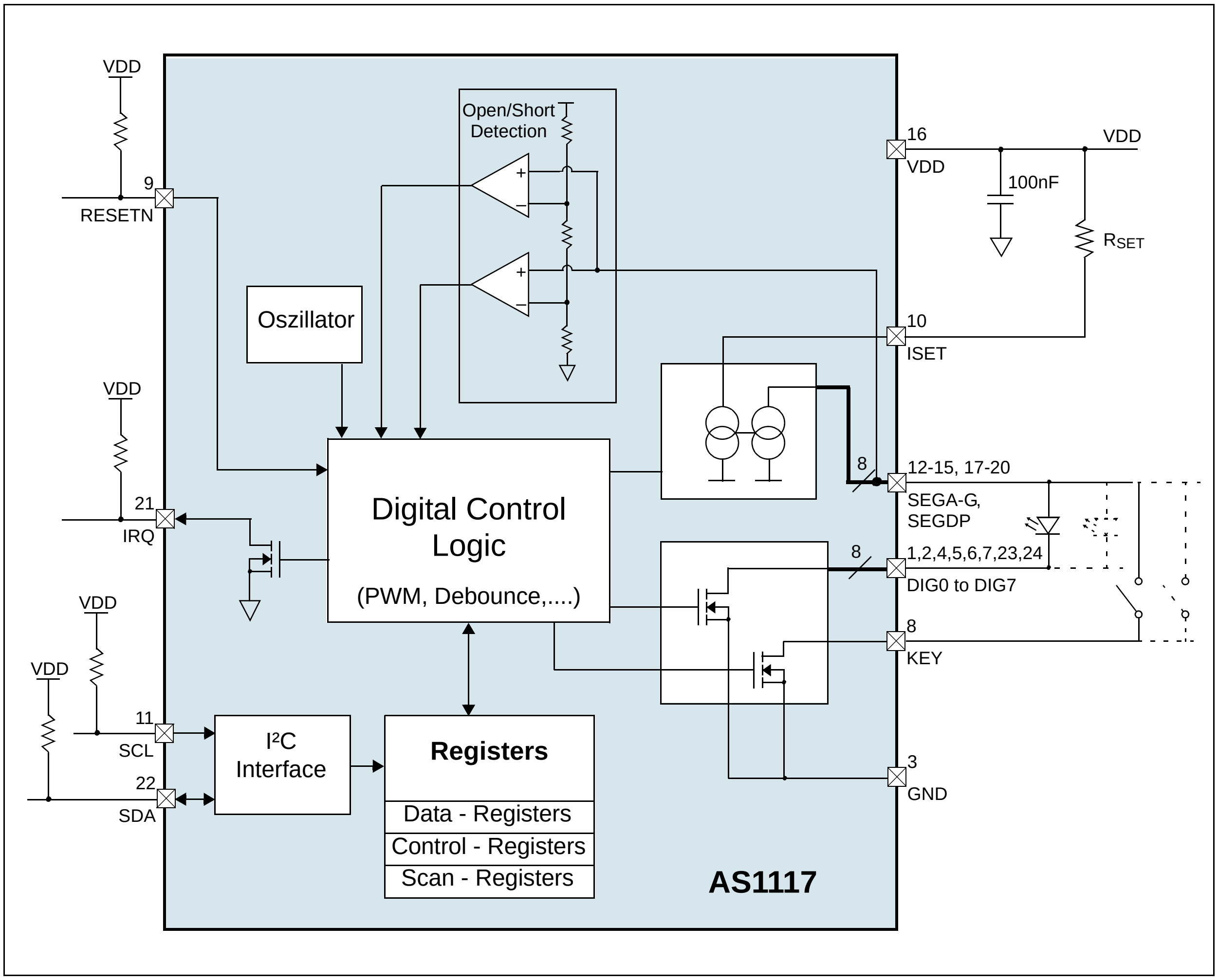
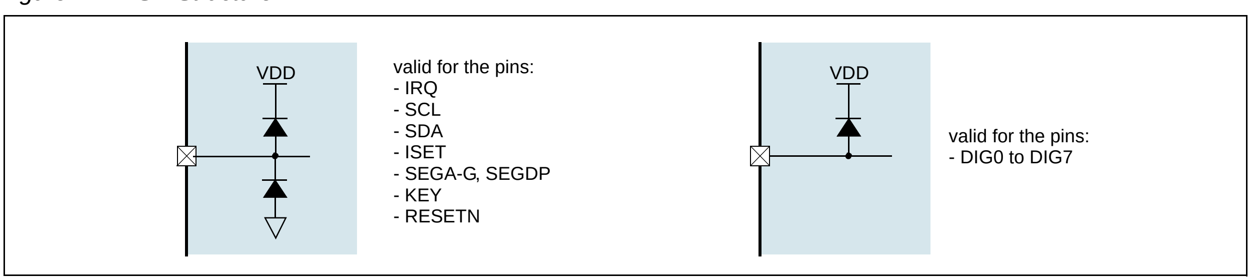


Figure 17. ESD Structure



I²C Interface

The AS1117 supports the I²C serial bus and data transmission protocol in high-speed mode at 3.4MHz. The AS1117 operates as a slave on the I²C bus. The bus must be controlled by a master device that generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions. Connections to the bus are made via the open-drain I/O pins SCL and SDA.

Figure 18. I²C Interface Initialisation

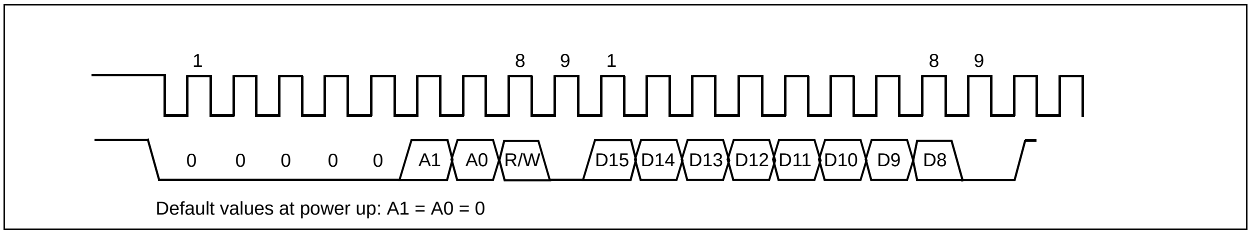
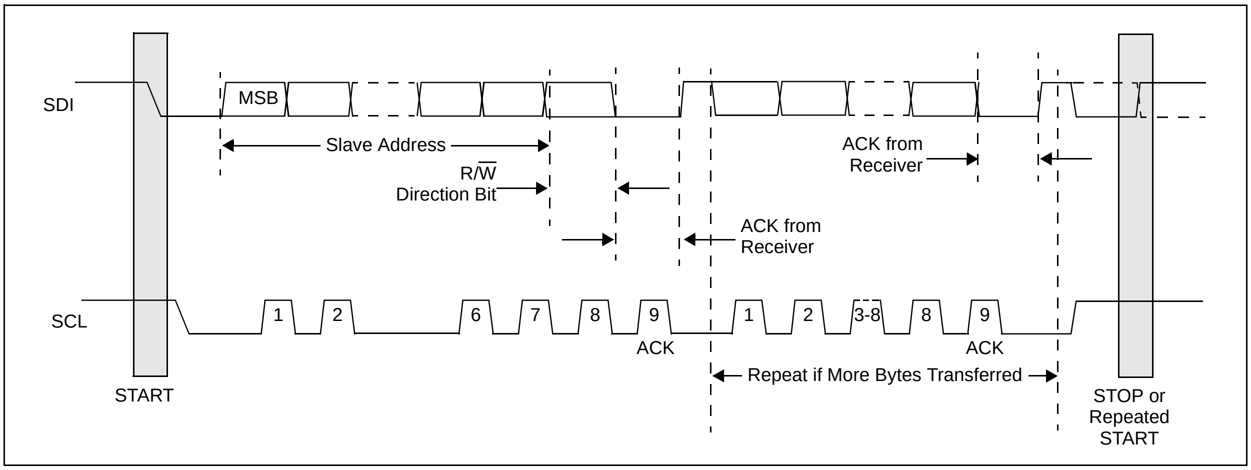


Figure 19. Bus Protocol



The bus protocol (as shown in Figure 19) is defined as:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as control signals.

The bus conditions are defined as:

- **Bus Not Busy**. Data and clock lines remain HIGH.
- **Start Data Transfer**. A change in the state of the data line, from HIGH to LOW, while the clock is HIGH, defines a START condition.
- **Stop Data Transfe**r. A change in the state of the data line, from LOW to HIGH, while the clock line is HIGH, defines the STOP condition.
- **Data Valid**. The state of the data line represents valid data, when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal. There is one clock pulse per bit of data.
  Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of data bytes transferred between START and STOP conditions is not limited and is determined by the master device. The information is transferred byte-wise and each receiver acknowledges with a ninth-bit.
  Within the I²C bus specifications a high-speed mode (3.4MHz clock rate) is defined.
- **Acknowledge**: Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse that is associated with this acknowledge bit. A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an

acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

- Figure 19 on page 9 details how data transfer is accomplished on the I²C bus. Depending upon the state of the $R/\overline{W}$ bit, two types of data transfer are possible:
- **Master Transmitter to Slave Receiver**. The first byte transmitted by the master is the slave address, followed by a number of data bytes. The slave returns an acknowledge bit after the slave address and each received byte.
- **Slave Transmitter to Master Receiver**. The first byte, the slave address, is transmitted by the master. The slave then returns an acknowledge bit. Next, a number of data bytes are transmitted by the slave to the master. The master returns an acknowledge bit after all received bytes other than the last byte. At the end of the last received byte, a not-acknowledge is returned. The master device generates all of the serial clock pulses and the START and STOP conditions. A transfer is ended with a STOP condition or a repeated START condition. Since a repeated START condition is also the beginning of the next serial transfer, the bus will not be released.

The AS1117 can operate in the following slave modes:

- **Slave Receiver Mode**. Serial data and clock are received through SDA and SCL. After each byte is received, an acknowledge bit is transmitted. START and STOP conditions are recognized as the beginning and end of a serial transfer. Address recognition is performed by hardware after reception of the slave address and direction bit.
- **Slave Transmitter Mode**. The first byte (the slave address) is received and handled as in the slave receiver mode. However, in this mode the direction bit will indicate that the transfer direction is reversed. Serial data is transmitted on SDA by the AS1117 while the serial clock is input on SCL. START and STOP conditions are recognized as the beginning and end of a serial transfer.

I²C Device Self Addressing

If this feature is used, 2 of the 8 key readback nodes can be left open or shorted for self-addressing. This is done with KEY together with SEGG and SEGF. This two nodes cannot be used for key-readback in this case. After startup all devices have the predefined adress 0000000. A single command for self-addressing will update all connected AS1117. This command has to be done after startup or everytime the AS1117 gets disconnected from the supply. The I²C address definition must be done with fixed connection, since I²C detection is excluded from debounce time of key registers.

I²C Device Address Byte

The address byte (see Figure 20) is the first byte received following the START condition from the master device.

Figure 20. I²C Device Address Byte

	MSB	6	5	4	3	2	1	LSB
predefined address:	0	0	0	0	0	0	0	$R/\overline{W}$
	MSB	6	5	4	3	2	1	LSB
updated address:	0	0	0	0	0	A1	A0	$R/\overline{W}$

- The default slave address is factory-set to 0000000.
- The two LSB bits of the address byte are the device select bits, A0 to A1, which can be set by the self-adress command after startup. A maximum of four devices with the same pre-set code can therefore be connected on the same bus at one time.
- The last bit of the address byte ($R/\overline{W}$) define the operation to be performed. When set to a 1 a read operation is selected; when set to a 0 a write operation is selected.

Following the START condition, the AS1117 monitors the I²C bus, checking the device type identifier being transmitted. Upon receiving the address code, and the $R/\overline{W}$ bit, the slave device outputs an acknowledge signal on the SDA line.

Command Byte

The AS1117 operation, (see Table 7) is determined by a command byte (see Figure 21 on page 11).

Figure 21. Command Byte

MSB	6	5	4	3	2	1	LSB
D15	D14	D13	D12	D11	D10	D09	D08

Figure 22. Command and Single Data Byte Received

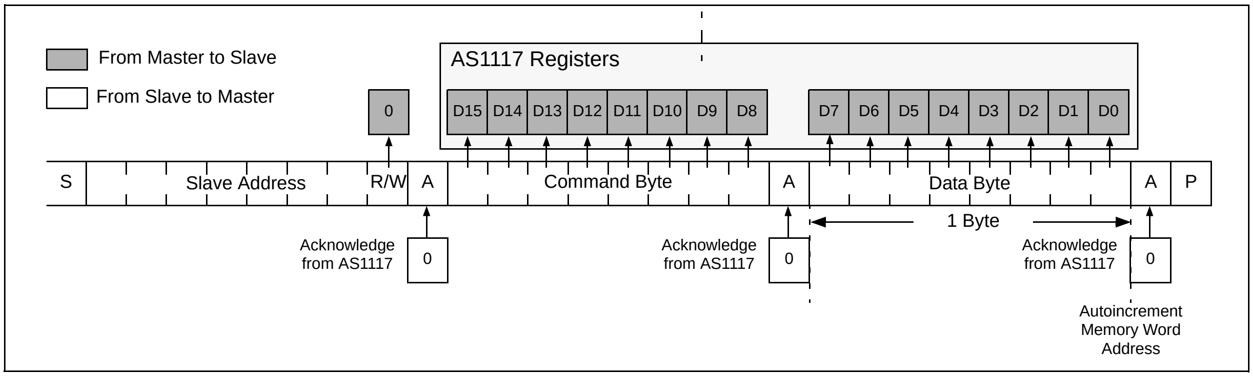


Figure 23. Setting the Pointer to a Address Register to select a Data Register for a Read Operation

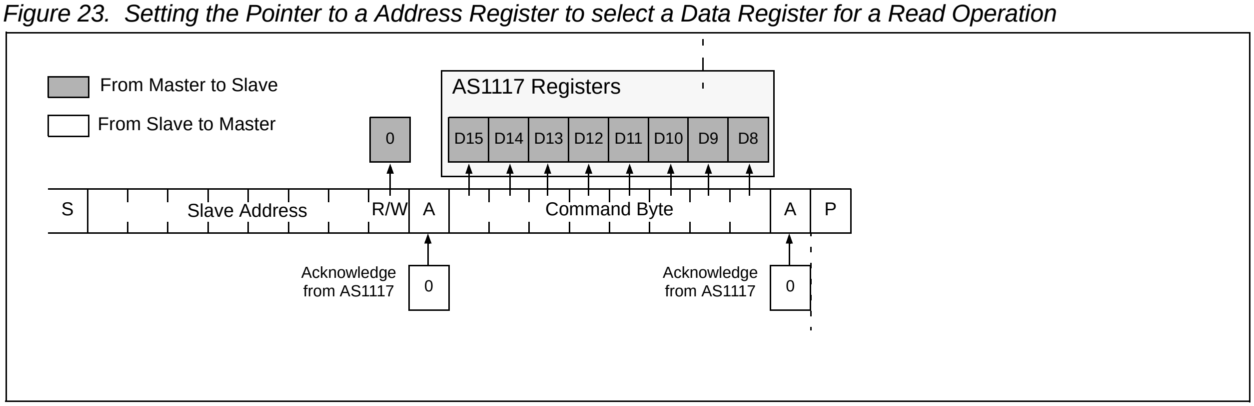
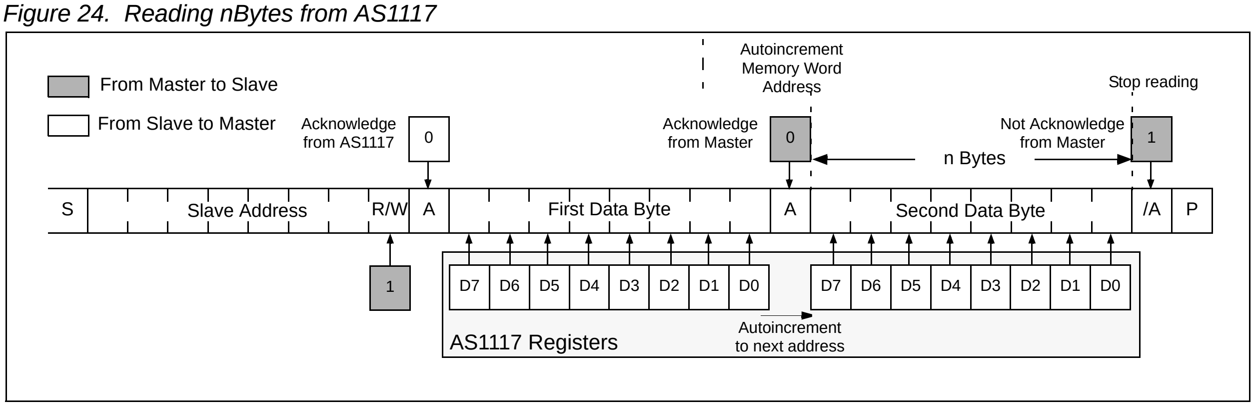


Figure 24. Reading nBytes from AS1117



Initial Power-Up

On initial power-up, the AS1117 registers are reset to their default values, the display is blanked, and the device goes into shutdown mode. At this time, all registers should be programmed for normal operation.

Note: The default settings enable only scanning of one digit; the internal decoder is disabled and the Intensity Control Register (see page 17) is set to the minimum values.

Shutdown Mode

The AS1117 devices feature a shutdown mode, where they consume only 200nA (typ) current. Shutdown mode is entered via a write to the Shutdown Register (see Table 8) or via pulling the pin RESTEN to logic low. When pin RESETN is set to logic low an according write to the Shutdown Register is done internally. During shutdown mode the Digit-Registers maintain their data.

Note: When pin RESETN is pulled to logic high again, a write to the Shutdown Register in necessary to leave the shutdown mode.

Shutdown mode can either be used as a means to reduce power consumption or for generating a flashing display (repeatedly entering and leaving shutdown mode). For minimum supply current in shutdown mode, logic input should be at GND or V_{DD} (CMOS logic level).

When entering or leaving shutdown mode, the Feature Register is reset to its default values (all 0s) when Shutdown Register bit D7 (page 13) = 0.

Note: When Shutdown Register bit D7 = 1, the Feature Register is left unchanged when entering or leaving shutdown mode. If the AS1117 is used with an external clock, Shutdown Register bit D7 should be set to 1 when writing to the Shutdown Register.

Digit- and Control-Registers

The AS1117 devices contain 8 Digit-Registers,11 control-registers and 10 diagnostic-registers, which are listed in Table 7. All registers are selected using a 8-bit address word, and communication is done via the I²C interface.

- Digit Registers – These registers are realized with an on-chip 64-bit memory. Each digit can be controlled directly without rewriting the whole register contents.
- Control Registers – These registers consist of decode mode, display intensity, number of scanned digits, shutdown, display test and features selection registers.

Table 7. Register Address Map

Type	Register	Address							Page
		D15:D13	D12	D11	D10	D9	D8	D7:D0	
Digit Register	Digit 0	000	0	0	0	0	1	(see Table 10 on page 14, Table 11 on page 14 and Table 12 on page 15)	N/A
	Digit 1	000	0	0	0	1	0		N/A
	Digit 2	000	0	0	0	1	1		N/A
	Digit 3	000	0	0	1	0	0		N/A
	Digit 4	000	0	0	1	0	1		N/A
	Digit 5	000	0	0	1	1	0		N/A
	Digit 6	000	0	0	1	1	1		N/A
	Digit 7	000	0	1	0	0	0		N/A

Table 7. Register Address Map

Type	Register	Address							Page
		D15:D13	D12	D11	D10	D9	D8	D7:D0	
Control Register	Decode-Mode	000	0	1	0	0	1	(see Table 9 on page 14)	13
	Global Intensity	000	0	1	0	1	0	(see Table 18 on page 17)	17
	Scan Limit	000	0	1	0	1	1	(see Table 20 on page 17)	17
	Shutdown	000	0	1	1	0	0	(see Table 8 on page 13)	12
	Self-Adressing	001	0	1	1	0	1		N/A
	Feature	000	0	1	1	1	0	(see Table 21 on page 18)	18
	Display Test Mode	000	0	1	1	1	1	(see Table 15 on page 16)	14
	DIG0:DIG1 Intensity	000	1	0	0	0	0	(see Table 19 on page 17)	
	DIG2:DIG3 Intensity	000	1	0	0	0	1	(see Table 19 on page 17)	
	DIG4:DIG5 Intensity	000	1	0	0	1	0	(see Table 19 on page 17)	
	DIG6:DIG7 Intensity	000	1	0	0	1	1	(see Table 19 on page 17)	
Keyscan/Diagnostic Register	Diagnostic Digit 0	000	1	0	1	0	0		N/A
	Diagnostic Digit 1	000	1	0	1	0	1		N/A
	Diagnostic Digit 2	000	1	0	1	1	0		N/A
	Diagnostic Digit 3	000	1	1	0	1	1		N/A
	Diagnostic Digit 4	000	1	1	0	0	0		N/A
	Diagnostic Digit 5	000	1	1	0	0	1		N/A
	Diagnostic Digit 6	000	1	1	0	1	0		N/A
	Diagnostic Digit 7	000	1	1	0	1	1		N/A
	KEY	000	1	1	1	0	0		

The Shutdown Register controls AS1117 shutdown mode.

Table 8. Shutdown Register Format (Address (HEX) = 0x0C))

Mode	HEX Code	Register Data							
		D7	D6	D5	D4	D3	D2	D1	D0
Shutdown Mode, Reset Feature Register to Default Settings	0x00	0	X	X	X	X	X	X	0
Shutdown Mode, Feature Register Unchanged	0x80	1	X	X	X	X	X	X	0
Normal Operation, Reset Feature Register to Default Settings	0x01	0	X	X	X	X	X	X	1
Normal Operation, Feature Register Unchanged	0x81	1	X	X	X	X	X	X	1

Decode Enable Register (0x09)

The Decode Enable Register sets the decode mode. BCD/HEX decoding (either BCD code – characters 0:9, E, H, L, P, and -, or HEX code – characters 0:9 and A:F) is selected by bit D2 (page 18) of the Feature Register. The Decode Enable Register is used to select the decode mode or no-decode for each digit. Each bit in the Decode Enable Register corresponds to its respective display digit (i.e., bit D0 corresponds to digit 0, bit D1 corresponds to digit 1 and so on). Table 10 on page 14 lists some examples of the possible settings for the Decode Enable Register bits.

Note: A logic high enables decoding and a logic low bypasses the decoder altogether.

When decode mode is used, the decoder looks only at the lower-nibble (bits D3:D0) of the data in the Digit-Registers, disregarding bits D6:D4. Bit D7 sets the decimal point (SEG DP) independent of the decoder and is positive logic (bit D7 = 1 turns the decimal point on). Table 10 on page 14 lists the code-B font; Table 11 on page 14 lists the HEX font.

When no-decode mode is selected, data bits D7:D0 of the Digit-Registers correspond to the segment lines of the AS1117. Table 12 on page 15 shows the 1:1 pairing of each data bit to the appropriate segment line.

Table 9. Decode Enable Register Format Examples

Decode Mode	HEX Code	Register Data							
		D7	D6	D5	D4	D3	D2	D1	D0
No decode for digits 7:0	0x00	0	0	0	0	0	0	0	0
Code-B/HEX decode for digit 0. No decode for digits 7:1	0x01	0	0	0	0	0	0	0	1
Code-B/HEX decode for digit 0:2. No decode for digits 7:3	0x07	0	0	0	0	0	1	1	1
Code-B/HEX decode for digits 0:5. No decode for digits 7:6	0x3F	0	0	1	1	1	1	1	1
Code-B/HEX decode for digits 0,2,5. No decode for digits 1, 3, 4, 6, 7	0x25	0	0	1	0	0	1	0	1

Figure 25. Standard 7-Segment LED Intensity Control and Inter-Digit Blanking

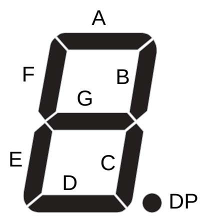


Table 10. Code-B Font

Character	Register Data						Character	Register Data						Character	Register Data					
	D7	D6:D4	D3	D2	D1	D0		D7	D6:D4	D3	D2	D1	D0		D7	D6:D4	D3	D2	D1	D0
0		X	0	0	0	0	6		X	0	1	1	0	H		X	1	1	0	0
1		X	0	0	0	1	7		X	0	1	1	1	L		X	1	1	0	1
2		X	0	0	1	0	8		X	1	0	0	0	P		X	1	1	1	0
3		X	0	0	1	1	9		X	1	0	0	1			X	1	1	1	1
4		X	0	1	0	0	-		X	1	0	1	0	.	1*	X	X	X	X	X
5		X	0	1	0	1	E		X	1	0	1	1							

* The decimal point can be enabled with every character by setting bit D7 = 1.

Table 11. HEX Font

Character	Register Data						Character	Register Data						Character	Register Data					
	D7	D6:D4	D3	D2	D1	D0		D7	D6:D4	D3	D2	D1	D0		D7	D6:D4	D3	D2	D1	D0
0		X	0	0	0	0	6		X	0	1	1	0	C		X	1	1	0	0
1		X	0	0	0	1	7		X	0	1	1	1	d		X	1	1	0	1
2		X	0	0	1	0	8		X	1	0	0	0	E		X	1	1	1	0

Table 11. HEX Font

Character	Register Data						Character	Register Data						Character	Register Data					
	D7	D6:D4	D3	D2	D1	D0		D7	D6:D4	D3	D2	D1	D0		D7	D6:D4	D3	D2	D1	D0
3		X	0	0	1	1	9		X	1	0	0	1	F		X	1	1	1	1
4		X	0	1	0	0	A		X	1	0	1	0	.	1*	X	X	X	X	X
5		X	0	1	0	1	b		X	1	0	1	1							

* The decimal point can be enabled with every character by setting bit D7 = 1.

Table 12. No-Decode Mode Data Bits and Corresponding Segment Lines

	D7	D6	D5	D4	D3	D2	D1	D0
Corresponding Segment Line	DP	A	B	C	D	E	F	G

I²C Self Addressing

If this feature is used, 2 of the 8 key readback nodes can be left open or shorted for self-addressing. This is done with KEY together with SEGG and SEGF. This two nodes cannot be used for key-readback in this case. After startup all devices have the predefined adress 0000000. A single command for selfaddressing will update all connected AS1117. This command has to be done after startup or everytime the AS1117 gets disconnected from the supply. The I²C address definition must be done with fixed connection, since I²C detection is excluded from debounce time of key registers.

Note: A short writes a logical “0” whereas an open writes a logical “1” as address bit.

Table 13. Self Addressing Register (Address (HEX) = 0x2D))

	D7	D6	D5	D4	D3	D2	D1	D0
Factory-set IC address	X	X	X	X	X	X	X	0
User-set IC address	X	X	X	X	X	X	X	1

Keyscan Register

These two registers contain the result of the keyscan input of the 8 keys. To ensure proper results the data in these registers are updated only if the logic data scanned is stable for 20ms (debounce time). A change of the data stored within these two registers is indicated by a logic low on the IRQ pin. The IRQ is high-impedance if a read operation on the key scan registers is started.

Table 14. LED Diagnostic Register Address

Register HEX Address		Segment							
		D7	D6	D5	D4	D3	D2	D1	D0
0x1C	KEY	DP	A	B	C	D	E	F	G

Note: If I²C self addressing is used segment G&F of KEY is used for the two LSB of the I²C address. In this case these two nodes cannot be used as a key. Additionally the debounce time is disabled for these two bits.
The data within the keyscan register is updated continuously during every cycle (1/10 of refresh rate). Therefore, to get a valid readback of keys it is recommended to read out the keyscan registers immediately after the IRQ is triggered. A short writes a logical “0” whereas an open writes a logical “1” as keyscan register bit.

Display-Test Mode

The AS1117 can detect open or shorted LEDs. Readout of either open LEDs or short LEDs is possible, as well as a OR relation of open and short.

Note: All settings of the digit- and control-registers are maintained.

Table 15. Testmode Register *Summary*

D7	D6	D5	D4	D3	D2	D1	D0
X	RSET_short	RSET_open	LED_global	LED_test	LED_open	LED_short	DISP_test

Table 16. Testmode Register Bit Description (Address (HEX) = 0x0F))

Addr: 0x0F		Address		
Bit	**Bit Name**	**Default**	**Access**	**D7:D0**
D0	DISP_test	0	W	Optical display test. (Testmode for external visual test.) 0: Normal operation; 1: Run display test (All digits are tested independently from scan limit & shutdown register.)
D1	LED_short	0	W	Starts a test for shorted LEDs. (Can be set together with D2) 0: Normal operation; 1: Activate testmode
D2	LED_open	0	W	Starts a test for open LEDs. (Can be set together with D1) 0: Normal operation; 1: Activate testmode
D3	LED_test	0	R	Indicates an ongoing open/short LED test 0: No ongoing LED test; 1: LED test in progress
D4	LED_global	0	R	Indicates that the last open/short LED test has detected an error 0: No error detected; 1: Error detected
D5	RSET_open	0	R	Checks if external resistor RSET is open 0: RSET correct; 1: RSET is open
D6	RSET_short	0	R	Checks if external resistor RSET is shorted 0: RSET correct; 1: RSET is shorted
D7		0	-	Not used

LED Diagnostic Registers

These eight registers contain the result of the LED open/short test for the individual LED of each digit.

Table 17. LED Diagnostic Register Address

Register HEX Address	Digit	Segment								Register HEX Address	Digit	Segment							
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**			**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0x14	DIG0	DP	A	B	C	D	E	F	G	*0x18*	DIG4	DP	A	B	C	D	E	F	G
0x15	DIG1									*0x19*	DIG5								
0x16	DIG2									*0x1A*	DIG6								
0x17	DIG3									*0x1B*	DIG7								

Note: If one or more short occures in the LED array, detection of individual LED fault could become ambiguous.

Intensity Control Register (0x0A)

The brightness of the display can be controlled by digital means using the Intensity Control Registers and by analog means using RSET (see Selecting RSET Resistor Value and Using External Drivers on page 19). The intensity can be controlled globally for all digits, or for each digit individually. The global intensity command will write intensity data to all four individual brightness registers, while the individual intesity command will only write to the associated individual intensity register.

Display brightness is controlled by an integrated pulse-width modulator which is controlled by the lower-nibble of the Intensity Control Register. The modulator scales the average segment-current in 16 steps from a maximum of 15/16 down to 1/16 of the peak current set by RSET.

Table 18. Intensity Register Format

Duty Cycle	HEX Code	Register Data					Duty Cycle	HEX Code	Register Data			
		MSB	D2	D1	LSB				MSB	D2	D1	LSB
1/16 (min on)	0xX0	0	0	0	0		9/16	0xX8	1	0	0	0
2/16	0xX1	0	0	0	1		10/16	0xX9	1	0	0	1
3/16	0xX2	0	0	1	0		11/16	0xXA	1	0	1	0
4/16	0xX3	0	0	1	1		12/16	0xXB	1	0	1	1
5/16	0xX4	0	1	0	0		13/16	0xXC	1	1	0	0
6/16	0xX5	0	1	0	1		14/16	0xXD	1	1	0	1
7/16	0xX6	0	1	1	0		15/16	0xXE	1	1	1	0
8/16	0xX7	0	1	1	1		15/16 (max on)	0xXF	1	1	1	1

Table 19. Intensity Register Address

Register HEX Address		Register Data	
	Type	D7:D4	D3:D0
0x0A	Global	X	Global Intensity
0x10	Digit	Digit 1 Intensity	Digit 0 Intensity
0x11	Digit	Digit 3 Intensity	Digit 2 Intensity
0x12	Digit	Digit 5 Intensity	Digit 4 Intensity
0x13	Digit	Digit 7 Intensity	Digit 6 Intensity

Scan-Limit Register (0x0B)

The Scan-Limit Register controls which of the digits are to be displayed. When all 8 digits are to be displayed, the update frequency is typically 700Hz. If the number of digits displayed is reduced, the update frequency is increased. The frequency can be calculated using 10 x fOSC/(N+2), where N is the number of digits.

Note: To avoid differences in brightness this register should not be used to blank parts of the display (leading zeros).

Table 20. Scan-Limit Register Format (Address (HEX) = 0x0B))

Scan Limit	HEX Code	Register Data					Scan Limit	HEX Code	Register Data			
		D7:D3	D2	D1	D0				D7:D3	D2	D1	D0
Display digit 0 only	0xX0	X	0	0	0		Display digits 0:4	0xX4	X	1	0	0
Display digits 0:1	0xX1	X	0	0	1		Display digits 0:5	0xX5	X	1	0	1
Display digits 0:2	0xX2	X	0	1	0		Display digits 0:6	0xX6	X	1	1	0
Display digits 0:3	0xX3	X	0	1	1		Display digits 0:7	0xX7	X	1	1	1

Feature Register (0x0E)

The Feature Register is used for enabling various features including switching the device into external clock mode, applying an external reset, selecting code-B or HEX decoding, enabling or disabling blinking, setting the blinking rate, and resetting the blink timing.

Note: At power-up the Feature Register is initialized to 0.

Table 21. Feature Register Summary

D7	D6	D5	D4	D3	D2	D1	D0
blink_ start	sync	blink_ freq_sel	blink_en	NU	decode_sel	reg_res	clk_en

Table 22. Feature Register Bit Descriptions (Address (HEX) = 0xXE)

Addr: 0xXE		**Feature Register** Enables and disables various device features.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
D0	clk_en	0	R/W	External clock active. 0 = Internal oscillator is used for system clock. 1 = Pin CLK of the serial interface operates as system clock input.
D1	reg_res	0	R/W	Resets all control registers except the Feature Register. 0 = Reset Disabled. Normal operation. 1 = All control registers are reset to default state (except the Feature Register) identically after power-up. **Note:** The Digit Registers maintain their data.
D2	decode_sel	0	R/W	Selects display decoding for the selected digits (Table 9 on page 14). 0 = Enable Code-B decoding (see Table 10 on page 14). 1 = Enable HEX decoding (see Table 11 on page 14).
D3	NU			Not used
D4	blink_en	0	R/W	Enables blinking. 0 = Disable blinking. 1 = Enable blinking.
D5	blink_freq_sel	0	R/W	Sets blink with low frequency (with the internal oscillator enabled): 0 = Blink period typically is 1 second (0.5s on, 0.5s off). 1 = Blink period is 2 seconds (1s on, 1s off).
D6	sync	0	R/W	Synchronizes blinking on the rising edge of pin LD/CS. The multiplex and blink timing counter is cleared on the rising edge of pin LD/CS. By setting this bit in multiple devices, the blink timing can be synchronized across all the devices.
D7	blink_start	0	R/W	Start Blinking with display enabled phase. When bit D4 (blink_en) is set, bit D7 determines how blinking starts. 0 = Blinking starts with the display turned off. 1 = Blinking starts with the display turned on.

9 Typical Application

Selecting R_{SET} Resistor Value and Using External Drivers

Brightness of the display segments is controlled via R_{SET}. The current that flows into I_{SET} defines the current that flows through the LEDs.

Segment current is about 200 times the current in I_{SET}. Typical values for R_{SET} for different segment currents, operating voltages, and LED voltage drop (V_{LED}) are given in Table 23 & Table 24. The maximum current the AS1117 can drive is 47mA. If higher currents are needed, external drivers must be used, in which case it is no longer necessary that the devices drive high currents.

Note: The display brightness can also be logically controlled (see Intensity Control Register (0x0A) on page 16).

Table 23. R_{SET} vs. Segment Current and LED Forward Voltage, V_{DD} = 2.7V & 3.3V & 3.6V

I_{SEG} (mA)		V_{LED}			V_{LED}				V_{LED}			
		1.5V	2.0V		1.5V	2.0V	2.5V		1.5V	2.0V	2.5V	3.0V
40	V_{DD} = 2.7V	5kΩ	4.4kΩ	V_{DD} = 3.3V	6.7kΩ	6.4kΩ	5.7kΩ	V_{DD} = 3.6V	7.5kΩ	7.2kΩ	6.6kΩ	5.5kΩ
30		6.9kΩ	5.9kΩ		9.1kΩ	8.8kΩ	8.1kΩ		10.18kΩ	9.8kΩ	9.2kΩ	7.5kΩ
20		10.7kΩ	9.6kΩ		13.9kΩ	13.3kΩ	12.6kΩ		15.6kΩ	15kΩ	14.3kΩ	13kΩ
10		22.2kΩ	20.7kΩ		28.8kΩ	27.7kΩ	26kΩ		31.9kΩ	31kΩ	29.5kΩ	27.3kΩ

Table 24. R_{SET} vs. Segment Current and LED Forward Voltage, V_{DD} = 4.0V & 5.0V

I_{SEG} (mA)		V_{LED}						V_{LED}					
		1.5V	2.0V	2.5V	3.0V	3.5V		1.5V	2.0V	2.5V	3.0V	3.5V	4.0V
40	V_{DD} = 4.0V	8.6kΩ	8.3kΩ	7.9kΩ	7.6kΩ	5.2kΩ	V_{DD} = 5.0V	11.35kΩ	11.12kΩ	10.84kΩ	10.49kΩ	10.2kΩ	9.9kΩ
30		11.6kΩ	11.2kΩ	10.8kΩ	9.9kΩ	7.8kΩ		15.4kΩ	15.1kΩ	14.7kΩ	14.4kΩ	13.6kΩ	13.1kΩ
20		17.7kΩ	17.3kΩ	16.6kΩ	15.6kΩ	13.6kΩ		23.6kΩ	23.1kΩ	22.6kΩ	22kΩ	21.1kΩ	20.2kΩ
10		36.89kΩ	35.7kΩ	34.5kΩ	32.5kΩ	29.1kΩ		48.9kΩ	47.8kΩ	46.9kΩ	45.4kΩ	43.8kΩ	42kΩ

Calculating Power Dissipation

The upper limit for power dissipation (PD) for the AS1117 is determined from the following equation:

$$PD = (V_{DD} \times 5mA) + (V_{DD} - V_{LED})(DUTY \times I_{SEG} \times N) \qquad \text{(EQ 1)}$$

Where:

V_{DD} is the supply voltage.
DUTY is the duty cycle set by intensity register (page 17).
N is the number of segments driven (worst case is 8)
V_{LED} is the LED forward voltage
I_{SEG} = segment current set by RSET

Dissipation Example:

$$I_{SEG} = 40mA,\ N = 8,\ DUTY = 15/16,\ V_{LED} = 2.2V \text{ at } 40mA,\ V_{DD} = 5V \qquad \text{(EQ 2)}$$

$$PD = 5V(5mA) + (5V - 2.2V)(15/16 \times 40mA \times 8) = 0.865W \qquad \text{(EQ 3)}$$

Thus, for a TQFN(4x4)-24 package Θ_{JA} = +30.5°C/W, the maximum allowed T_{AMB} is given by:

$$T_{J,MAX} = T_{AMB} + PD \times \Theta_{JA} = 150°C = T_{AMB} + 0.865W \times 30.5°C/W \qquad \text{(EQ 4)}$$

In this example the maximum ambient temperature must stay below 123.61°C.

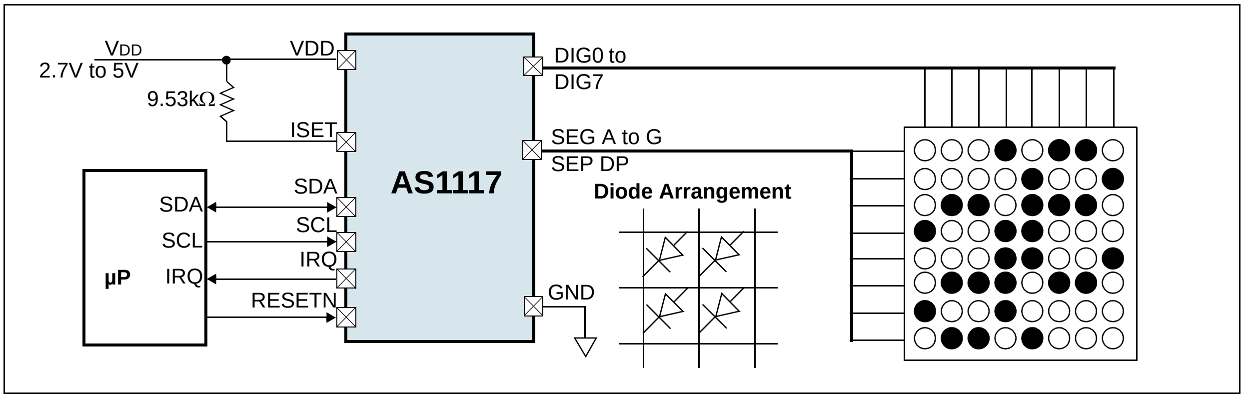
8x8 Dot Matrix Mode

The application example in Figure 26 shows the AS1117 in the 8x8 LED dot matrix mode.

The LED columns have common cathodes and are connected to the DIG0:7 outputs. The rows are connected to the segment drivers. Each of the 64 LEDs can be addressed separately. The columns are selected via the digits as listed in Table 7 on page 12.

The Decode Enable Register (see page 13) must be set to ‘00000000’ as described in Table 9 on page 14. Single LEDs in a column can be addressed as described in Table 12 on page 15, where bit D0 corresponds to segment G and bit D7 corresponds to segment DP.

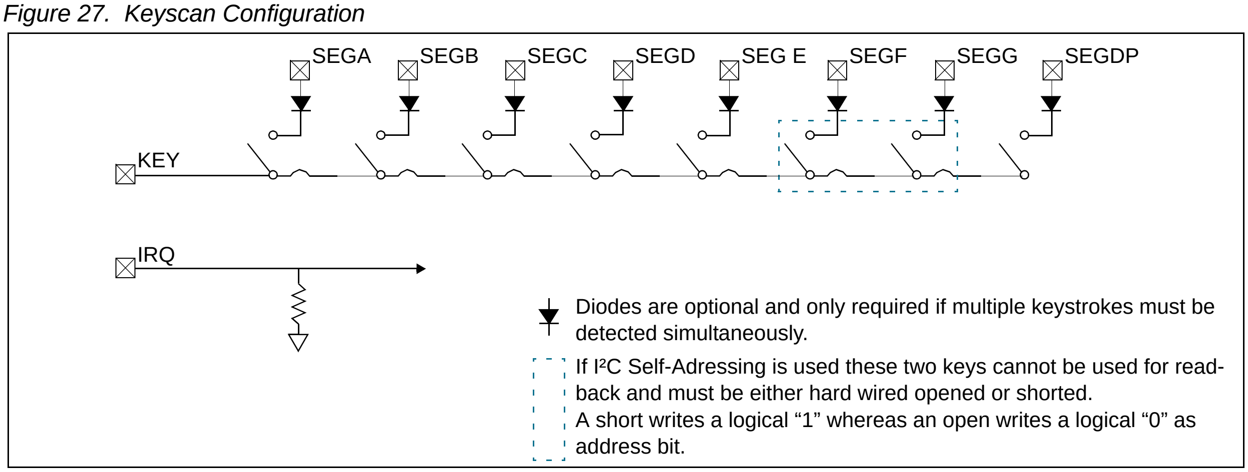
Figure 26. Application Example as LED Dot Matrix Driver



Keyscan

The key readback of the AS1117 can be used either for push buttons as well as switches. If only a single key is pressed (shorted) at a time no additional diodes are required. If a detection of multiple simultaneous keystrokes is required diodes within the keypath, as shown in Figure 27, are required. Pressing multiple keys without the diodes would result in ambiguous results.

Figure 27. Keyscan Configuration



Supply Bypassing and Wiring

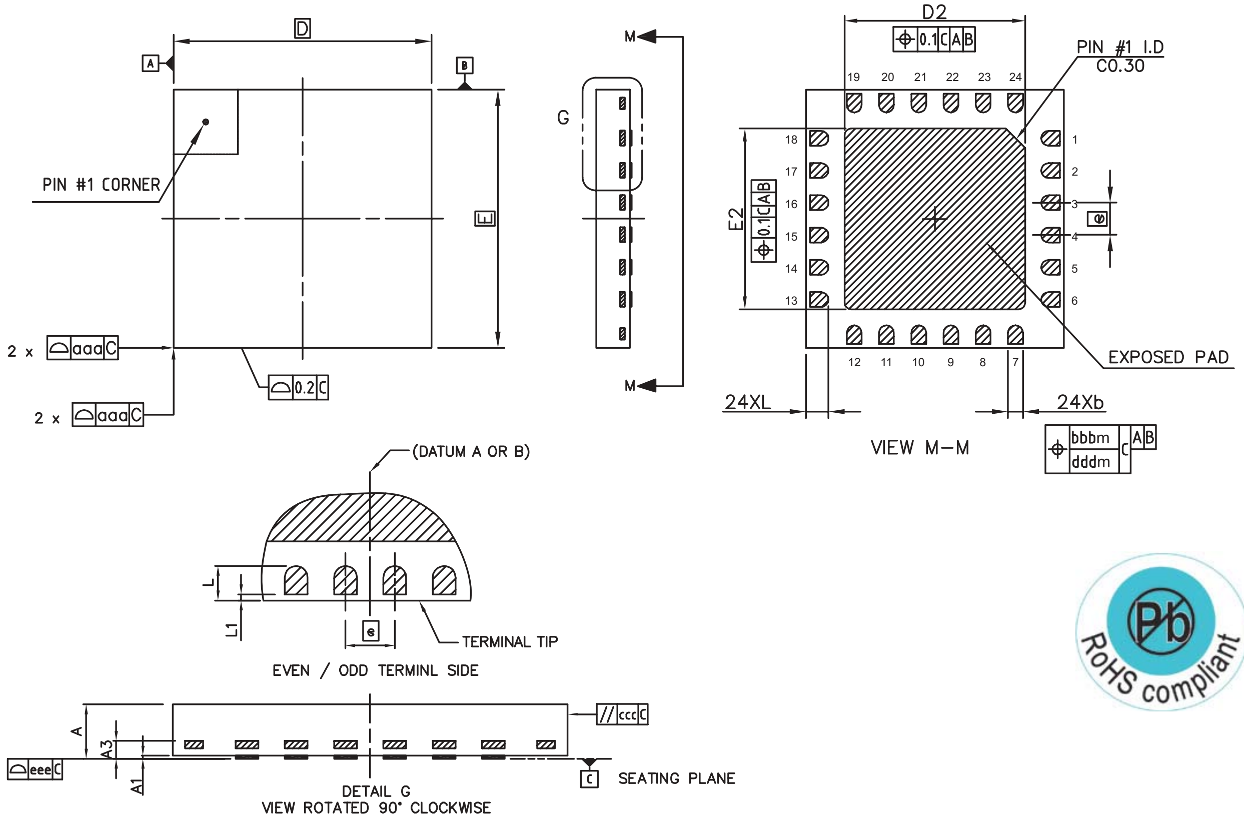
In order to achieve optimal performance the AS1117 should be placed very close to the LED display to minimize effects of electromagnetic interference and wiring inductance.

Furthermore, it is recommended to connect a 10µF and a 0.1µF ceramic capacitor between pins VDD and GND to avoid power supply ripple (see Figure 16 on page 8).

10 Package Drawings and Markings

The AS1117 is available in the TQFN(4x4)-24 package.

Figure 28. TQFN(4x4)-24 Package



Symbol	Min	Typ	Max
A	0.50	0.55	0.60
A1	0.00		0.05
A3		0.152REF	
b	0.18	0.23	0.28
D		4.00BSC	
E		4.00BSC	
D2	2.70	2.80	2.90
E2	2.70	2.80	2.90

Symbol	Min	Typ	Max
e		0.50BSC	
L	0.30	0.35	0.40
L1	0.00		0.10
aaa		0.10	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	

Notes: Unilateral coplanarity zone applies to the exposed heat sink slug as well as the terminals.

1. All dimensions are in millimeters; angles in degrees.
2. Dimension b applies to metallized terminal and is measured between 0.25mm and 0.30mm from terminal tip. Dimension L1 represents terminal full back from package edge up to 0.1mm is acceptable.
3. Coplanarity applies to the exposed heat slug as well as the terminal.
4. Radius on terminal is optional.

11 Ordering Information

The devices are available as the standard products shown in Table 25.

Table 25. Ordering Information

Ordering Code	Marking	Description	Delivery Form	Package
AS1117-BQFT	ASSU	64 LED Driver for Mobile Applications with Error Detection	Tape and Reel	TQFN(4x4)-24

Note: All products are RoHS compliant.
Buy our products or get free samples online at ICdirect: http://www.austriamicrosystems.com/ICdirect

Technical Support is found at http://www.austriamicrosystems.com/Technical-Support

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- Экспресс доставка в любую точку России;
- Помощь Конструкторского Отдела и консультации квалифицированных инженеров;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Поставка электронных компонентов под контролем ВП;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- При необходимости вся продукция военного и аэрокосмического назначения проходит испытания и сертификацию в лаборатории (по согласованию с заказчиком);
- Поставка специализированных компонентов военного и аэрокосмического уровня качества (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Actel, Aeroflex, Peregrine, VPT, Syfer, Eurofarad, Texas Instruments, MS Kennedy, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits, General Dynamics и др.);

Компания «Океан Электроники» является официальным дистрибьютором и эксклюзивным представителем в России одного из крупнейших производителей разъемов военного и аэрокосмического назначения **«JONHON»**, а так же официальным дистрибьютором и эксклюзивным представителем в России производителя высокотехнологичных и надежных решений для передачи СВЧ сигналов **«FORSTAR»**.

«JONHON» (основан в 1970 г.)

Разъемы специального, военного и аэрокосмического назначения:

(Применяются в военной, авиационной, аэрокосмической, морской, железнодорожной, горно- и нефтедобывающей отраслях промышленности)

«FORSTAR» (основан в 1998 г.)

ВЧ соединители, коаксиальные кабели, кабельные сборки и микроволновые компоненты:

(Применяются в телекоммуникациях гражданского и специального назначения, в средствах связи, РЛС, а так же военной, авиационной и аэрокосмической отраслях промышленности).

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