

Six Pair, N- and P-Channel Enhancement-Mode MOSFET

Features

- ▶ High voltage, vertical DMOS technology
- ▶ Integrated gate-to-source resistor
- ▶ Integrated gate-to-source Zener diode
- ▶ Typical peak output +/-3.5A at 50V
- ▶ Low threshold, low on-resistance
- ▶ Low input & output capacitance
- ▶ Fast switching speeds
- ▶ Electrically isolated N- and P-MOSFET pairs

Applications

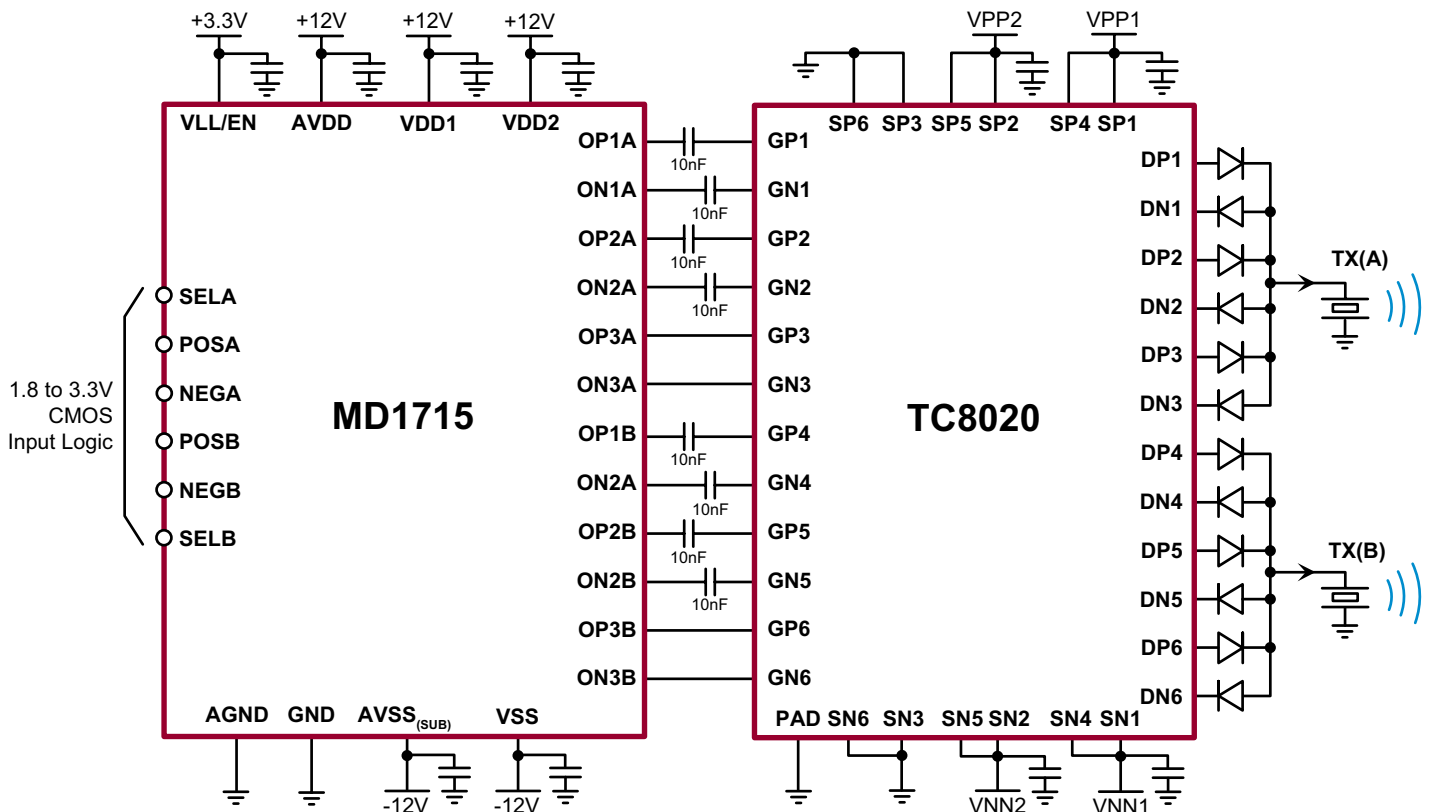
- ▶ High voltage pulsers
- ▶ Amplifiers
- ▶ Buffers
- ▶ Piezoelectric transducer drivers
- ▶ General purpose line drivers
- ▶ Logic level interfaces

General Description

The Supertex TC8020 consists of six pairs of high voltage, low threshold N- and P-channel MOSFETs in a 56-lead QFN package. All MOSFETs have integrated gate-to-source resistors and gate-to-source Zener diode clamps which are desired for high voltage pulser applications. The complimentary, high-speed, high voltage, gate-clamped N- and P-channel MOSFET pairs utilize an advanced vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces a device with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices.

Characteristic of all MOS structures, this device is free from thermal runaway and thermally-induced secondary breakdown. Supertex's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input and output capacitance, and fast switching speeds are desired.

Typical Application



Ordering Information

| Part Number | Package Option | Packing |
|-------------|-------------------|----------|
| TC8020K6-G | 56-Lead QFN (8x8) | 250/Tray |

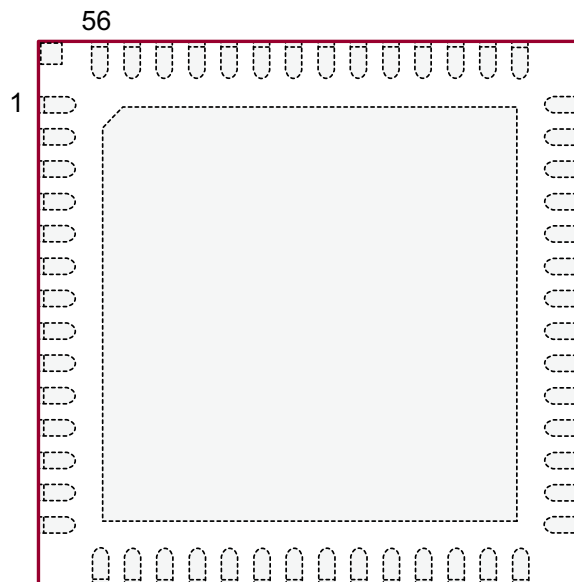
-G indicates package is RoHS compliant ('Green')



Product Summary

| BV_{DSS}/BV_{DGS} (V) | | $R_{DS(ON)}$ (max) (Ω) | |
|----------------------------|-----------|------------------------------------|-----------|
| N-Channel | P-Channel | N-Channel | P-Channel |
| 200 | -200 | 8.0 | 9.5 |

Pin Configuration



56-Lead QFN (K6)
Top View

Absolute Maximum Ratings

| Parameter | Value |
|-----------------------------------|-----------------|
| Drain-to-source voltage | BV_{DSS} |
| Drain-to-gate voltage | BV_{DGS} |
| Operating and storage temperature | -55°C to +150°C |

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

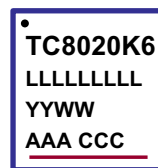
* Distance of 1.6mm from case for 10 seconds.

Thermal Characteristics

| Package | θ_{ja} |
|------------------|---------------|
| 56-Lead QFN (K6) | 27°C/W |

Note:
1.0oz, 4-layer, 3"x4" PCB

Package Marking



- L = Lot Number
- YY = Year Sealed
- WW = Week Sealed
- A = Assembler ID
- C = Country of Origin
- ___ = "Green" Packaging

Package may or may not include the following marks: Si or

56-Lead QFN (K6)

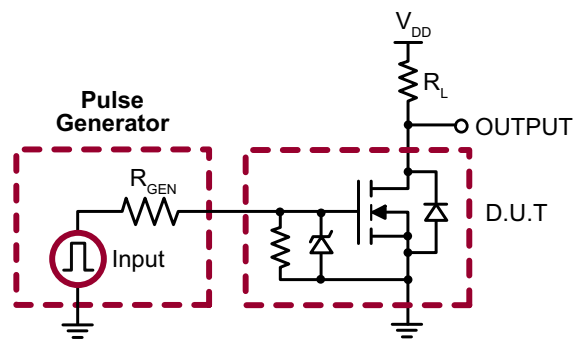
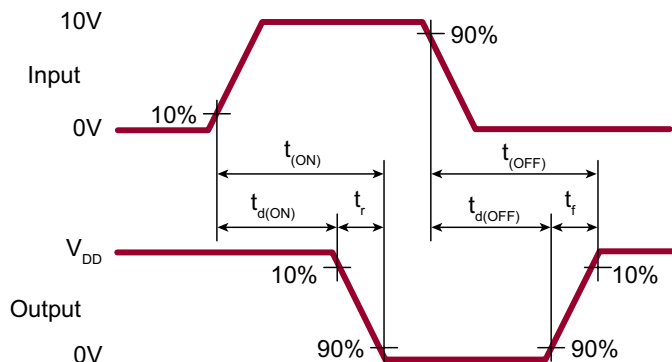
N-Channel Electrical Characteristics ($T_A = 25^\circ\text{C}$ unless otherwise specified)

| Sym | Parameter | Min | Typ | Max | Units | Conditions |
|---------------------|--|------|-----|------|------------|---|
| BV_{DSS} | Drain-to-source breakdown voltage | 200 | - | - | V | $V_{GS} = 0V, I_D = 1.0mA$ |
| $V_{GS(th)}$ | Gate threshold voltage | 1.0 | - | 2.4 | V | $V_{GS} = V_{DS}, I_D = 1.0mA$ |
| $\Delta V_{GS(th)}$ | Change in $V_{GS(th)}$ with temperature | - | - | -4.5 | mV/°C | $V_{GS} = V_{DS}, I_D = 1.0mA$ |
| R_{GS} | Gate-to-source shunt resistor | 5.0 | - | 26 | K Ω | $I_{GS} = 100\mu A$ |
| VZ_{GS} | Gate-to-source Zener voltage | 13.2 | - | 25 | V | $I_{GS} = 2.0mA$ |
| I_{DSS} | Zero gate voltage drain current | - | - | 10.0 | μA | $V_{DS} = \text{Max rating}, V_{GS} = 0V$ |
| | | - | - | 1.0 | mA | $V_{DS} = 0.8 \text{ Max Rating}, V_{GS} = 0V, T_A = 125^\circ\text{C}$ |
| $I_{D(ON)}$ | On-state drain current | 1.2 | 1.8 | - | A | $V_{GS} = 4.5V, V_{DS} = 25V$ |
| | | 2.0 | 3.2 | - | | $V_{GS} = 10V, V_{DS} = 25V$ |
| $R_{DS(ON)}$ | Static drain-to-source on-state resistance | - | 6.0 | 9.0 | Ω | $V_{GS} = 4.5V, I_D = 150mA$ |
| | | - | 5.3 | 8.0 | | $V_{GS} = 10V, I_D = 1.0A$ |
| $\Delta R_{DS(ON)}$ | Change in $R_{DS(ON)}$ with temperature | - | - | 1.0 | %/°C | $V_{GS} = 10V, I_D = 1.0A$ |
| G_{FS} | Forward transconductance | 400 | - | - | mmho | $V_{DS} = 25V, I_D = 500mA$ |
| C_{ISS} | Input capacitance | - | 50 | - | pF | $V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz$ |
| C_{OSS} | Common source output capacitance | - | 18 | - | | |
| C_{RSS} | Reverse transfer capacitance | - | 7.0 | - | | |
| $t_{d(ON)}$ | Turn-on delay time | - | - | 10 | ns | $V_{DD} = 25V, I_D = 500mA, R_{GEN} = 25\Omega$ |
| t_r | Rise time | - | - | 15 | | |
| $t_{d(OFF)}$ | Turn-off delay time | - | - | 20 | | |
| t_f | Fall time | - | - | 15 | | |
| V_{SD} | Diode forward voltage drop | - | - | 1.8 | V | $V_{GS} = 0V, I_{SD} = 500mA$ |
| t_{rr} | Reverse recovery time | - | 300 | - | ns | $V_{GS} = 0V, I_{SD} = 500mA$ |

Notes:

1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

N-Channel Switching Waveforms and Test Circuit



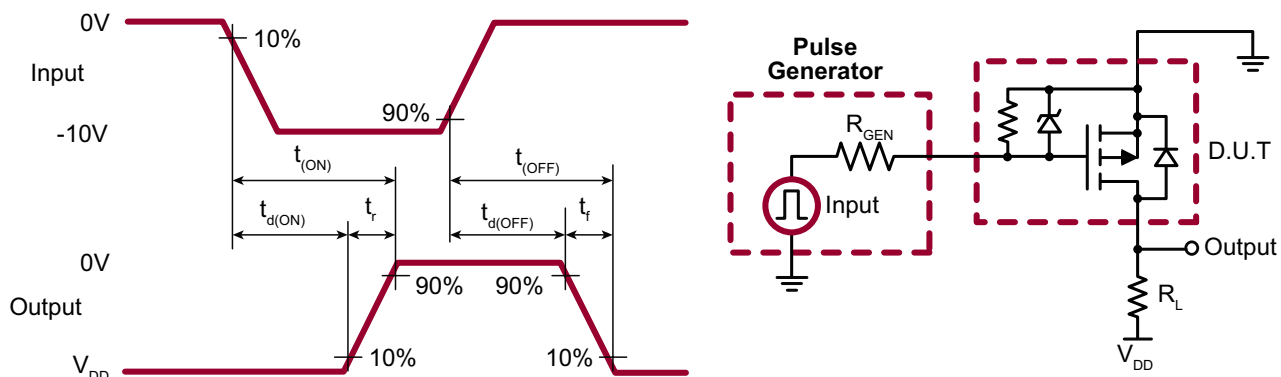
P-Channel Electrical Characteristics ($T_A = 25^\circ\text{C}$ unless otherwise specified)

| Sym | Parameter | Min | Typ | Max | Units | Conditions |
|---------------------|--|-------|-------|-------|------------|---|
| BV_{DSS} | Drain-to-source breakdown voltage | -200 | - | - | V | $V_{GS} = 0V, I_D = -1.0mA$ |
| $V_{GS(th)}$ | Gate threshold voltage | -1.0 | - | -2.4 | V | $V_{GS} = V_{DS}, I_D = -1.0mA$ |
| $\Delta V_{GS(th)}$ | Change in $V_{GS(th)}$ with temperature | - | - | 4.5 | mV/°C | $V_{GS} = V_{DS}, I_D = -1.0mA$ |
| R_{GS} | Gate-to-source shunt resistor | 5.0 | - | 26 | K Ω | $I_{GS} = -100\mu A$ |
| VZ_{GS} | Gate-to-source Zener voltage | -13.2 | - | -24.0 | V | $I_{GS} = -2.0mA$ |
| I_{DSS} | Zero gate voltage drain current | - | - | -10 | μA | $V_{DS} = \text{Max rating}, V_{GS} = 0V$ |
| | | - | - | -1.0 | mA | $V_{DS} = 0.8 \text{ Max Rating}, V_{GS} = 0V, T_A = 125^\circ\text{C}$ |
| $I_{D(ON)}$ | On-state drain current | -0.80 | -1.25 | - | A | $V_{GS} = -4.5V, V_{DS} = -25V$ |
| | | -2.00 | -2.80 | - | | $V_{GS} = -10V, V_{DS} = -25V$ |
| $R_{DS(ON)}$ | Static drain-to-source on-state resistance | - | 7.0 | 10 | Ω | $V_{GS} = -4.5V, I_D = -150mA$ |
| | | - | 6.5 | 9.5 | | $V_{GS} = -10V, I_D = -1.0A$ |
| $\Delta R_{DS(ON)}$ | Change in $R_{DS(ON)}$ with temperature | - | - | 1.0 | %/°C | $V_{GS} = -10V, I_D = -1.0A$ |
| G_{FS} | Forward transconductance | 400 | - | - | mmho | $V_{DS} = -25V, I_D = -500mA$ |
| C_{ISS} | Input capacitance | - | 55 | - | pF | $V_{GS} = 0V, V_{DS} = -25V, f = 1.0MHz$ |
| C_{OSS} | Common source output capacitance | - | 20 | - | | |
| C_{RSS} | Reverse transfer capacitance | - | 8.0 | - | | |
| $t_{d(ON)}$ | Turn-on delay time | - | - | 10 | ns | $V_{DD} = -25V, I_D = -1.0A, R_{GEN} = 25\Omega$ |
| t_r | Rise time | - | - | 15 | | |
| $t_{d(OFF)}$ | Turn-off delay time | - | - | 20 | | |
| t_f | Fall time | - | - | 15 | | |
| V_{SD} | Diode forward voltage drop | - | - | -1.8 | V | $V_{GS} = 0V, I_{SD} = -500mA$ |
| t_{rr} | Reverse recovery time | - | 300 | - | ns | $V_{GS} = 0V, I_{SD} = -500mA$ |

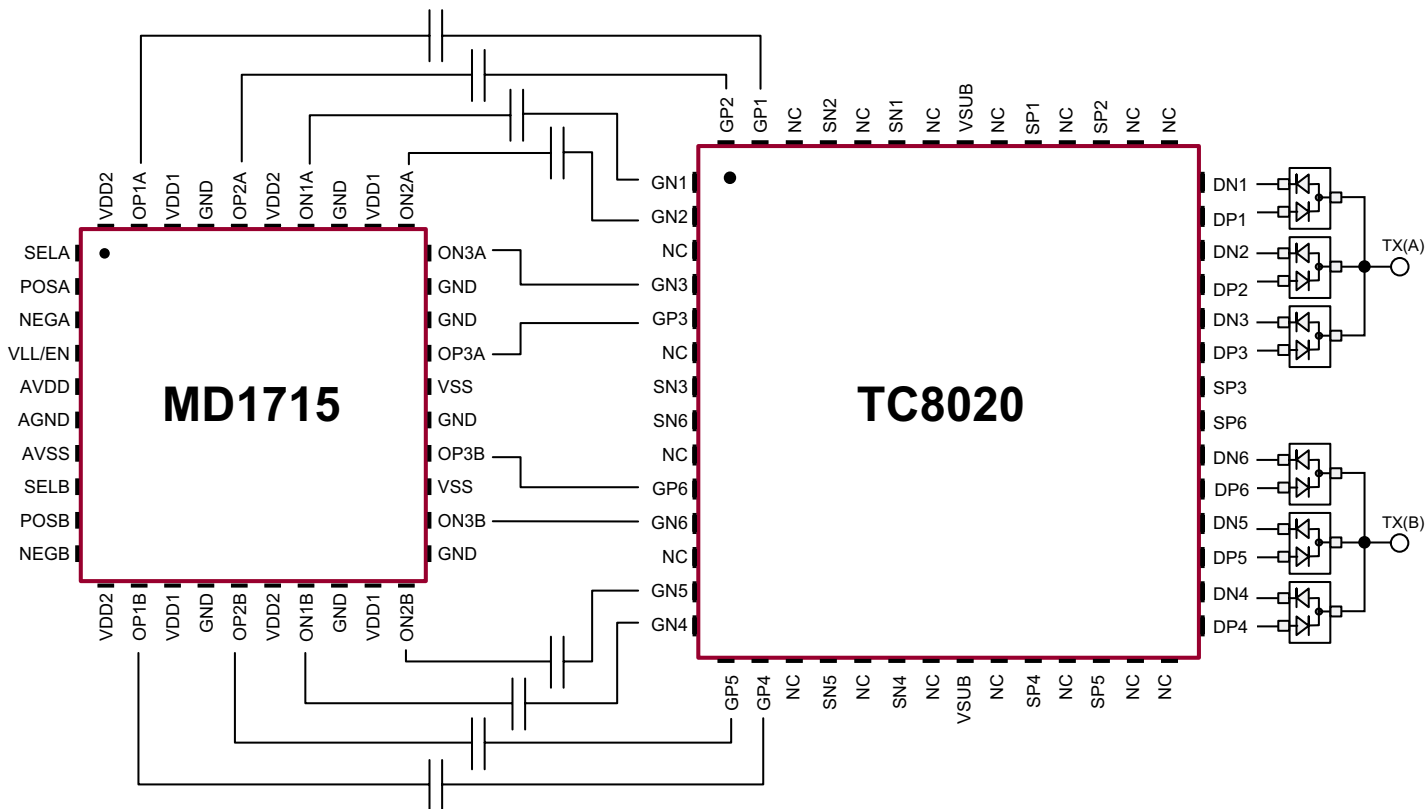
Notes:

1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

P-Channel Switching Waveforms and Test Circuit



Circuit Pin Layout



Pin Description

| Pin | Function | Description |
|-----|----------|----------------------|
| 1 | GN1 | Gate of N-MOSFET 1 |
| 2 | GN2 | Gate of N-MOSFET 2 |
| 3 | NC | No Connection |
| 4 | GN3 | Gate of N-MOSFET 3 |
| 5 | GP3 | Gate of P-MOSFET 3 |
| 6 | NC | No Connection |
| 7 | SN3 | Source of N-MOSFET 3 |
| 8 | SN6 | Source of N-MOSFET 6 |
| 9 | NC | No Connection |
| 10 | GP6 | Gate of P-MOSFET 6 |
| 11 | GN6 | Gate of N-MOSFET 6 |
| 12 | NC | No Connection |
| 13 | GN5 | Gate of N-MOSFET 5 |
| 14 | GN4 | Gate of N-MOSFET 4 |
| 15 | GP5 | Gate of P-MOSFET 5 |
| 16 | GP4 | Gate of P-MOSFET 4 |
| 17 | NC | No Connection |
| 18 | SN5 | Source of N-MOSFET 5 |

Pin Description (cont.)

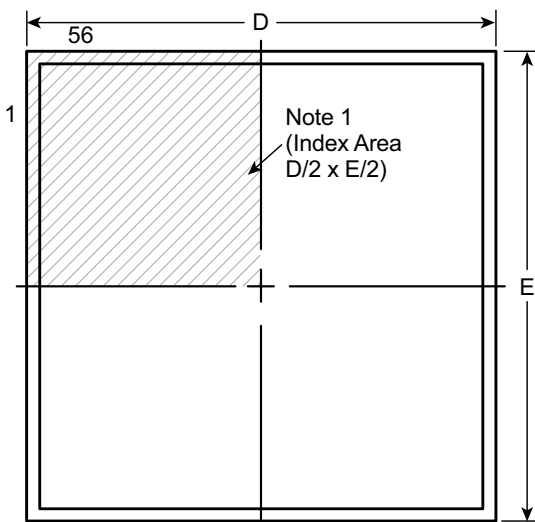
| Pin | Function | Description |
|-----|----------|--|
| 19 | NC | No Connection |
| 20 | SN4 | Source of N-MOSFET 4 |
| 21 | NC | No Connection |
| 22 | VSUB | Die attachment substrate, must be grounded externally. |
| 23 | NC | No Connection |
| 24 | SP4 | Source of P-MOSFET 4 |
| 25 | NC | No Connection |
| 26 | SP5 | Source of P-MOSFET 5 |
| 27 | NC | No Connection |
| 28 | NC | No Connection |
| 29 | DP4 | Drain of P-MOSFET 4 |
| 30 | DN4 | Drain of N-MOSFET 4 |
| 31 | DP5 | Drain of P-MOSFET 5 |
| 32 | DN5 | Drain of N-MOSFET 5 |
| 33 | DP6 | Drain of P-MOSFET 6 |
| 34 | DN6 | Drain of N-MOSFET 6 |
| 35 | SP6 | Source of P-MOSFET 6 |
| 36 | SP3 | Source of P-MOSFET 3 |
| 37 | DP3 | Drain of P-MOSFET 3 |
| 38 | DN3 | Drain of N-MOSFET 3 |
| 39 | DP2 | Drain of P-MOSFET 2 |
| 40 | DN2 | Drain of N-MOSFET 2 |
| 41 | DP1 | Drain of P-MOSFET 1 |
| 42 | DN1 | Drain of N-MOSFET 1 |
| 43 | NC | No Connection |
| 44 | NC | No Connection |
| 45 | SP2 | Source of P-MOSFET 2 |
| 46 | NC | No Connection |
| 47 | SP1 | Source of P-MOSFET 1 |
| 48 | NC | No Connection |
| 49 | VSUB | Die attachment substrate, must be grounded externally. |
| 50 | NC | No Connection |
| 51 | SN1 | Source of N-MOSFET 1 |
| 52 | NC | No Connection |
| 53 | SN2 | Source of N-MOSFET 2 |
| 54 | NC | No Connection |
| 55 | GP1 | Gate of P-MOSFET 1 |
| 56 | GP2 | Gate of P-MOSFET 2 |

Note:

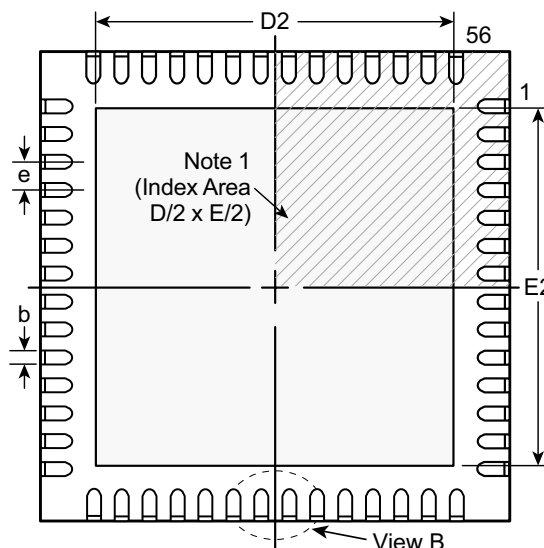
Thermal Pad must be grounded externally.

56-Lead QFN Package Outline (K6)

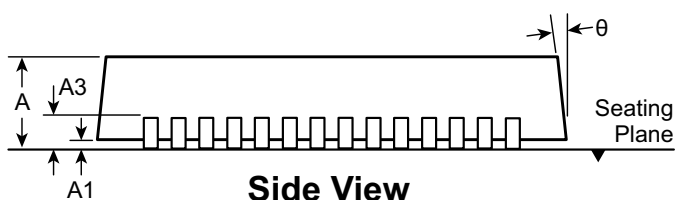
8.00x8.00mm body, 1.00mm height (max), 0.50mm pitch



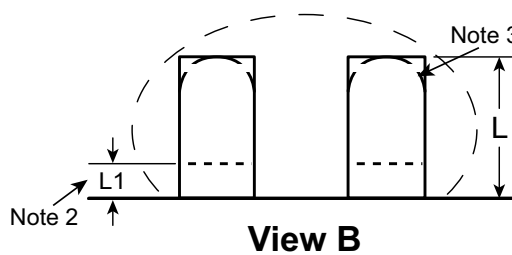
Top View



Bottom View



Side View



View B

Notes:

1. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.
2. Depending on the method of manufacturing, a maximum of 0.15mm pullback (L1) may be present.
3. The inner tip of the lead may be either rounded or square.

| Symbol | A | A1 | A3 | b | D | D2 | E | E2 | e | L | L1 | θ | |
|----------------|-----|------|------|----------|------|-------|-------|-------|-------|----------|------|------|-----|
| Dimension (mm) | MIN | 0.80 | 0.00 | 0.20 REF | 0.18 | 7.85* | 2.75 | 7.85* | 2.75 | 0.50 BSC | 0.30 | 0.00 | 0° |
| | NOM | 0.90 | 0.02 | | 0.25 | 8.00 | 5.70 | 8.00 | 5.70 | | 0.40 | - | - |
| | MAX | 1.00 | 0.05 | | 0.30 | 8.15* | 6.70† | 8.15* | 6.70† | | 0.50 | 0.15 | 14° |

JEDEC Registration MO-220, Variation VLLD-2, Issue K, June 2006.

* This dimension is not specified in the JEDEC drawing.

† This dimension differs from the JEDEC drawing.

Drawings are not to scale.

Supertex Doc.#: DSPD-56QFNK68X8P050, Version A031010.

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to <http://www.supertex.com/packaging.html>.)

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