Dual Half Bridge Driver

■ GENERAL DESCRIPTION

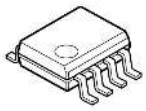
The NJW4810A is a general-purpose dual half bridge driver capable of supplying 1A current. Output duty=100% can be operated by high side P channel MOSFET. It can use as a full bridge driver by connecting VDD1 and VDD2.

The internal gate driver drives high-side/low-side power MOSFET; therefore, it is able to fast switching.

Additionally, it has protection features such as over current protection and thermal shutdown. And in the case of failure, it can output a fault flag.

It is suitable for power switching applications of DSP/micro controller.

■ PACKAGE OUTLINE

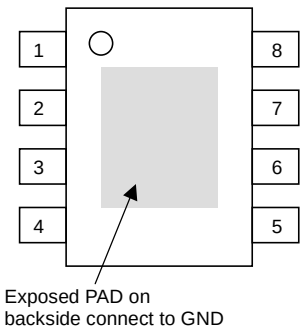


NJW4810AGM1

■ FEATURES

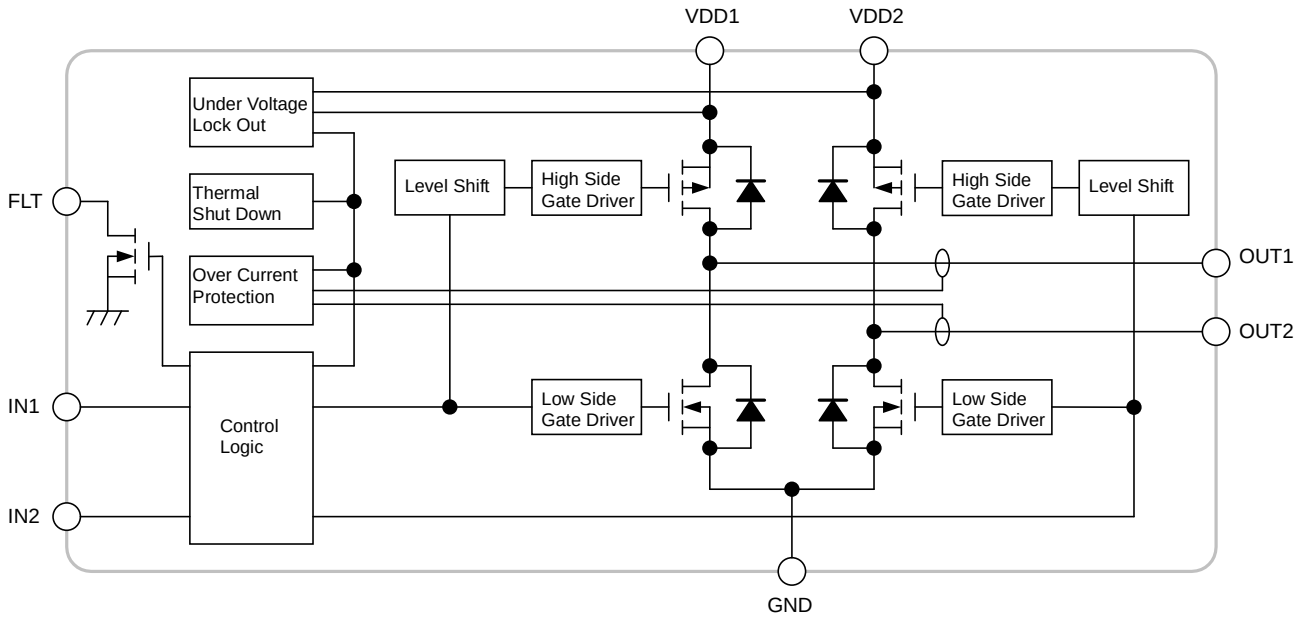
- Output Switch Current ±1A
- Operating Voltage 8.0V to 40V
- Thermal Shut Down
- Over Current Protection
- Under Voltage Lockouts
- Fault Indicator Output
- High Heat Radiation Package
- Package Outline HSOP8

■PIN CONFIGURATION



1. IN2
2. IN1
3. VDD1
4. OUT1
5. GND
6. OUT2
7. VDD2
8. FLT

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

PARAMETER	SYMBOL	MAXIMUM RATINGS	UNIT	REMARKS
Supply Voltage	V^+1, V^+2	+45	V	VDD1-GND pin VDD2-GND pin
Input Voltage	V_{IN}	–0.3 to +6	V	IN1-GND pin IN2-GND pin
FLT pin Voltage	V_{FLT}	–0.3 to +6	V	FLT-GND pin
FLT pin Current	I_{FLT}	1	mA	
Power Dissipation	P_D	0.9 (*1) 3.1 (*2)	W	–
Operating Junction Temperature	T_j	–40 to +150	°C	–
Operating Temperature Range	T_{opr}	–40 to +85	°C	–
Storage Temperature Range	T_{stg}	–50 to +150	°C	–

(*1): Mounted on glass epoxy board. (76.2×114.3×1.6mm:based on EIA/JDEC standard, 2Layers)

(*2): Mounted on glass epoxy board. (76.2×114.3×1.6mm:based on EIA/JDEC standard, 4Layers)

(For 4Layers: Applying 74.2×74.2mm inner Cu area and a thermal via hole to a board based on JEDEC standard JESD51-5)

■ RECOMMENDED OPERATING CONDITIONS (Ta=25°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	REMARKS
Operating Voltage	V^+1 V^+2	8	–	40	V	VDD1-GND pin VDD2-GND pin
Output Switch Current	I_{OM}	0	–	1	A	OUT1, OUT2 pin
Input Voltage	V_{IN}	0	–	5.5	V	IN1-GND pin, IN2-GND pin
FLT pin Voltage	V_{FLT}	0	–	5.5	V	FLT-GND pin

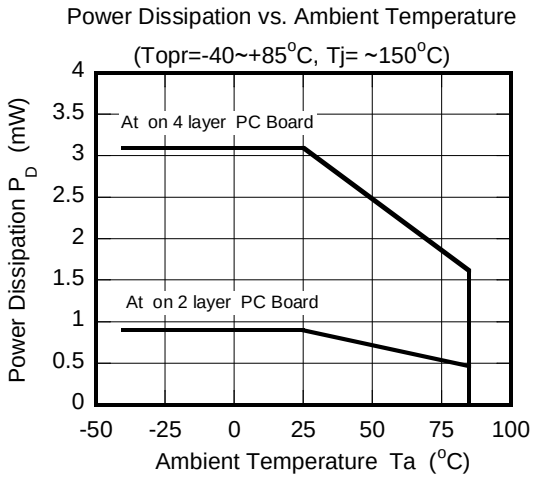
■ THERMAL CHARACTERISTICS

PARAMETER	SYMBOL	THERMAL RESISTANCE	UNIT
Junction-to-Ambient Temperature	θja	139 (*1) 40 (*2)	°C/W
Junction-to-Case	ψjt	19 (*1) 3.7 (*2)	°C/W

(*1): Mounted on glass epoxy board. (76.2×114.3×1.6mm:based on EIA/JDEC standard, 2Layers)

(*2): Mounted on glass epoxy board. (76.2×114.3×1.6mm:based on EIA/JDEC standard, 4Layers)

(For 4Layers: Applying 74.2×74.2mm inner Cu area and a thermal via hall to a board based on JEDEC standard JESD51-5)



■ ELECTRICAL CHARACTERISTICS (Unless otherwise noted, V^+1= V^+2=12V, Ta=25°C)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
General Characteristics							
Quiescent Current 1 (Operating)	I_{Q1}	V_{IN1}=V_{IN2}=0V	V^+1	–	0.9	1.7	mA
			V^+2	–	0.3	0.8	
Quiescent Current 2 (Switching)	I_{Q2}	V_{IN1}=V_{IN2}=0V to 3V, f_{IN1}= f_{IN2}=750kHz antiphase 50% Duty Cycle	V^+1	–	3.7	5.5	mA
			V^+2	–	3.2	5.0	
Output Block							
High-side SW ON Resistance	R_{DSH}	$I_{OSOURCE}$=600mA		–	1.0	1.8	Ω
Low-side SW ON Resistance	R_{DSL}	I_{OSINK}=600mA		–	0.75	1.3	Ω
Over Current Limit (*3)	I_{LIMIT}	High-side and Low-side		1	2	3	A
Over Current Limit Protection Time (*3)	t_{OCP}	High-side and Low-side R_{FLT}=47kΩ, V_{FLT}=5V		15	30	80	ms
Output Rise Time	tr	V_{IN1}=V_{IN2}= 0 to 3V		–	3	–	ns
Output Fall Time	tf	V_{IN1}=V_{IN2}= 3 to 0V		–	5	–	ns
Dead Time	Dt	V_{IN1}=V_{IN2}= 0 to 3V		–	50	–	ns
Output Rise Delay Time	t_{d_ON}	V_{IN1}=V_{IN2}= 0 to 3V		–	120	–	ns
Output Fall Delay Time	t_{d_OFF}	V_{IN1}=V_{IN2}= 3 to 0V		–	120	–	ns
High-side SW Leak Current at OFF state	$I_{OLEAKOUTH}$	V^+1=V^+2=5.5V, V_{OUT1}=V_{OUT2}=0V		–	–	1	μA
Low-side SW Leak Current at OFF state	$I_{OLEAKOUTL}$	V^+1=V^+2=5.5V, V_{OUT1}=V_{OUT2}=5.5V		–	–	1	μA
OUT pin – VDD pin Potential Difference	V_{PDOV}	I_{ORH}=1A, V^+1=V^+2=5.5V		–	0.9	1.5	V
GND pin – OUT pin Potential Difference	V_{PDGO}	I_{ORL}=1A, V^+1=V^+2=5.5V		–	0.9	1.5	V

(*3): The overcurrent detection time may take 1μs (max). During this time overcurrent protection circuit does not detect an overcurrent. Therefore, you should control the pulse width and frequency of IN1/IN2 pin to prevent a continuous over-current in short-term.

Input Circuit Block						
Input pin High Voltage	V_{IHIN}		2.0	–	5.5	V
Input pin Low Voltage	V_{ILIN}		0	–	0.8	V
Input pin sink current	I_{IIN}	V_{IN1}=V_{IN2}= 5.5V	–	0.01	1	μA
Under Voltage Lockout (UVLO) Block						
UVLO Release Voltage (*4)	V_{UVLO2}	V^+1=V^+2=L→H	6.3	7.0	7.7	V
UVLO Operation Voltage (*4)	V_{UVLO1}	V^+1=V^+2=H→L	6.0	6.7	7.4	V
UVLO Hysteresis Voltage	ΔV_{UVLO}	V_{UVLO2}-V_{UVLO1}	–	0.3	–	V

(*4): UVLO operates at each line (V^+1 and V^+2)

Fault Function (FLT pin)						
Low Level Output Voltage	V_{LFLT}	I_{FLT}=500μA	–	0.25	0.5	V
OFF Leak Current	$I_{OLEAKFLT}$	V^+1=V^+2=5.5V, V_{FLT}=5.5V	–	–	1	μA

■ PIN OPERATION TABLE

INPUT			OUTPUT					Mode
IN1	IN2	VDD1, VDD2	FLT	OUT1 High-side SW	OUT1 Low-side SW	OUT2 High-side SW	OUT2 Low-side SW	
L	L	V^+1 and $V^+2 \geq V_{UVLO2}$	ON	OFF	ON	OFF	ON	Normal
L	H	V^+1 and $V^+2 \geq V_{UVLO2}$	ON	OFF	ON	ON	OFF	Normal
H	L	V^+1 and $V^+2 \geq V_{UVLO2}$	ON	ON	OFF	OFF	ON	Normal
H	H	V^+1 and $V^+2 \geq V_{UVLO2}$	ON	ON	OFF	ON	OFF	Normal
—	—	V^+1 or $V^+2 < V_{UVLO1}$	OFF	OFF	OFF	OFF	OFF	UVLO

INPUT			OUTPUT					Mode
Tj	I_{OUT1}	I_{OUT2}	FLT	OUT1 High-side SW	OUT1 Low-side SW	OUT2 High-side SW	OUT2 Low-side SW	
$Tj > 150°C$	—	—	OFF	OFF	OFF	OFF	OFF	TSD (*5)
—	$I_{OUT1} \geq I_{LIMIT}$	—	OFF	OFF	OFF	OFF	OFF	OCP (*6)
—	—	$I_{OUT2} \geq I_{LIMIT}$	OFF	OFF	OFF	OFF	OFF	OCP (*6)

(*5): After the TSD function operation, when the junction temperature becomes less than 125°C, NJW4810A returns to normal mode.

(*6): NJW4810A returns to normal mode after the elapse of a certain period of time after the OCP function operating.

■ TIMING CHART

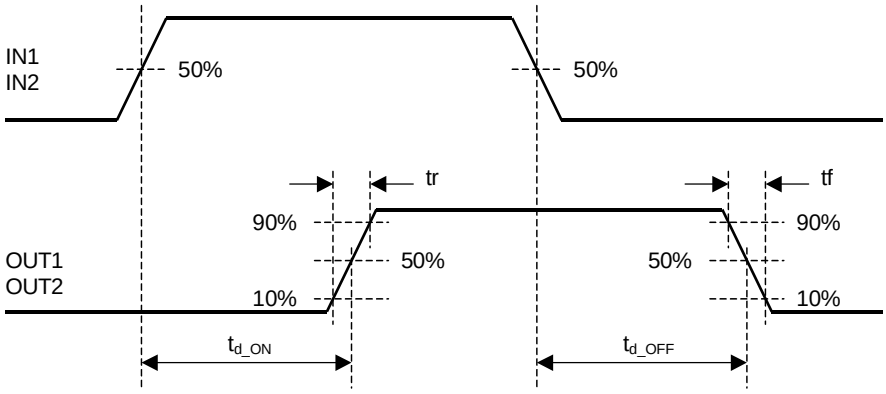


Fig1. Output Rise/Fall Time, PWM Rise/Fall Delay Time

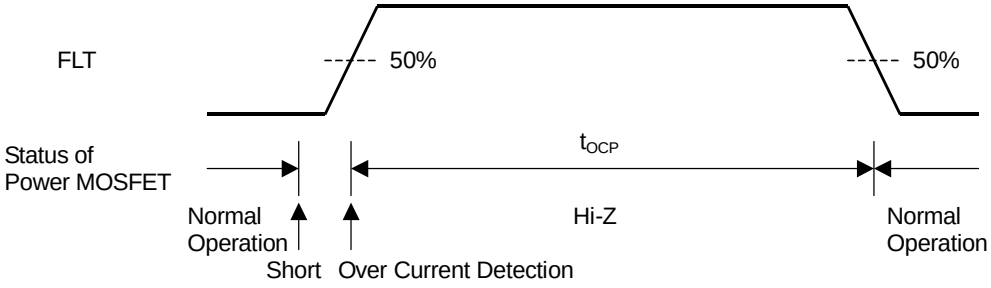


Fig2. Over Current Limit Protection Time

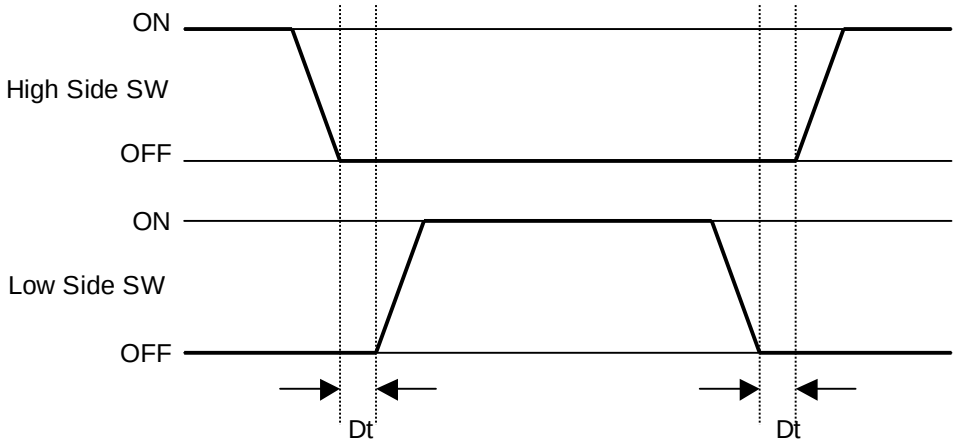
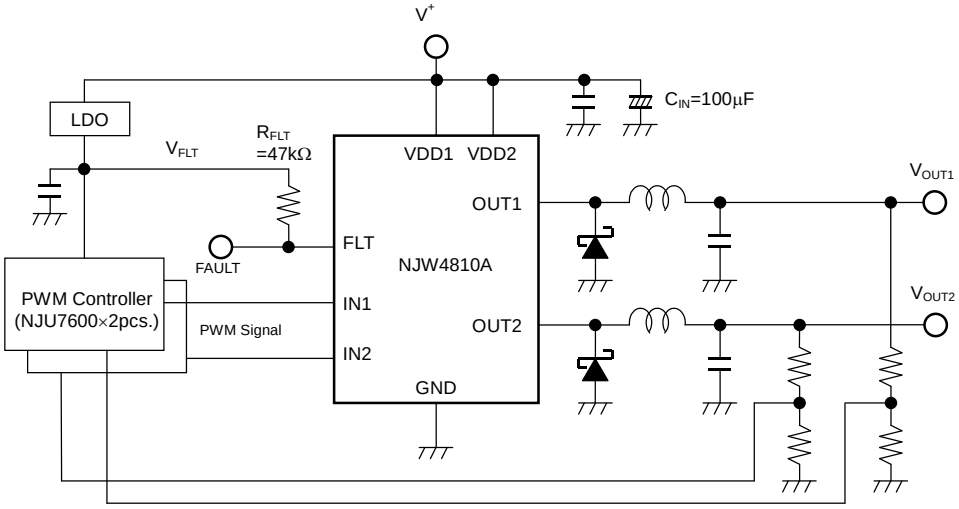
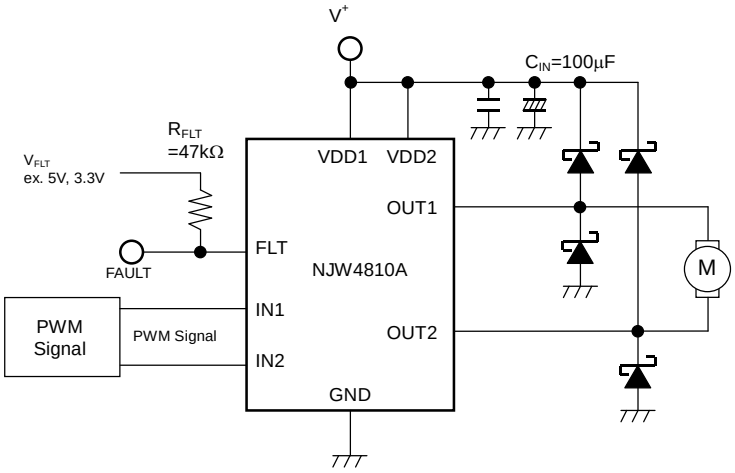


Fig3. SW Operation and Dead Time

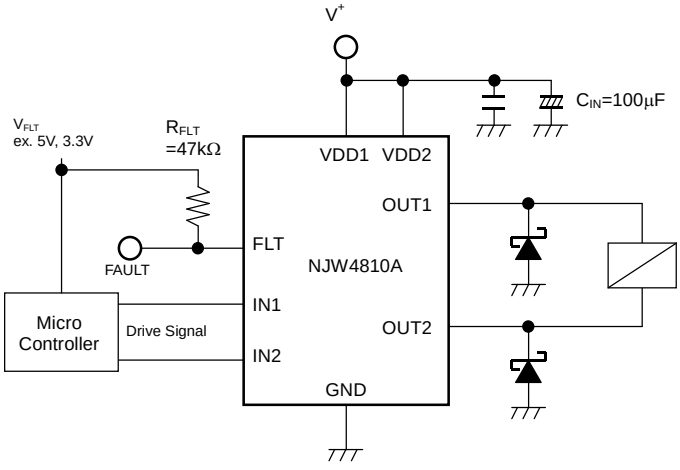
■ TYPICAL APPLICATIONS



2ch Synchronous PWM step down switching regulator



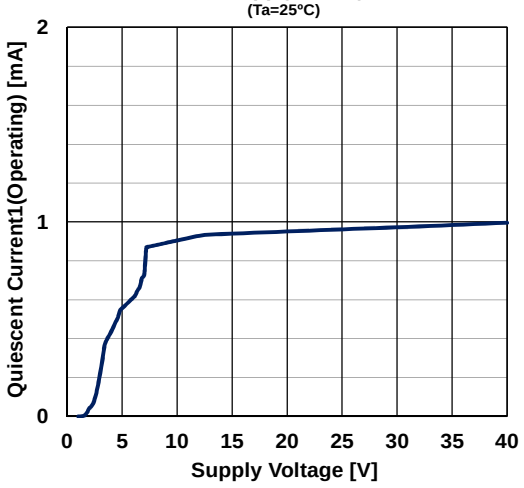
Full bridge motor driver



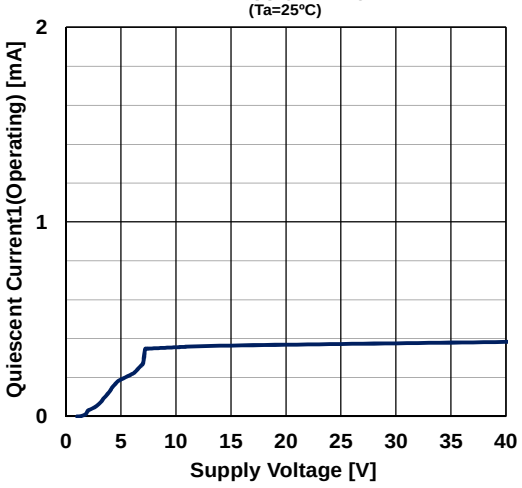
Latch type solenoid driver

■ CHARACTERISTICS

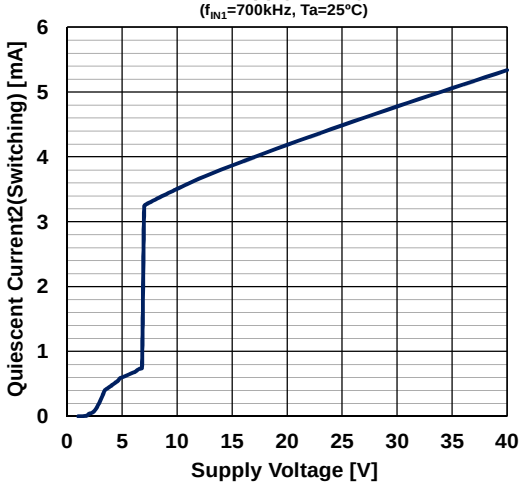
Quiescent Current1(Operating) on V+1
vs. Supply Voltage
(Ta=25ºC)



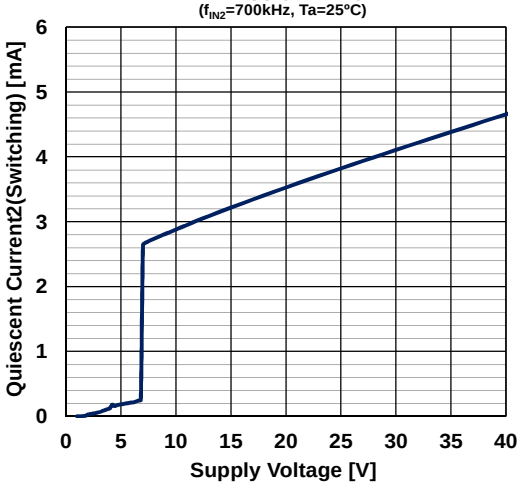
Quiescent Current1(Operating) on V+2
vs. Supply Voltage
(Ta=25ºC)



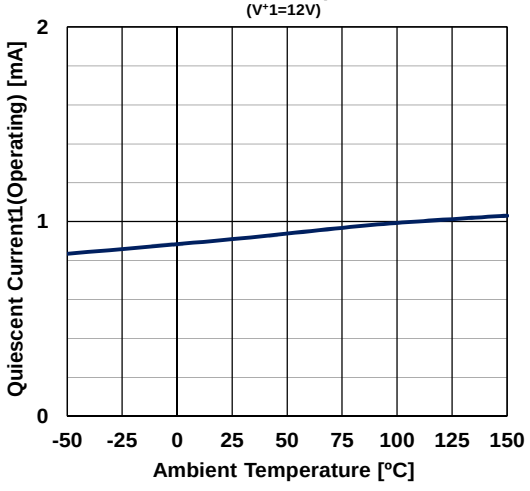
Quiescent Current2(Switching) on V+1
vs. Supply Voltage
(f_{IN1}=700kHz, Ta=25ºC)



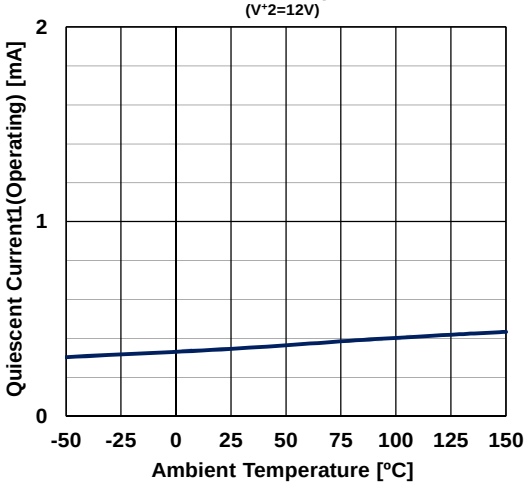
Quiescent Current2(Switching) on V+2
vs. Supply Voltage
(f_{IN2}=700kHz, Ta=25ºC)



Quiescent Current1(Operating) on V+1
vs.Ambient Temperature
(V+1=12V)

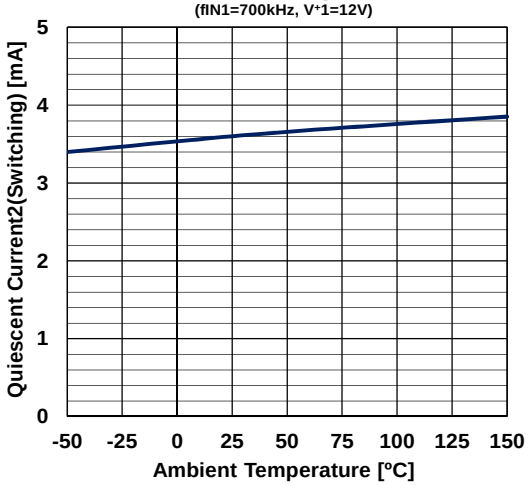


Quiescent Current1(Operating) on V+2
vs.Ambient Temperature
(V+2=12V)

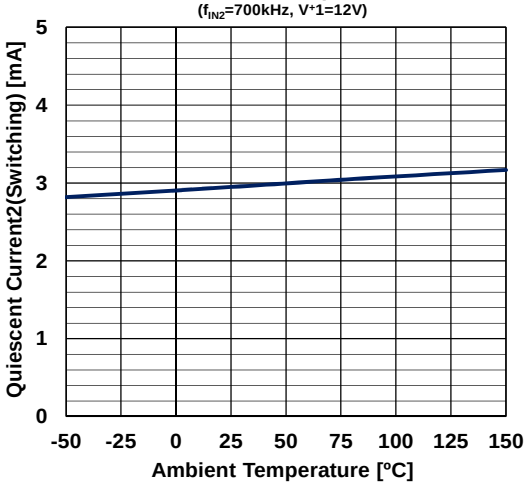


■ CHARACTERISTICS

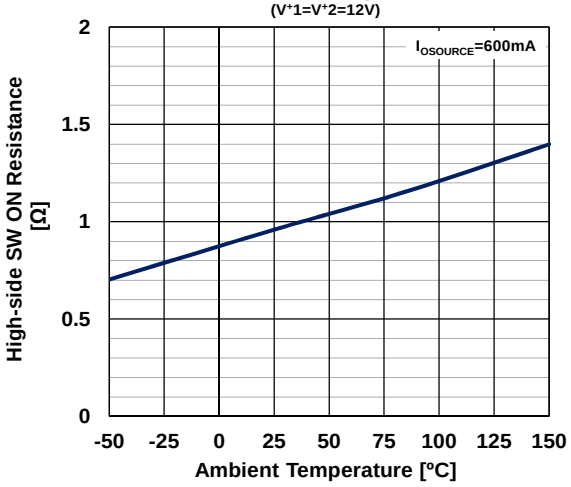
Quiescent Current2(Switching) on V+1
vs.Ambient Temperature
(fIN1=700kHz, V+1=12V)



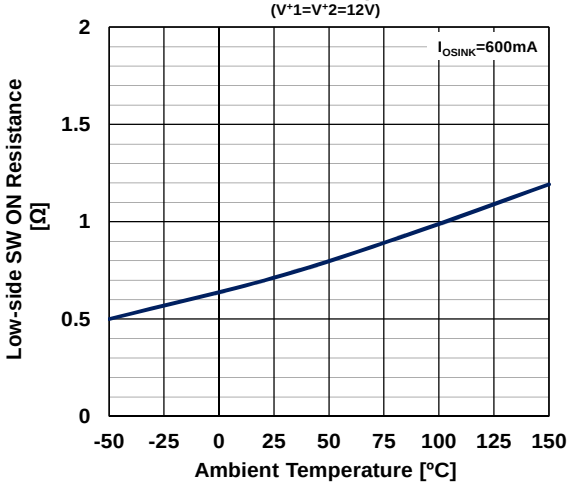
Quiescent Current2(Switching) on V+2
vs.Ambient Temperature
(f_{IN2}=700kHz, V+1=12V)



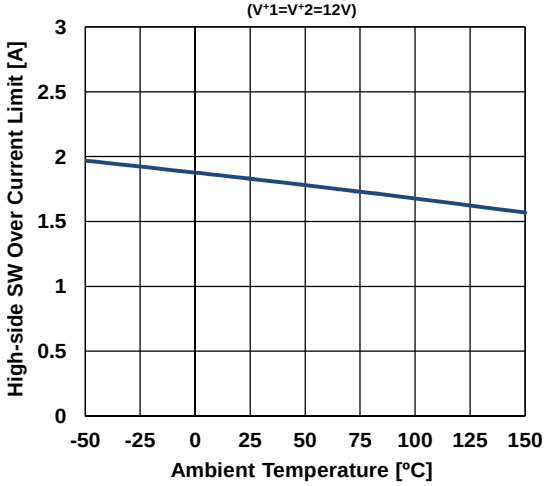
High-side SW ON Resistance
vs.Ambient Temperature
(V+1=V+2=12V)



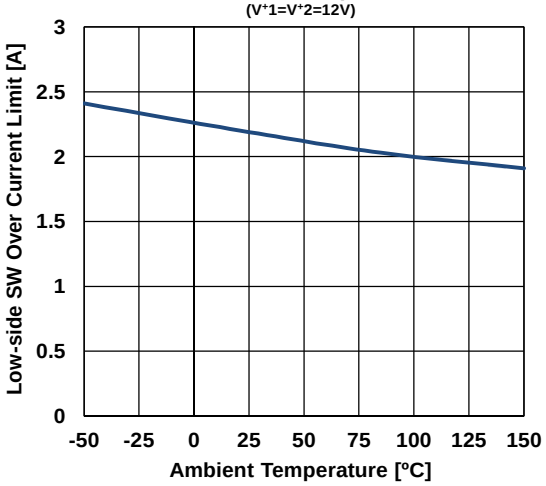
Low-side SW ON Resistance
vs.Ambient Temperature
(V+1=V+2=12V)



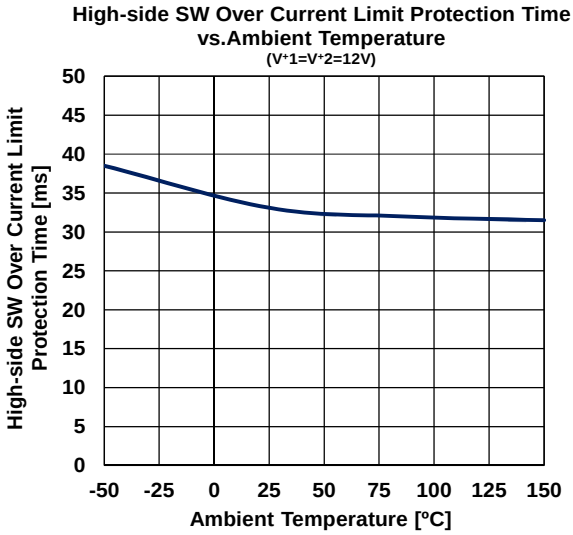
High-side SW Over Current Limit
vs.Ambient Temperature
(V+1=V+2=12V)

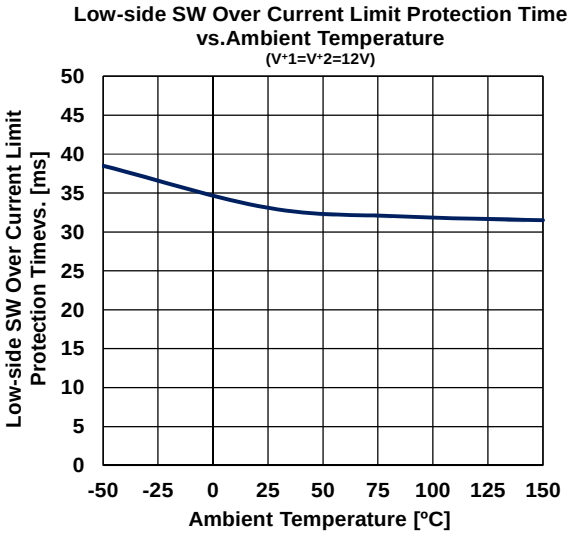


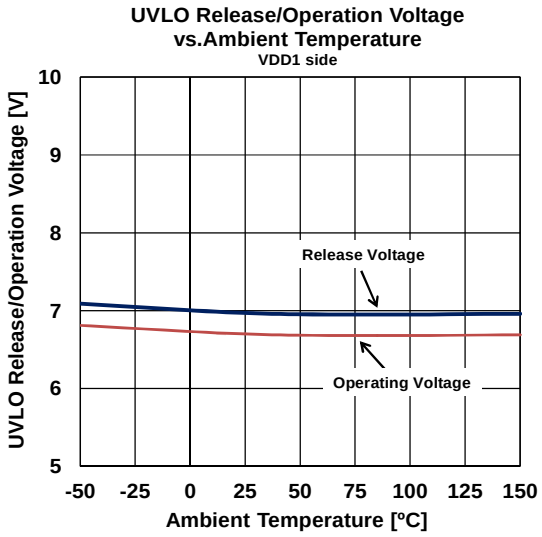
Low-side SW Over Current Limit
vs.Ambient Temperature
(V+1=V+2=12V)

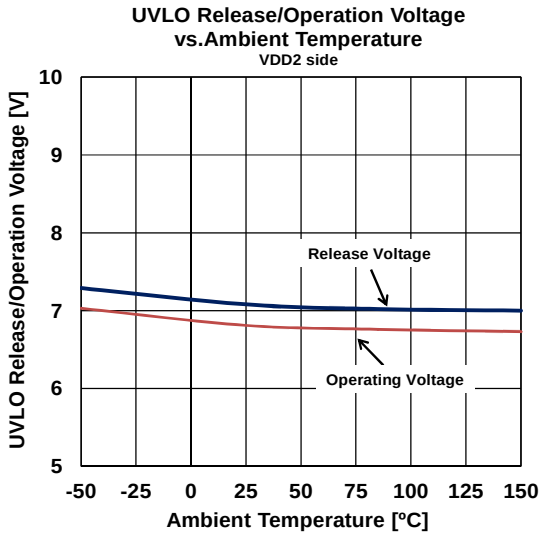


■ CHARACTERISTICS









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