

32-Channel Vacuum Fluorescent Display Driver

Features

- Thirty-two Output Lines
- 90V Output Swing
- Active Pull-down
- Latches on all Outputs
- Up to 6 MHz at $V_{DD} = 5V$
- $-40^{\circ}C$ to $+85^{\circ}C$ Operation

Applications

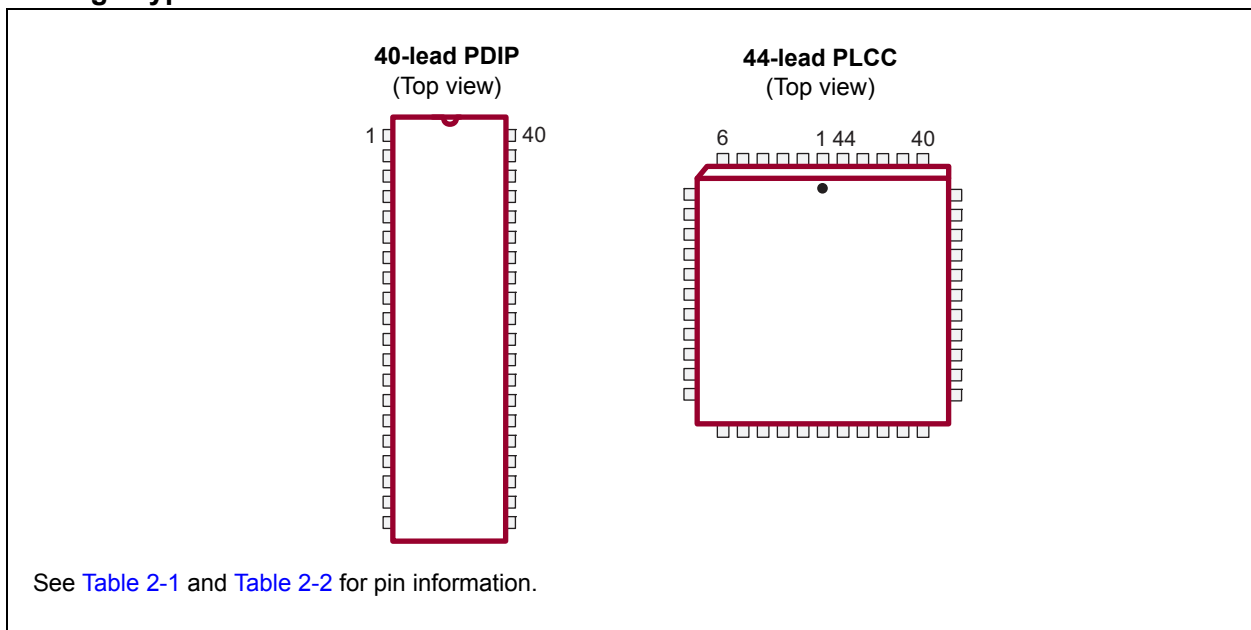
- Vacuum Fluorescent Displays
- DC Plasma Displays

General Description

The HV518 is designed for vacuum fluorescent or DC plasma applications where it can serve as a segment, digit or matrix display driver. Each device has 32 outputs, 32 latches and a 32-bit cascable Shift register.

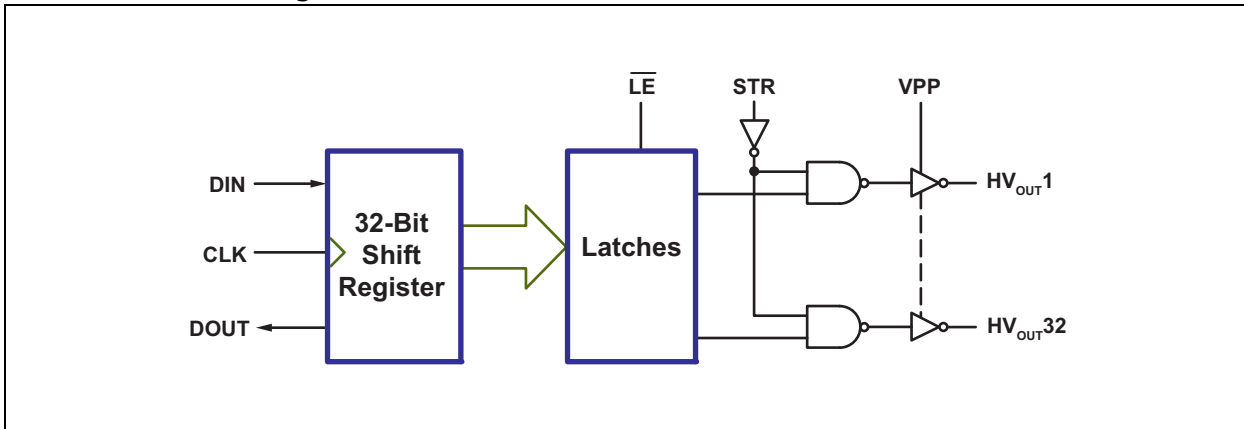
Serial data enters the Shift register on the low-to-high transition of the clock input. With latch enable (\overline{LE}) high, parallel data is transferred to the output buffers through a 32-bit latch. When \overline{LE} is low, the data is stored in the latch. When strobe (STR) is low, all outputs are enabled. If the strobe is high, all outputs are low.

Package Types

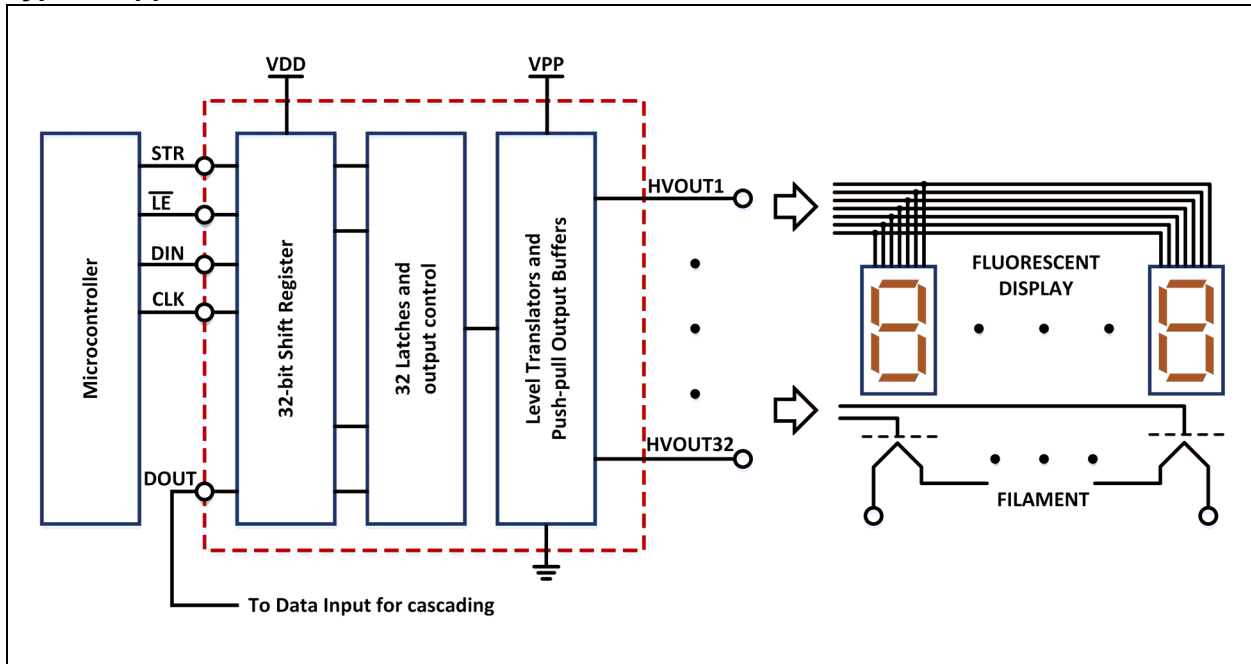


HV518

Functional Block Diagram



Typical Application Circuit



HV518

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

| | |
|--|------------------------|
| Low-voltage Supply Voltage, V_{DD} | -0.5V to +6V |
| High-voltage Supply Voltage, V_{PP} | -0.5V to +90V |
| Logic Input Levels | -0.5V to $V_{DD}+0.5V$ |
| Operating Ambient Temperature, T_A | -40°C to +85°C |
| Storage Temperature, T_S | -65°C to +150°C |
| Continuous Total Power Dissipation: | |
| 40-lead PDIP (Note 1 , Note 2) | 1200 mW |
| 44-lead PLCC (Note 1 , Note 2) | 1200 mW |

† **Notice:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

- Note 1:** Duty cycle is limited by the total power dissipated in the package.
Note 2: For operations above 25°C ambient, derate linearly to 85°C at 20 mW/°C.

RECOMMENDED OPERATING CONDITIONS

| Electrical Specifications: $T_A = 25^\circ\text{C}$ unless otherwise indicated. | | | | | | |
|---|--------------|------|------|------|------|--|
| Parameter | Sym. | Min. | Typ. | Max. | Unit | Conditions |
| Logic Supply Voltage | V_{DD} | 4.5 | — | 5.5 | V | |
| High-voltage Supply Voltage | V_{PP} | 8 | — | 80 | V | |
| High-level Input Voltage | V_{IH} | 3.5 | — | — | V | $V_{DD} = 4.5V$ (See Figure 3-1.) |
| Low-level Input Voltage | V_{IL} | — | — | 1 | V | $V_{DD} = 4.5V$ (See Figure 3-1.) |
| High-level Output Current | I_{OH} | -25 | — | — | mA | |
| Low-level Output Current | I_{OL} | — | — | 2 | mA | |
| Clock Frequency | f_{CLK} | — | — | 6 | MHz | $V_{DD} = 4.5V$ (See Figure 3-1.) |
| Pulse Duration, Clock High | $t_{W(CKH)}$ | 83 | — | — | ns | $V_{DD} = 4.5V$ |
| Pulse Duration, Clock Low | $t_{W(CKL)}$ | 83 | — | — | ns | $V_{DD} = 4.5V$ |
| Setup Time, Data before Clock | t_{SU} | 75 | — | — | ns | $V_{DD} = 4.5V$ |
| Hold Time, Data after Clock | t_H | 75 | — | — | ns | $V_{DD} = 4.5V$ |
| Operating Ambient Temperature | T_A | -40 | — | +85 | °C | |

ELECTRICAL CHARACTERISTICS

| Electrical Specifications: Over recommended operating conditions unless otherwise indicated | | | | | | | |
|---|---------------|----------|------|------|---------------|--|---|
| Parameter | Sym. | Min. | Typ. | Max. | Unit | Conditions | |
| Supply Current | I_{DD} | — | — | 10 | mA | $V_{DD} = 5V, f_{CH} = 6 \text{ MHz}$ | |
| Quiescent Supply Current | I_{DDQ} | — | — | 0.5 | mA | $V_{DD} = 5.5V, V_{IN} = 0V$ | |
| Supply Current | I_{PP} | — | — | 12 | mA | Outputs high, $T_A = -40^\circ\text{C}$ | |
| | | — | 7 | 10 | mA | Outputs high, $T_A = 0^\circ\text{C}$ to $+85^\circ\text{C}$ | |
| | | — | — | 500 | μA | Outputs low | |
| HV _{IN} Operating Current | HV Output | V_{OH} | 70 | — | — | V | $I_{OH} = -25\text{mA}$ |
| | Serial Output | | 4.5 | 4.9 | 5 | V | $V_{DD} = 5V, I_{OH} = -20 \mu\text{A}$ |
| LV _{IN} Operating Current | HV Output | V_{OL} | — | — | 5 | V | $I_{OL} = 1 \text{ mA}$ |
| | Serial Output | | — | 0.06 | 0.8 | V | $I_{OL} = 20 \mu\text{A}$ |
| Logic Input Current High | I_{IH} | — | 0.1 | 1 | μA | $V_{IH} = V_{DD}$ | |
| Logic Input Current Low | I_{IL} | — | -0.1 | -1 | μA | $V_{IL} = 0V$ | |

Note 1: The power dissipation is determined by the number of output at ON state and their duty cycles. The total power must not exceed the allowable package power dissipation.

SWITCHING CHARACTERISTICS

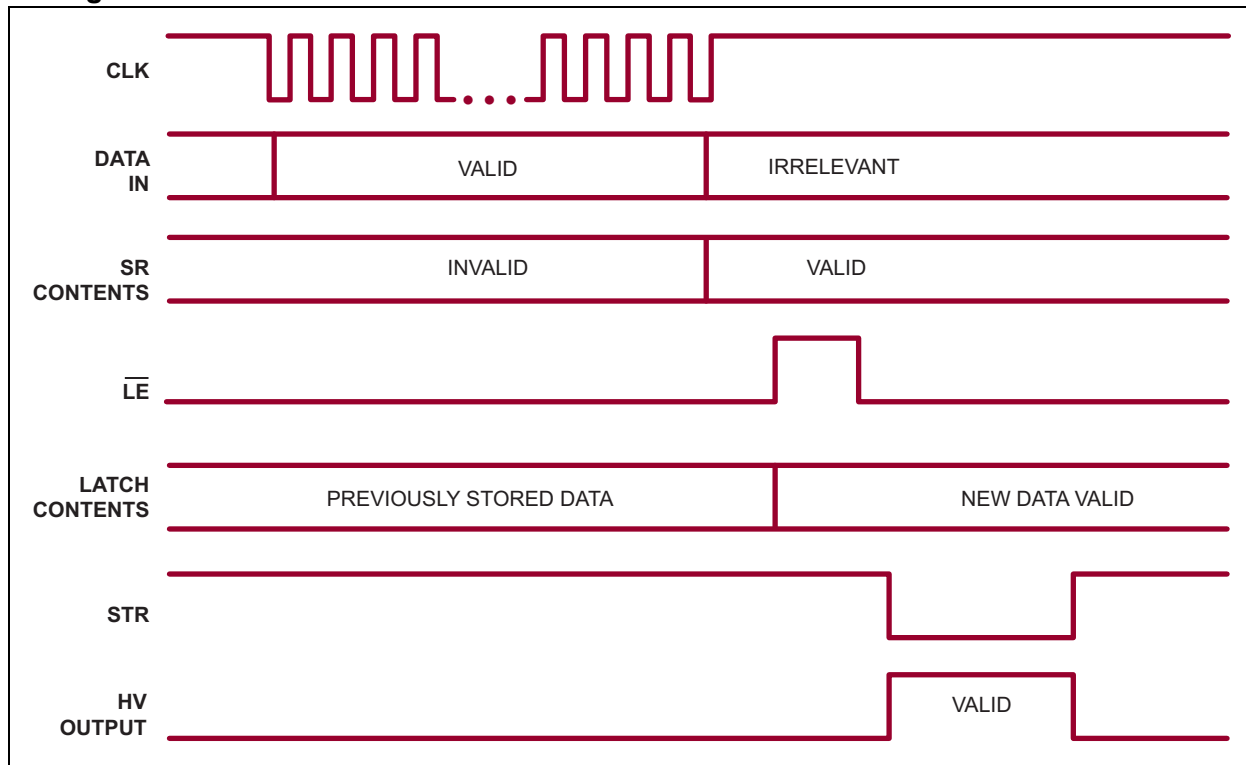
| Electrical Specifications: $V_{PP} = 80V, C_L = 50 \text{ pF}$ and $T_A = 25^\circ\text{C}$ unless otherwise noted. | | | | | | | |
|---|-------------------|-----------|------|------|---------------|---|-----------------------------------|
| Parameter | Sym. | Min. | Typ. | Max. | Unit | Conditions | |
| Delay Time, Clock-to-data Output | t_d | — | — | 600 | ns | $C_L = 15 \text{ pF}$ (See Figure 3-2.) | |
| Delay Time, High-to-low Level, HV Output | From Latch Enable | t_{DHL} | — | — | 1.5 | μs | $V_{DD} = 4.5V$ (See Figure 3-3.) |
| | From Strobe | | — | — | 1 | μs | $V_{DD} = 4.5V$ (See Figure 3-4.) |
| Delay Time, Low-to-high Level, HV Output | From Latch Enable | t_{DLH} | — | — | 1.5 | μs | $V_{DD} = 4.5V$ (See Figure 3-3.) |
| | From Strobe | | — | — | 1 | μs | $V_{DD} = 4.5V$ (See Figure 3-4.) |
| Transition Time, High-to-low Level, HV Output | t_{THL} | — | — | 3 | μs | $V_{DD} = 4.5V$ (See Figure 3-4.) | |
| Transition Time, Low-to-high Level, HV Output | t_{TLH} | — | — | 2.5 | μs | $V_{DD} = 4.5V$ (See Figure 3-4.) | |

TEMPERATURE SPECIFICATIONS

| Parameter | Sym. | Min. | Typ. | Max. | Unit | Conditions |
|-----------------------------------|---------------|------|------|------|--------------------|------------|
| TEMPERATURE RANGE | | | | | | |
| Operating Ambient Temperature | T_A | -40 | — | +85 | $^\circ\text{C}$ | |
| Storage Temperature | T_S | -65 | — | +150 | $^\circ\text{C}$ | |
| PACKAGE THERMAL RESISTANCE | | | | | | |
| 40-lead PDIP | θ_{JA} | — | 39 | — | $^\circ\text{C/W}$ | |
| 44-lead PLCC | θ_{JA} | — | 37 | — | $^\circ\text{C/W}$ | |

HV518

Timing Waveforms



2.0 PIN DESCRIPTION

The details on the pins of HV518 40-lead PDIP and 44-lead PLCC are listed on [Table 2-1](#) and [Table 2-2](#), respectively. Refer to [Package Types](#) for the location of pins.

TABLE 2-1: 40-LEAD PDIP PIN FUNCTION TABLE

| Pin Number | Pin Name | Description |
|------------|-----------------|--|
| 1 | VPP | High-voltage power supply |
| 2 | SERIAL OUT | Serial data output |
| 3 | HVOUT32 | High-voltage output |
| 4 | HVOUT31 | High-voltage output |
| 5 | HVOUT30 | High-voltage output |
| 6 | HVOUT29 | High-voltage output |
| 7 | HVOUT28 | High-voltage output |
| 8 | HVOUT27 | High-voltage output |
| 9 | HVOUT26 | High-voltage output |
| 10 | HVOUT25 | High-voltage output |
| 11 | HVOUT24 | High-voltage output |
| 12 | HVOUT23 | High-voltage output |
| 13 | HVOUT22 | High-voltage output |
| 14 | HVOUT21 | High-voltage output |
| 15 | HVOUT20 | High-voltage output |
| 16 | HVOUT19 | High-voltage output |
| 17 | HVOUT18 | High-voltage output |
| 18 | HVOUT17 | High-voltage output |
| 19 | STR | Strobe |
| 20 | GND | Ground |
| 21 | CLK | Data Shift register clock. Inputs are shifted into the Shift register on the positive edge of the clock. |
| 22 | \overline{LE} | Latch enable |
| 23 | HVOUT16 | High-voltage output |
| 24 | HVOUT15 | High-voltage output |
| 25 | HVOUT14 | High-voltage output |
| 26 | HVOUT13 | High-voltage output |
| 27 | HVOUT12 | High-voltage output |
| 28 | HVOUT11 | High-voltage output |
| 29 | HVOUT10 | High-voltage output |
| 30 | HVOUT9 | High-voltage output |
| 31 | HVOUT8 | High-voltage output |
| 32 | HVOUT7 | High-voltage output |
| 33 | HVOUT6 | High-voltage output |

HV518

TABLE 2-1: 40-LEAD PDIP PIN FUNCTION TABLE (CONTINUED)

| Pin Number | Pin Name | Description |
|------------|----------|--------------------------|
| 34 | HVOUT5 | High-voltage output |
| 35 | HVOUT4 | High-voltage output |
| 36 | HVOUT3 | High-voltage output |
| 37 | HVOUT2 | High-voltage output |
| 38 | HVOUT1 | High-voltage output |
| 39 | DATA IN | Serial data input |
| 40 | VDD | Low-voltage power supply |

TABLE 2-2: 44-LEAD PLCC PIN FUNCTION TABLE

| Pin Number | Pin Name | Description |
|------------|------------------------|--|
| 1 | VPP | High-voltage power supply |
| 2 | SERIAL OUT | Serial data output |
| 3 | HVOUT32 | High-voltage output |
| 4 | HVOUT31 | High-voltage output |
| 5 | HVOUT30 | High-voltage output |
| 6 | NC | No connection |
| 7 | HVOUT29 | High-voltage output |
| 8 | HVOUT28 | High-voltage output |
| 9 | HVOUT27 | High-voltage output |
| 10 | HVOUT26 | High-voltage output |
| 11 | HVOUT25 | High-voltage output |
| 12 | HVOUT24 | High-voltage output |
| 13 | HVOUT23 | High-voltage output |
| 14 | HVOUT22 | High-voltage output |
| 15 | HVOUT21 | High-voltage output |
| 16 | HVOUT20 | High-voltage output |
| 17 | HVOUT19 | High-voltage output |
| 18 | NC | No connection |
| 19 | HVOUT18 | High-voltage output |
| 20 | HVOUT17 | High-voltage output |
| 21 | STR | Strobe |
| 22 | GND | Ground |
| 23 | CLK | Data Shift register clock. Inputs are shifted into the Shift register on the positive edge of the clock. |
| 24 | $\overline{\text{LE}}$ | Latch enable |
| 25 | HVOUT16 | High-voltage output |
| 26 | HVOUT15 | High-voltage output |
| 27 | HVOUT14 | High-voltage output |
| 28 | NC | No connection |

TABLE 2-2: 44-LEAD PLCC PIN FUNCTION TABLE (CONTINUED)

| Pin Number | Pin Name | Description |
|------------|----------|--------------------------|
| 29 | NC | No connection |
| 30 | HVOUT13 | High-voltage output |
| 31 | HVOUT12 | High-voltage output |
| 32 | HVOUT11 | High-voltage output |
| 33 | HVOUT10 | High-voltage output |
| 34 | HVOUT9 | High-voltage output |
| 35 | HVOUT8 | High-voltage output |
| 36 | HVOUT7 | High-voltage output |
| 37 | HVOUT6 | High-voltage output |
| 38 | HVOUT5 | High-voltage output |
| 39 | HVOUT4 | High-voltage output |
| 40 | HVOUT3 | High-voltage output |
| 41 | HVOUT2 | High-voltage output |
| 42 | HVOUT1 | High-voltage output |
| 43 | DATA IN | Serial data input |
| 44 | VDD | Low-voltage power supply |

3.0 FUNCTIONAL DESCRIPTION

3.1 Parameter Measurement Information

Figure 3-1 to Figure 3-4 show parametric measurement information. For testing purposes, all input pulses have maximum rise and fall times of 30 nanoseconds.

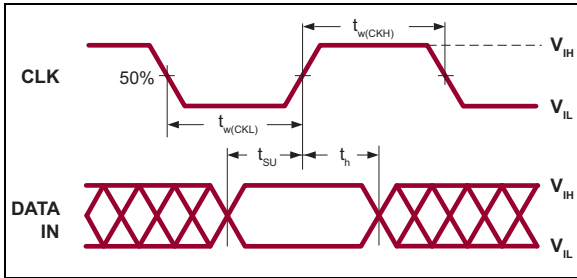


FIGURE 3-1: Input Timing Voltage Waveforms.

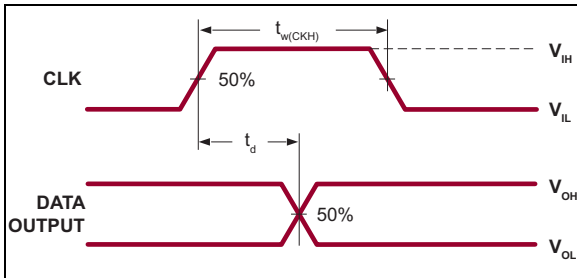


FIGURE 3-2: Output Timing Voltage Waveforms.

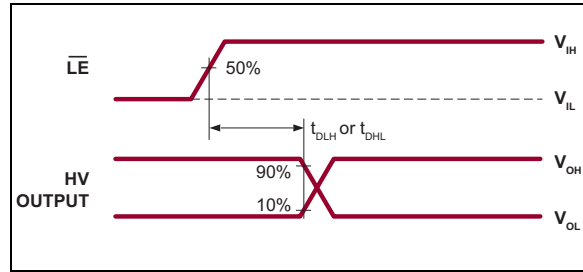


FIGURE 3-3: Latch Enable Timing Voltage Waveforms.

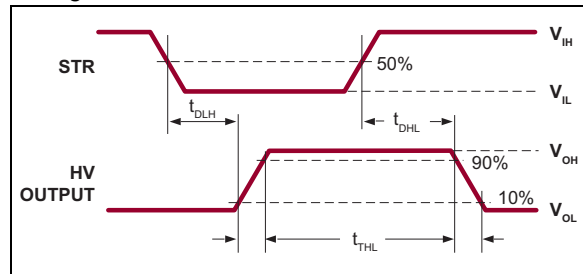


FIGURE 3-4: Switching-Time Voltage Waveforms.

3.2 Power-up and Power-down Sequence

Follow the steps below to power up and power down the HV518:

TABLE 3-1: POWER-UP AND POWER-DOWN SEQUENCE

| Power-up | | Power-down | |
|----------|--|------------|-------------------------------------|
| Step | Description | Step | Description |
| 1 | Connect ground. | 1 | Remove V_{PP} . (Note 1) |
| 2 | Apply V_{DD} . | 2 | Remove all inputs. |
| 3 | Set all inputs (Data, CLK, EN, etc.) to a known state. | 3 | Remove V_{DD} . |
| 4 | Apply V_{PP} . (Note 1) | 4 | Disconnect ground. |

Note 1: The V_{PP} should not drop below V_{DD} during operation.

TABLE 3-2: TRUTH FUNCTION TABLE

| Inputs | | | Outputs | | | |
|---------|-----------|----------------|---------|-----------------|-----|---------------------|
| Data In | CLK | Data Out | Data In | \overline{LE} | STR | High-voltage Output |
| H | | H | X | X | H | All low |
| L | | L | H | H | L | High |
| X | No change | Previous state | L | H | L | Low |
| | | | X | L | L | Previous state |

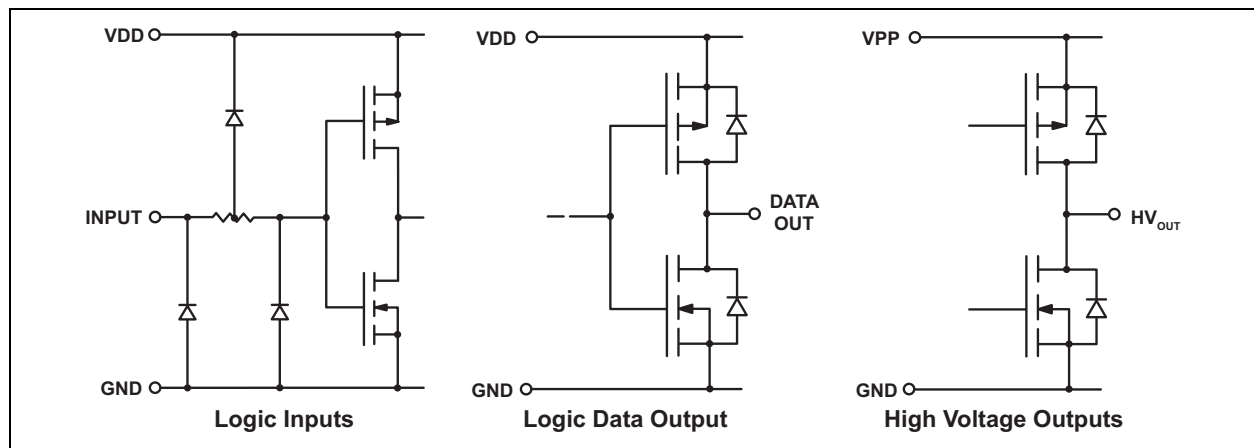


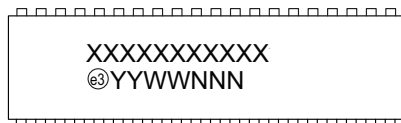
FIGURE 3-5: Input and Output Equivalent Circuits.

HV518

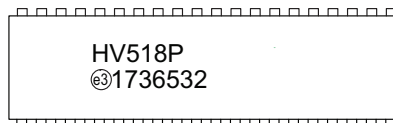
4.0 PACKAGE MARKING INFORMATION

4.1 Packaging Information

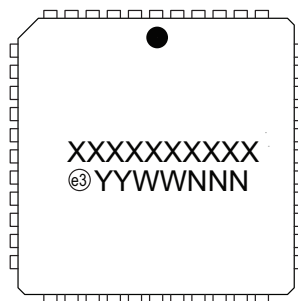
40-lead PDIP



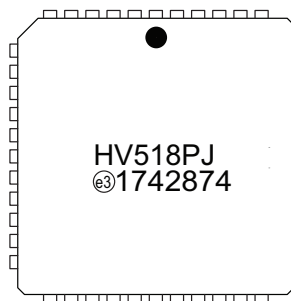
Example



44-lead PLCC



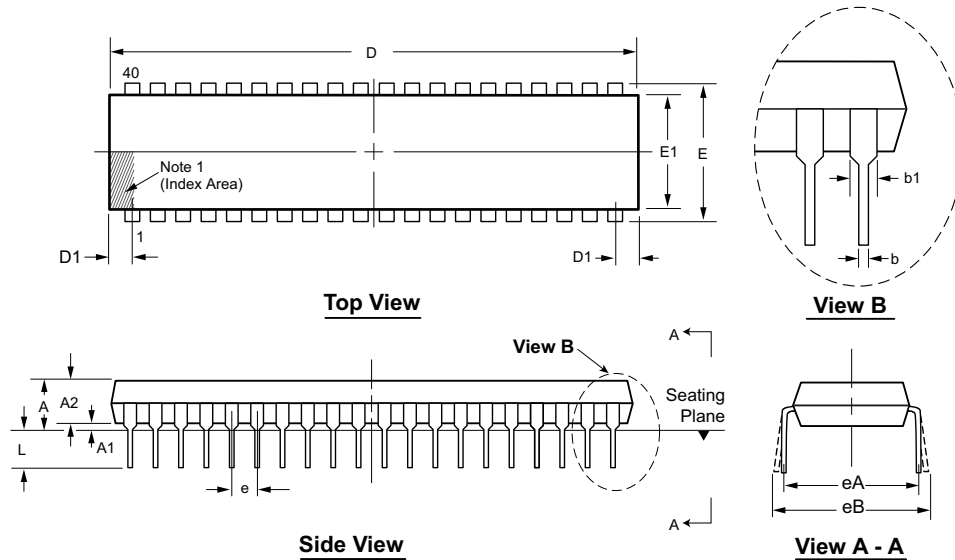
Example



| | | |
|----------------|--------|--|
| Legend: | XX...X | Product Code or Customer-specific information |
| | Y | Year code (last digit of calendar year) |
| | YY | Year code (last 2 digits of calendar year) |
| | WW | Week code (week of January 1 is week '01') |
| | NNN | Alphanumeric traceability code |
| | (e3) | Pb-free JEDEC® designator for Matte Tin (Sn) |
| | * | This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package. |

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for product code or customer-specific information. Package may or not include the corporate logo.

40-Lead PDIP (.600in Row Spacing) Package Outline (P) 2.095x.580in body (max), .250in height (max), .100in pitch



Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

Note:

1. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.

| Symbol | A | A1 | A2 | b | b1 | D | D1 | E | E1 | e | eA | eB | L | |
|--------------------|-----|-------|-------|------|-------|------|-------|-------|-------|------|-------------|-------------|-------|------|
| Dimension (inches) | MIN | .140* | .015 | .125 | .014 | .030 | 1.980 | .065† | .590† | .485 | .100 BSC | .600 BSC | .600* | .115 |
| | NOM | - | - | - | - | - | - | - | - | - | | | | |
| | MAX | .250 | .055* | .195 | .023† | .070 | 2.095 | .085* | .625 | .580 | | | | |

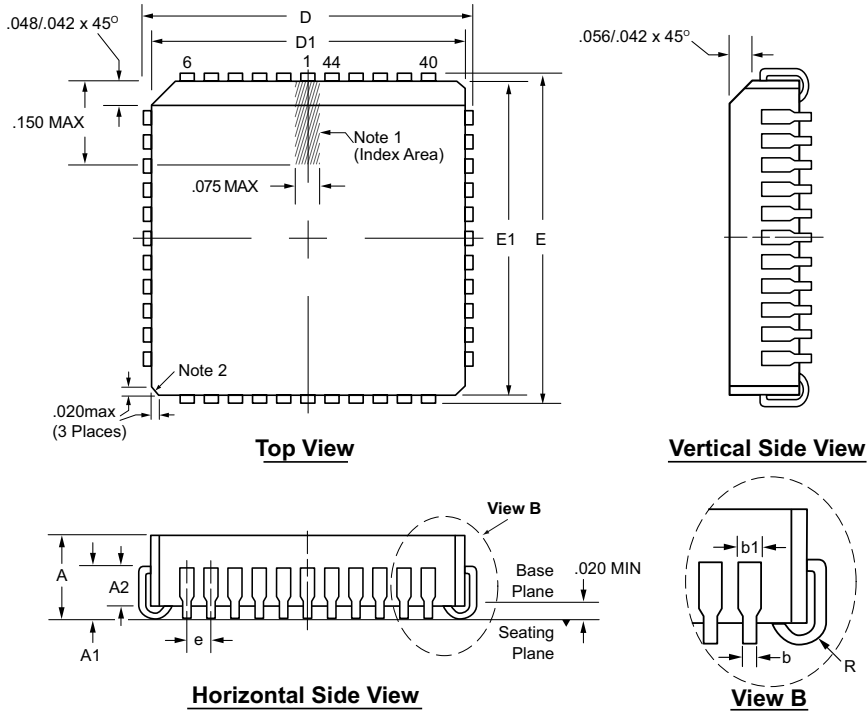
JEDEC Registration MS-011, Variation AC, Issue B, June, 1988.

* This dimension is not specified in the JEDEC drawing.

† This dimension differs from the JEDEC drawing.

Drawings not to scale.

44-Lead PLCC Package Outline (PJ) .653x.653in body, .180in height (max), .050in pitch



Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

Notes:

1. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.
2. Actual shape of this feature may vary.

| Symbol | A | A1 | A2 | b | b1 | D | D1 | E | E1 | e | R |
|--------------------|-----|------|------|------|------|-------------------|------|------|------|------|------|
| Dimension (inches) | MIN | .165 | .090 | .062 | .013 | .026 | .685 | .650 | .685 | .650 | .025 |
| | NOM | .172 | .105 | - | - | - | .690 | .653 | .690 | .653 | .035 |
| | MAX | .180 | .120 | .083 | .021 | .036 [†] | .695 | .656 | .695 | .656 | .045 |

JEDEC Registration MS-018, Variation AC, Issue A, June, 1993.

[†] This dimension differs from the JEDEC drawing.

Drawings not to scale.

APPENDIX A: REVISION HISTORY

Revision A (October 2017)

- Converted Supertex Doc# DSFP-HV518 to Microchip DS20005847A
- Changed the package marking format
- Made minor text changes throughout the document

HV518

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

| <u>PART NO.</u> | <u>XX</u> | - | <u>X</u> | - | <u>X</u> |
|-----------------|-----------------|---|--|---|------------|
| Device | Package Options | | Environmental | | Media Type |
| Device: | HV518 | = | 32-Channel Vacuum Fluorescent Display Driver | | |
| Packages: | P | = | 40-lead PDIP | | |
| | PJ | = | 44-lead PLCC | | |
| Environmental: | G | = | Lead (Pb)-free/RoHS-compliant Package | | |
| Media Types: | (blank) | = | 9/Tube for a P Package | | |
| | (blank) | = | 27/Tube for a PJ Package | | |
| | M903 | = | 500/Reel for a PJ Package | | |

| Examples: | |
|--------------------|--|
| a) HV518P-G: | 32-Channel Vacuum Fluorescent Display Driver, 40-lead PDIP, 9/Tube |
| b) HV518PJ-G: | 32-Channel Vacuum Fluorescent Display Driver, 44-lead PLCC, 27/Tube |
| c) HV518PJ-G-M903: | 32-Channel Vacuum Fluorescent Display Driver, 44-lead PLCC, 500/Reel |

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