Product Specification

PE4242

SPDT UltraCMOS™ RF Switch

Features

- Single-pin or complementary CMOS logic control inputs
- +3.0-volt power supply needed for single-pin control mode
- Low insertion loss: 0.7 dB at 1000 MHz, 0.9 dB at 2000 MHz
- Isolation of 32 dB at 1000 MHz, 23 dB at 2000 MHz
- Typical input 1 dB compression point of +27 dBm
- Ultra-small SC-70 package

Product Description

The PE4242 UltraCMOS™ RF Switch is designed to cover a broad range of applications from near DC through 3000 MHz. This reflective switch integrates on-board CMOS control logic with a low voltage CMOS-compatible control interface, and can be controlled using either single-pin or complementary control inputs. Using a nominal +3-volt power supply voltage, a typical input 1 dB compression point of +27 dBm can be achieved.

The PE4242 UltraCMOS™ RF Switch is manufactured in Peregrine's patented Ultra Thin Silicon (UTSi®) CMOS process, offering the performance of GaAs with the economy and integration of conventional CMOS.

Figure 1. Functional Diagram

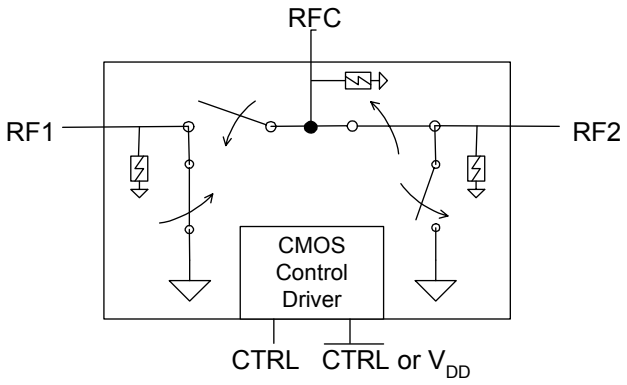


Figure 2. Package Type

6-lead SC-70



Table 1. Electrical Specifications @ +25 °C, V_{DD} = 3 V (Z_S = Z_L = 50 Ω)

Parameter	Conditions	Minimum	Typical	Maximum	Units
Operation Frequency[1]		DC		3000	MHz
Insertion Loss	1000 MHz		0.7	0.85	dB
	2000 MHz		0.9	1.05	dB
Isolation	1000 MHz	30	32		dB
	2000 MHz	21	23		dB
Return Loss	1000 MHz	18	22		dB
	2000 MHz	16	18		dB
'ON' Switching Time	50% CTRL to 0.1 dB of final value, 1 GHz		300		ns
'OFF' Switching Time	50% CTRL to 25 dB isolation, 1 GHz		200		ns
Video Feedthrough[2]			15		mV_{pp}
Input 1 dB Compression	2000 MHz	26	27		dBm
Input IP3	2000 MHz, 14 dBm input power	43	45		dBm

Notes: 1. Device linearity will begin to degrade below 10 MHz.

2. The DC transient at the output of any port of the switch when the control voltage is switched from Low to High or High to Low in a 50 Ω test set-up, measured with 1ns risetime pulses and 500 MHz bandwidth.

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Figure 3. Pin Configuration (Top View)

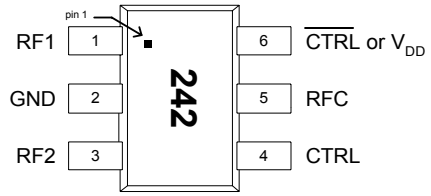


Table 2. Pin Descriptions

Pin No.	Pin Name	Description
1	RF1	RF1 port (Note 1)
2	GND	Ground connection. Traces should be physically short and connected to ground plane for best performance.
3	RF2	RF2 port (Note 1)
4	CTRL	Switch control input, CMOS logic level.
5	RFC	Common RF port for switch (Note 1)
6	$\overline{\text{CTRL}}$ or V_{DD}	This pin supports two interface options: *Single-pin control mode*. A nominal 3-volt supply connection is required. *Complementary-pin control mode*. A complementary CMOS control signal to CTRL is supplied to this pin. By-passing on this pin is not required in this mode.

Note 1: All RF pins must be DC blocked with an external series capacitor or held at 0 V_{DC}.

Table 3. Absolute Maximum Ratings

Symbol	Parameter/Conditions	Min	Max	Units
V_{DD}	Power supply voltage	-0.3	4.0	V
V_I	Voltage on any input	-0.3	V_{DD}+ 0.3	V
T_{ST}	Storage temperature range	-65	150	°C
T_{OP}	Operating temperature range	-40	85	°C
P_{IN}	Input power (50Ω)		30	dBm
V_{ESD}	ESD voltage (Human Body Model)		1500	V

Table 4. DC Electrical Specifications

Parameter	Min	Typ	Max	Units
V_{DD} Power Supply Voltage	2.7	3.0	3.3	V
I_{DD} Power Supply Current (V_{DD} = 3V, V_{CTRL} = 3V)		250	500	nA
Control Voltage High	0.7x V_{DD}			V
Control Voltage Low			0.3x V_{DD}	V

Electrostatic Discharge (ESD) Precautions

When handling this UltraCMOS™ device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the specified rating.

Latch-Up Avoidance

Unlike conventional CMOS devices, UltraCMOS™ devices are immune to latch-up.

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Table 5. Single-pin Control Logic Truth Table

Control Voltages	Signal Path
Pin 6 (V_{DD}) = V_{DD} Pin 4 (CTRL) = Low	RFC to RF1
Pin 6 (V_{DD}) = V_{DD} Pin 4 (CTRL) = High	RFC to RF2

Table 6. Complementary-pin Control Logic Truth Table

Control Voltages	Signal Path
Pin 6 ($\overline{CTRL}$ or V_{DD}) = High Pin 4 (CTRL) = Low	RFC to RF1
Pin 6 ($\overline{CTRL}$ or V_{DD}) = Low Pin 4 (CTRL) = High	RFC to RF2

Control Logic Input

The PE4242 is a versatile RF CMOS switch that supports two operating control modes; single-pin control mode and complementary-pin control mode.

Single-pin control mode enables the switch to operate with a single control pin (pin 4) supporting a +3-volt CMOS logic input, and requires a dedicated +3-volt power supply connection on pin 6 (V_{DD}). This mode of operation reduces the number of control lines required and simplifies the switch control interface typically derived from a CMOS µProcessor I/O port.

Complementary-pin control mode allows the switch to operate using complementary control pins CTRL and $\overline{CTRL}$ (pins 4 & 6), that can be directly driven by +3-volt CMOS logic or a suitable µProcessor I/O port. This enables the PE4242 to be used as a potential alternate source for SPDT RF switch products used in positive control voltage mode and operating within the PE4242 operating limits.

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Evaluation Kit

The SPDT Switch Evaluation Kit board was designed to ease customer evaluation of the PE4242 SPDT switch. The RF common port is connected through a 50 Ω transmission line to the top left SMA connector, J1. Port 1 and Port 2 are connected through 50 Ω transmission lines to the top two SMA connectors on the right side of the board, J3 and J2, respectively. A through transmission line connects SMA connectors J4 and J5. This transmission line can be used to estimate the loss of the PCB over the environmental conditions being evaluated.

The board is constructed of a two metal layer FR4 material with a total thickness of 0.031". The bottom layer provides ground for the RF transmission lines. The transmission lines were designed using a coplanar waveguide with ground plane model using a trace width of 0.0476", trace gaps of 0.030", dielectric thickness of 0.028", metal thickness of 0.0021" and ε_r of 4.4.

J6 provides a means for controlling DC and digital inputs to the device. Starting from the lower left pin, the second pin to the right (J6-3) is connected to the device V1 or CTRL input. The fourth pin to the right (J6-7) is connected to the device V2 or CTRL/V_{DD} input.

Figure 4. Evaluation Board Layout
Peregrine Specification 101/0083

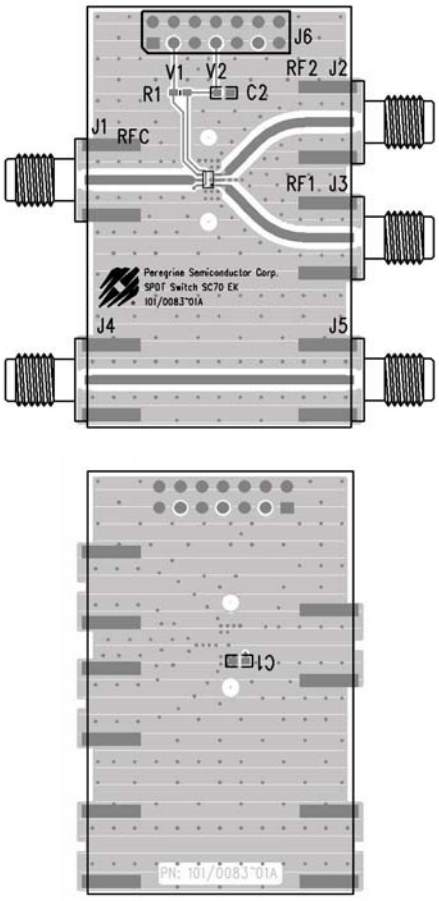
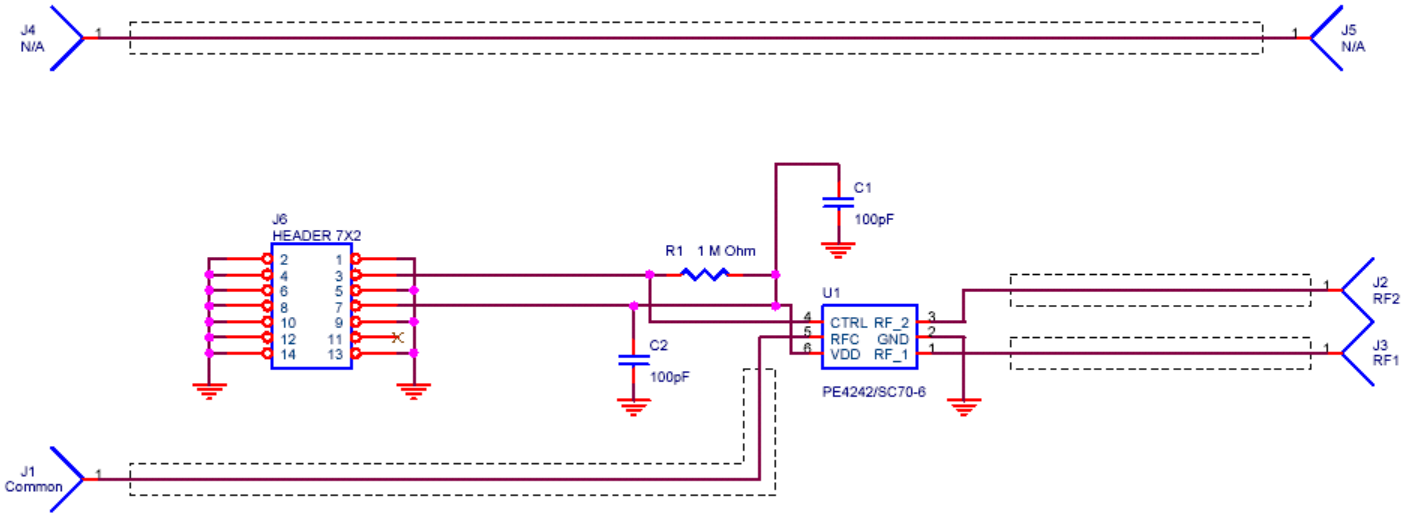


Figure 5. Evaluation Board Schematic
Peregrine Specification 102/0145



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Typical Performance Data @ -40 °C to 85 °C (Unless otherwise noted)

Figure 6. Insertion Loss – RFC to RF1

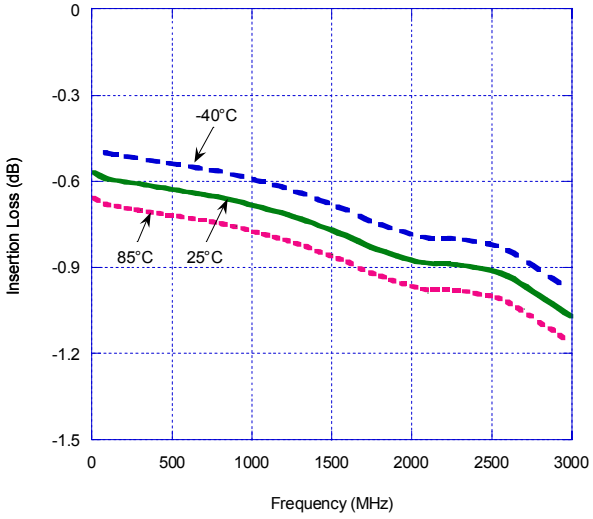


Figure 7. Input 1 dB Compression Point & IIP3 (Typical performance @ 25 °C)

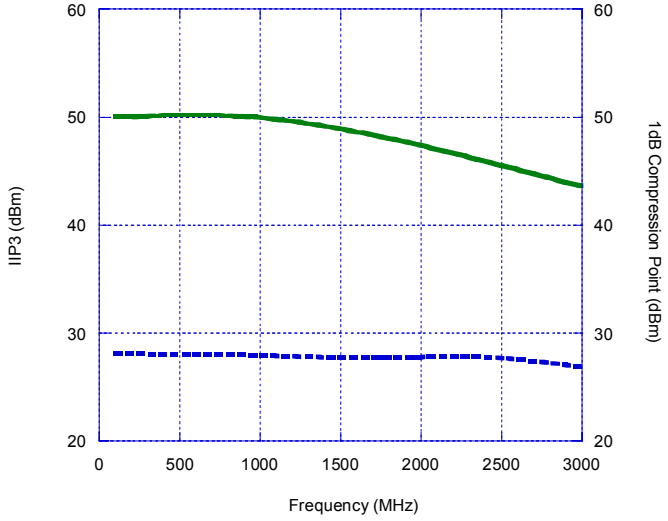


Figure 8. Insertion Loss – RFC to RF2

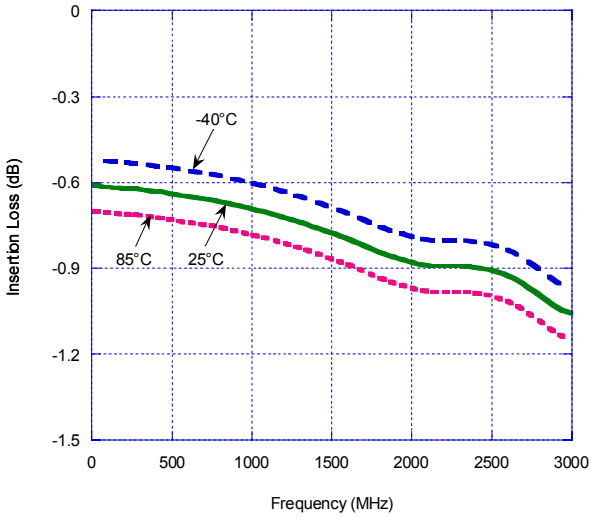
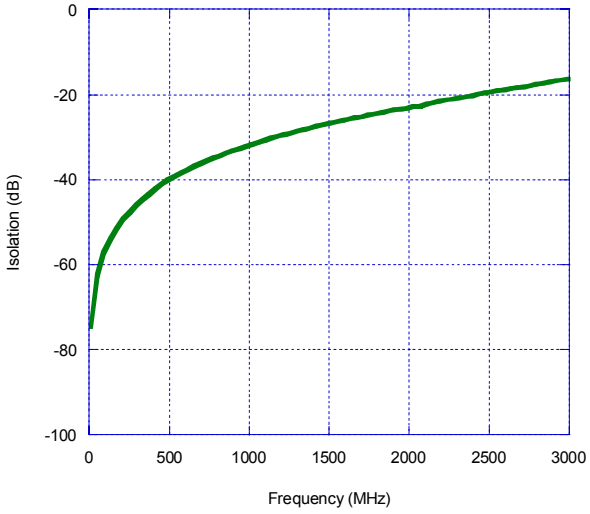


Figure 9. Isolation – RFC to RF1 (Typical performance @ 25 °C)



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Typical Performance Data @ 25°C

Figure 10. Isolation – RFC to RF2

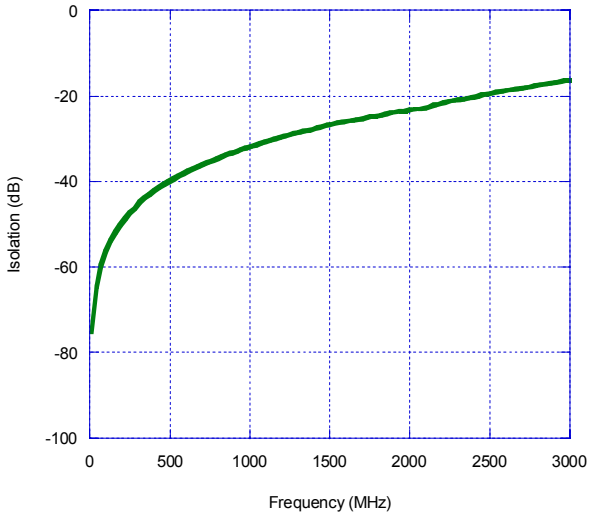


Figure 11. Isolation – RF1 to RF2, RF2 to RF1

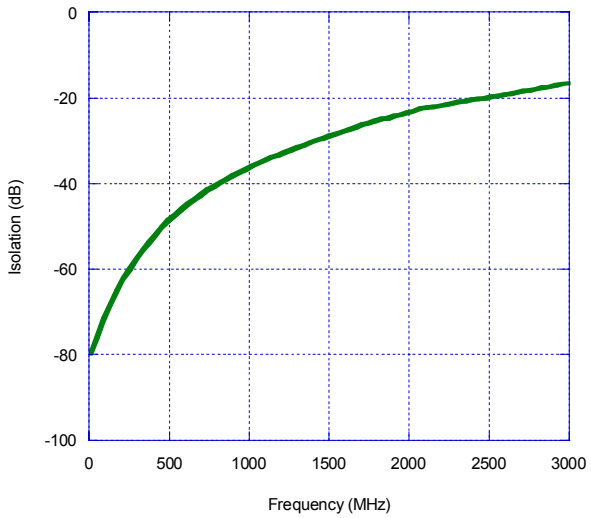


Figure 12. Return Loss – RFC to RF1, RF2

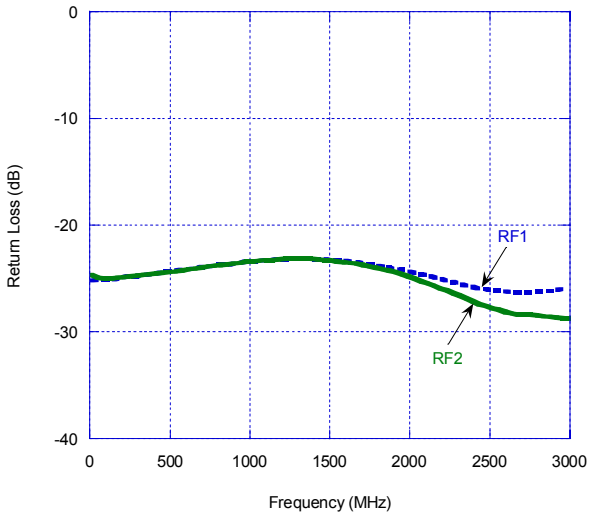
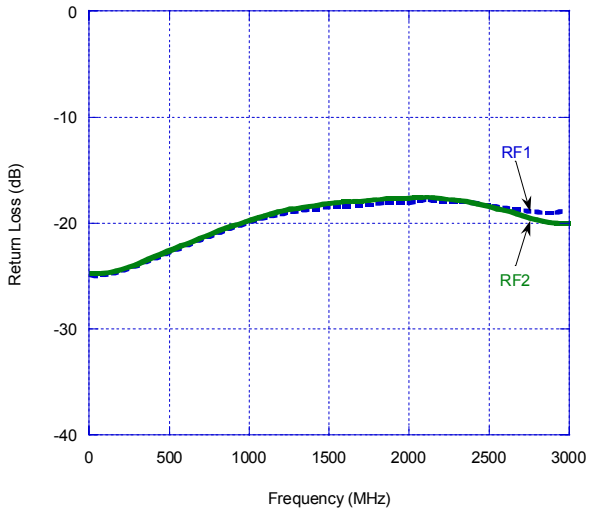


Figure 13. Return Loss – RF1, RF2



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Figure 14. Package Drawing

6-lead SC-70

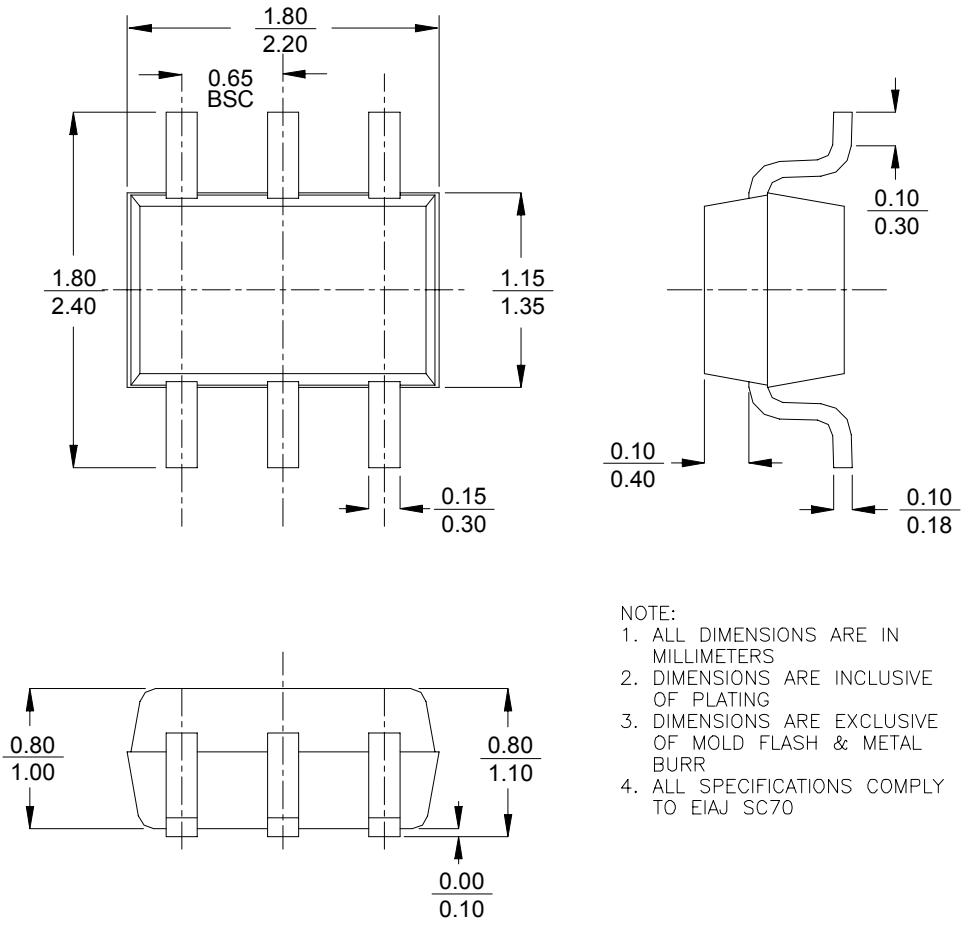


Table 7. Ordering Information

Order Code	Part Marking	Description	Package	Shipping Method
4242-01	242	PE4242-06SC70-7680F	6-lead SC-70	7680 units / Canister
4242-02	242	PE4242-06SC70-3000C	6-lead SC-70	3000 units / T&R
4242-00	PE4242-EK	PE4242-06SC70-EK	Evaluation Kit	1 / Box
4242-51	242	PE4242G-06SC70-7680A	Green 6-lead SC-70	7680 units / Canister
4242-52	242	PE4242G-06SC70-3000C	Green 6-lead SC-70	3000 units / T&R

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Sales Offices

The Americas

Peregrine Semiconductor Corp.
9450 Carroll Park Drive
San Diego, CA 92121
Tel 858-731-9400
Fax 858-731-9499

Europe

Peregrine Semiconductor Europe
Commercial Products:
Bâtiment Maine
13-15 rue des Quatre Vents
F- 92380 Garches, France
Tel: +33-1-47-41-91-73
Fax : +33-1-47-41-91-73
Space and Defense Products:
180 Rue Jean de Guiramand
13852 Aix-En-Provence cedex 3, France
Tel: +33(0) 4 4239 3361
Fax: +33(0) 4 4239 7227

North Asia Pacific

Peregrine Semiconductor K.K.
5A-5, 5F Imperial Tower
1-1-1 Uchisaiwaicho, Chiyoda-ku
Tokyo 100-0011 Japan
Tel: +81-3-3502-5211
Fax: +81-3-3502-5213

South Asia Pacific

Peregrine Semiconductor
28G, Times Square,
No. 500 Zhangyang Road,
Shanghai, 200122, P.R. China
Tel: +86-21-5836-8276
Fax: +86-21-5836-7652

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Телефон: 8 (812) 309-75-97 (многоканальный)
Факс: 8 (812) 320-03-32
Электронная почта: ocean@oceanchips.ru
Web: http://oceanchips.ru/
Адрес: 198099, г. Санкт-Петербург, ул. Калинина, д. 2, корп. 4, лит. А