TEXAS INSTRUMENTS

Data sheet acquired from Harris Semiconductor
SCHS076D – Revised March 2004

# CD4518B, CD4520B Types

## CMOS Dual Up-Counters

High-Voltage Types (20-Volt Rating)

CD4518B Dual BCD Up-Counter
CD4520B Dual Binary Up-Counter

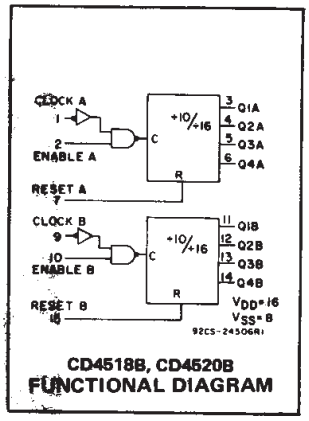
■ CD4518 Dual BCD Up-Counter and CD4520 Dual Binary Up-Counter each consist of two identical, internally synchronous 4-stage counters. The counter stages are D-type flip-flops having interchangeable CLOCK and ENABLE lines for incrementing on either the positive-going or negative-going transition. For single-unit operation the ENABLE input is maintained high and the counter advances on each positive-going transition of the CLOCK. The counters are cleared by high levels on their RESET lines.

The counter can be cascaded in the ripple mode by connecting Q4 to the enable input of the subsequent counter while the CLOCK input of the latter is held low.

The CD4518B and CD4520B types are supplied in 16-lead hermetic dual-in-line ceramic packages (F3A suffix), 16-lead dual-in-line plastic packages (E suffix), 16-lead small-outline packages (M, M96, and NSR suffixes), and 16-lead thin shrink small-outline packages (PW and PWR suffixes).

*Features:*

- Medium-speed operation – 6-MHz typical clock frequency at 10 V
- Positive- or negative-edge triggering
- Synchronous internal carry propagation
- 100% tested for quiescent current at 20 V
- Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (over full package-temperature range): 1 V at $V_{DD}$ = 5 V, 2 V at $V_{DD}$ = 10 V, 2.5 V at $V_{DD}$ = 15 V
- 5-V, 10-V, and 15-V parametric ratings
- Standardized, symmetrical output characteristics
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"




CD4518B, CD4520B
FUNCTIONAL DIAGRAM

*Applications:*

- Multistage synchronous counting
- Multistage ripple counting
- Frequency dividers

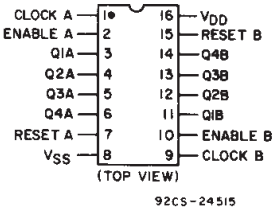
TRUTH TABLE

| CLOCK | ENABLE | RESET | ACTION |
|---|---|---|---|
| ⌐ | 1 | 0 | Increment Counter |
| 0 | ¬ | 0 | Increment Counter |
| ¬ | X | 0 | No Change |
| X | ⌐ | 0 | No Change |
| ⌐ | 0 | 0 | No Change |
| 1 | ¬ | 0 | No Change |
| X | X | 1 | Q1 thru Q4 = 0 |

X = Don't Care  1 ≡ High State  0 ≡ Low State

**MAXIMUM RATINGS,** *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, ($V_{DD}$)
(Voltages referenced to $V_{SS}$ Terminal) ..... -0.5V to +20V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5V to $V_{DD}$ +0.5V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10mA
POWER DISSIPATION PER PACKAGE ($P_D$):
For $T_A$ = -55°C to +100°C ..... 500mW
For $T_A$ = +100°C to +125°C ..... Derate Linearity at 12mW/°C to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR $T_A$ = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) ..... 100mW
OPERATING-TEMPERATURE RANGE ($T_A$) ..... -55°C to +125°C
STORAGE TEMPERATURE RANGE ($T_{stg}$) ..... -65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max ..... +265°C




CD4518B, CD4520B
TERMINAL ASSIGNMENT

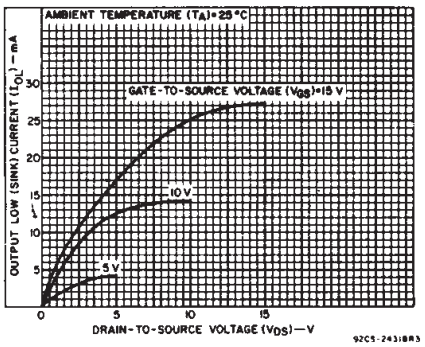



*Fig. 1 – Typical output low (sink) current characteristics.*

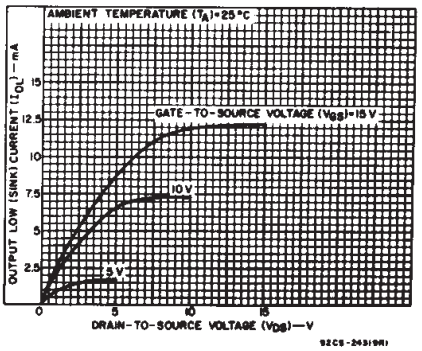



*Fig. 2 – Minimum output low (sink) current characteristics.*

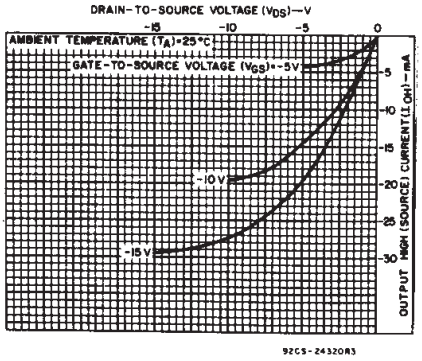



*Fig. 3 – Typical output high (source) current characteristics.*

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**STATIC ELECTRICAL CHARACTERISTICS**

| CHARACTERISTIC | CONDITIONS | | | LIMITS AT INDICATED TEMPERATURES (°C) | | | | | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | +25 | | | |
| | $V_O$ (V) | $V_{IN}$ (V) | $V_{DD}$ (V) | −55 | −40 | +85 | +125 | Min. | Typ. | Max. | |
| Quiescent Device Current, $I_{DD}$ Max. | – | 0,5 | 5 | 5 | 5 | 150 | 150 | – | 0.04 | 5 | μA |
| | – | 0,10 | 10 | 10 | 10 | 300 | 300 | – | 0.04 | 10 | |
| | – | 0,15 | 15 | 20 | 20 | 600 | 600 | – | 0.04 | 20 | |
| | – | 0,20 | 20 | 100 | 100 | 3000 | 3000 | – | 0.08 | 100 | |
| Output Low (Sink) Current $I_{OL}$ Min. | 0.4 | 0,5 | 5 | 0.64 | 0.61 | 0.42 | 0.36 | 0.51 | 1 | – | mA |
| | 0.5 | 0,10 | 10 | 1.6 | 1.5 | 1.1 | 0.9 | 1.3 | 2.6 | – | |
| | 1.5 | 0,15 | 15 | 4.2 | 4 | 2.8 | 2.4 | 3 4 | 6.8 | – | |
| Output High (Source) Current, $I_{OH}$ Min. | 4.6 | 0,5 | 5 | −0.64 | −0.61 | −0.42 | −0.36 | −0.51 | −1 | – | |
| | 2.5 | 0,5 | 5 | −2 | −1.8 | −1.3 | −1.15 | −1.6 | −3.2 | – | |
| | 9.5 | 0,10 | 10 | −1.6 | −1.5 | −1.1 | −0.9 | −1.3 | −2.6 | – | |
| | 13.5 | 0,15 | 15 | −4.2 | −4 | −2.8 | −2.4 | −3.4 | −6.8 | – | |
| Output Voltage: Low-Level, $V_{OL}$ Max. | – | 0,5 | 5 | 0.05 | | | | – | 0 | 0.05 | V |
| | – | 0,10 | 10 | 0.05 | | | | – | 0 | 0.05 | |
| | – | 0,15 | 15 | 0.05 | | | | – | 0 | 0.05 | |
| Output Voltage: High-Level, $V_{OH}$ Min. | – | 0,5 | 5 | 4.95 | | | | 4.95 | 5 | – | |
| | – | 0,10 | 10 | 9.95 | | | | 9.95 | 10 | – | |
| | – | 0,15 | 15 | 14.95 | | | | 14.95 | 15 | – | |
| Input Low Voltage, $V_{IL}$ Max. | 0.5, 4.5 | – | 5 | 1.5 | | | | — | — | 1.5 | V |
| | 1, 9 | – | 10 | 3 | | | | — | — | 3 | |
| | 1.5,13.5 | – | 15 | 4 | | | | — | — | 4 | |
| Input High Voltage, $V_{IH}$ Min. | 0.5, 4.5 | – | 5 | 3.5 | | | | 3.5 | — | — | |
| | 1, 9 | – | 10 | 7 | | | | 7 | — | — | |
| | 1.5,13.5 | - | 15 | 11 | | | | 11 | — | — | |
| Input Current $I_{IN}$ Max. | – | 0,18 | 18 | ±0.1 | ±0.1 | ±1 | ±1 | – | $±10^{-5}$ | ±0.1 | μA |

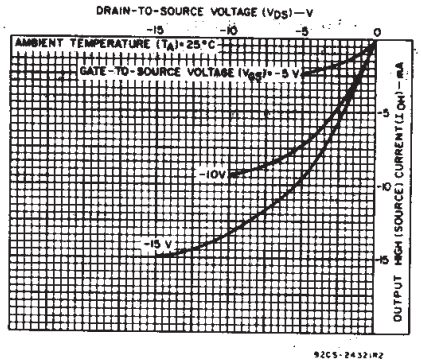



*Fig. 4 — Minimum output high (source) current characteristics.*

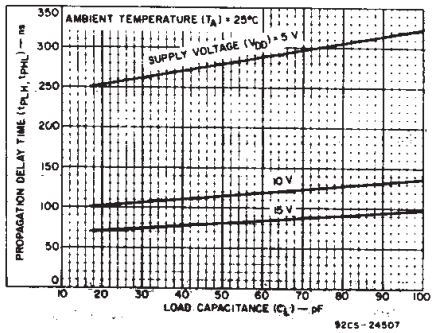



*Fig. 5 — Typical propagation delay vs. load capacitance, clock or enable to output.*

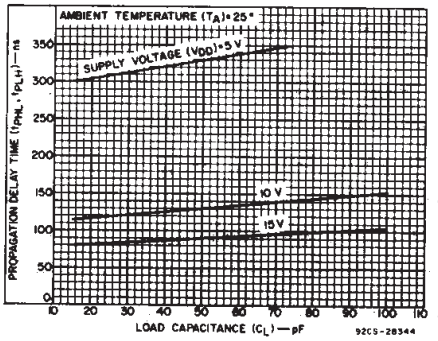



*Fig. 6 — Typical propagation delay time vs. load capacitance, reset to output.*

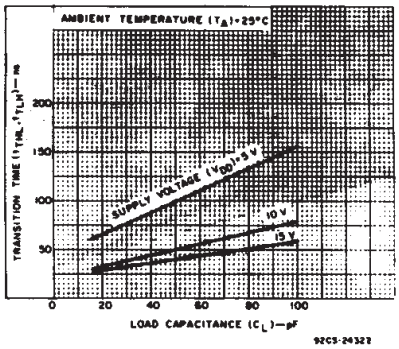



*Fig. 7 — Typical transition time vs. load capacitance.*

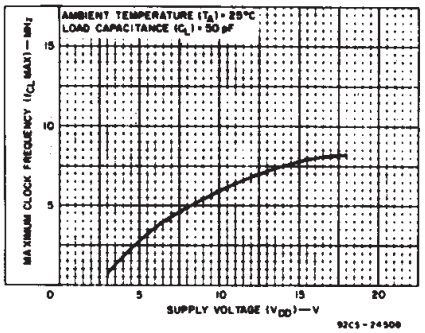



*Fig. 8 — Typical maximum-clock-frequency vs. supply voltage.*

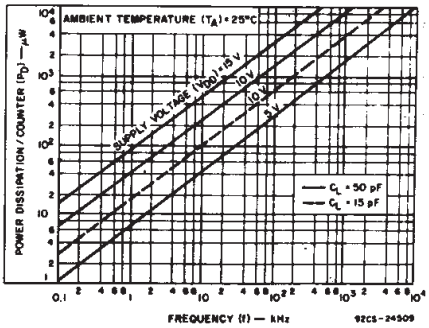



*Fig. 9 — Typical power dissipation characteristics.*

**RECOMMENDED OPERATING CONDITIONS at $T_A$ = 25°C, Except as Noted.**
**For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:**

| CHARACTERISTIC | $V_{DD}$ (V) | LIMITS | | UNITS |
|---|---|---|---|---|
| | | Min. | Max. | |
| Supply-Voltage Range (For $T_A$=Full Package-Temperature Range) | | 3 | 18 | V |
| Enable Pulse Width, $t_W$ | 5 | 400 | – | ns |
| | 10 | 200 | – | |
| | 15 | 140 | – | |
| Clock Pulse Width, $t_W$ | 5 | 200 | – | ns |
| | 10 | 100 | – | |
| | 15 | 70 | – | |
| Clock Input Frequency, $f_{CL}$ | 5 | dc | 1.5 | MHz |
| | 10 | | 3 | |
| | 15 | | 4 | |
| Clock Rise or Fall Time, $t_rCL$ or $t_fCL$: | 5 | – | 15 | μs |
| | 10 | – | 5 | |
| | 15 | – | 5 | |
| Reset Pulse Width, $t_W$ | 5 | 250 | – | ns |
| | 10 | 110 | – | |
| | 15 | 80 | – | |

**DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A$=25°C;**
**Input $t_r$,$t_f$=20 ns, $C_L$=50 pF, $R_L$=200 KΩ**

| CHARACTERISTIC | TEST CONDITIONS | $V_{DD}$ V | LIMITS Min. | Typ. | Max. | UNITS |
|---|---|---|---|---|---|---|
| Propagation Delay Time, $t_{PHL}$, $t_{PLH}$: Clock or Enable to Output | | 5 | – | 280 | 560 | ns |
| | | 10 | – | 115 | 230 | |
| | | 15 | – | 80 | 160 | |
| Reset to Output | | 5 | – | 330 | 650 | |
| | | 10 | – | 130 | 225 | |
| | | 15 | – | 90 | 170 | |
| Transition Time, $t_{THL}$, $t_{TLH}$ | | 5 | – | 100 | 200 | ns |
| | | 10 | – | 50 | 100 | |
| | | 15 | – | 40 | 80 | |
| Maximum Clock Input Frequency, $f_{CL}$ | | 5 | 1.5 | 3 | – | MHz |
| | | 10 | 3 | 6 | – | |
| | | 15 | 4 | 8 | – | |
| Minimum Clock Pulse Width, $t_W$ | | 5 | | 100 | 200 | ns |
| | | 10 | | 50 | 100 | |
| | | 15 | | 35 | 70 | |
| Clock Rise or Fall Time, $t_r$ or $t_f$: | | 5 | – | – | 15 | μs |
| | | 10, 15 | – | – | 5 | |
| Minimum Reset Pulse Width, $t_W$ | | 5 | | 125 | 250 | ns |
| | | 10 | | 55 | 110 | |
| | | 15 | – | 40 | 80 | |
| Minimum Enable Pulse Width, $t_W$ | | 5 | – | 200 | 400 | ns |
| | | 10 | | 100 | 200 | |
| | | 15 | | 70 | 140 | |
| Input Capacitance, $C_{IN}$ | Any Input | | | 5 | 7.5 | pF |

**TEST CIRCUITS**

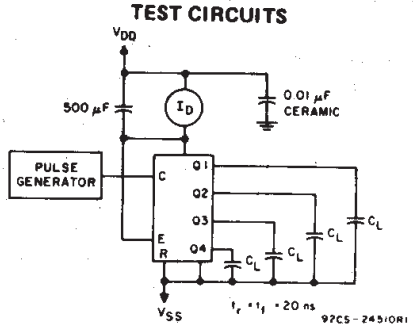



*Fig. 10 – Dynamic power dissipation.*

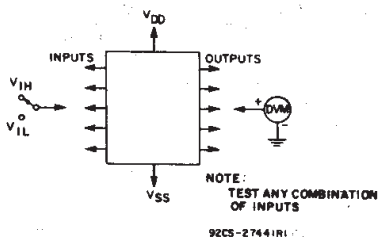



*Fig. 11 – Input voltage.*

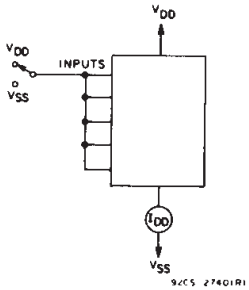



*Fig. 12 – Quiescent device current test circuit.*

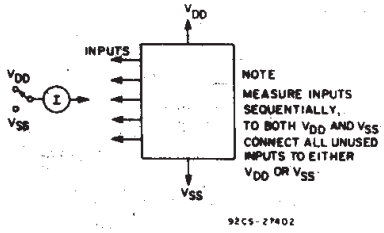



*Fig. 13 – Input leakage-current test circuit.*

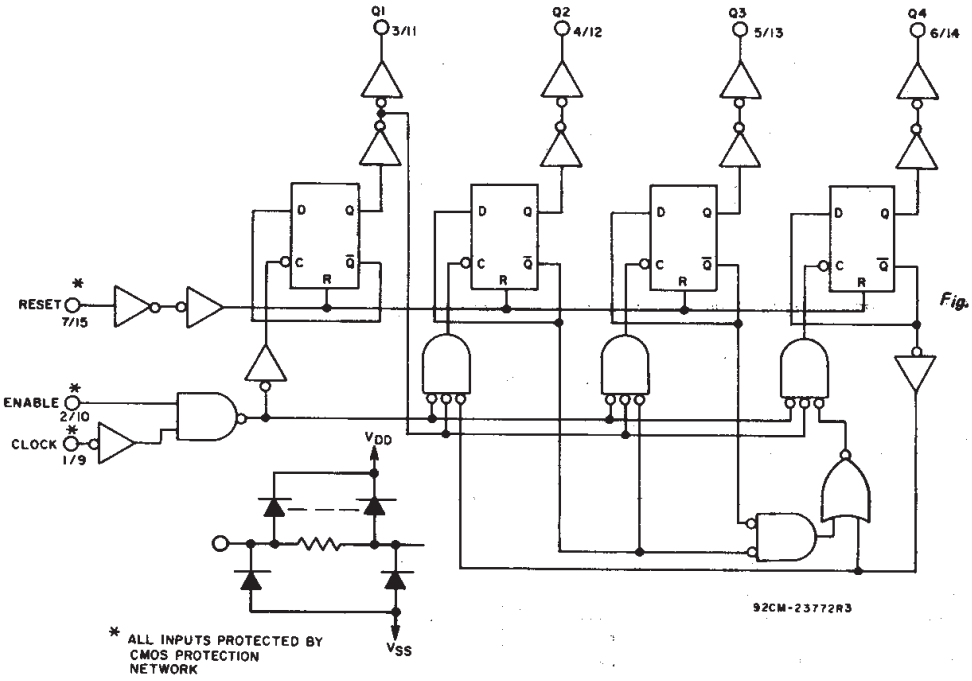



*Fig. 14 — Decade counter (CD4518B) logic diagram for one of two identical counters.*

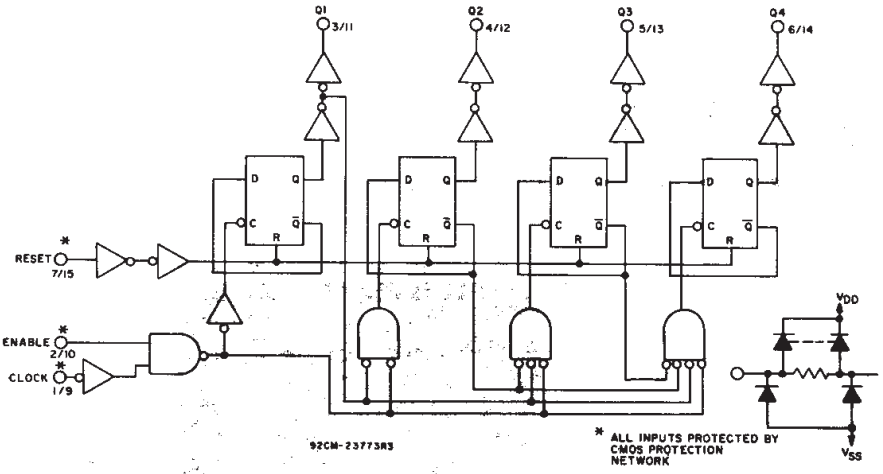



*Fig. 15 — Binary counter (CD4520B) logic diagram for one of two identical counters.*

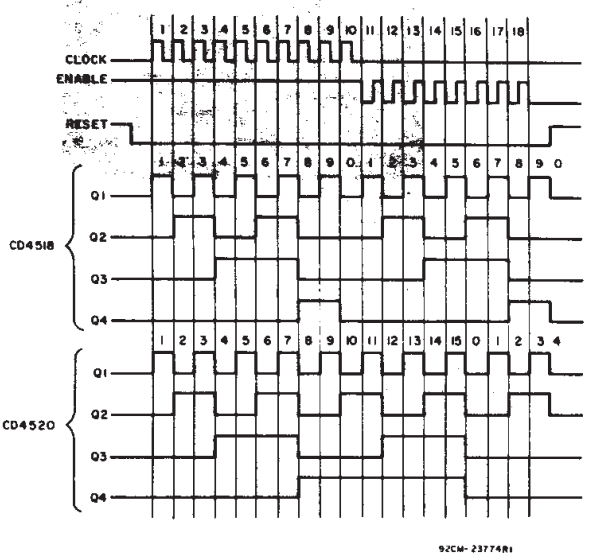



*Fig. 16 — Timing diagrams for CD4518B and CD4520B.*

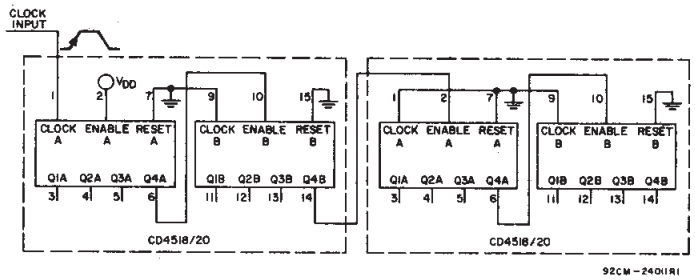
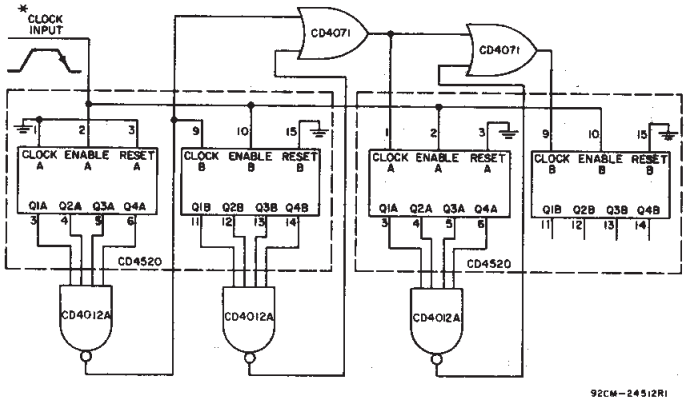
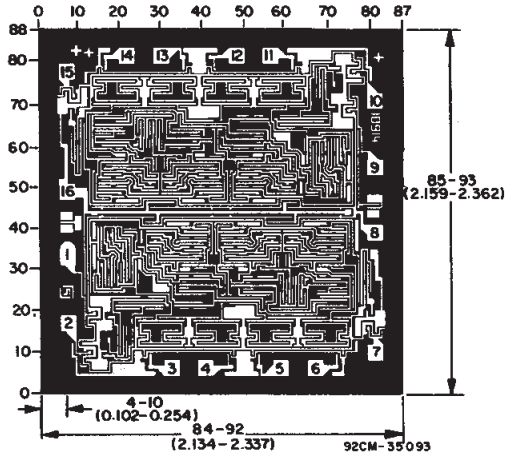



*Fig. 17 – Ripple cascading of four counters with positive edge triggering.*

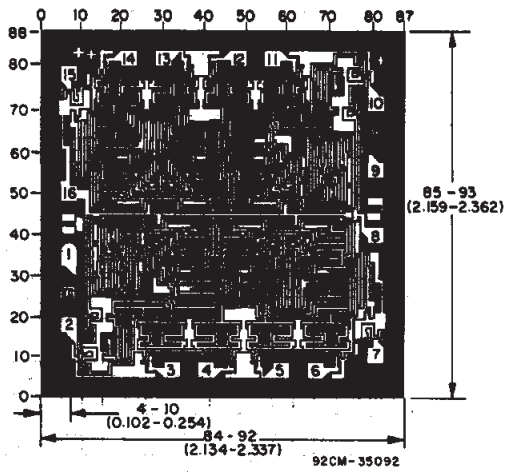



*NOTE: FOR SYNCHRONOUS CASCADING, THE CLOCK TRANSITION TIME SHOULD BE MADE LESS THAN OR EQUAL TO THE SUM OF THE FIXED PROPAGATION DELAY AT 15 pF AND THE TRANSITION TIME OF THE OUTPUT DRIVER STAGE FOR THE ESTIMATED CAPACITATIVE LOAD.

*Fig. 18 – Synchronous cascading of four binary counters with negative edge triggering.*




*Dimensions and pad layout for CD4518BH chip.*




*Dimensions and pad layout for CD4520BH chip.*

*Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils ($10^{-3}$ inch).*

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) |
|---|---|---|---|---|---|---|---|---|
| 7702301EA | ACTIVE | CDIP | J | 16 | 1 | None | Call TI | Level-NC-NC-NC |
| CD4518BE | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | Level-NC-NC-NC |
| CD4518BF | ACTIVE | CDIP | J | 16 | 1 | None | Call TI | Level-NC-NC-NC |
| CD4518BF3A | ACTIVE | CDIP | J | 16 | 1 | None | Call TI | Level-NC-NC-NC |
| CD4518BM | ACTIVE | SOIC | D | 16 | 40 | Pb-Free (RoHS) | CU NIPDAU | Level-2-260C-1 YEAR/ Level-1-235C-UNLIM |
| CD4518BM96 | ACTIVE | SOIC | D | 16 | 2500 | Pb-Free (RoHS) | CU NIPDAU | Level-2-260C-1 YEAR/ Level-1-235C-UNLIM |
| CD4518BNSR | ACTIVE | SO | NS | 16 | 2000 | Pb-Free (RoHS) | CU NIPDAU | Level-2-260C-1 YEAR/ Level-1-235C-UNLIM |
| CD4518BPW | ACTIVE | TSSOP | PW | 16 | 90 | Pb-Free (RoHS) | CU NIPDAU | Level-1-250C-UNLIM |
| CD4518BPWR | ACTIVE | TSSOP | PW | 16 | 2000 | Pb-Free (RoHS) | CU NIPDAU | Level-1-250C-UNLIM |
| CD4520BE | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | Level-NC-NC-NC |
| CD4520BF | ACTIVE | CDIP | J | 16 | 1 | None | Call TI | Level-NC-NC-NC |
| CD4520BF3A | ACTIVE | CDIP | J | 16 | 1 | None | Call TI | Level-NC-NC-NC |
| CD4520BM | ACTIVE | SOIC | D | 16 | 40 | Pb-Free (RoHS) | CU NIPDAU | Level-2-260C-1 YEAR/ Level-1-235C-UNLIM |
| CD4520BM96 | ACTIVE | SOIC | D | 16 | 2500 | Pb-Free (RoHS) | CU NIPDAU | Level-2-260C-1 YEAR/ Level-1-235C-UNLIM |
| CD4520BNSR | ACTIVE | SO | NS | 16 | 2000 | Pb-Free (RoHS) | CU NIPDAU | Level-2-260C-1 YEAR/ Level-1-235C-UNLIM |
| CD4520BPW | ACTIVE | TSSOP | PW | 16 | 90 | Pb-Free (RoHS) | CU NIPDAU | Level-1-250C-UNLIM |
| CD4520BPWR | ACTIVE | TSSOP | PW | 16 | 2000 | Pb-Free (RoHS) | CU NIPDAU | Level-1-250C-UNLIM |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - May not be currently available - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**None:** Not yet available Lead (Pb-Free).
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDECindustry standard classifications, and peak solder temperature.

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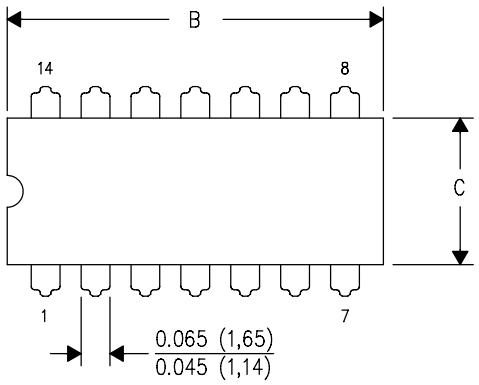
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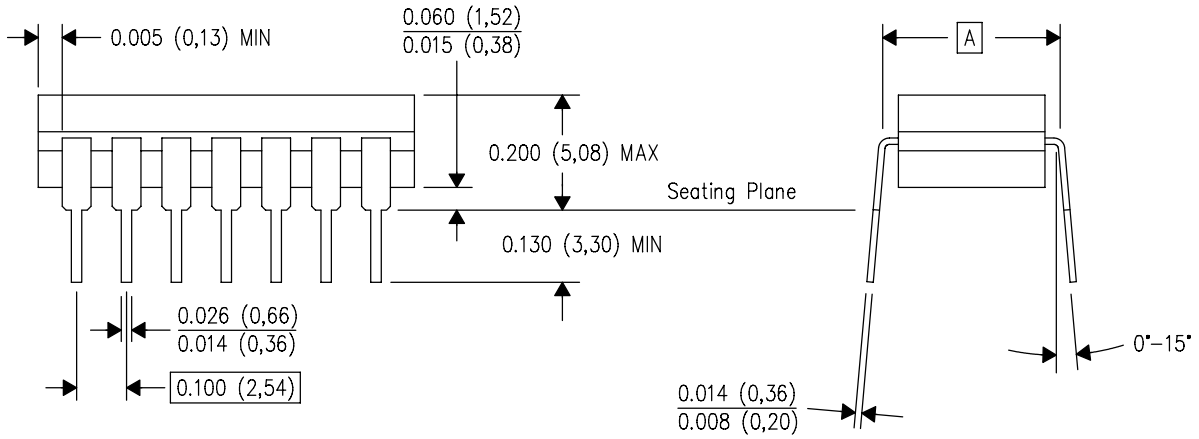
J (R–GDIP–T**)

14 LEADS SHOWN

# CERAMIC DUAL IN–LINE PACKAGE




| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |



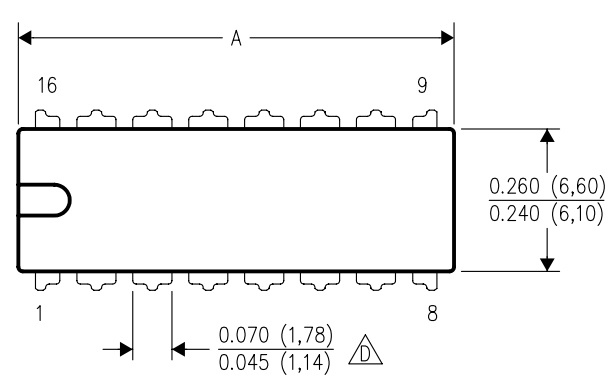

4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

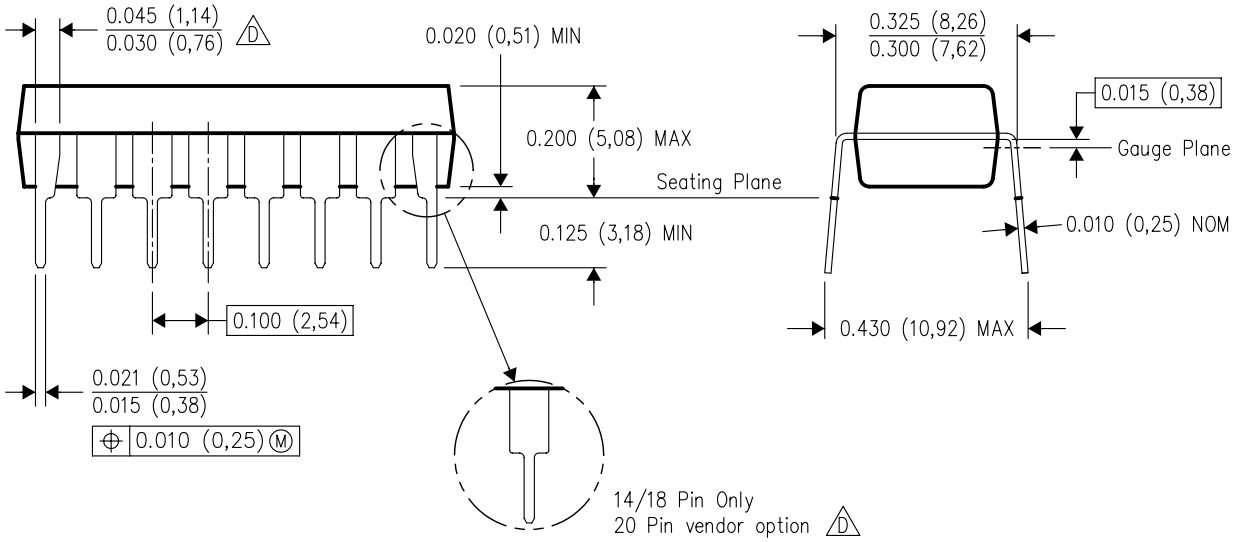
## N (R–PDIP–T**)

## PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



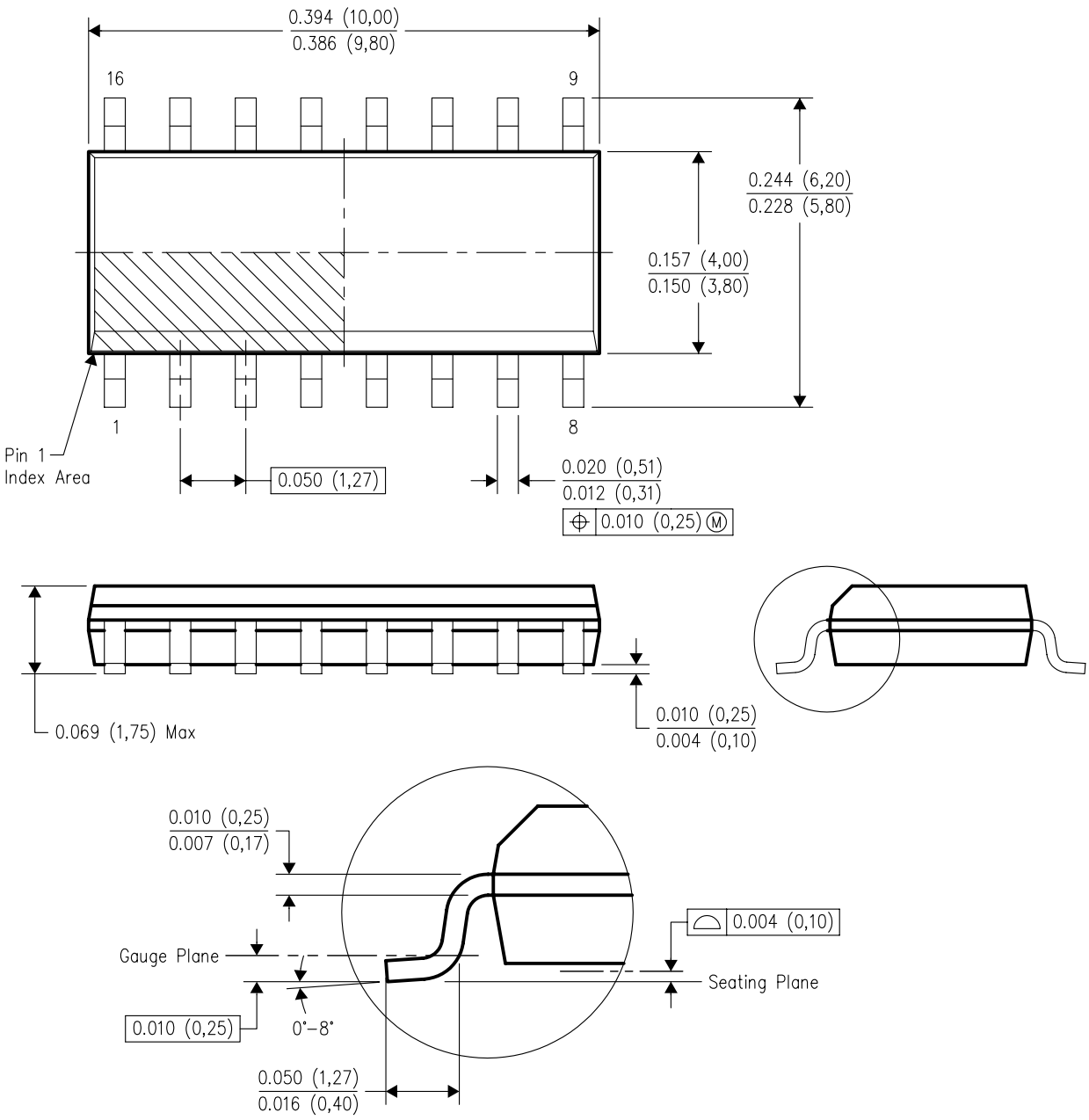

| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS–001 VARIATION (C) | AA | BB | AC | AD |




4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

## D (R–PDSO–G16) PLASTIC SMALL–OUTLINE PACKAGE

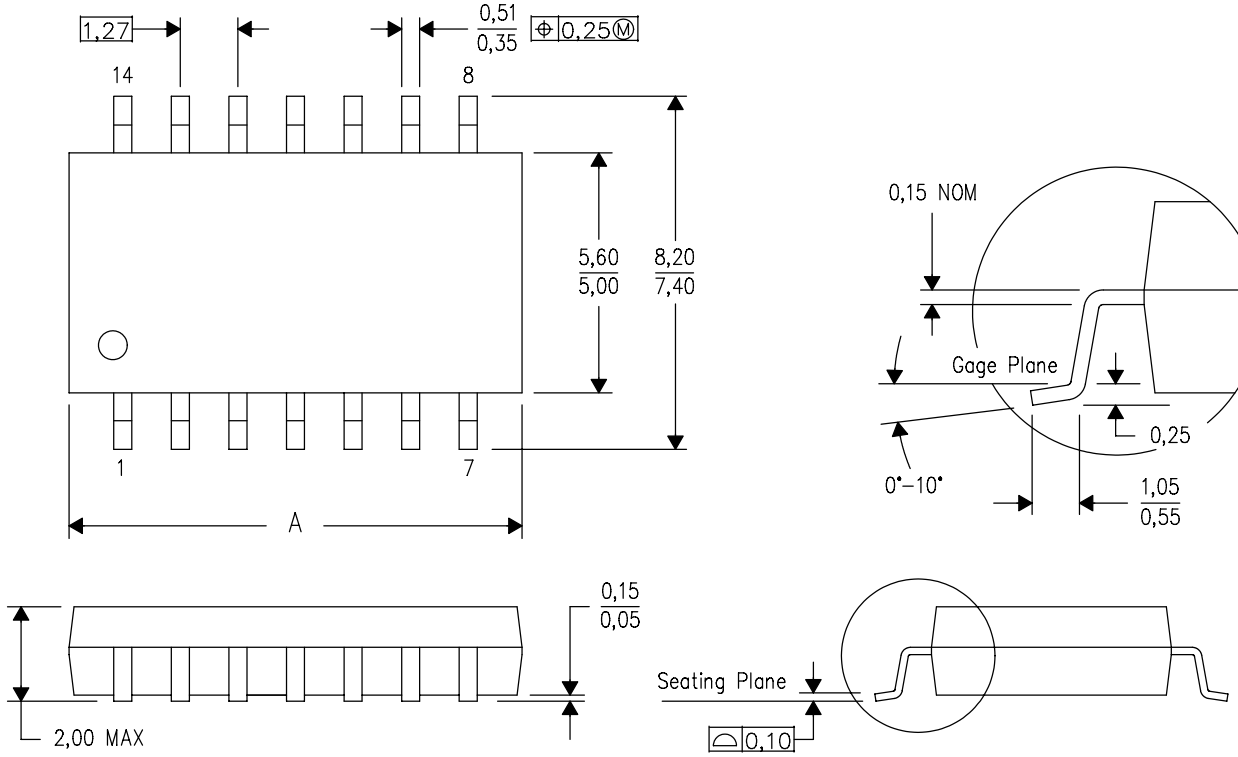



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–012 variation AC.

## MECHANICAL DATA

**NS (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

**14-PINS SHOWN**



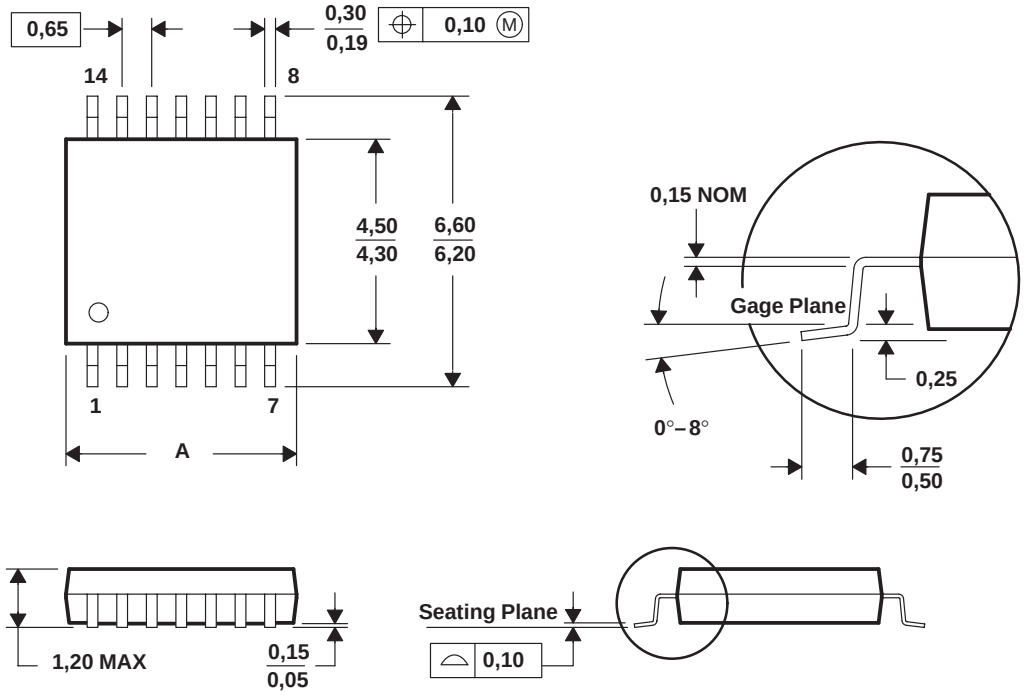

| DIM \ PINS ** | 14 | 16 | 20 | 24 |
|---|---|---|---|---|
| A MAX | 10,50 | 10,50 | 12,90 | 15,30 |
| A MIN | 9,90 | 9,90 | 12,30 | 14,70 |

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

**PW (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

**14 PINS SHOWN**




| DIM \ PINS ** | 8 | 14 | 16 | 20 | 24 | 28 |
|---|---|---|---|---|---|---|
| A MAX | 3,10 | 5,10 | 5,10 | 6,60 | 7,90 | 9,80 |
| A MIN | 2,90 | 4,90 | 4,90 | 6,40 | 7,70 | 9,60 |

**4040064/F 01/97**

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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