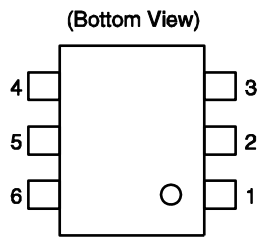
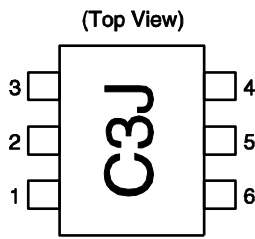




**PIN CONNECTIONS**



Pin No.	Pin Name
1	INPUT
2	GND
3	GND
4	OUTPUT
5	GND
6	V <sub>CC</sub>

**PRODUCT LINE-UP OF 5 V-BIAS SILICON MMIC MEDIUM OUTPUT AMPLIFIER**  
 (T<sub>A</sub> = +25°C, f = 1 GHz, V<sub>CC</sub> = V<sub>out</sub> = 5.0 V, Z<sub>s</sub> = Z<sub>L</sub> = 50 Ω)

Part No.	f <sub>u</sub> (GHz)	P <sub>O(sat)</sub> (dBm)	G <sub>P</sub> (dB)	NF (dB)	I <sub>cc</sub> (mA)	Package	Marking
μPC2708TB	2.9	+10.0	15	6.5	26	6-pin super minimold	C1D
μPC2709TB	2.3	+11.5	23	5.0	25		C1E
μPC2710TB	1.0	+13.5	33	3.5	22		C1F
μPC2776TB	2.7	+8.5	23	6.0	25		C2L
μPC3223TB	3.2	+12.0	23	4.5	19		C3J

**Remark** Typical performance. Please refer to **ELECTRICAL CHARACTERISTICS** in detail.

**PIN EXPLANATIONS**

PIN No.	Pin Name	Applied Voltage (V)	Pin Voltage (V) Note	Function and Applications
1	INPUT	–	0.96	Signal input pin. A internal matching circuit, configured with resistors, enables 50 Ω connection over a wide band. A multi-feedback circuits is designed to cancel the deviations of $h_{FE}$ and resistance. This pin must be coupled to signal source with capacitor for DC cut.
4	OUTPUT	Voltage as same as $V_{CC}$ through external inductor	–	Signal output pin. The inductor must be attached between $V_{CC}$ and output pins to supply current to the internal output transistors.
6	$V_{CC}$	4.5 to 5.5	–	Power suply pin. Witch biases the internal input transistor. This pin should be externally equipped with bypass capacitor to minimize its impedance.
2 3 5	GND	0	–	Ground pin. This pin should be connected to system ground with minimum inductance. Ground pattern on the board should be formed as wide as possible. All the ground pins must be connected together with wide ground pattern to decrease impedance difference.

**Note** Pin Voltage is measured at  $V_{CC} = 5.0\text{ V}$

**ABSOLUTE MAXIMUM RATINGS**

Parameter	Symbol	Conditions	Ratings	Unit
Supply Voltage	V <sub>CC</sub>	T <sub>A</sub> = +25°C, Pin 4 and 6	6.0	V
Total Circuit Current	I <sub>CC</sub>	T <sub>A</sub> = +25°C	40	mA
Power Dissipation	P <sub>D</sub>	T <sub>A</sub> = +85°C <b>Note</b>	270	mW
Operating Ambient Temperature	T <sub>A</sub>		-40 to +85	°C
Storage Temperature	T <sub>stg</sub>		-55 to +150	°C
Input Power	P <sub>in</sub>	T <sub>A</sub> = +25°C	+10	dBm

**Note** Mounted on double-sided copper-clad 50 × 50 × 1.6 mm epoxy glass PWB

**RECOMMENDED OPERATING RANGE**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Supply Voltage	V <sub>CC</sub>	The same voltage should be applied to pin 4 and 6.	4.5	5.0	5.5	V
Operating Ambient Temperature	T <sub>A</sub>		-40	+25	+85	°C

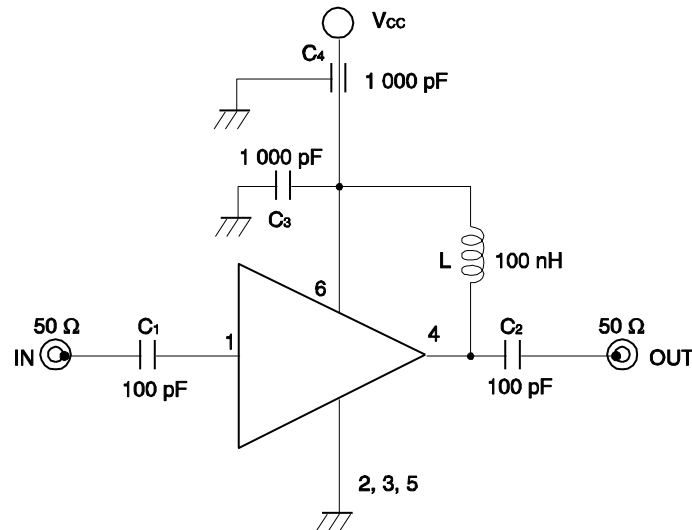
**ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = +25°C, V<sub>CC</sub> = V<sub>out</sub> = 5.0 V, Z<sub>s</sub> = Z<sub>L</sub> = 50 Ω)**

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Circuit Current	I <sub>CC</sub>	No input signal	15.0	19.0	24.0	mA
Power Gain	G <sub>P</sub>	f = 1.0 GHz, P <sub>in</sub> = -30 dBm	20.5	23.0	25.5	dB
		f = 2.2 GHz, P <sub>in</sub> = -30 dBm	20.0	23.0	26.0	
Saturated Output Power	P <sub>O(sat)</sub>	f = 1.0 GHz, P <sub>in</sub> = -5 dBm	+9.0	+12.0	-	dBm
		f = 2.2 GHz, P <sub>in</sub> = -5 dBm	+6.0	+9.0	-	
Gain 1 dB Compression Output Power	P <sub>O(1 dB)</sub>	f = 1.0 GHz	+4.5	+6.5	-	dBm
		f = 2.2 GHz	+3.0	+5.0	-	
Noise Figure	NF	f = 1.0 GHz	-	4.5	6.0	dB
		f = 2.2 GHz	-	4.0	5.5	
Upper Limit Operating Frequency	f <sub>u</sub>	3 dB down below flat gain at f = 0.1 GHz	2.8	3.2	-	GHz
Isolation	ISL	f = 1.0 GHz, P <sub>in</sub> = -30 dBm	28.0	33.0	-	dB
		f = 2.2 GHz, P <sub>in</sub> = -30 dBm	28.0	33.0	-	
Input Return Loss	RL <sub>in</sub>	f = 1.0 GHz, P <sub>in</sub> = -30 dBm	9.0	12.0	-	dB
		f = 2.2 GHz, P <sub>in</sub> = -30 dBm	12.0	17.5	-	
Output Return Loss	RL <sub>out</sub>	f = 1.0 GHz, P <sub>in</sub> = -30 dBm	9.0	12.0	-	dB
		f = 2.2 GHz, P <sub>in</sub> = -30 dBm	9.0	12.0	-	
Gain Flatness	ΔG <sub>P</sub>	f = 0.1 to 2.2 GHz	-	±0.9	-	dB

**OTHER CHARACTERISTICS, FOR REFERENCE PURPOSES ONLY**  
**(T<sub>A</sub> = +25°C, V<sub>CC</sub> = V<sub>out</sub> = 5.0 V, Z<sub>s</sub> = Z<sub>L</sub> = 50 Ω)**

Parameter	Symbol	Test Conditions	Reference Value	Unit
Output Intercept Point	OIP <sub>3</sub>	f = 1.0 GHz	+17.8	dBm
		f = 2.2 GHz	+14.8	

**TEST CIRCUIT**



The application circuits and their parameters are for reference only and are not intended for use in actual design-ins.

**COMPONENTS OF TEST CIRCUIT FOR MEASURING ELECTRICAL CHARACTERISTICS**

	Type	Value
C <sub>1</sub> , C <sub>2</sub>	Chip Capacitor	100 pF
C <sub>3</sub>	Chip Capacitor	1 000 pF
C <sub>4</sub>	Feed-through Capacitor	1 000 pF
L	Chip Inductor	100 nH

**INDUCTOR FOR THE OUTPUT PIN**

The internal output transistor of this IC consumes 20 mA, to output medium power. To supply current for output transistor, connect an inductor between the Vcc pin (pin 6) and output pin (pin 4). Select large value inductance, as listed above.

The inductor has both DC and AC effects. In terms of DC, the inductor biases the output transistor with minimum voltage drop to output enable high level. In terms of AC, the inductor makes output-port impedance higher to get enough gain. In this case, large inductance and Q is suitable.

**CAPACITORS FOR THE Vcc, INPUT AND OUTPUT PINS**

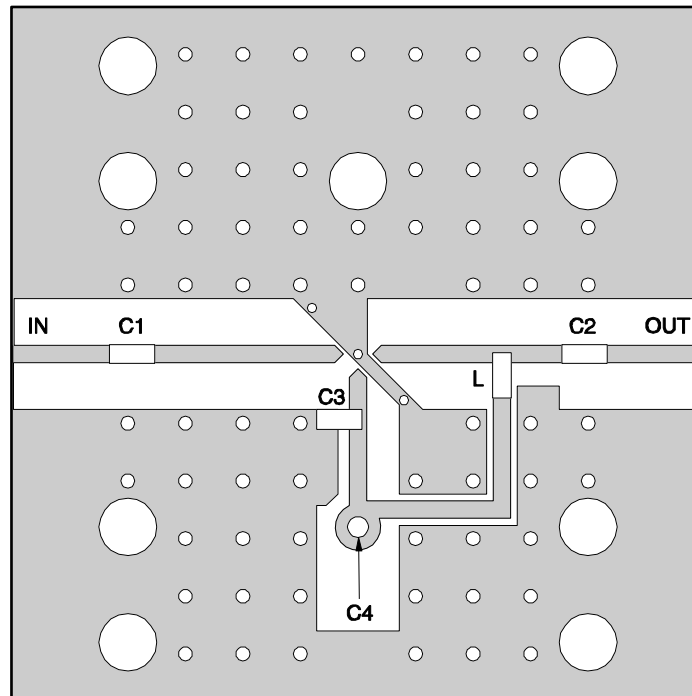
Capacitors of 1000 pF are recommendable as the bypass capacitor for the Vcc pin and the coupling capacitors for the input and output pins.

The bypass capacitor connected to the Vcc pin is used to minimize ground impedance of Vcc pin. So, stable bias can be supplied against Vcc fluctuation.

The coupling capacitors, connected to the input and output pins, are used to cut the DC and minimize RF serial impedance. Their capacitances are therefore selected as lower impedance against a 50 Ω load. The capacitors thus perform as high pass filters, suppressing low frequencies to DC.

To obtain a flat gain from 100 MHz upwards, 1 000 pF capacitors are used in the test circuit. In the case of under 10 MHz operation, increase the value of coupling capacitor such as 10 000 pF. Because the coupling capacitors are determined by equation,  $C = 1/(2 \pi Rfc)$ .

ILLUSTRATION OF THE TEST CIRCUIT ASSEMBLED ON EVALUATION BOARD



**COMPONENT LIST**

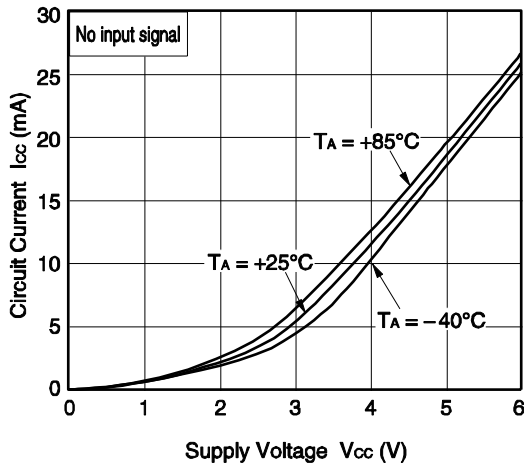
	Value
C <sub>1</sub> , C <sub>2</sub>	100 pF
C <sub>3</sub> , C <sub>4</sub>	1 000 pF
L	100 nH

**Notes**

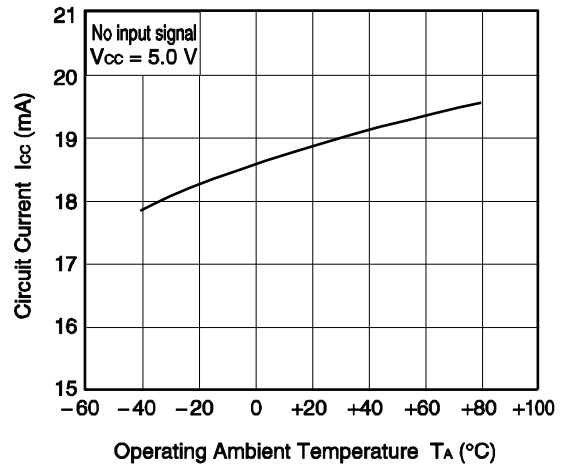
1. 30 × 30 × 0.4 mm double sided copper clad polyimide board.
2. Back side: GND pattern
3. Solder plated on pattern
4. ◦○: Through holes

TYPICAL CHARACTERISTICS ( $T_A = +25^\circ\text{C}$ , unless otherwise specified)

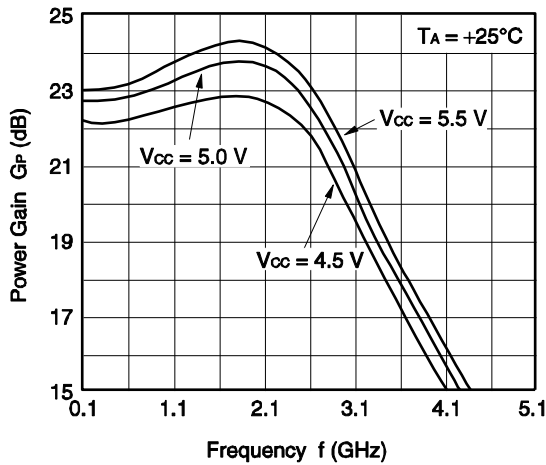
CIRCUIT CURRENT vs. SUPPLY VOLTAGE



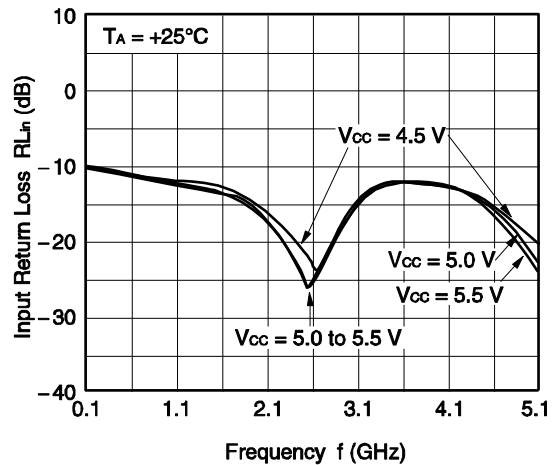
CIRCUIT CURRENT vs. OPERATING AMBIENT TEMPERATURE



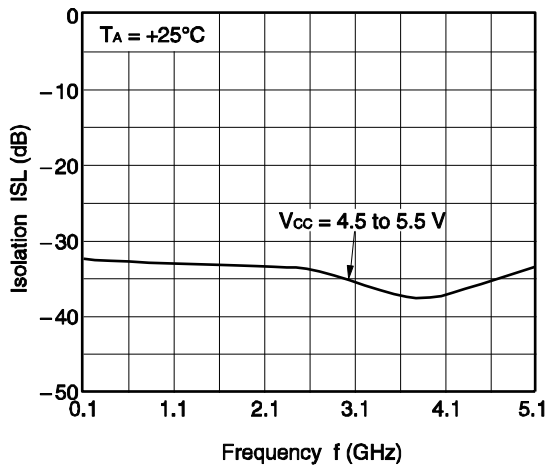
POWER GAIN vs. FREQUENCY



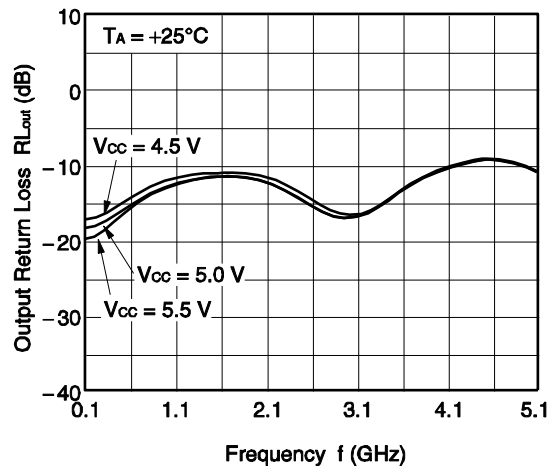
INPUT RETURN LOSS vs. FREQUENCY



ISOLATION vs. FREQUENCY



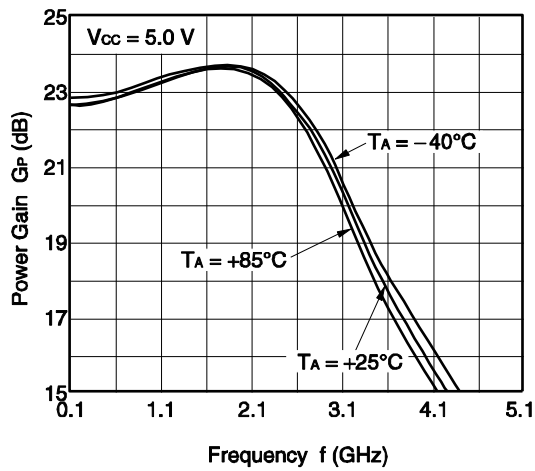
OUTPUT RETURN LOSS vs. FREQUENCY



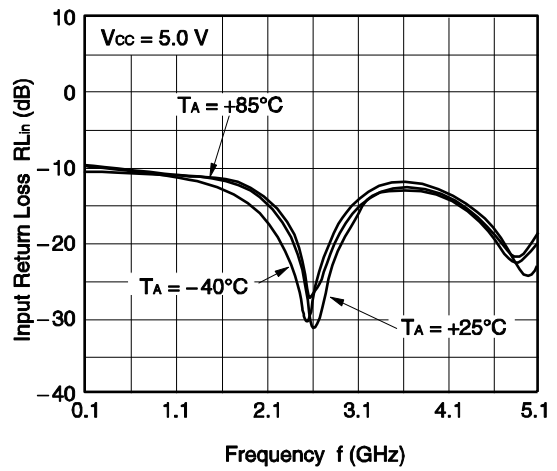
Remark The graphs indicate nominal characteristics.



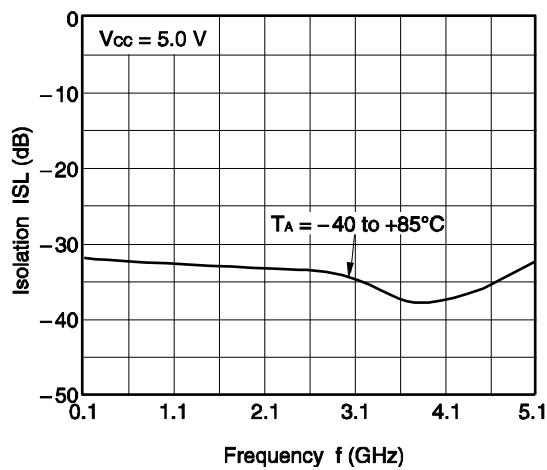
POWER GAIN vs. FREQUENCY



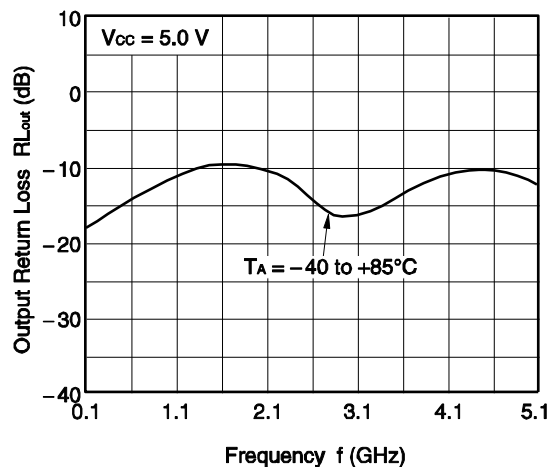
INPUT RETURN LOSS vs. FREQUENCY



ISOLATION vs. FREQUENCY

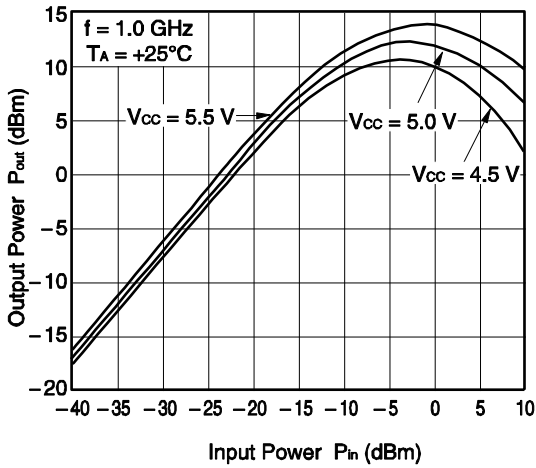


OUTPUT RETURN LOSS vs. FREQUENCY

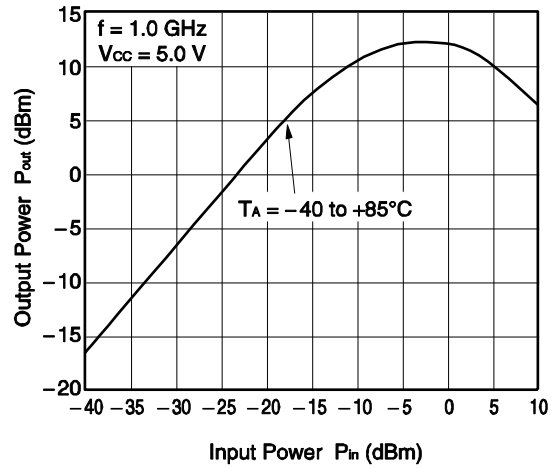


**Remark** The graphs indicate nominal characteristics.

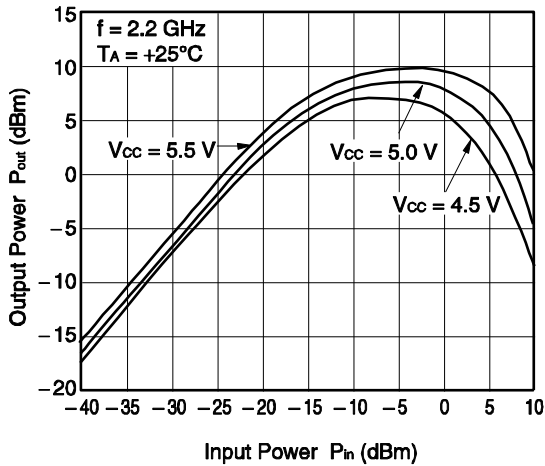
OUTPUT POWER vs. INPUT POWER



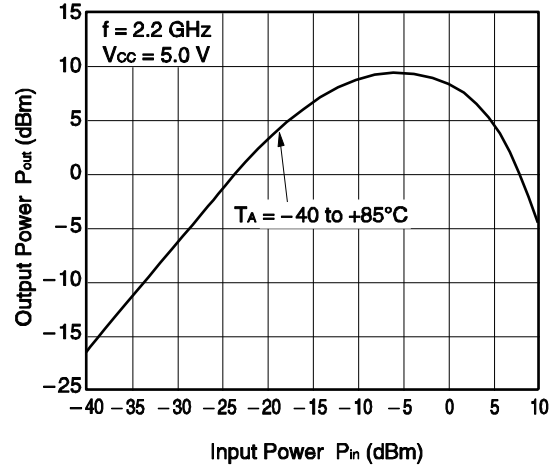
OUTPUT POWER vs. INPUT POWER



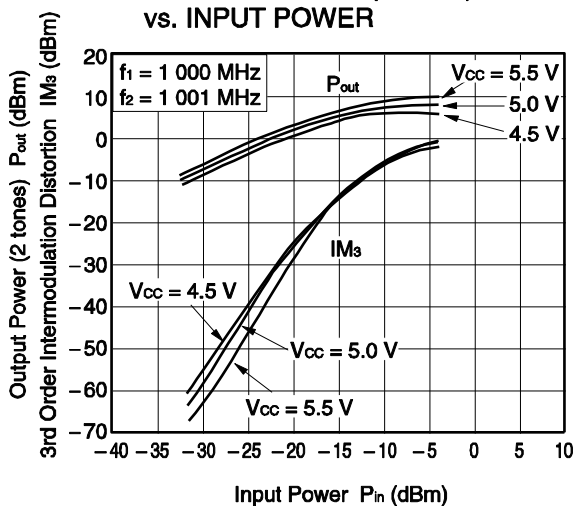
OUTPUT POWER vs. INPUT POWER



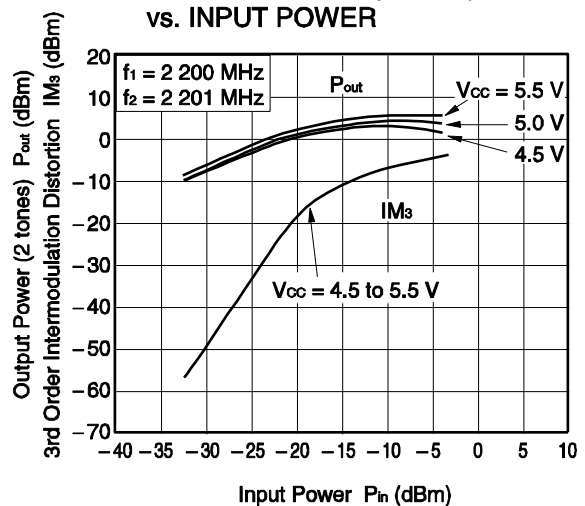
OUTPUT POWER vs. INPUT POWER



OUTPUT POWER (2 tones), IM3 vs. INPUT POWER



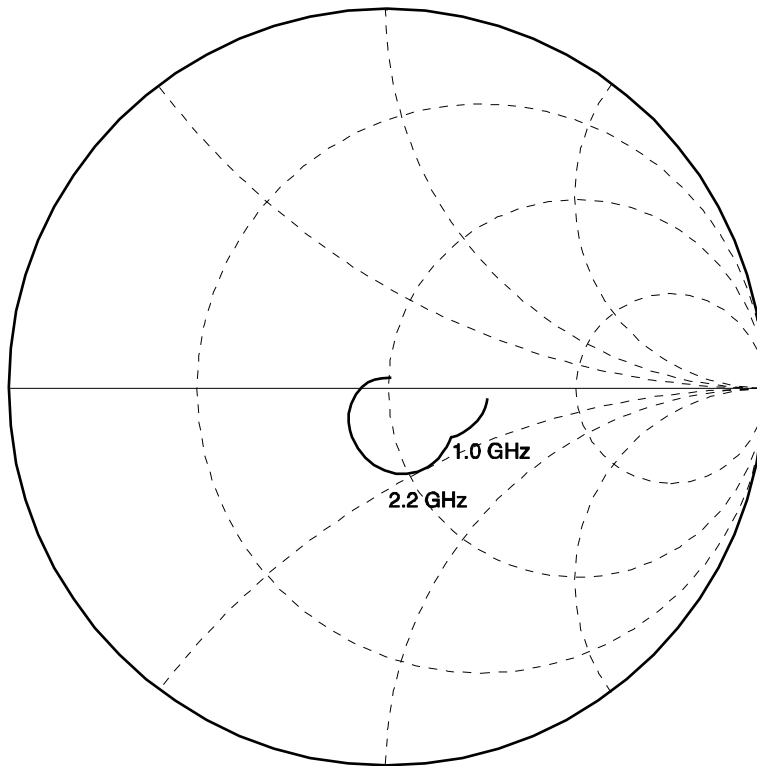
OUTPUT POWER (2 tones), IM3 vs. INPUT POWER



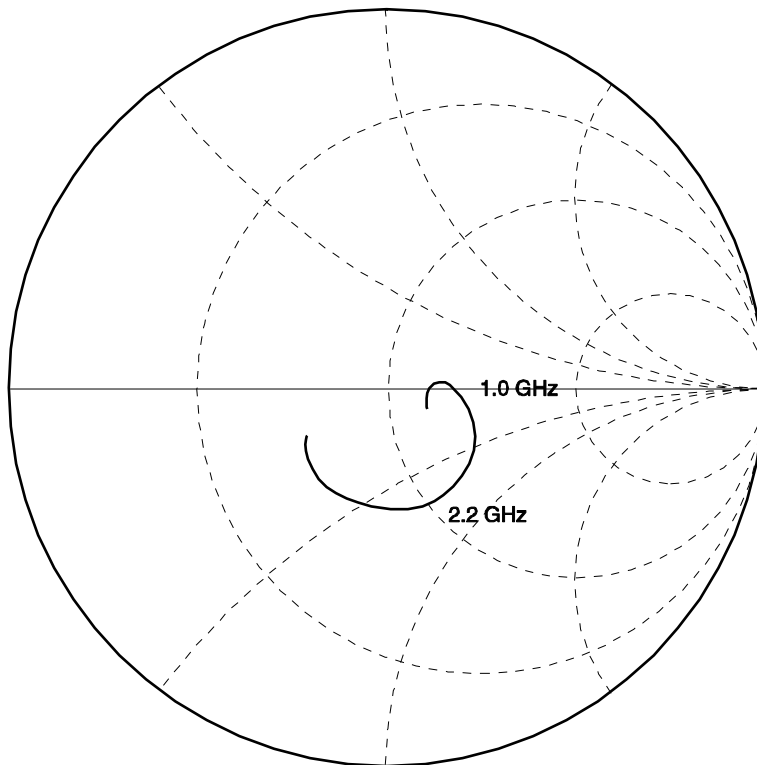
Remark The graphs indicate nominal characteristics.

**S-PARAMETERS ( $T_A = +25^\circ\text{C}$ ,  $V_{CC} = V_{out} = 5.0\text{ V}$ )**

**S<sub>11</sub>-FREQUENCY**

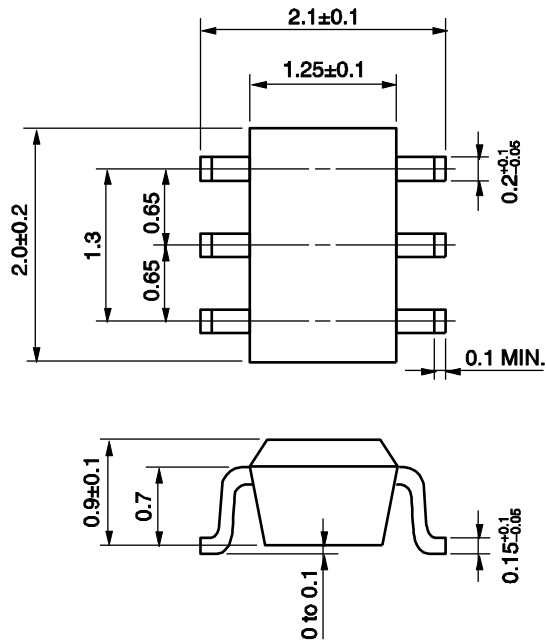


**S<sub>22</sub>-FREQUENCY**



PACKAGE DIMENSIONS

6-PIN SUPER MINIMOLD (UNIT: mm)



**NOTES ON CORRECT USE**

- (1) Observe precautions for handling because of electro-static sensitive devices.
- (2) Form a ground pattern as widely as possible to minimize ground impedance (to prevent undesired oscillation).  
All the ground pins must be connected together with wide ground pattern to decrease impedance difference.
- (3) The bypass capacitor should be attached to Vcc line.
- (4) The inductor must be attached between Vcc and output pins. The inductance value should be determined in accordance with desired frequency.
- (5) The DC cut capacitor must be each attached to input and output pin.

**RECOMMENDED SOLDERING CONDITIONS**

This product should be soldered and mounted under the following recommended conditions. For soldering methods and conditions other than those recommended below, contact your nearby sales office.

Soldering Method	Soldering Conditions	Condition Symbol
Infrared Reflow	Peak temperature (package surface temperature) : 260°C or below Time at peak temperature : 10 seconds or less Time at temperature of 220°C or higher : 60 seconds or less Preheating time at 120 to 180°C : 120±30 seconds Maximum number of reflow processes : 3 times Maximum chlorine content of rosin flux (% mass) : 0.2%(Wt.) or below	IR260
Wave Soldering	Peak temperature (molten solder temperature) : 260°C or below Time at peak temperature : 10 seconds or less Preheating temperature (package surface temperature) : 120°C or below Maximum number of flow processes : 1 time Maximum chlorine content of rosin flux (% mass) : 0.2%(Wt.) or below	WS260
Partial Heating	Peak temperature (pin temperature) : 350°C or below Soldering time (per side of device) : 3 seconds or less Maximum chlorine content of rosin flux (% mass) : 0.2%(Wt.) or below	HS350

**Caution Do not use different soldering methods together (except for partial heating).**

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Телефон: 8 (812) 309-75-97 (многоканальный)

Факс: 8 (812) 320-03-32

Электронная почта: [ocean@oceanchips.ru](mailto:ocean@oceanchips.ru)

Web: <http://oceanchips.ru/>

Адрес: 198099, г. Санкт-Петербург, ул. Калинина, д. 2, корп. 4, лит. А