

## Low voltage 16-bit constant current LED sink driver

Datasheet - production data



### Description

The STP16CPC26 is a monolithic, low voltage, 16-bit constant current LED sink driver. The device contains a 16-bit shift register and data latches, which convert serial input data into parallel output format. In the output stage sixteen regulated current generators provide 5 mA to 90 mA constant current to drive LEDs. The current is externally adjusted through a resistor. LED brightness can be adjusted from 0% to 100% via  $\overline{OE}$  pin.

The STP16CPC26 guarantees a 20 V driving capability, allowing users to connect more LEDs in series to each current source.

The high 30 MHz clock frequency makes the device suitable for high data rate transmission.

The thermal shutdown (170 °C with about 15 °C hysteresis) assures protection from overtemperature events.

The STP16CPC26 is housed in four different packages: QSOP24, SO-24, TSSOP-24 and HTSSOP-24 (with exposed pad).

### Features

- 16 constant current output channels
- Adjustable output current through external resistor
- Output current: 5 mA to 90 mA
- $\pm 1\%$  typical current accuracy bit to bit
- Max clock frequency: 30 MHz
- 20 V current generators rated voltage
- 3 - 5.5 V power supply
- Thermal shutdown for overtemperature protection

### Applications

- Video display panel LED driver
- Special lighting

Table 1: Device summary

Order code	Package	Packing
STP16CPC26MTR	SO-24	1000 parts per reel
STP16CPC26TTR	TSSOP24	2500 parts per reel
STP16CPC26XTR	TSSOP24 exposed pad	2500 parts per reel
STP16CPC26PTR	QSOP-24	2500 parts per reel

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# 1 Pin description

Figure 1: Pin connection



The exposed-pad (if present) should be electrically connected to a metal land electrically isolated or connected to ground.

Table 2: Pin description

Pin n°	Symbol	Name and function
1	GND	Ground terminal
2	SDI	Serial data input terminal
3	CLK	Clock input terminal
4	LE	Latch input terminal
5-20	OUT 0-15	Output terminal
21	$\overline{\text{OE}}$	Input terminal of output enable (active low)
22	SDO	Serial data out terminal
23	R-EXT	Input terminal for an external resistor for constant current programming
24	V <sub>DD</sub>	Supply voltage terminal

## 2 Electrical ratings

### 2.1 Absolute maximum ratings

Stressing the device above the rating listed in the “absolute maximum ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 3: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V <sub>DD</sub>	Supply voltage	0 to 7	V
V <sub>O</sub>	Output voltage	-0.5 to 20	V
I <sub>O</sub>	Output current	90	mA
V <sub>I</sub>	Input voltage	-0.4 to V <sub>DD</sub> +0.4	V
I <sub>GND</sub>	GND terminal current	1600	mA
ESD	Electrostatic discharge protection HBM human body model	±2	kV
f <sub>CLK</sub>	Clock frequency	30	MHz

### 2.2 Thermal data

Table 4: Thermal data

Symbol	Parameter	Value	Unit	
T <sub>A</sub>	Operating free-air temperature range	-40 to +125	°C	
T <sub>OPR</sub>	Operating temperature range	-40 to +150	°C	
T <sub>STG</sub>	Storage temperature range	-55 to +150	°C	
R <sub>thJA</sub>	Thermal resistance junction-ambient <sup>(1)</sup>	SO-24	60	°C/W
		TSSOP24	85	°C/W
		TSSOP24 <sup>(2)</sup> exposed pad	37.5	°C/W
		QSOP-24	72	°C/W

**Notes:**

<sup>(1)</sup> According with JEDEC standard 51-7.

<sup>(2)</sup> The exposed pad should be soldered directly to the PCB to realize the thermal benefits.

### 3 Electrical characteristics

$V_{DD} = 3.3\text{ V} - 5\text{ V}$ ,  $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise specified.

Table 5: Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{dd}$	Supply voltage		3		5.5	V
$V_{IH}$	Input voltage high level		$0.8 \cdot V_{dd}$	-	$V_{dd}$	
$V_{IL}$	Input voltage low level		GND	-	$0.2 \cdot V_{dd}$	
$V_{OL}$	Serial data output voltage (SDO) <sup>(1)</sup>	$I_{OH} = -1\text{ mA}$	-	-	0.4	
$V_{OH}$		$I_{OL} = +1\text{ mA}$	$V_{DD} - 0.4$	-	-	
$I_{OH}$	Output leakage current	$V_o = 20\text{ V}$ , Outn = OFF	-	-	0.5	$\mu\text{A}$
$\Delta I_{OL1}$	Current accuracy channel to channel <sup>(2)(3)</sup>	$V_{ds} = 0.3\text{ V}$ , $R_{EXT} = 900\text{ W}$ , $I_{OL} = 22\text{ mA}$	-	$\pm 1$	$\pm 3$	%
$\Delta I_{OL2}$		$V_{ds} = 0.6\text{ V}$ , $R_{EXT} = 360\text{ W}$ , $I_{OL} = 55\text{ mA}$	-	$\pm 1$	$\pm 3$	
$\Delta I_{OL3}$	Current accuracy device to device <sup>(2)</sup>	$V_{ds} = 0.3\text{ V}$ , $R_{EXT} = 900\text{ W}$ , $I_{OL} = 22\text{ mA}$	-	-	$\pm 6$	%
$\Delta I_{OL4}$		$V_{ds} = 0.6\text{ V}$ , $R_{EXT} = 360\text{ W}$ , $I_{OL} = 55\text{ mA}$	-	-	$\pm 6$	
$R_{IN(up)}$	Pull-up resistor for OE pin		250	500	800	KW
$R_{IN(down)}$	Pull-down resistor for LE pin		250	500	800	
IDD(OFF1)	Supply current (OFF)	$R_{EXT} = \text{OPEN}$ OUT 0 to 15 = OFF	-	3	7	mA
IDD(OFF2)		$R_{EXT} = 900\text{ W}$ OUT 0 to 15 = OFF	-	7	10	
IDD(OFF3)		$R_{EXT} = 360\text{ W}$ OUT 0 to 15 = OFF	-	11	13.5	
IDD(ON1)	Supply current (ON)	$R_{EXT} = 900\text{ W}$ OUT 0 to 15 = ON	-	7	11	
IDD(ON2)		$R_{EXT} = 360\text{ W}$ OUT 0 to 15 = ON	-	11	15	
$\%/dV_{DS}$	Output current vs. output voltage regulation	$V_{DS}$ from 1.0 V to 3.0 V $I_o = 22\text{ mA}$ $I_o = 55\text{ mA}$	-	$\pm 0.1$	-	$\%/V$

**Electrical characteristics**

**STP16CPC26**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
%/dV <sub>DD</sub>	Output current vs. supply voltage regulation <sup>(4)</sup>	I <sub>o</sub> = 22 mA; V <sub>DS</sub> = 0.3 V I <sub>o</sub> = 55 mA; V <sub>DS</sub> = 0.6 V	-	±1	-	%/V
Tsd	Thermal shutdown		-	170	-	°C
Tsd-hy	Thermal shutdown hysteresis <sup>(4)</sup>		-	15	20	

**Notes:**

<sup>(1)</sup> Specification referred to T<sub>J</sub> from -40 °C to +125 °C. Specification over the -40 to +125 °C T<sub>J</sub> temperature range are assured by design, characterization and statistical correlation.

<sup>(2)</sup> Tested with just one output ON.

<sup>(3)</sup>  $\Delta I_{OL+} = ((I_{OLmax} - I_{OLmean}) / I_{OLmean}) * 100$ ,  $D_{IOL-} = ((I_{OLmin} - I_{OLmean}) / I_{OLmean}) * 100$ , where  $I_{OLmean} = (I_{OLout1} + I_{OLout2} + \dots + I_{OLout16}) / 16$ .

<sup>(4)</sup> Guaranteed by design.

V<sub>DD</sub> = 3.3 V - 5 V, T<sub>j</sub> = 25 °C, unless otherwise specified.

Table 6: Switching characteristics

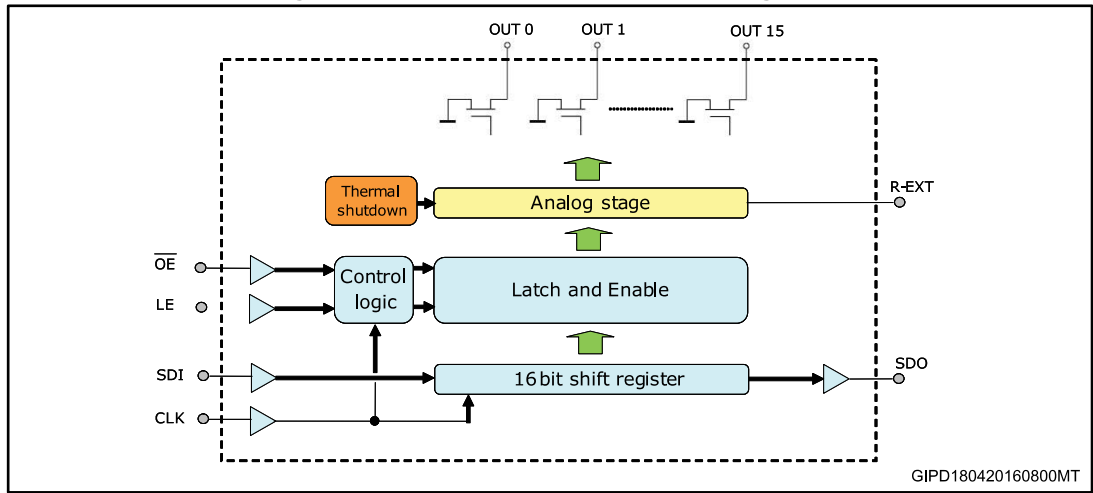
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit	
f <sub>clk</sub>	Clock frequency		-	-	30	MHz	
t <sub>PLH1</sub>	CLK - OUTn	V <sub>DS</sub> = 0.8 V V <sub>IH</sub> = V <sub>DD</sub> V <sub>IL</sub> = GND R <sub>EXT</sub> = 900 Ω R <sub>L</sub> = 50 Ω C <sub>L</sub> = 10 pF	-	100	-	ns	
t <sub>PLH2</sub>	LE - OUTn		-	100	-		
t <sub>PLH3</sub>	OE - OUTn		-	100	-		
t <sub>PLHa</sub>	CLK - SDO		V <sub>DD</sub> = 3.3 V	-	30		-
t <sub>PLHb</sub>			V <sub>DD</sub> = 5 V	-	20		-
t <sub>PHL1</sub>	CLK - OUTn		-	28	-		
t <sub>PHL2</sub>	LE - OUTn		-	28	-		
t <sub>PHL3</sub>	OE - OUTn		-	25	-		
t <sub>PHLa</sub>	CLK - SDO		V <sub>DD</sub> = 3.3 V	-	30		-
t <sub>PHLb</sub>			V <sub>DD</sub> = 5 V	-	20		-
t <sub>w(CLK)</sub>	CLK		Pulse width	20	-		-
t <sub>w(L)</sub>	LE			20	-		-
t <sub>w(OE)</sub>	OE			150	-		-
t <sub>su(L)</sub>	Setup time for LE		5	-	-		
t <sub>h(L)</sub>	Hold time for LE		5	-	-		
t <sub>su(D)</sub>	Setup time for SDI		5	-	-		
t <sub>h(D)</sub>	Hold time for SDI		10	-	-		
t <sub>r</sub> <sup>(1)</sup>	Maximum CLK rise time		-	-	5000		
t <sub>f</sub> <sup>(1)</sup>	Maximum CLK fall time		-	-	5000		
t <sub>or1a</sub>	Output rise time of Vout	V <sub>IH</sub> = V <sub>DD</sub> , V <sub>IL</sub> = GND	V <sub>DD</sub> = 3.3 V	-	95	-	
t <sub>or1b</sub>	Output rise time of Vout		V <sub>DD</sub> = 5 V	-	85	-	
t <sub>of1a</sub>	Output fall time of Vout	V <sub>DS</sub> = 0.8 V, R <sub>L</sub> = 50 Ω	V <sub>DD</sub> = 3.3 V	-	40	-	
t <sub>of1b</sub>	Output fall time of Vout	C <sub>L</sub> = 10 pF I <sub>out</sub> = 22 mA	V <sub>DD</sub> = 5 V	-	25	-	
t <sub>or2a</sub>	Output rise time of Vout	V <sub>IH</sub> = V <sub>DD</sub> , V <sub>IL</sub> = GND	V <sub>DD</sub> = 3.3 V	-	80	-	
t <sub>or2b</sub>	Output rise time of Vout		V <sub>DD</sub> = 5 V	-	70	-	
t <sub>of2a</sub>	Output fall time of Vout	V <sub>DS</sub> = 0.8 V R <sub>L</sub> = 50 Ω	V <sub>DD</sub> = 3.3 V	-	40	-	
t <sub>of2b</sub>	Output fall time of Vout	C <sub>L</sub> = 10 pF I <sub>out</sub> = 55 mA	V <sub>DD</sub> = 5 V	-	30	-	
I <sub>out-ov</sub>	Output current turn-on overshoot	V <sub>DS</sub> = 0.6 to 3V C <sub>L</sub> = 10 pF I <sub>out</sub> = 5 to 60 mA		-	-	0	%

Notes:

<sup>(1)</sup>If devices are connected in cascade and t<sub>r</sub> or t<sub>f</sub> is large, it may be critical to achieve the timing required for data transfer between two cascaded devices.

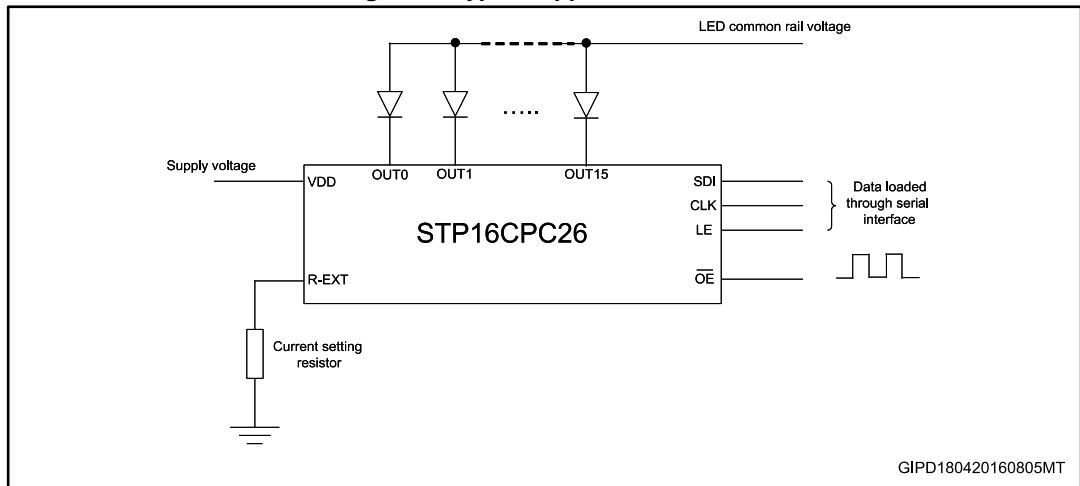
### 4 Simplified internal block diagram

Figure 2: STP16CPC26 simplified block diagram



### 5 Typical application circuit

Figure 3: Typical application circuit





## 6 Equivalent circuit and outputs

Figure 4: OE terminal



Figure 5: LE terminal

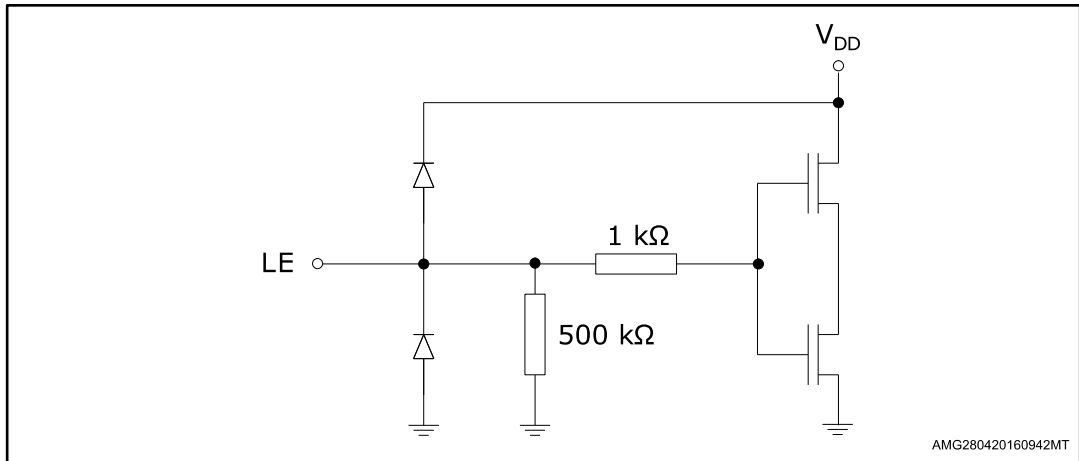


Figure 6: CLK, SDI terminal

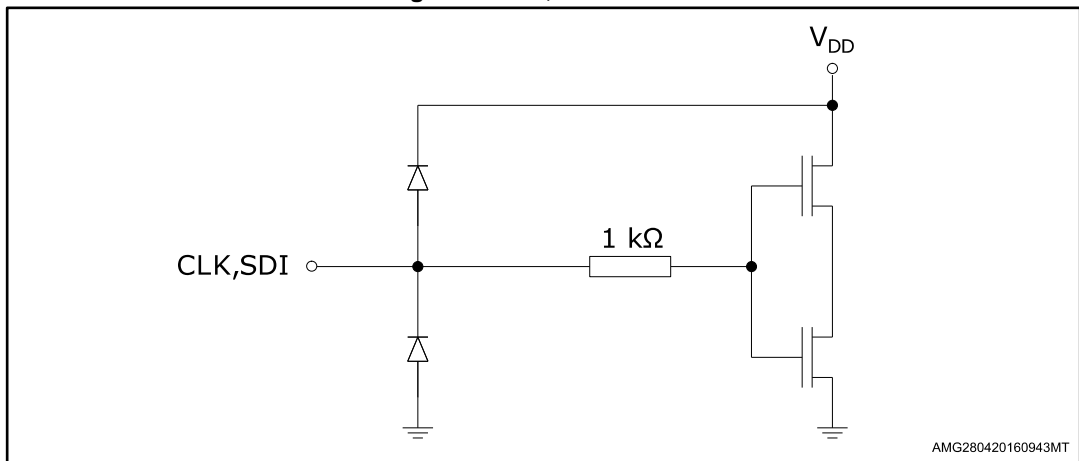


Figure 7: SDO terminal



## 7 Typical test circuits

Figure 8: "Typical test circuit for electrical characteristics" and Figure 9: "Typical test circuit for switching characteristics" show respectively the typical test circuit used measuring electrical (e.g. input voltage high/low level, output leakage current, supply current, etc.) and switching characteristics (propagation delays, set-up and hold time, rise and fall time of  $V_{OUT}$ , etc.). The resistor  $R_L$  and capacitor  $C_L$  in parallel connected to each output in Figure 8: "Typical test circuit for electrical characteristics" simulate a LED behavior.

Figure 8: Typical test circuit for electrical characteristics

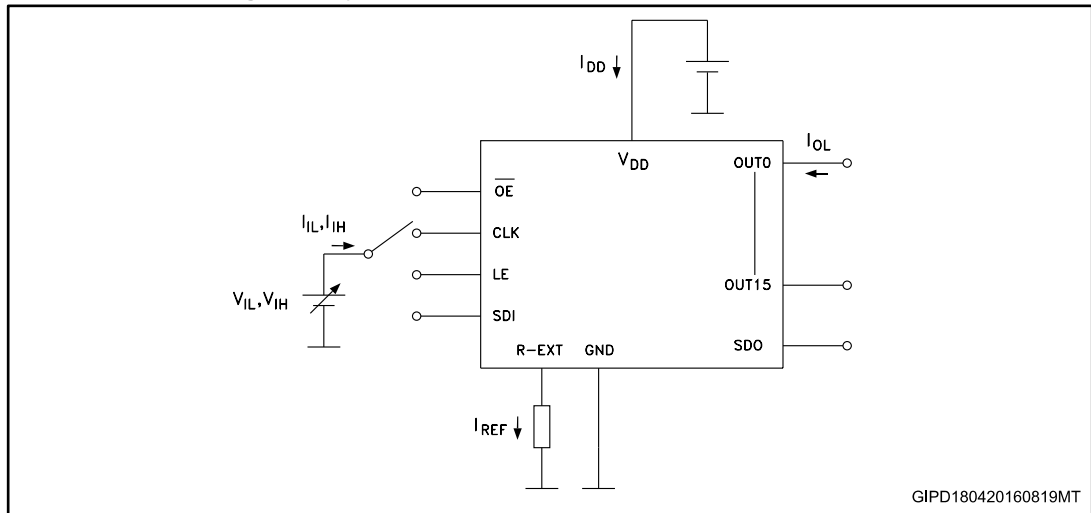
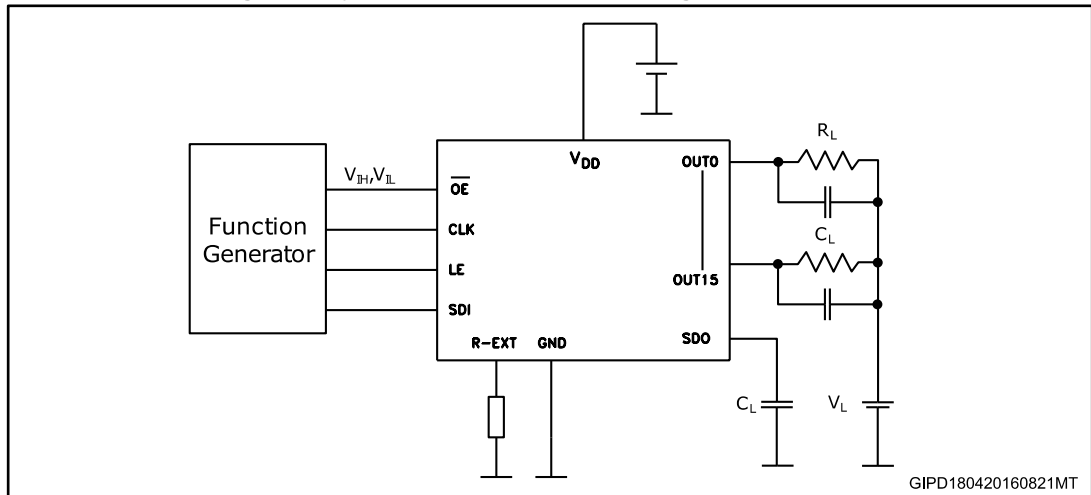


Figure 9: Typical test circuit for switching characteristics



## 8 Timing diagrams

The timing diagram shown in *Figure 10: "Timing diagram"* and the truth table in *Table 7: "Truth table"* explain how to send data to the device. This can be summarized in the following points:

- LE and  $\overline{OE}$  are level sensitive and not synchronized with the CLK signal
- When LE is at low level, the latch circuit holds previous data
- If LE is high level, data present in the shift register are latched
- When  $\overline{OE}$  is at low level, the status of the outputs OUT0 to OUT15 depends on the data in the latch circuits
- With  $\overline{OE}$  at high level, all outputs are switched off independently on the data stored in the latch circuits
- Every rising edge of the CLK signal, a new data on SDI pin is sampled. This data is loaded into the shift register, whereas a bit is shifted out from SDO

Figure 10: Timing diagram



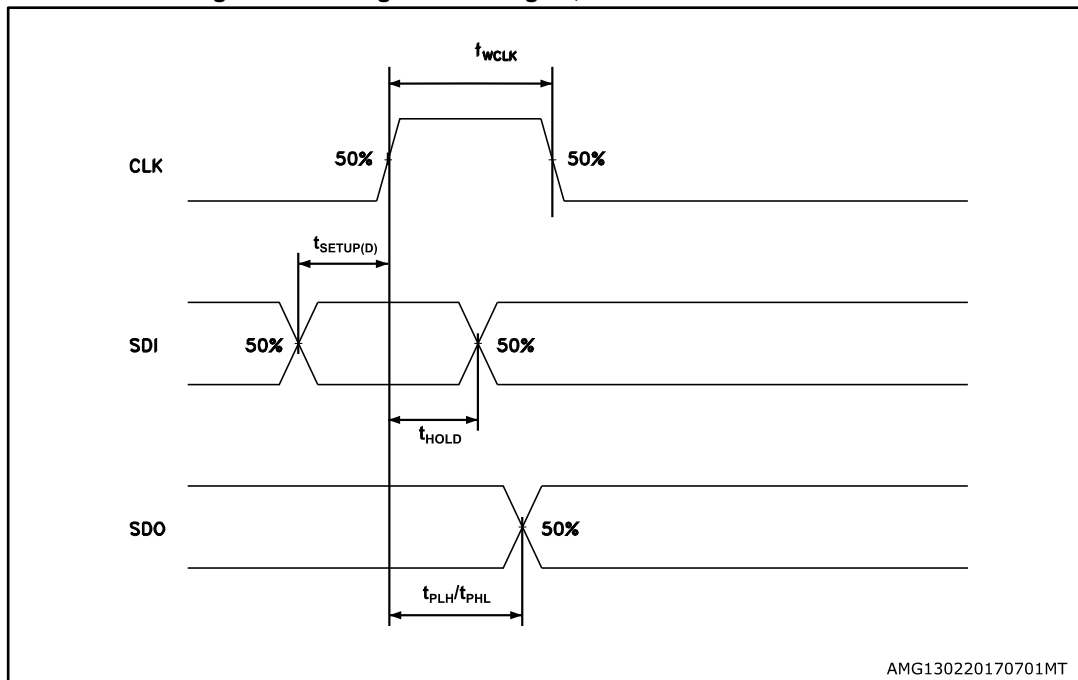
Table 7: Truth table

Clock	LE	$\overline{OE}$	Serial-IN	$\overline{OUT0}$ ..... $\overline{OUT7}$ ..... $\overline{OUT15}$ <sup>(1)</sup>	SDO
┌┐	H	L	Dn	Dn ..... Dn - 7 ..... Dn -15	Dn - 15
┌┐	L	L	Dn + 1	No change	Dn - 14
┌┐	H	L	Dn + 2	Dn + 2 ..... Dn - 5 ..... Dn -13	Dn - 13
┐┌	X	L	Dn + 3	Dn + 2 ..... Dn - 5 ..... Dn -13	Dn - 13
┐┌	X	H	Dn + 3	OFF	Dn - 13

**Notes:**

<sup>(1)</sup> OUTn = ON when Dn = H, OUTn = OFF when Dn = L.

Figure 11: Timing for clock signal, serial-in and serial out data

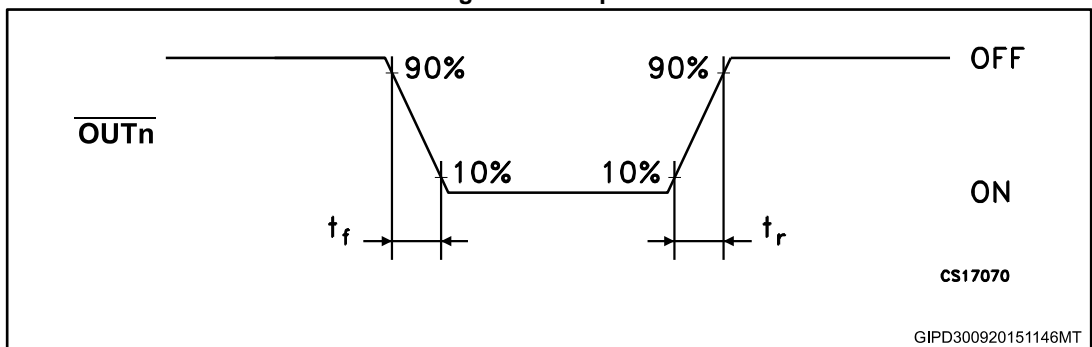


The correct sampling of the data depends on the stability of the data at SDI on the rising edge of the clock signal and it is assured by a proper data setup and hold time ( $t_{\text{SETUP}(D)}$  and  $t_{\text{HOLD}}$ ), as shown in [Figure 11: "Timing for clock signal, serial-in and serial out data"](#). The same figure shows the propagation delay from CLK to SDO ( $t_{\text{PLH}}/t_{\text{PHL}}$ ). [Figure 12: "Timing for clock signal serial-in data, latch enable, output enable and outputs"](#) describes the setup times for LE and  $\overline{\text{OE}}$  signals ( $t_{\text{SETUP}2}$  and  $t_{\text{SETUP}3}$  respectively), the minimum duration of these signals ( $t_{\text{WLAT}}$  and  $t_{\text{WENA}}$  respectively) and the propagation delay from CLK to  $\text{OUT}_n$ , LE to  $\text{OUT}_n$  and  $\overline{\text{OE}}$  to  $\text{OUT}_n$  ( $t_{\text{PLH}1}/t_{\text{PHL}1}$ ,  $t_{\text{PLH}2}/t_{\text{PHL}2}$  and  $t_{\text{PLH}3}/t_{\text{PHL}3}$  respectively). Finally [Figure 13: "Outputs"](#) defines the turn-on and turn-off time ( $t_r$  and  $t_f$ ) of the current generators.

Figure 12: Timing for clock signal serial-in data, latch enable, output enable and outputs



Figure 13: Outputs

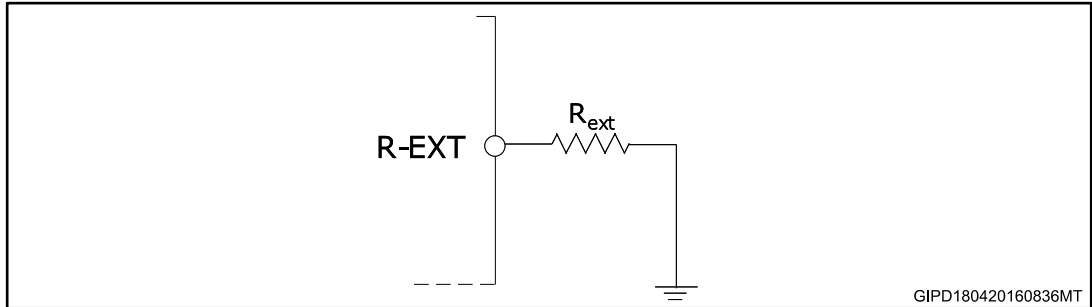


## 9 Current generators characteristics

### 9.1 Current setting

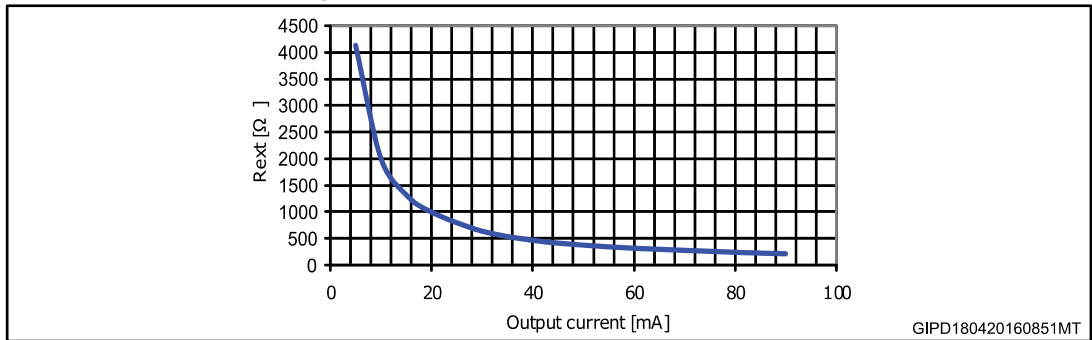
The current of all outputs is programmed through an external resistor connected to R-EXT pin, as shown in [Figure 14: "Resistor for current programming"](#). The curve in [Figure 15: "Output current vs R-EXT resistor"](#) describes the relation between the current and the resistor connected to R-EXT pin, whereas the [Table 8: "Recommended values of R<sub>ext</sub> for some output current value"](#) shows how to set some typical current values.

Figure 14: Resistor for current programming



GIPD180420160836MT

Figure 15: Output current vs R-EXT resistor



GIPD180420160851MT

Table 8: Recommended values of R<sub>ext</sub> for some output current value

Output current [mA]	R <sub>ext</sub> [Ω]	Closer standard value (E24 series) [Ω]
5	4129	4300
10	2005	200
20	999	1000
40	471	470
60	322	330
90	217	220

### 9.2 Current accuracy

A typical current accuracy of ±1% (±3% maximum) between channels is guaranteed at 22 mA and 55 mA output current (refer to [Table 6: "Switching characteristics"](#)) and ± 6% (maximum) current accuracy between ICs.

### 9.3 Generators voltage drop

In order to correctly regulate the current, a minimum dropout voltage must be assured across the current generators.

*Figure 16: "Dropout voltage vs output current" and Table 9: "Dropout voltage vs output current" provides just an indicative idea about the dropout voltage to assure over the current range. However it is recommended to use value of  $V_{DROP}$  slightly higher than those indicated in Figure 16: "Dropout voltage vs output current" and Table 9: "Dropout voltage vs output current".*

**Figure 16: Dropout voltage vs output current**



**Table 9: Dropout voltage vs output current**

Output current [mA]	$V_{DROP}$ @ 3.3 V [mV]	$V_{DROP}$ @ 5 V [mV]
5	44	44
10	85	85
20	170	170
40	350	330
60	530	500
90	820	770

## 10 Thermal shutdown

The STP16CPC26 is featured with a thermal shutdown. This protection is triggered if the junction temperature reaches 170 °C. When the thermal shutdown is activated, all outputs are turned off independently on the data latched. Once the temperature decreases (thermal shutdown hysteresis is typically 15 °C), the outputs are enabled again and the device keeps on working.

Once the temperature decreases (thermal shutdown hysteresis is typically 15°C), the outputs are enabled again and the device keeps on working.



## 11 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

# 11.1 QSOP-24 package information

Figure 17: QSOP-24 package outline



Table 10: QSOP-24 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	1.54	1.62	1.73
A1	0.10	0.15	0.25
A2		1.47	
b	0.20		0.31
c	0.17		0.254
D	8.56	8.66	8.76
E	5.80	6.00	6.20
E1	3.80	3.91	4.01
e		0.635	
L	0.40	0.635	0.89
h	0.25	0.33	0.41
<	0°		8°

### 11.2 SO-24 package information

Figure 18: SO-24 package outline



Table 11: SO-24 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.35		2.65
A1	0.10		0.30
B	0.33		0.51
C	0.23		0.32
D	15.20		15.60
E	7.40		7.60
e		1.27	
H	10.00		10.65
h	0.25		0.75
L	0.40		1.27
k	0		8
ddd			0.10

### 11.3 TSSOP24 package information

Figure 19: TSSOP24 package outline

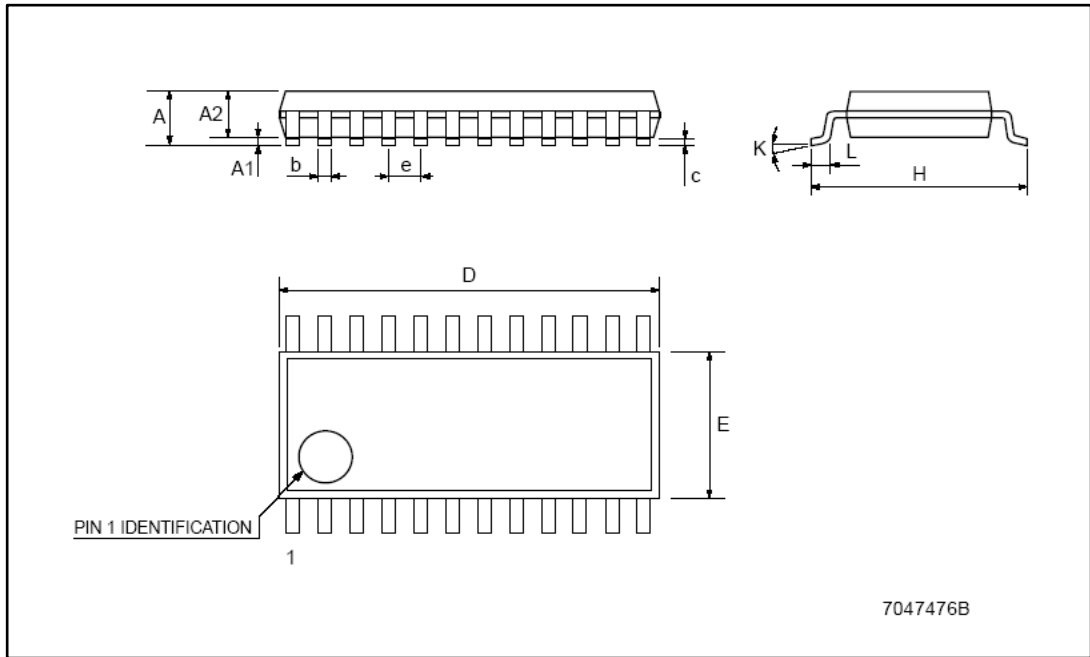


Table 12: TSSOP24 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			1.1
A1	0.05		0.15
A2		0.9	
b	0.19		0.30
c	0.09		0.20
D	7.7		7.9
E	4.3		4.5
e		0.65 BSC	
H	6.25		6.5
K	0°		8°
L	0.50		0.70

### 11.4 TSSOP24 exposed pad package information

Figure 20: TSSOP24 exposed pad package outline



Table 13: TSSOP24 exposed pad mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			1.20
A1			0.15
A2	0.80	1.00	1.05
b	0.19		0.30
c	0.09		0.20
D	7.70	7.80	7.90
D1	4.80	5.00	5.2
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
E2	3.00	3.20	3.40
e		0.65	
L	0.45	060	075
L1		1.00	
k	0°		8°
aaa			0.10



### 11.5 TSSOP24, TSSOP24 exposed pad and SO-24 packing information

Figure 21: TSSOP24, TSSOP24 exposed pad and SO-24 reel outline

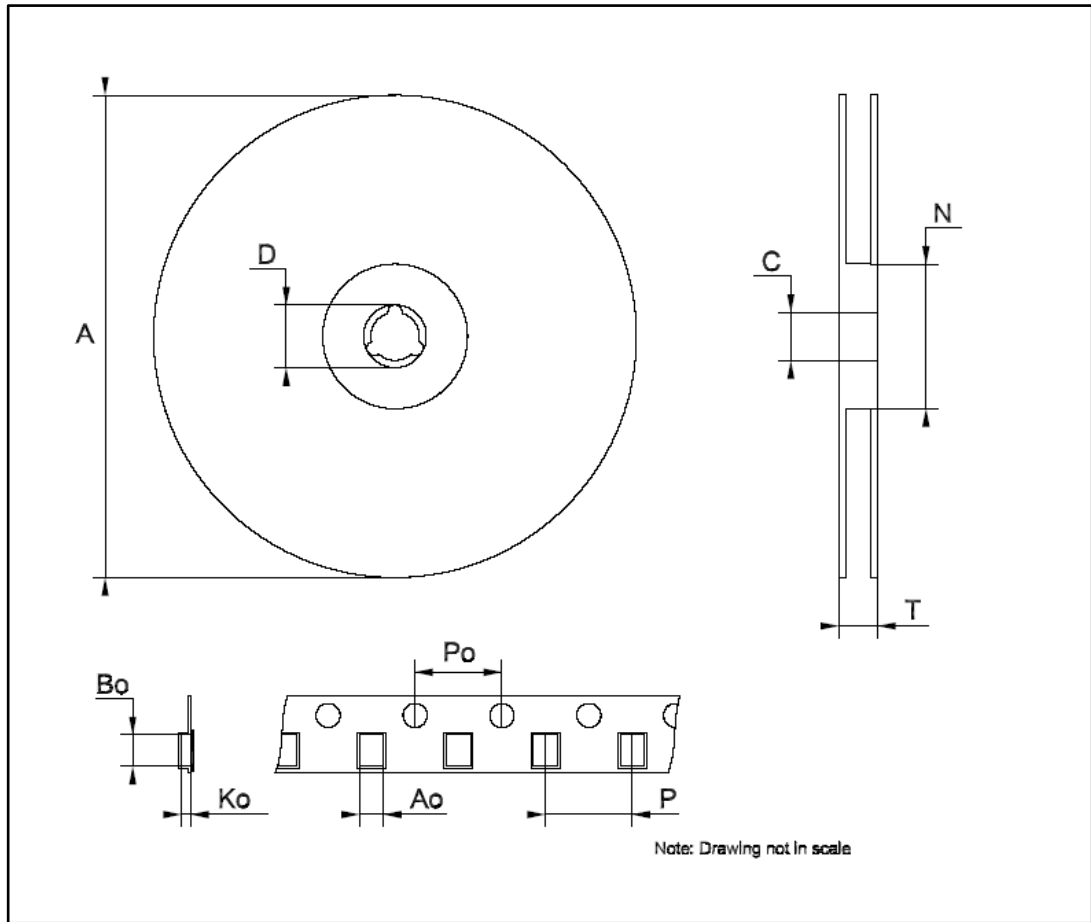


Table 14: TSSOP24 and TSSOP24 exposed pad tape and reel mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A		-	330
C	12.8	-	13.2
D	20.2	-	
N	60	-	
T		-	22.4
Ao	6.8	-	7
Bo	8.2	-	8.4
Ko	1.7	-	1.9
Po	3.9	-	4.1
P	11.9	-	12.1

Table 15: SO-24 tape and reel mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A		-	330
C	12.8	-	13.2
D	20.2	-	
N	60	-	
T		-	30.4
Ao	10.8	-	11.0
Bo	15.7	-	15.9
Ko	2.9	-	3.1
Po	3.9	-	4.1
P	11.9	-	12.1

## 12 Revision history

**Table 16: Document revision history**

Date	Revision	Changes
04-Mar-2011	1	First release
05-Apr-2011	2	Updated Table 6
19-Jul-2012	3	Updated Table 7.
19-Jul-2012	4	Updated characteristics in Table 5: Electrical characteristics and Table 6: Switching characteristics. Minor text changes.
1-Jun-2014	5	Updated template and value Table 13: TSSOP24 exposed pad mechanical data.
13-Apr-2017	6	Updated <i>Figure 11: "Timing for clock signal, serial-in and serial out data"</i> and <i>Figure 12: "Timing for clock signal serial-in data, latch enable, output enable and outputs"</i> , <i>Section 11.1: "QSOP-24 package information"</i> . Minor text changes.

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