Lattice 7:1 LVDS Video Demo Kit User's Guide

June 2007 Technical Note TN1134

Introduction

The Lattice 7:1 LVDS Video Demo Kit is a set of boards intended to bring RGB video data into the LatticeECP2™ FPGA where it can be processed and transmitted to an output display. It is intended to be used as a reference design and to demonstrate the capabilities of the LatticeECP2 FPGA in video processing applications.

The complete kit consists of up to five boards. The heart of the kit is the LatticeECP2 Advanced Evaluation Board, featuring a LatticeECP2-50 FPGA device. The kit is optionally available without this board.

The other four boards feature the required I/O interfaces to complete the demonstration. These are described in more detail below.

About This Guide

This document includes descriptions of the design of the boards, the design of the IP for the LatticeECP2™ FPGA, the items required to run the demonstration, and how to connect the boards and the cables for the demo.

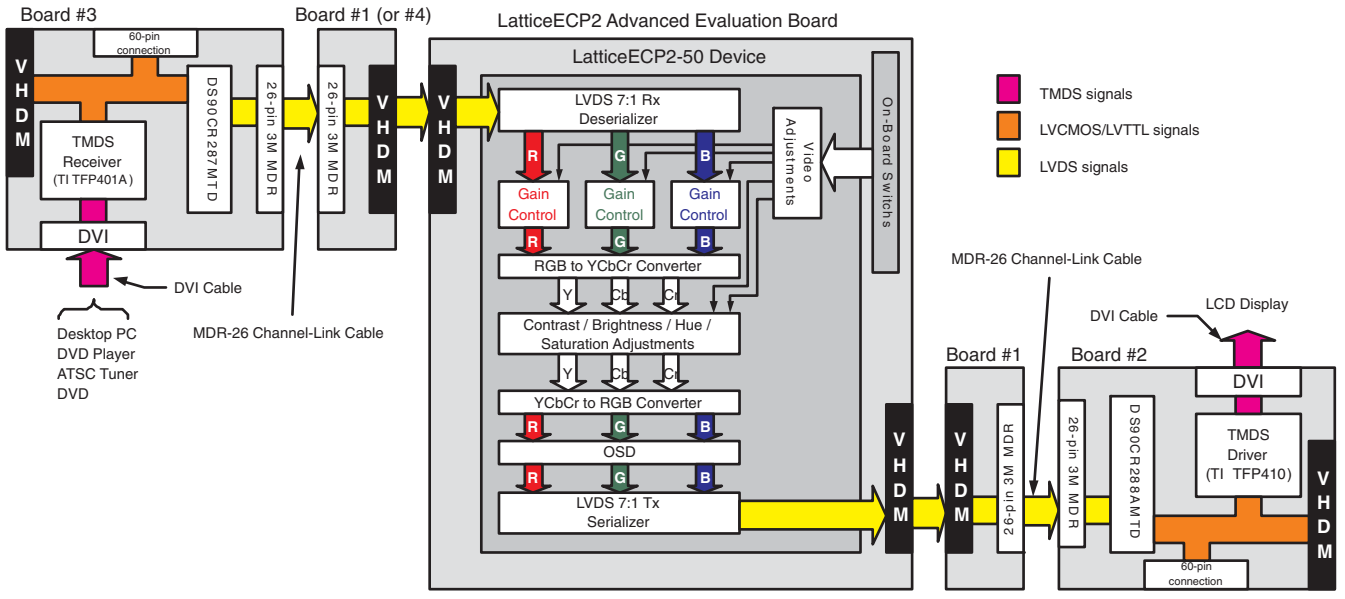
Additional Resources

Additional resources related to the Lattice 7:1 LVDS Video Demo Kit, including updated documentation, HDL source and bitstream programming files for the LatticeECP2 FPGA, a user's guide for the LatticeECP2 Advanced Evaluation Board, and other related materials can be downloaded from the Lattice web site at: www.latticesemi.com/boards. Navigate to the page for the Lattice 7:1 LVDS Video Demo Kit, and see the "documents and downloads" link on the left side of the page.

7:1 Video Demonstration Setup and Design

Figure 1 is an overview of the connection between the boards, the required cables, and a block diagram of the demo design implemented in LatticeECP2-50. The video signals are color-coded to indicate the different I/O standards including TMDS (pink), LVCMOS/LVTTL (orange), and LVDS (yellow).

Figure 1. Block Diagram of the Lattice 7:1 LVDS Video Demo Kit Setup



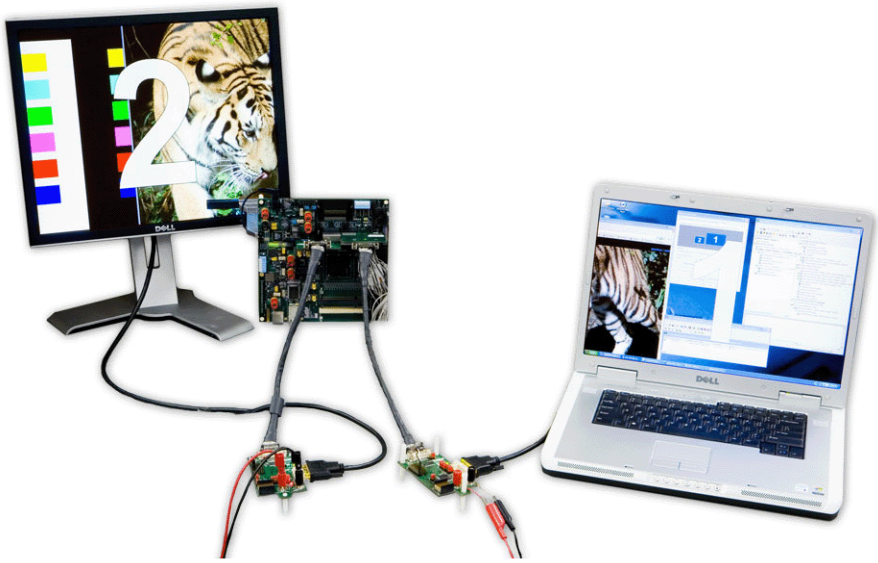
In this setup, DVI-I video signals must first be generated by a PC or an equivalent source. On Video Demo board #3, the TMDS signals of the DVI-I interface are first converted to LVCMOS/LVTTL using the TFP401A, then converted again to LVDS using the DS90CR287MTD. These LVDS signals are then fed to the LatticeECP2-50 through the MDR Channel Link cable and Video Demo Board #4. Video Demo Board #4 is connected to the LatticeECP2 Advanced Evaluation Board with a VHDM connector.

The demo design is implemented in the LatticeECP2-50 FPGA. This design is described in further detail later in this guide, and is based on Lattice reference design RD1030, *LatticeECP2/M 7:1 LVDS Video Interface.* Source code for this design is available in both the VHDL and Verilog languages. The LVDS video signal is de-serialized by the LatticeECP2-50 for extracting the 8-bit R, 8-bit G, and 8-bit B pixel datum. Then the 8-bit R, G, B pixel datum are adjusted by their own gain control block, and then the Contrast/Brightness/Hue/Saturation adjustment block, before adding the OSD (On-Screen-Display). After the OSD is added to the video stream, the final R, G, B datum are serialized and transmitted via the LatticeECP2-50 LVDS I/Os.

The remainder of the setup is similar to the video input side but reversed. The LVDS signals are fed via a VHDM connector to the Video Demo board #1, then to the Video Demo board #2 via the MDR cable. The LVDS signals are then converted to LVCMOS/LVTTL using the DS90CR288A on the Video Demo board #2. Finally the LVCMOS/LVTTL video signals are converted to the DVI / TMDS signals using the TFP410 and sent to the LCD display.

Figure 2 shows a complete Video Demo system setup, with an input source (laptop) and monitor. In this example, power is supplied to Video Demo Boards 2 and 3 from an external source (not shown).

Figure 2. Video Demo System Setup



Prepare for the Video Demo

Before running the demo, you need the following video source and video sink.

- Video source: a desktop or a laptop PC with a DVI output port.
- Video sink: a LCD display with a DVI input port and a DVI cable.

  Note: The display must be an actual DVI, digital display. Some DVI sources also include an RGB analog component, which allow the use a simple VGA -> DVI converter to supply input to an analog VGA monitor. These converters simply adapt the physical plugs to supply the RGB component signals contained in the DVI cable to a VGA style plug. However, this video demo kit does not re-transmit any analog component signals; the output is purely digital. As such, a simple converter will not work.

If your PC does not have a DVI output, you may purchase a VGA-to-DVI converter (such as the CP-261D) to convert your PC's video signal from VGA to DVI. The PC screen resolution needs to be set to any of the following to run this demo.

- 640x480, 75Hz
- 800x600, 60Hz or 75Hz
- 1024x768, 60Hz or 75Hz
- 1152x864, 75Hz
- 1280x1024, 60Hz

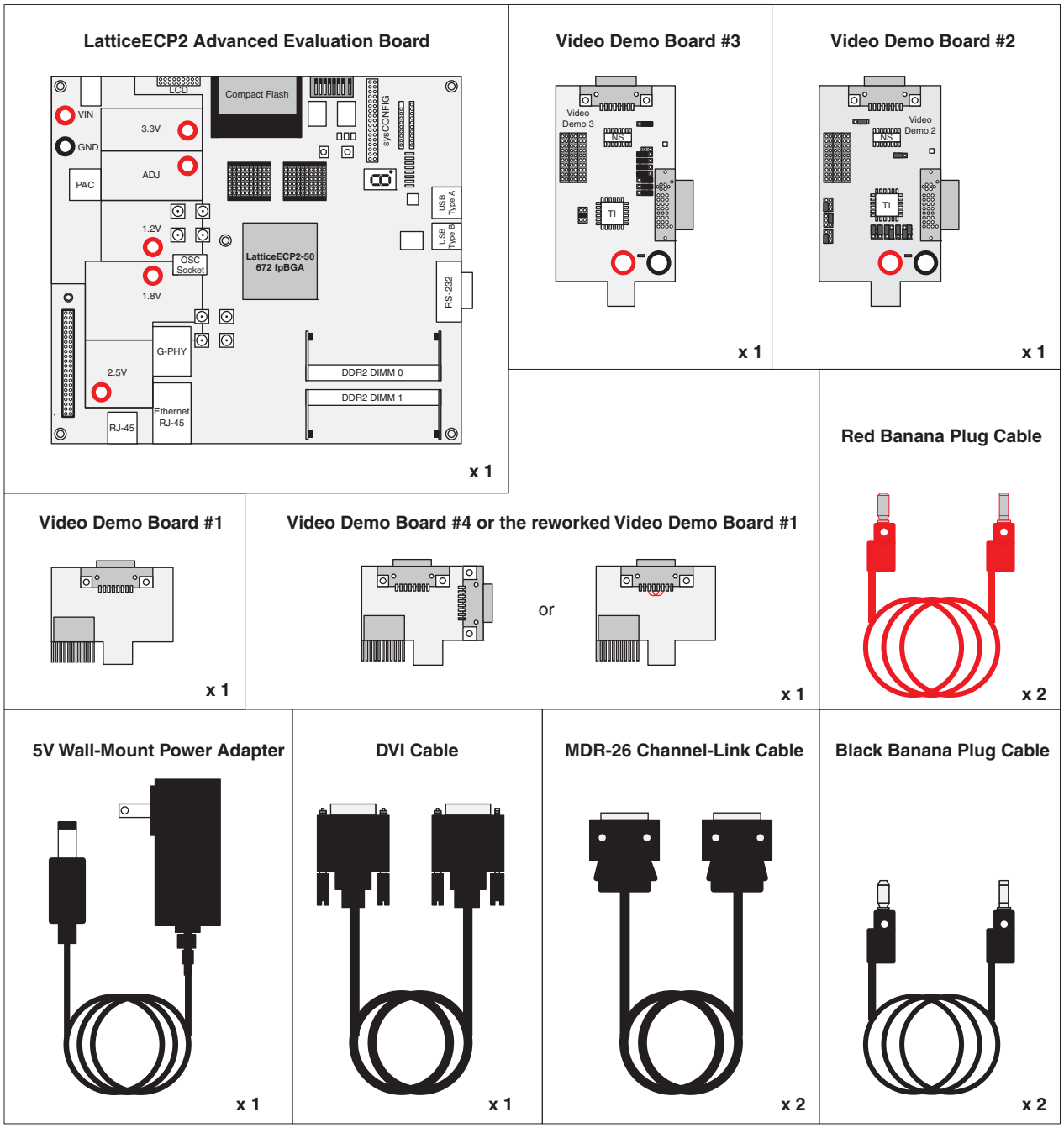
The Lattice 7:1 Video Demo Kit includes the following items:

Table 1. Lattice 7:1 Video Demo Kit Contents

Item	Description	Quantity
1	LatticeECP2 672fpBGA Advanced Evaluation board[1]	1
2	5V wall-mount power adapter[1]	1
3	Video Demo board #1	1
4	Video Demo board #4[2]	1
5	Video Demo board #2	1
6	Video Demo board #3	1
7	DVI cable	1
8	MDR-26 Channel-Link cable	2
9	Black banana plug cable	2
10	Red banana plug cable	2

1. The Lattice 7:1 Video Demo Kit is available with or without the LatticeECP2 Advanced Evaluation Board and 5V wall-mount power adapter.
2. Some early versions of this kit may include a modified version of "Video Demo Board #1" as a substitute for the "Video Demo Board #4". In these cases, Video Demo Board #4 can be differentiated by two small wires connected to the MDR I/O. See the diagram below for an example. In this document, this board will be referenced only as "Video Demo Board #4", as the function of either version is the same.

Figure 3. Lattice 7:1 Video Demo Kit Contents

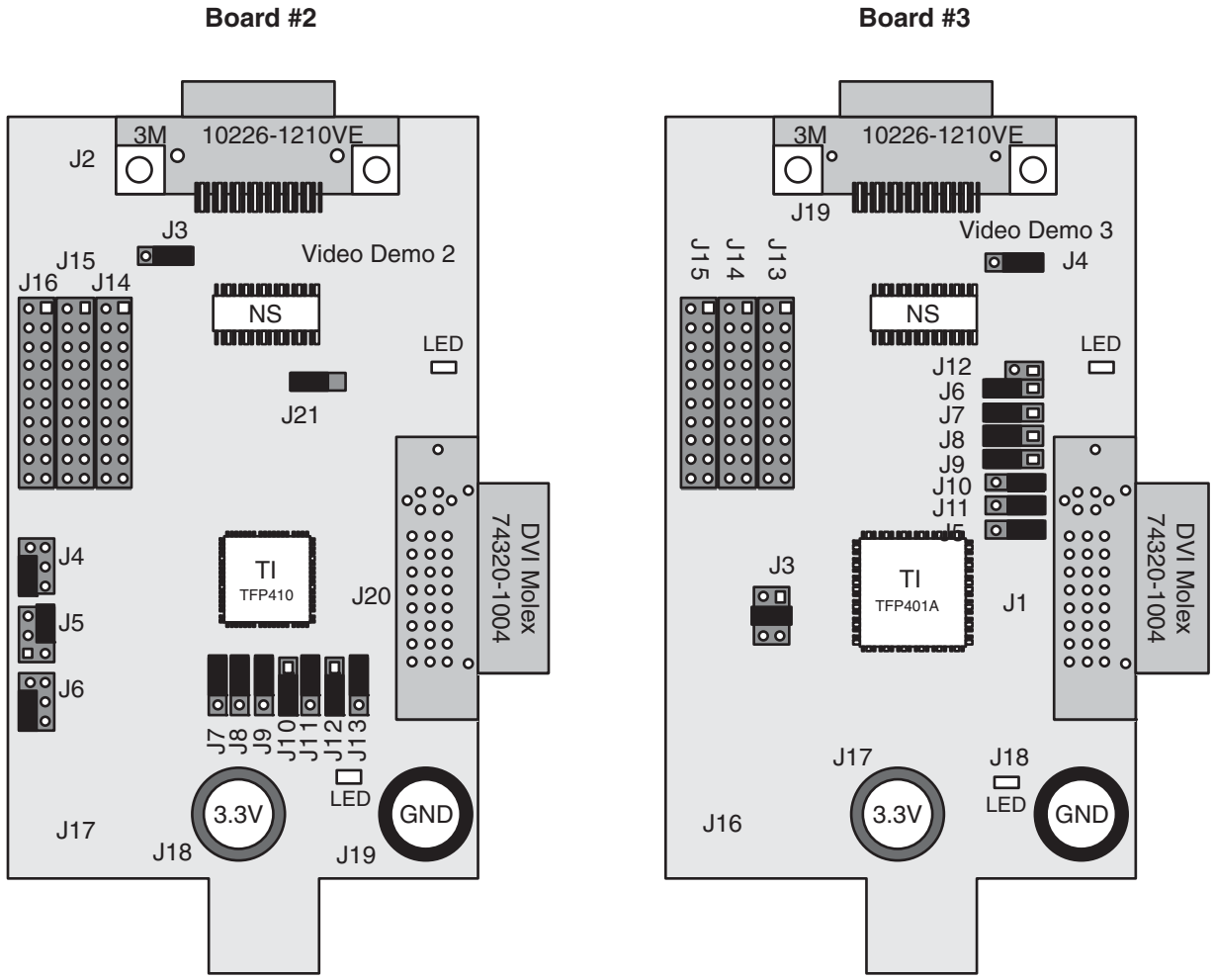


After you verify you have the proper equipment for the video demo, make sure all the jumpers on the boards are set correctly. The default jumper settings of Video Demo Boards #2 and #3 are shown below. The detailed functions of these jumpers can be found in Appendix A and Appendix B at the end of this user's guide.

- Video Demo Board #2 Default Jumper Settings:
  - Install jumpers on pin1-pin2 of J3, J7, J8, J9, J11, J13 and J21.
  - Install jumpers on pin2-pin3 of J10 and J12.
  - Install jumpers on pin1-pin3 of J4 and J6.
  - Install jumper on pin4-pin6 of J5.

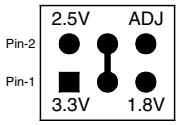
- Video Demo Board #3 Default Jumper Settings:
  - Install jumpers on pin1-pin2 of J4, J5, J10 and J11.
  - Install jumpers on pin2-pin3 of J6, J7, J8 and J9.
  - Install jumper on pin3-pin4 of J3.

Figure 4. Block Diagram and Default Jumper Settings of Video Demo Boards #2 and #3



For the I/O bank voltage setting on the LatticeECP2 Advanced Evaluation Board, bank 2 and bank 3 must be to be set to 2.5V. Bank 0, 1, 4, 7 should all be set to 3.3V. The following table shows the proper jumper settings for the Lattice 7:1 Video Demo.

Table 2. Jumper Settings for the LatticeECP2 Advanced Board

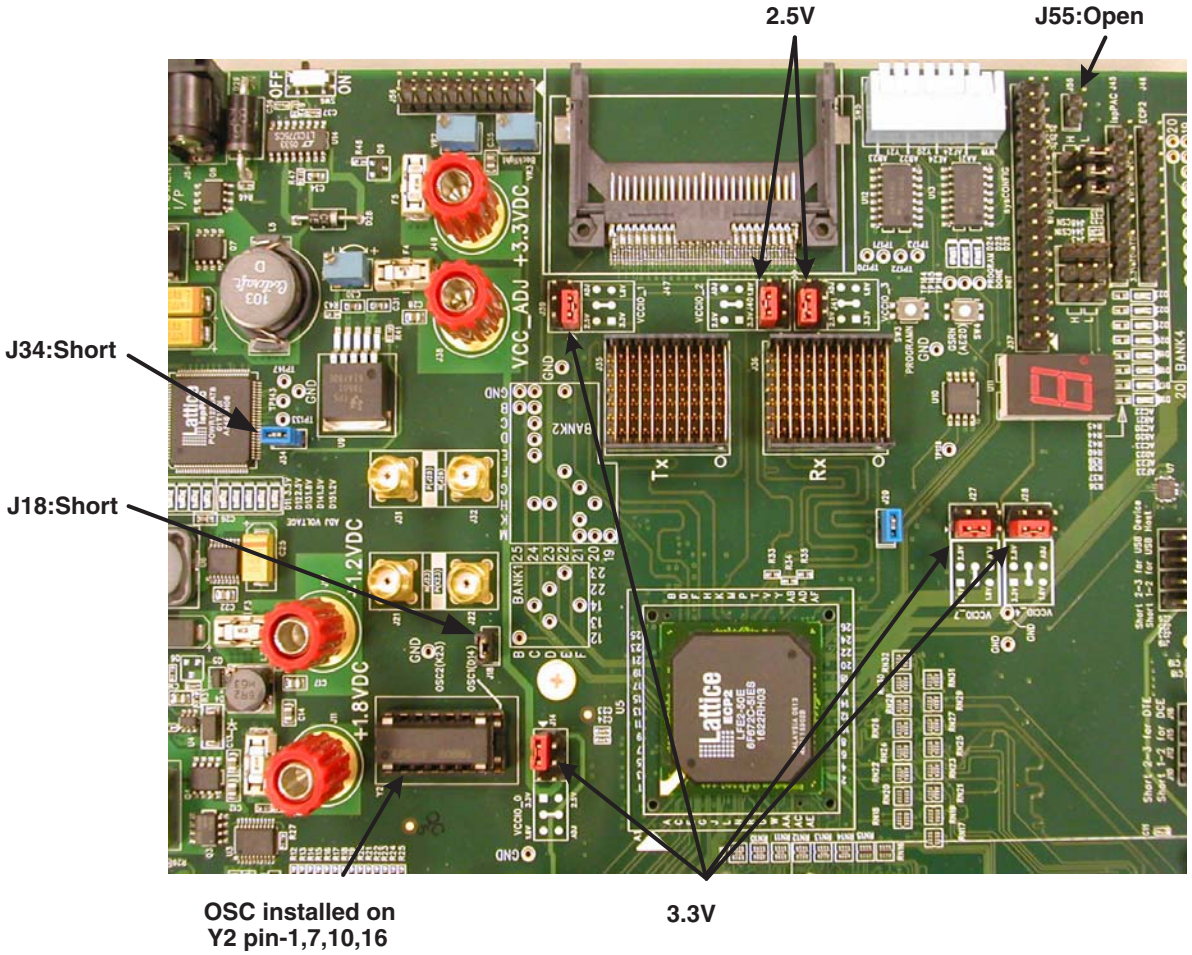
sysIO Bank	Jumper	Jumper on Pins	
0	J14	1-3 -> VCC_3.3V 2-4 -> VCC_2.5V 3-5 -> VCC_1.8V 4-6 -> VCC_ADJ	
1	J39		
2	J40		
3	J41		
4	J28		
7	J27		
5	NA	Tied to 1.8V (Cannot be changed)	
6			

Jumpers J34 and J55 are used for the JTAG chain connection setting. Please make sure they are at their default settings (J34: short and J55: open), which makes the LatticeECP2-50 the only device in the JTAG chain.

The OSD of this demo is controlled by a LatticeMico8™ microprocessor that requires an external clock from the on-board oscillator. If a full size oscillator is used, make sure the oscillator on Y2 is installed on pins 1, 7, 10 and 16, as seen in Figure 5. If a half size oscillator is used, make sure the oscillator on Y2 is installed on pins 1, 4, 13 and 16. In addition, Jumper J18 must be shorted to connect the oscillator clock output to the LatticeECP2-50 device.

The locations of these jumpers are shown below.

Figure 5. Jumper Settings on the LatticeECP2 Advanced Evaluation Board



If you are using the optional CP-261D VGA-to-DVI converter to convert your PC's video signal from VGA to DVI, set both the input switches and the output switches to "RGB".

Boards and Cables Connections

Once you have everything needed for the demo and all the board settings are correct, you may start connecting the boards and cables, step by step. If this is your first time to run this demo, it's highly recommended to follow the steps below.

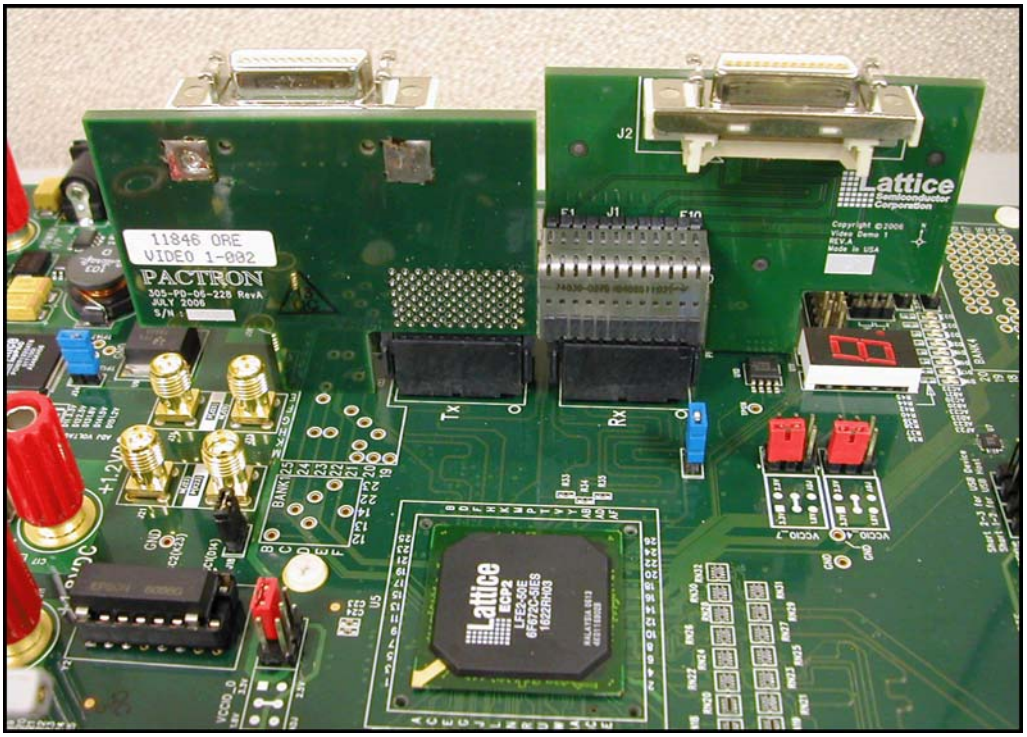
- **Step 1: Install Board #1 and Board #4**
  Boards #1 and #4 convert the LVDS signals on the MDR-26 Channel Link cable to the VHDM connector, so the LVDS signals can be transmitted to the LatticeECP2-50 672 fpBGA device.

Board #4 is used for the LVDS input on the Rx side and should be installed onto J36 of the LatticeECP2 Advanced Evaluation Board.

Board #1 is used for the LVDS output on the Tx side and should be installed onto J35 of the LatticeECP2 Advanced Evaluation Board.

After installation of these two boards, the boards should be perpendicular to the LatticeECP2 Advanced Evaluation Board. Figure 6 shows the proper installation of Board #1 (Tx side on the left) and Board #4 (Rx side on the right) installed on the LatticeECP2 Advanced Evaluation Board. (Note: in this figure, the Board #4 shown is the earlier, modified version of Board #1).

Figure 6. Proper Installation of Video Demo Boards #1 and #4 to the Lattice ECP2 Advanced Evaluation Board

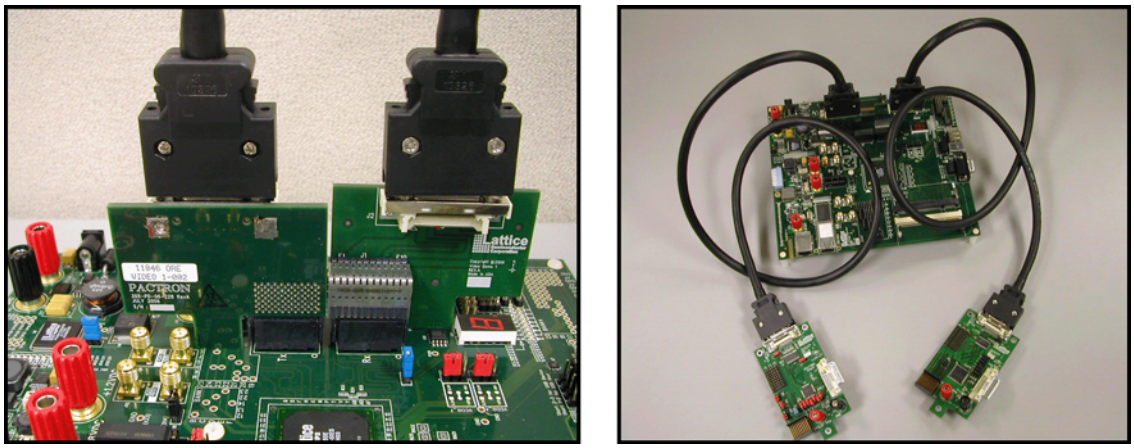


- **Step 2: Connect the MDR-26 Cables**
  The two MDR-26 Channel Link cables are used for connecting the Rx and the Tx LVDS signals. They are used between the following boards:

  – Rx: Between Video Demo board #3 and #4
  – Tx: Between Video Demo board #2 and #1

Figure 7 shows the connections between these boards.

Figure 7. Proper Connection of the MDR-26 Channel Link Cables



- **Step 3: Connect the DVI Cables**
  This demo requires two DVI cables. The video demo kit contains only one DVI cable. Therefore, you must use the original DVI cable that comes with the LCD display as well.

  If you are using a VGA-to-DVI converter to supply the DVI input, please be sure to set the converter's input and output switches to "RGB", then connect the converter's power, the VGA and DVI cables.

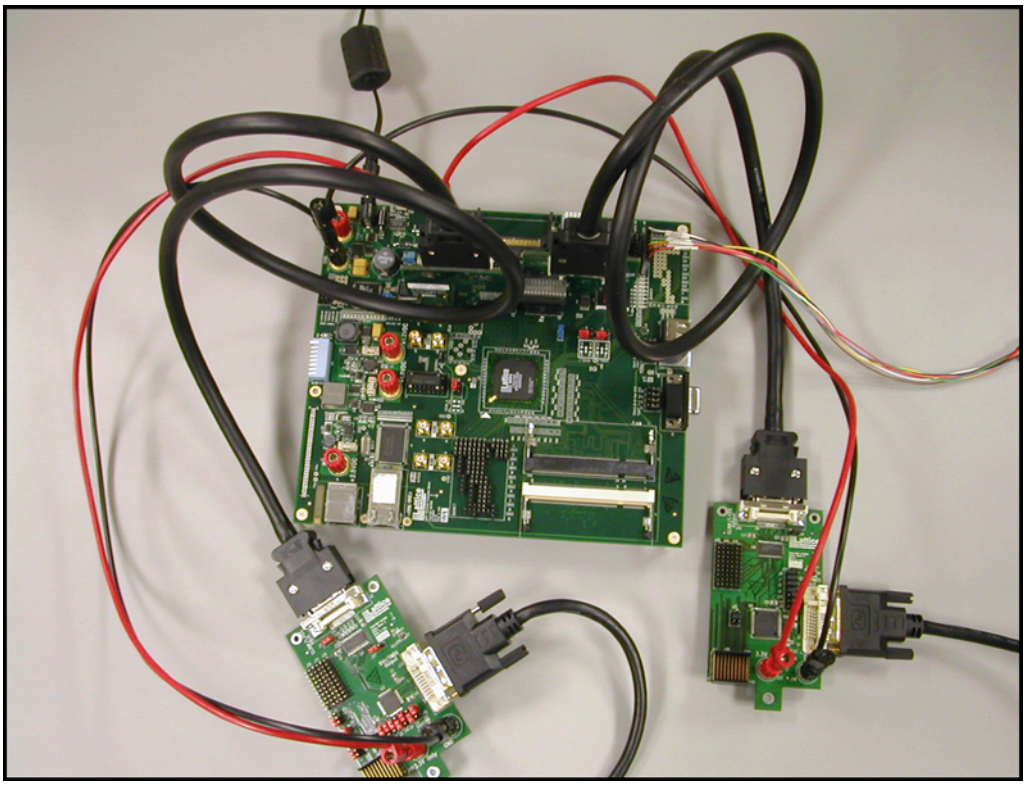
  Before you connect the two DVI cables to the Video Demo boards #2 and #3, set the screen resolution to any of those listed in the "Prepare for the Video Demo" section earlier in this document and check if your LCD display can display the image properly at this resolution. Note that the DVI interface includes pins to allow the video source getting the EDID (Extended Display Identification Data) from the video sink. These pins are not implemented on Video Demo boards #2 and #3. Some video source will not send out the video stream if it is not getting a proper EDID from the video sink. To prevent this from happening, you should first set the screen resolution and check if the video stream is transmitting properly to the LCD display before disconnecting the DVI cable, then reconnecting the cable to the demo system.

  The DVI port of your PC should be connected to the Video Demo board #3. Video Demo board #2 should be connected to the LCD display.

- **Step 4: Connect the JTAG Download Cable**
  The JTAG download cable is used for downloading the demo bitstream from a PC to the LatticeECP2 FPGA device. Connect it to the J46 on the LatticeECP2 Advanced Evaluation Board. The functions of the pins of J46 are shown on the board. Be sure the cable wires are connected to the right J46 pins. You should also make sure there is a jumper installed on J34 and no jumper installed on J55, so that the LatticeECP2-50 is the only device in the JTAG chain. For further information, see the *LatticeECP2 Advanced Evaluation Board User Manual*, available from the Lattice website at www.latticesemi.com/boards.

- **Step 5: Connect the Power Cables**
  Video Demo boards #2 and #3 require 3.3V power which can be obtained from the LatticeECP2 Advanced Evaluation Board using the red and black banana plug cables.

Figure 8. Power Cable Connections for Lattice 7:1 LVDS Video Demo Kit



After connecting the banana plug cables, you should connect the 5V wall-mount power adapter to the LatticeECP2 Advanced Evaluation Board. After completion of this step, the video demo system should look like Figure 8.

- **Step 6: Download the Video Demo Bitstream and Run the Video Demo**
  The DIP switch SW5 on the LatticeECP2 Advanced Evaluation Board controls several functions of this demo design. The functions of these controls and their default settings are listed in the flowing table. When the specific controls are selected, the push-button SW4 needs to be toggled to activate the adjustment. Note that once the Auto-Demo is enabled, the OSD will be moving its position and bounce back when it hits the edge of the display. This is for demonstration purpose and cannot be turned off.

Table 3. Switch for Video Color Adjustments, Demo and OSD Controls

SW5 Pin Number	ON (Pushed Down)	OFF (Pulled Up)
Pin-1	R-gain or Contrast deselected	R-gain or Contrast selected
Pin-2	G-gain or Brightness deselected	G-gain or Brightness selected
Pin-3	B-gain or Hue deselected	B-gain or Hue selected
Pin-4	Opacity or Saturation deselected	Opacity or Saturation selected
Pin-5	OSD enabled	OSD disabled
Pin-6	Auto-Demo enabled	Auto-Demo disabled
Pin-7	Select RGBO group	Select CBHS group
Pin-8	Decrease the selected controls when SW4 is toggled	Increase the selected controls when SW4 is toggled

Now you can apply power to the demo system by turning on the SW6 of the LatticeECP2 Advanced Evaluation Board. Then, launch ispVM® to download the demo bitstream. For full details on how to download the bitstream to the LatticeECP2 FPGA, please refer to the *LatticeECP2 Advanced Evaluation Board User Guide.*

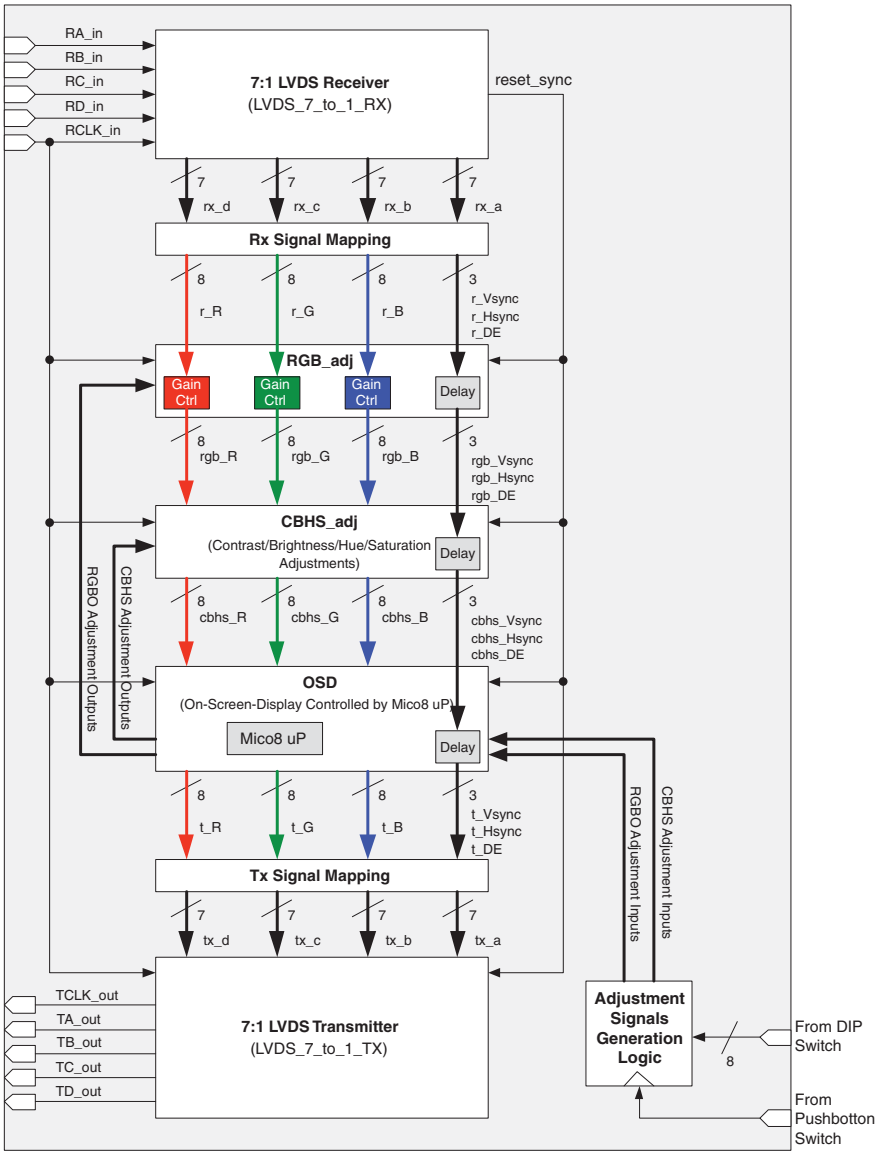
The bitstream file for this demo, as well as other resources, can be downloaded from the Lattice web site at: www.latticesemi.com/boards. Navigate to the page for the Lattice 7:1 Video Demo Kit, and see the "documents and downloads" link at the left of the page.

Video Demo Design Modules

This video demo design uses the Rx and Tx modules of Lattice reference design RD1030, *LatticeECP2/M 7:1 LVDS Video Interface*. For more information on this reference design, see the Lattice web site. Search for "RD1030", or navigate to the web page for the Lattice 7:1 LVDS Video Demo Kit at www.latticesemi.com/boards.

Figure 9 is a representation of the top level VHDL file of this design. The gray color blocks shown below are implemented in other VHDL files. The light green color blocks are modules generated using the IPexpress tool included with the Lattice ispLEVER design software.

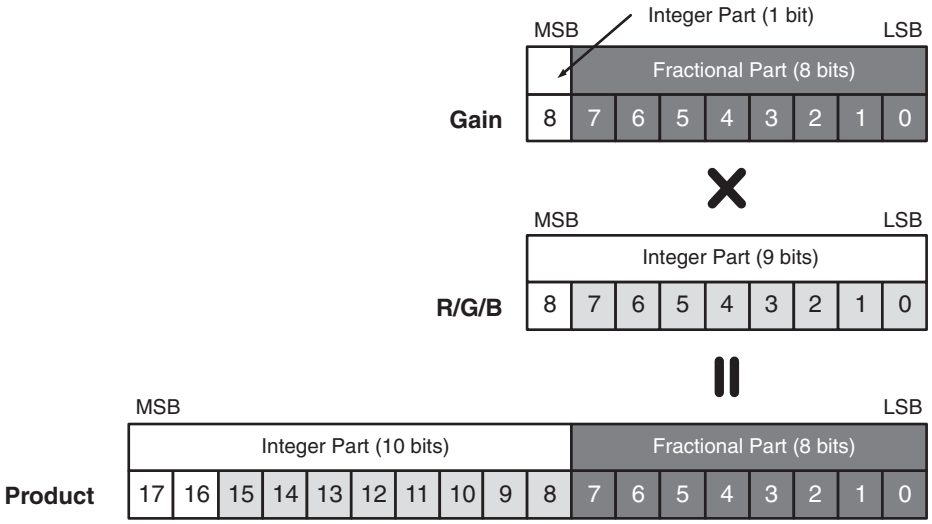
Figure 9. Video Processing Design Example



In addition to the Rx and Tx modules, this design also contains the modules for the RGB gain control, the Contrast/Brightness/Hue/Saturation controls, the OSD module and the LatticeMico8 microprocessor that automatically demonstrates the adjustments. These modules are an example design. You may implement other video applications in the LatticeECP2-50 FPGA using the video demo kit.

The Gain Control modules are 9x9 (9-bit by 9-bit) multipliers implemented using the sysDSP™ blocks of the LatticeECP2 FPGA. The 9-bit gain value defines a positive real number between 0 and 1.99609375 with 1 bit of integer part and 8 bits of fractional part as shown in Figure 10.

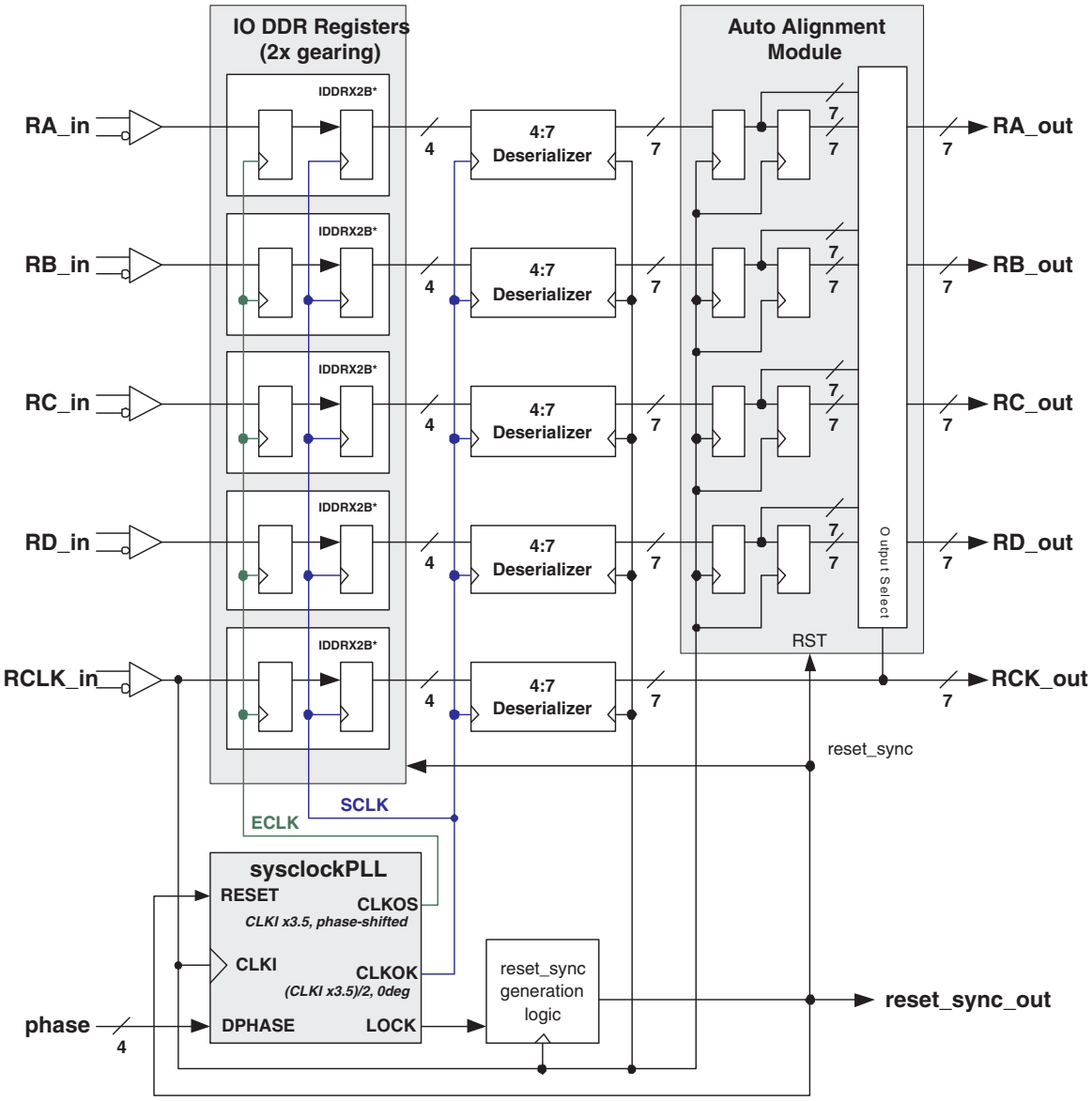
Figure 10. 18-Bit Data Value



The R, G, B in this design are colors with 8-bit color depth. Each color is represented by 8 binary bits. Before feeding them to the multiplier's multiplicand port, they are expanded from 8 bits to 9 bits with the most significant bit set to "0". The R, G, B gains are real numbers between 0 and 1 and are feeding to the multiplier port. After reset, these gains are set to their default values 1.0. The real number 1.0 is represented by the 9-bit binary "100000000". The maximum value of the gains are limited to 1.0. The product of the 9x9 multiplier is an 18-bit value with 10 integer part bits and 8 fractional part bits. However, only 8 integer part bits (bit-15 down to bit-8) are passed to the OSD module.

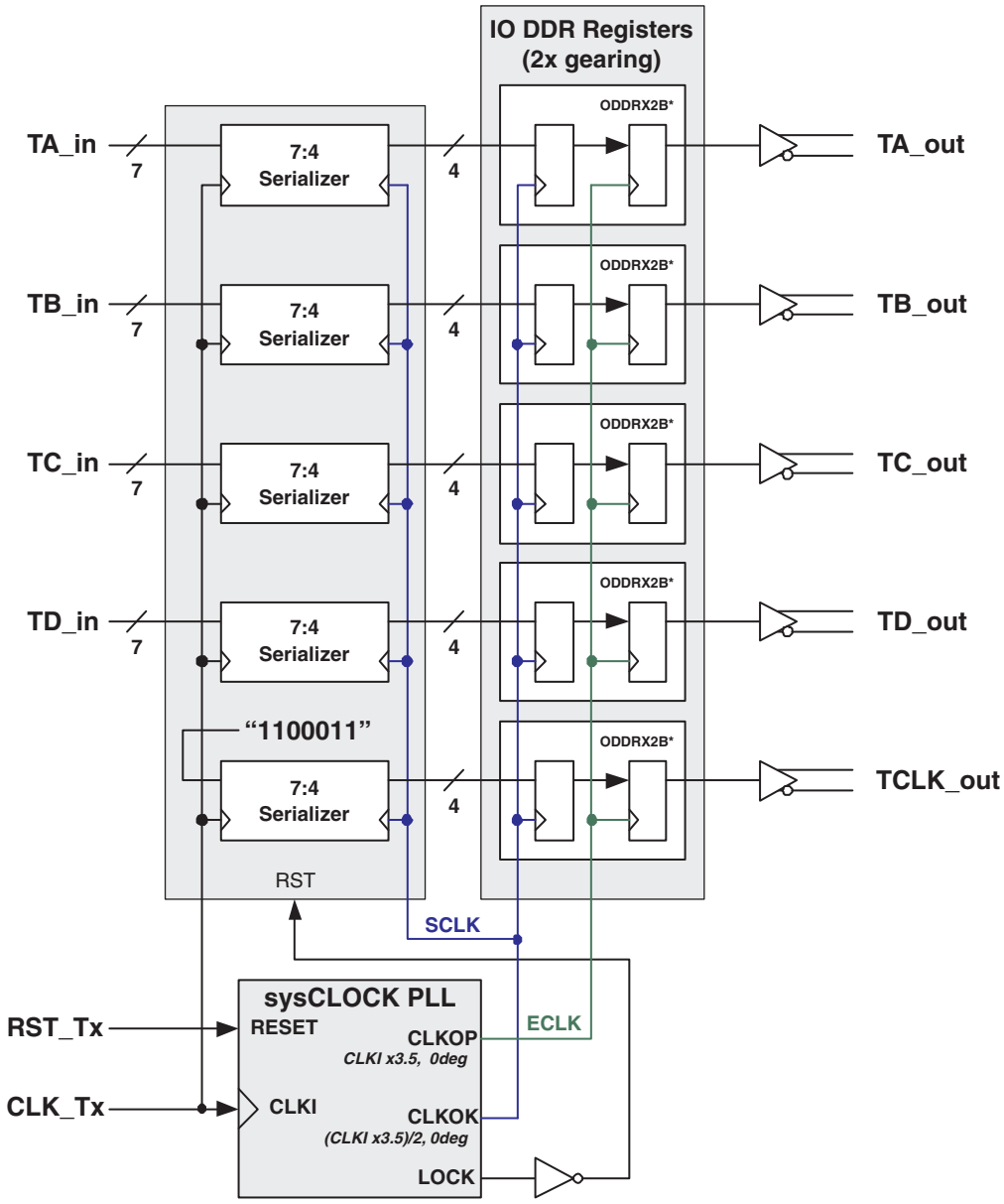
Figure 11 shows the block diagram of the 7:1 LVDS receiver module. This is the same receiver module as in the Lattice reference design RD1030, *LatticeECP2/M 7:1 LVDS Video Interface*. There is an auto-alignment logic in the receiver module that utilizes the deserialized data of RCLK_in to select the proper outputs of the four data pairs. This ensures the four data outputs are aligned at the pixel boundary. This logic will be reset whenever the PLL lock is lost. The DDR software primitives IDDRX2B with x2 gearing ratio are used for receiving the high speed 7:1 LVDS video stream. The 4-bit output of the IDDRX2B modules will then be sent to the 4-to-7 deserializers. Refer to reference design RD1030 for more detailed information. This can be found on the Lattice web site at: www.latticesemi.com by searching for "RD1030".

Figure 11. 7:1 Receiver Side Block Diagram



The block diagram of the 7:1 LVDS transmitter is shown in Figure 12. Four 7-to-4 serializers are used for serializing the parallel R, G, B, VSYNC, HSYNC and DE signals. There is another serializer used for generating the LVDS output clock. The "1100011" value is feeding to this serializer so that the generated LVDS clock has a clock/data relationship that complies to the Channel Link 7:1 LVDS specification. The 4-bit outputs of the serializers are sent to the 2x gearing ODDRX2B modules for pumping out of the LVDS I/Os. For more information about the transmitter, please refer to Lattice reference design RD1030, *LatticeECP2/M 7:1 LVDS Video Interface*.

Figure 12. Block Diagram of 7:1 LVDS Transmitter Module



Troubleshooting

Camera Link video camera is not supported.

Please note this kit uses the Channel-Link MDR-26 standard, not Camera-Link. These two LVDS video standards use the same MDR-26 connector, but have different pinouts and data packet standards, and are not compatible.

Please use a standard DVI source such as a laptop or desktop computer or a Channel Link source to the LVDS.

No video output when everything is connected.

There are a number of possible causes, some of the most common include:

1. Boards #1 and #4 are not installed properly. After these boards are installed on the LatticeECP2 Advanced Evaluation Board, the metal pieces of the VHDM connectors of Boards #1 and #4 should be touching each other.

2. If using a computer for the DVI source, it may need to identify the monitor for initialization. Refer to the Boards and Cable Connections section of this document, Step #3.

3. Check switches and jumpers:
   Make sure that DIP switch SW1, switches 1 and 2 on the LatticeECP2 Advanced Evaluation Board, are in the up position to correctly set the power supply options.

   There are a number of other jumper and switch settings which may affect the operation of the demo. Be sure to check the jumpers and switches on all the video demo boards, as well as the LatticeECP2 Advanced Evaluation Board.

4. The red LEDs on Boards #2 and #3 are not turned on. These LEDs indicate the 3.3V powers on these boards are properly supplied. All of the different power supplies on the LatticeECP2 Advanced Evaluation Board are controlled by the Lattice Power Manager II POWR1220AT8. If SW1 Pin 1 is on (pushed down), the POWR1220AT8 device will be reset and all powers including the 3.3V will be disabled.

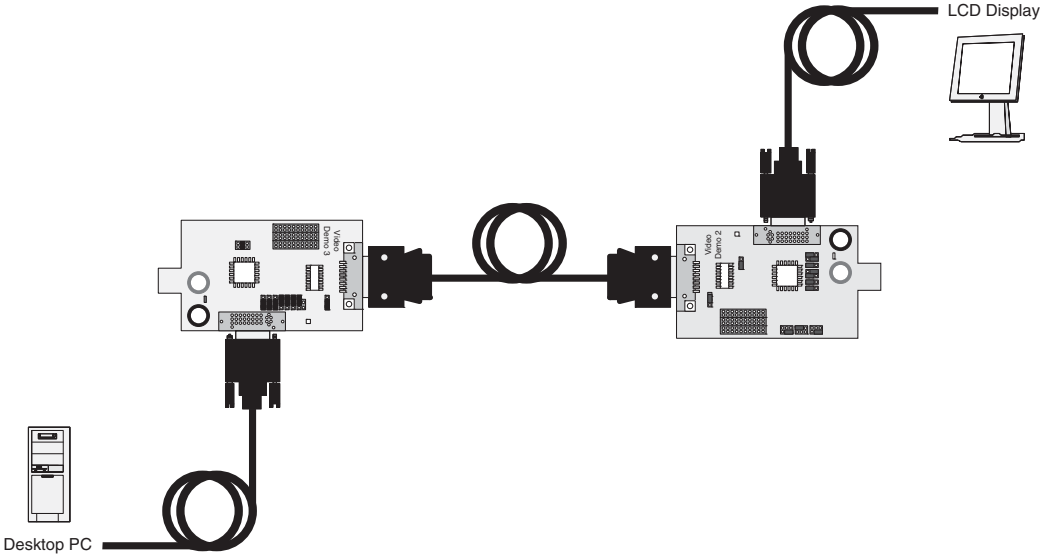
5. The monitor being used is a VGA monitor with a DVI -> VGA adapter. The monitor must be a DVI, digital monitor. There is no analog component output from the Video Demo. See the Preparing for the Video Demo section of this document for more information.

6. Make sure your monitor source is set to the supported resolutions and refresh rates listed in the "Prepare for the Video Demo" section earlier in this document.

Testing for Board #2 and Board #3.

If you suspect that something may be wrong with Board #2 or #3, you may wish to test them independently as part of the troubleshooting. To do this, disconnect Board #2 from the LatticeECP2 Advanced Evaluation Board and connect its LVDS cable directly into the input of Board #3. This removes the FPGA from the circuit. The video path then goes though the DVI - LVDS - DVI conversion and should be displayed. If it is not, refer to the Boards and Cable Connections section of this document, step #3. Figure 13 shows this arrangement.

Figure 13. Setup to Test Boards #2 and #3



Note: Power connections are not shown in Figure 13, but power must be applied.

Ordering Information

Description	Ordering Part Number	China RoHS Environment-Friendly Use Period (EFUP)
LatticeECP2 7:1 Video Development Kit (Includes LatticeECP2 Advanced Evaluation Board)	LFE2-50E-VID-EV	
Lattice 7:1 Video Interface Kit	HW-VID-KIT	

Technical Support Assistance

Hotline: 1-800-LATTICE (North America)
+1-503-268-8001 (Outside North America)
e-mail: techsupport@latticesemi.com
Internet:www.latticesemi.com

Revision History

Date	Version	Change Summary
December 2006	01.0	Initial release.
March 2007	01.1	Added Ordering Information section.
June 2007	01.2	Updated to match RD1030 version 01.2.

Appendix A. Jumpers of the Video Demo Board #2

Table 4. Functions of the Jumpers on Video Demo Board #2

Jumper	Function	Description	Default Setting
J3	/POWERDOWN	This is an active low control for forcing the DS90CR288A into the powerdown mode. The DS90CR288A outputs stay low under the powerdown mode.	Pin1 and Pin2 (high)
J4	CTL3	Multifunctional CTL3 input of TFP410.	Pin1 and Pin3
J5	CTL2	Multifunctional CTL2 input of TFP410.	Pin4 and Pin6
J6	CTL1	Multifunctional CTL1 input of TFP410.	Pin1 and Pin3
J7	VREF	This is the input reference voltage used to select the swing range of the TFP410 digital inputs. High-swing 3.3V input signal level is selected by the default setting.	Pin1 and Pin2 (high)
J8	EDGE	Edge select or hot plug input of TFP410.	Pin1 and Pin2 (high)
J9	DKEN	Data de-skew enable control of TFP410.	Pin1 and Pin2 (high)
J10	ISEL/RSTn	This is an active high I^2C select signal of TFP410 used for enabling the TFP410's I^2C interface. The I^2C state machine can be reset by bringing this signal low then back high. I^2C is disable by the default setting.	Pin2 and Pin3 (low)
J11	BSEL/SCL	Input bus select or I^2C clock input of TP410.	Pin1 and Pin2 (high)
J12	DSEL/SDA	DSEL or I^2C bidirectional data line of TP410.	Pin2 and Pin3 (low)
J13	PDN	This is an active low power down control of TP410. During power-down mode, only the digital I/O buffers and I^2C interface remain active.	Pin1 and Pin2 (high)
J21	NS_VDD	The power of the DS90CR288A is supported through this jumper's default setting. This jumper is used for disconnecting the DS90CR288A power and forcing its output to the high impedance state. Note that the powerdown mode puts the DS90CR288A outputs into low state instead of high impedance state.	Pin1 and Pin2

Appendix B. Jumpers of the Video Demo Board #3

Table 5. Functions of the Jumpers on Video Demo Board #3

Jumper	Function	Description	Default Setting
J3	TxIN7	This jumper selects which multifunctional pins of the TFP401A (CTL3, CTL2, or CTL1) is connected to the DS90CR287's TxIN7 input. CTL2 is selected by default.	Pin3 and Pin4
J4	/POWERDOWN	This is an active low control for forcing the DS90CR287 into the powerdown mode. The DS90CR287's LVDS outputs stay in the tri-state mode under powerdown mode.	Pin1 and Pin2 (high)
J5	OCK_INV	TFP401A's ODCK Polarity - Selects ODCK edge on which pixel data (QE[23:0] and QO[23:0]) and control signals (HSYNC, VSYNC, DE, CTL1-3) are latched.	Pin1 and Pin2 (high)
J6	DFO	TFP401A's Output clock data format - Controls the output clock (ODCK) format for either TFT or DSTN panel support.	Pin2 and Pin3 (low)
J7	PIXS	TFP401A's Pixel select - Selects between one or two pixels per clock output modes.	Pin2 and Pin3 (low)
J8	STAGN	Staggered pixel select of TFP401A.	Pin2 and Pin3 (low)
J9	ST	Output strength select of TFP401A. The default setting set the drive strength to low drive strength.	Pin2 and Pin3 (low)
J10	PDN	This is an active low power down control of TP401A. During powerdown mode, all output buffers are in the high impedance state.	Pin1 and Pin2 (high)
J11	PDON	This is an active low output drive power down control of TP401A. During output drive powerdown mode, all output drivers except SCDT and CTL1 are driven to a high impedance state.	Pin1 and Pin2 (high)

Appendix C. Schematics of the Video Demo Boards #1, #2, #3 and #4

Video Demo Board #1

Figure 14. Video Demo Board #1 Schematic

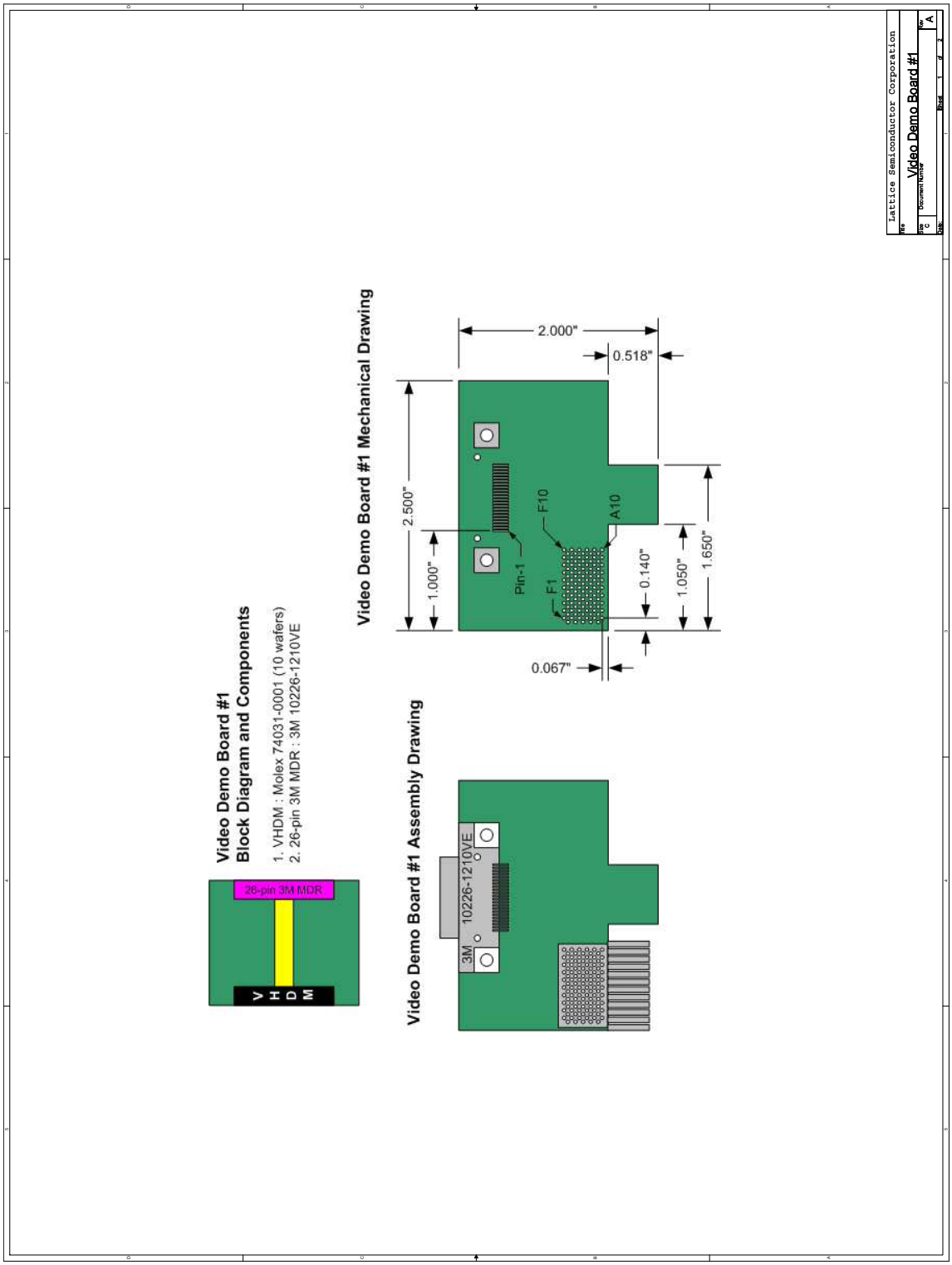
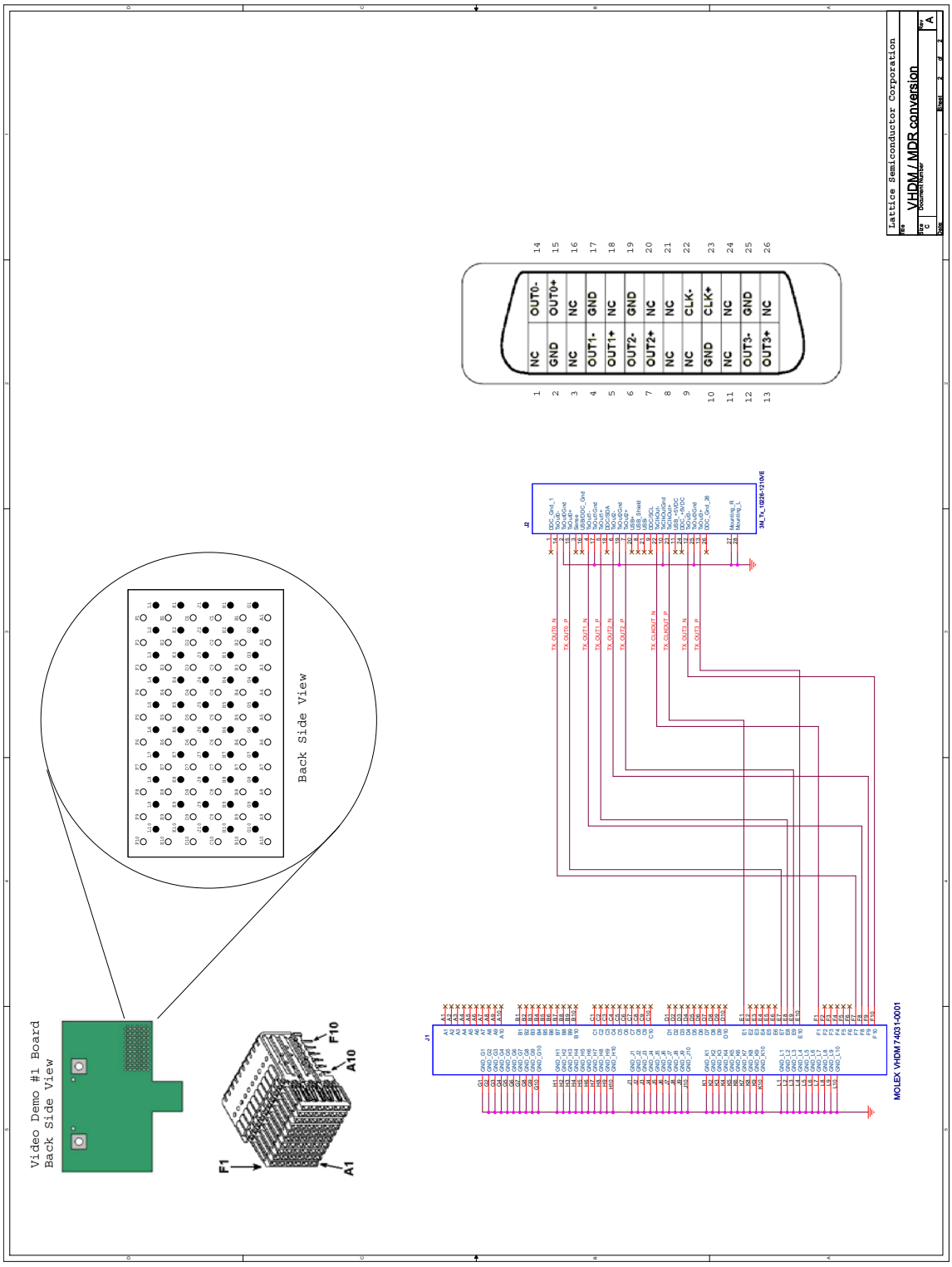


Figure 12. Video Demo Board #1 Schematic (Cont).



Video Demo Board #2

Figure 15. Video Demo Board #2 Schematic

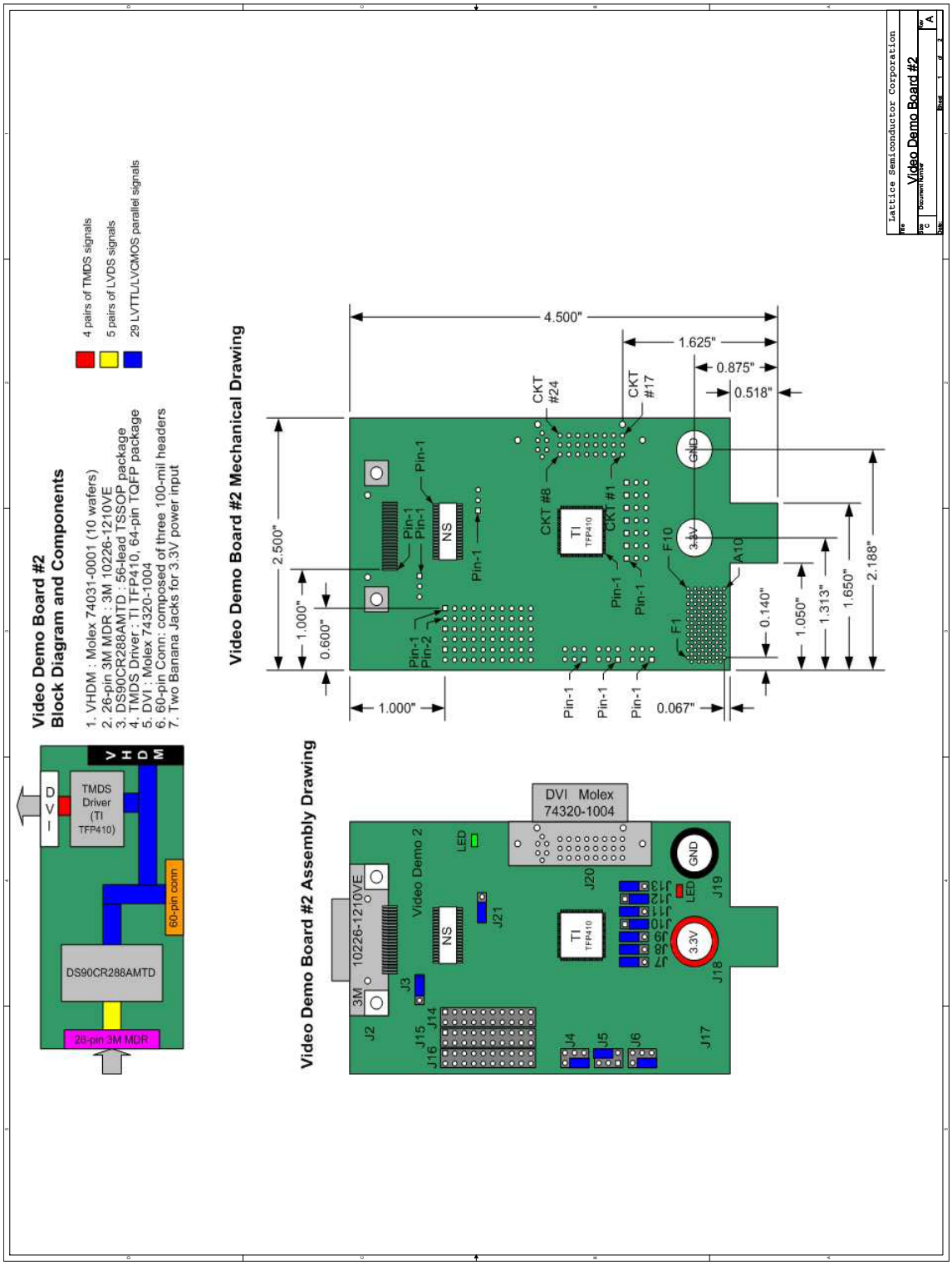
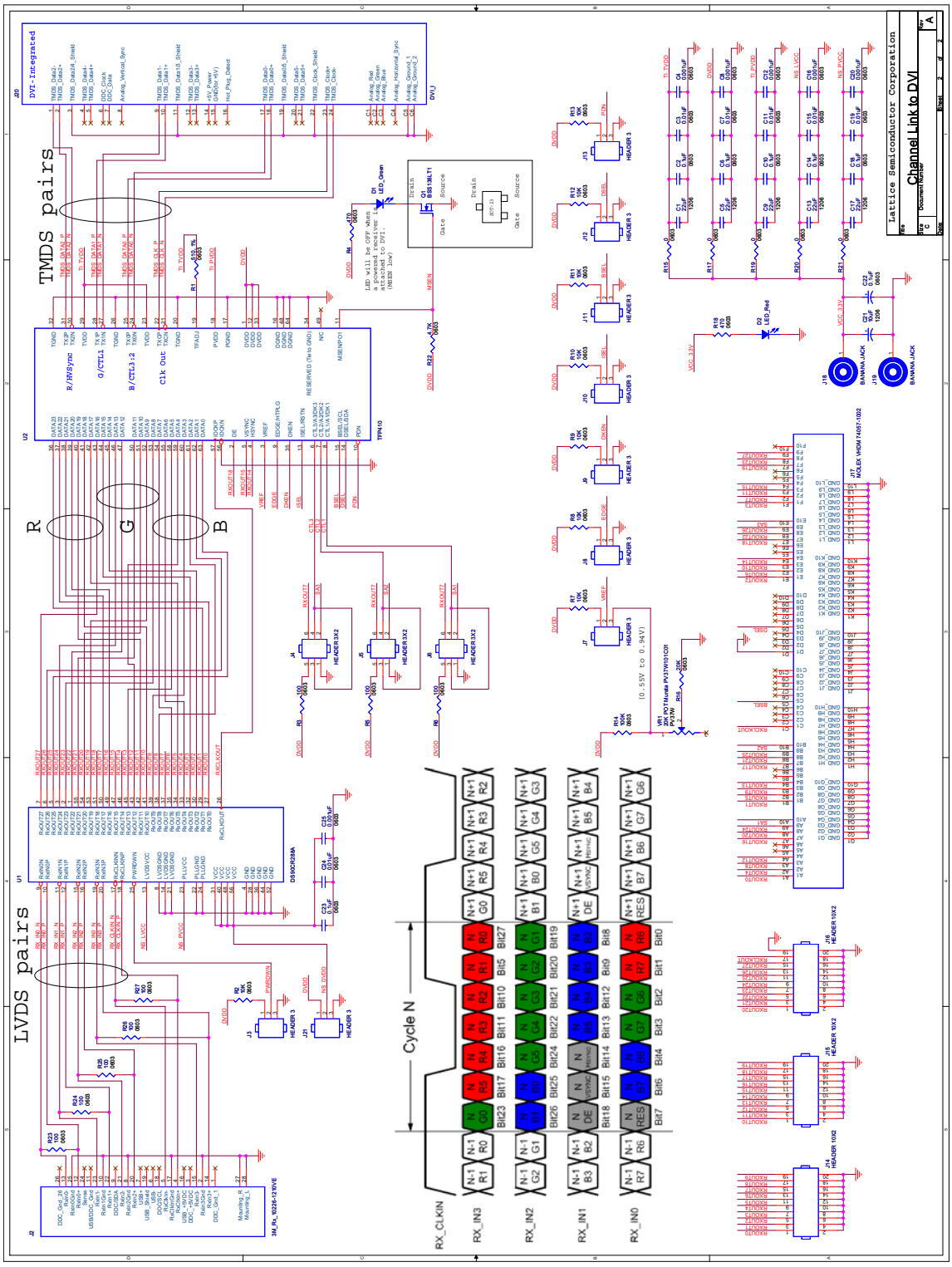


Figure 13. Video Demo Board #2 Schematic (Cont.)



Video Demo Board #3

Figure 16. Video Demo Board #3 Schematic

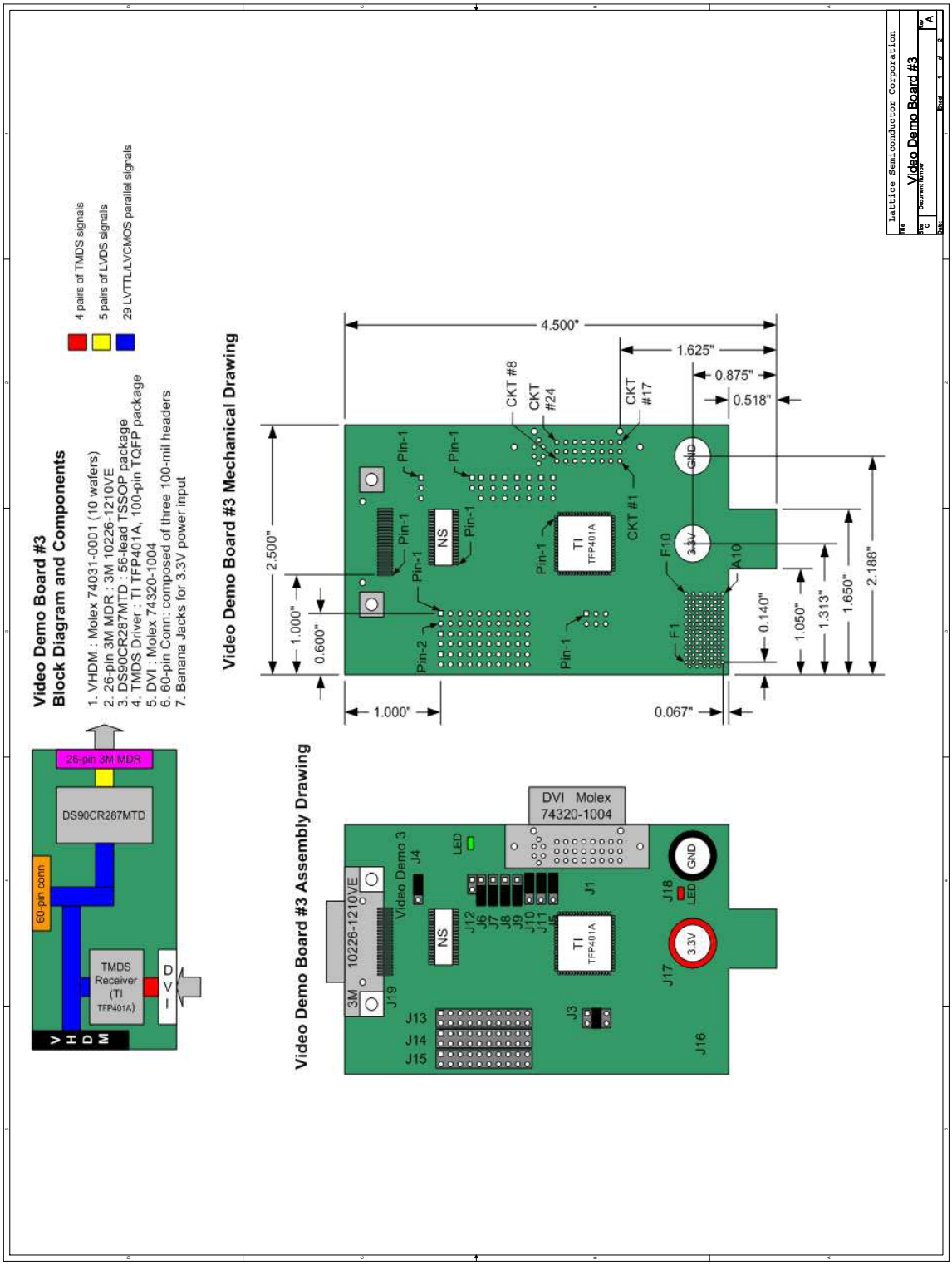
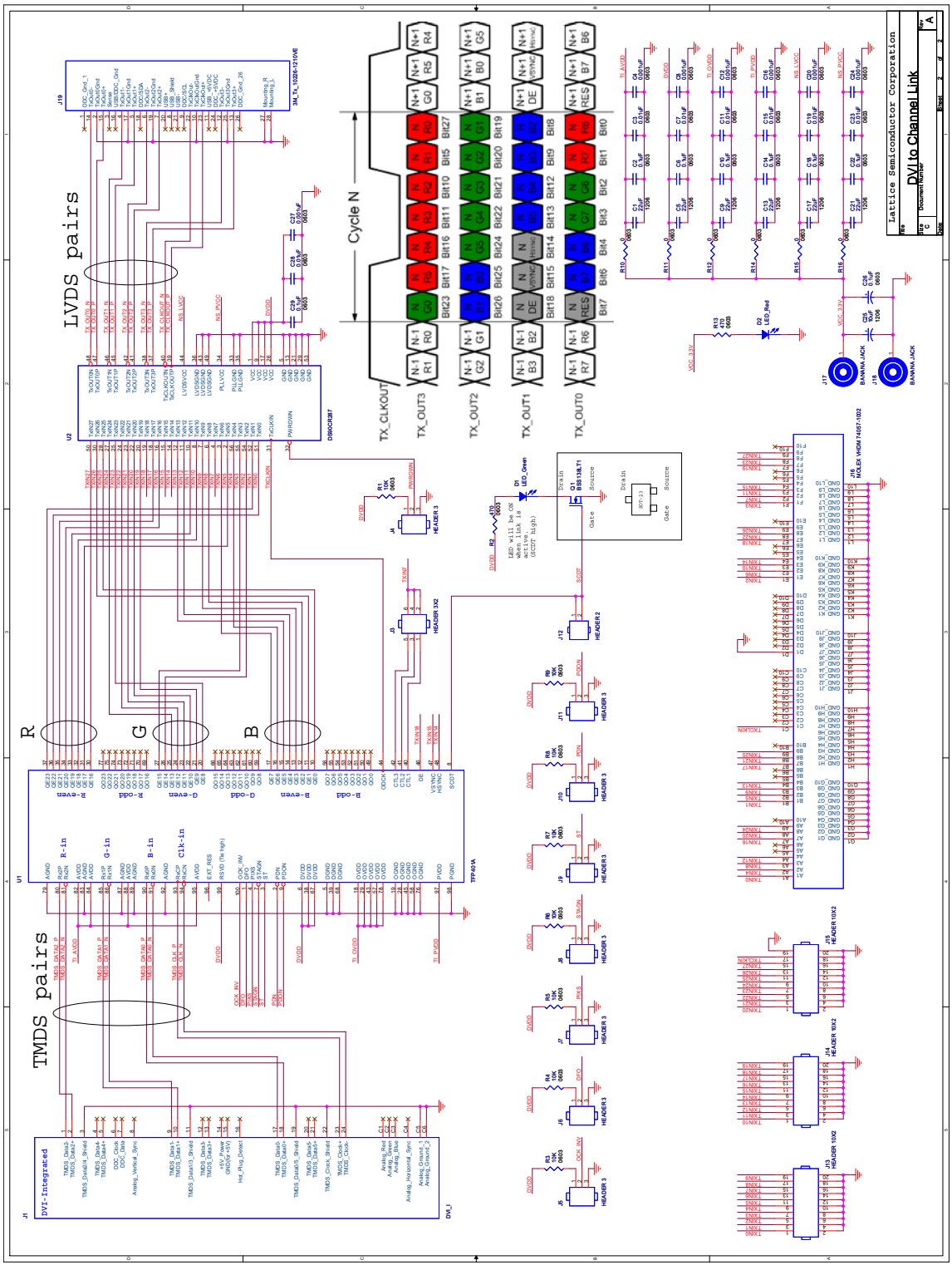


Figure 14. Video Demo Board #3 Schematic (Cont.)



Video Demo Board #4

Figure 17. Video Demo Board #4 Schematic

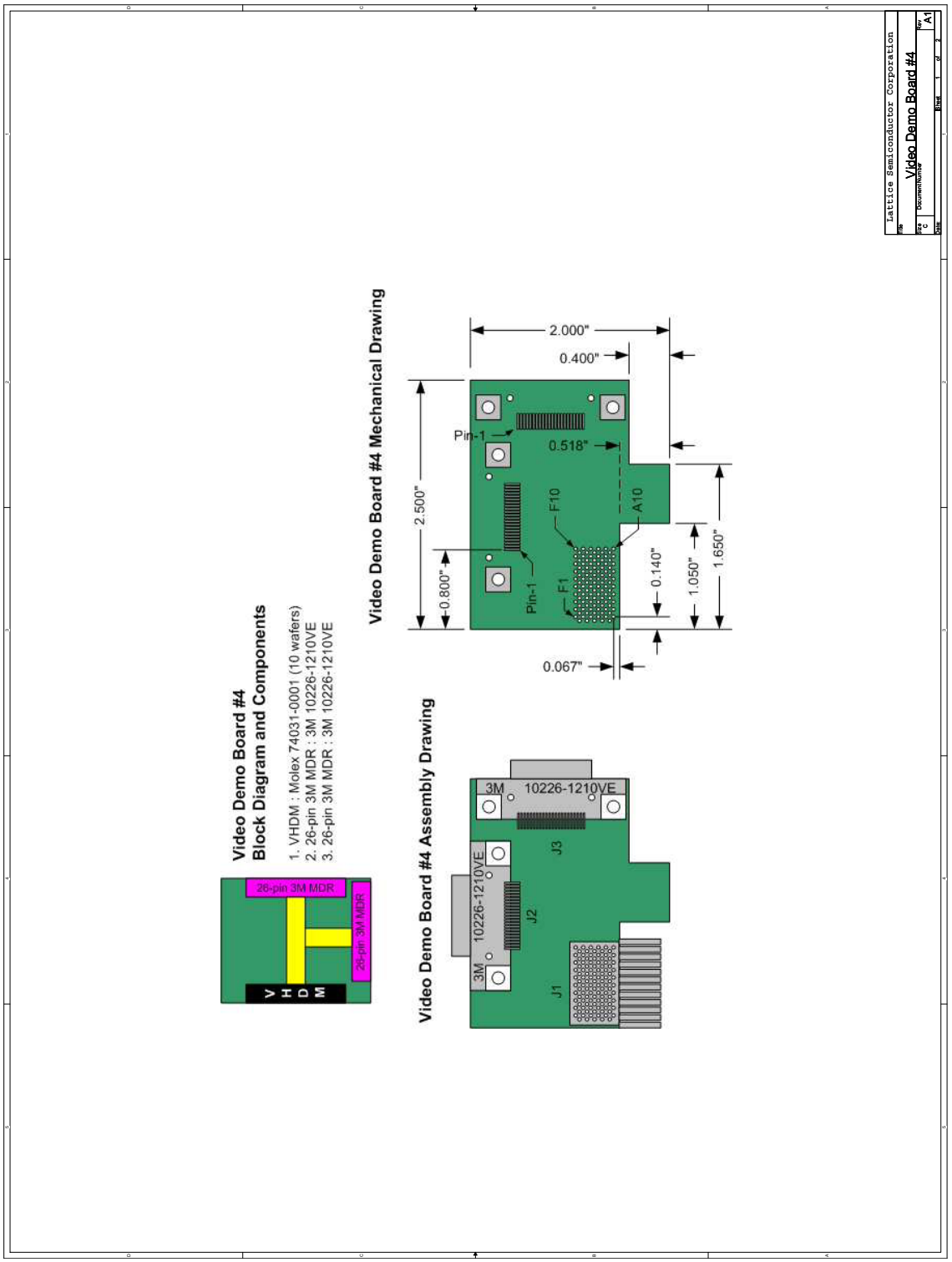
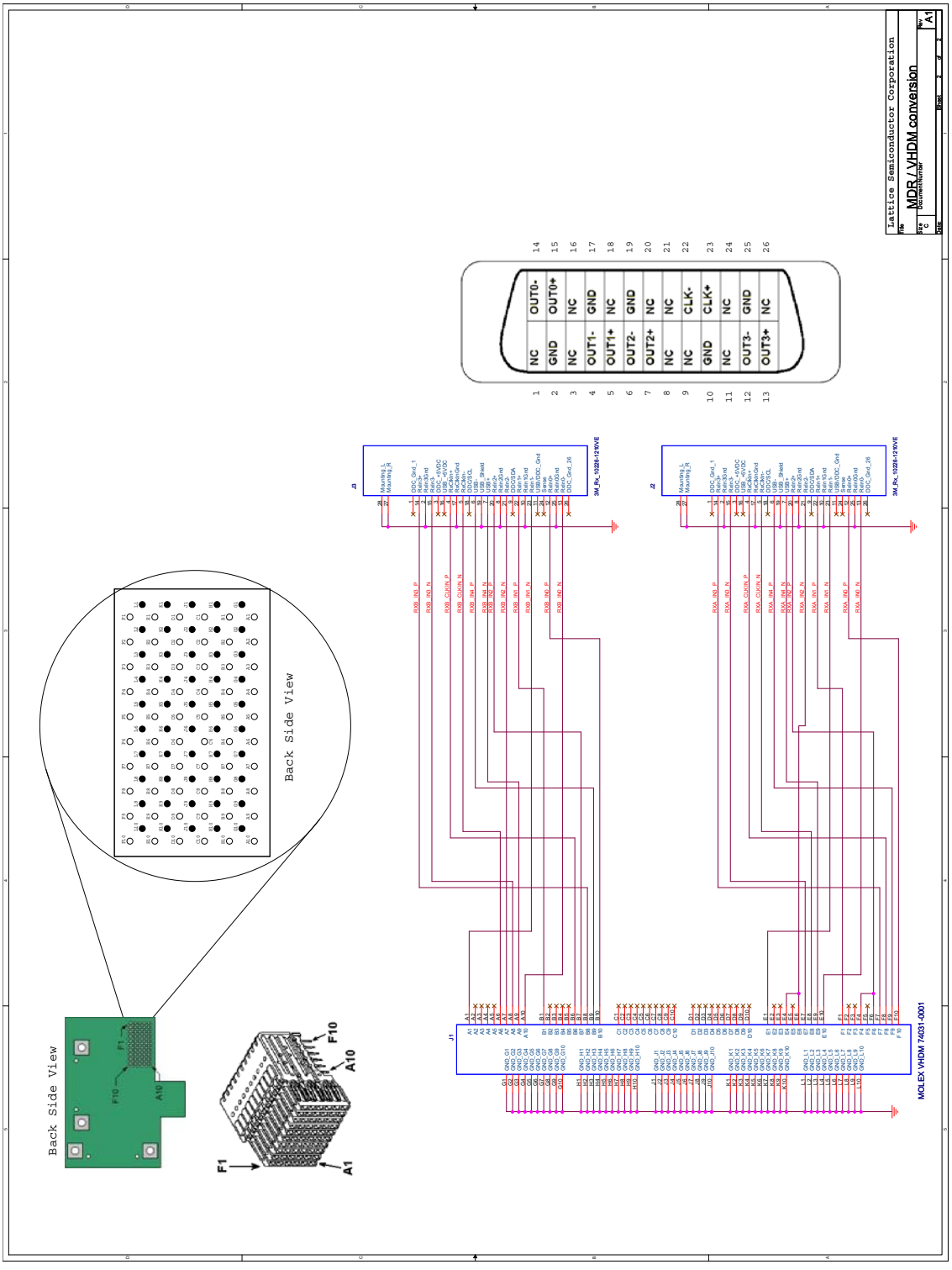


Figure 15. Video Demo Board #4 Schematic (Cont.)



Modified Video Demo Board #1 Schematic

Rework instructions for Video Demo Board #1 so that it can be used on the Rx side. (Note that the reworked Video Demo Board #1 is not equivalent to Video Demo Board #4. Please modify the .lpf preference file of reference design RD1030, *LatticeECP2/M 7:1 LVDS Video Interface*, to match the board that you are using on the Rx side. The Tx side can use either the reworked Board #1, non-reworked Board #1 or Board #4).

1. Solder a short wire from J2 pin 6 to J2 pin 20.

2. Use another short wire with the same length to connect J2 pin 7 to J2 pin 21.

OCEAN CHIPS
Океан Электроники
Поставка электронных компонентов

Компания «Океан Электроники» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

Наши преимущества:

- Поставка оригинальных импортных электронных компонентов напрямую с производств Америки, Европы и Азии, а так же с крупнейших складов мира;
- Широкая линейка поставок активных и пассивных импортных электронных компонентов (более 30 млн. наименований);
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Помощь Конструкторского Отдела и консультации квалифицированных инженеров;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Поставка электронных компонентов под контролем ВП;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- При необходимости вся продукция военного и аэрокосмического назначения проходит испытания и сертификацию в лаборатории (по согласованию с заказчиком);
- Поставка специализированных компонентов военного и аэрокосмического уровня качества (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Actel, Aeroflex, Peregrine, VPT, Syfer, Eurofarad, Texas Instruments, MS Kennedy, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits, General Dynamics и др.);

Компания «Океан Электроники» является официальным дистрибьютором и эксклюзивным представителем в России одного из крупнейших производителей разъемов военного и аэрокосмического назначения «**JONHON**», а так же официальным дистрибьютором и эксклюзивным представителем в России производителя высокотехнологичных и надежных решений для передачи СВЧ сигналов «**FORSTAR**».

AVIC JONHON

«JONHON» (основан в 1970 г.)

Разъемы специального, военного и аэрокосмического назначения:

(Применяются в военной, авиационной, аэрокосмической, морской, железнодорожной, горно- и нефтедобывающей отраслях промышленности)

«FORSTAR» (основан в 1998 г.)

ВЧ соединители, коаксиальные кабели, кабельные сборки и микроволновые компоненты:

(Применяются в телекоммуникациях гражданского и специального назначения, в средствах связи, РЛС, а так же военной, авиационной и аэрокосмической отраслях промышленности).

FORSTAR®

Телефон: 8 (812) 309-75-97 (многоканальный)
Факс: 8 (812) 320-03-32
Электронная почта: ocean@oceanchips.ru
Web: http://oceanchips.ru/
Адрес: 198099, г. Санкт-Петербург, ул. Калинина, д. 2, корп. 4, лит. А