

General Description

The MAX4999 differential Hi-Speed USB analog multiplexer features low on-capacitance (C_{ON}) switching, making it an ideal solution for the USB server/mass storage market. The MAX4999 is designed for USB 2.0 low-/full-/Hi-Speed applications with capability of supporting data rates up to 480Mbps.

The MAX4999 is a differential 8:1 multiplexer. The MAX4999 features three digital inputs to control the signal path. Typical applications include switching a USB connector between eight USB hosts and a USB device.

An enable input (EN) is provided to disable all channels and place the device into a high-impedance state (standby mode), shutting off the charge pump for minimum power consumption.

The MAX4999 operates from a +3.0V to +3.6V power-supply voltage and is specified over the -40°C to +85°C extended temperature range. The MAX4999 is available in a 5mm x 5mm, 32-pin TQFN package.

Applications

- Keyboard, Video, Mouse (KVM)
- Servers/RAID
- Mass Storage
- Workstations

Benefits and Features

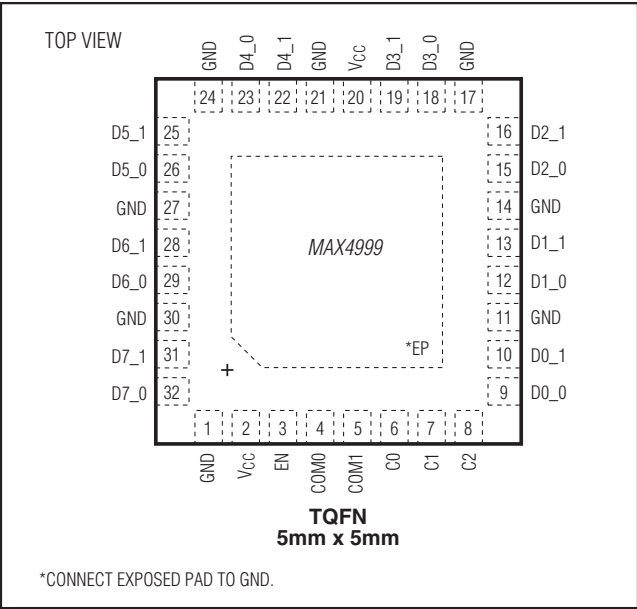
- Increased Flexibility and Performance
 - Multiplexer Supports USB 2.0 Standard
 - 3dB Bandwidth: 1200MHz (typ)
- Low On-Resistance and Power Management Features Minimize System Losses
 - 6.5Ω (typ) On-Resistance (R_{ON})
 - Single +3.0V to +3.6V Power-Supply Voltage
 - Enable Input Puts All Channels in High-Impedance State (Standby Mode)
 - Low Operating Current (1μA) and Ultra-Low Quiescent Current (30nA) in Standby Mode
- Reduce Component Count and Design Complexity
 - Low Threshold Eliminates the Need for Translators in 1.8V Low-Voltage Systems
- Saves Board Space
 - 32-Pin, 5mm x 5mm, TQFN Package

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX4999ETJ+	-40°C to +85°C	32 TQFN-EP*

+ Denotes a lead(Pb)-free/RoHS-compliant package.
*EP = Exposed pad.

Pin Configuration



Absolute Maximum Ratings

(All voltages referenced to GND.)

V_{CC} -0.3V to +4V
 All Other Pins (Note 1) -0.3V to +4V
 Continuous Current (COM_ to any switch) ±60mA
 Peak Current (COM_ to any switch) (pulsed at 1ms,
 10% duty cycle) ±120mA

Continuous Power Dissipation (T_A = +70°C)

32-Lead TQFN (derate 34.5mW/°C above +70°C) 2759mW
 Operating Temperature Range -40°C to +85°C
 Storage Temperature Range -65°C to +150°C
 Lead Temperature (soldering, 10s) +300°C
 Soldering Temperature (reflow) +260°C

Note 1: Signals exceeding GND are clamped by internal diodes. Limit forward-diode current to maximum current rating.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 2)

TQFN

Junction-to-Ambient Thermal Resistance (θ_{JA}) 29°C/W
 Junction-to-Case Thermal Resistance (θ_{JC}) 2.0°C/W

Note 2: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

Electrical Characteristics

(V_{CC} = +3.0V to +3.6V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V and T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY						
Supply Voltage	V _{CC}		3.0		3.6	V
Quiescent Supply Current	I _O	Charge pump on			5	μA
		Charge pump off			1	
ANALOG SWITCH						
On-Resistance	R _{ON}	I _{COM_} = ±10mA		6.5	12	Ω
On-Resistance Match	ΔR _{ONSC}	V _{COM_} = 1V, T _A = +25°C			0.8	Ω
On-Resistance Match Between Channels	ΔR _{ONBC}	V _{COM_} = 1V, T _A = +25°C			1	Ω
Leakage Current COM_, D_ _0, D_ _1	I _L	V _{CC} = +3.6V	-1		+1	μA
SWITCH AC PERFORMANCE (Note 4)						
Crosstalk	V _{DCT1}	Any switch to non-paired switch at 500MHz (Figure 3)		-30		dB
Off-Isolation	V _{OFF}	Any switch to non-paired switch at 240MHz (Figure 3)		-27		dB
Bandwidth -3dB	BW	R _L = 45Ω unbalanced (Figure 3)		1200		MHz
On-Capacitance	C _{ON}	f = 1MHz		6		pF
		Taken from S11 parameters at f = 240MHz		3.0		
Off-Capacitance	C _{OFF}	f = 1MHz, COM_		5		pF
		Taken from S11 parameters at f = 240MHz		3.0		
Propagation Delay	t _{PD}	R _L = R _S = 50Ω (Figure 2)		300		ps
Turn-On Time	t _{ON}	V _{D_ _0} or V _{D_ _1} = +1.5V, R _L = 300Ω, C _L = 35pF, V _{IH} = V _{CC} , V _{IL} = 0V (Figure 1)		10		μs

($V_{CC} = +3.0V$ to $+3.6V$, $T_A = -40^{\circ}C$ to $+85^{\circ}C$, unless otherwise noted. Typical values are at $V_{CC} = +3.3V$ and $T_A = +25^{\circ}C$.) (Note 3)

Note 3: All units are 100% production tested at $T_A = +85^{\circ}\text{C}$. Limits over the operating temperature range are guaranteed by design and not production tested.

Note 4: Guaranteed by design.

MAX499

V_{CC}

V_{IN}

D_0
OR D_1

COM_

V_{OUT}

R_L

C_L

C_

GND

LOGIC INPUT

LOGIC INPUT

V_{IH}

V_{IL}

50%

t_R < 5ns

t_F < 5ns

SWITCH OUTPUT

0V

V_{OUT}

0.9 x V_{OUT}

0.9 x V_{OUT}

t_{ON}

t_{OFF}

IN DEPENDS ON SWITCH CONFIGURATION;
INPUT POLARITY DETERMINED BY SENSE OF SWITCH.

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Electrical Characteristics Test Circuits/Timing Diagrams (continued)

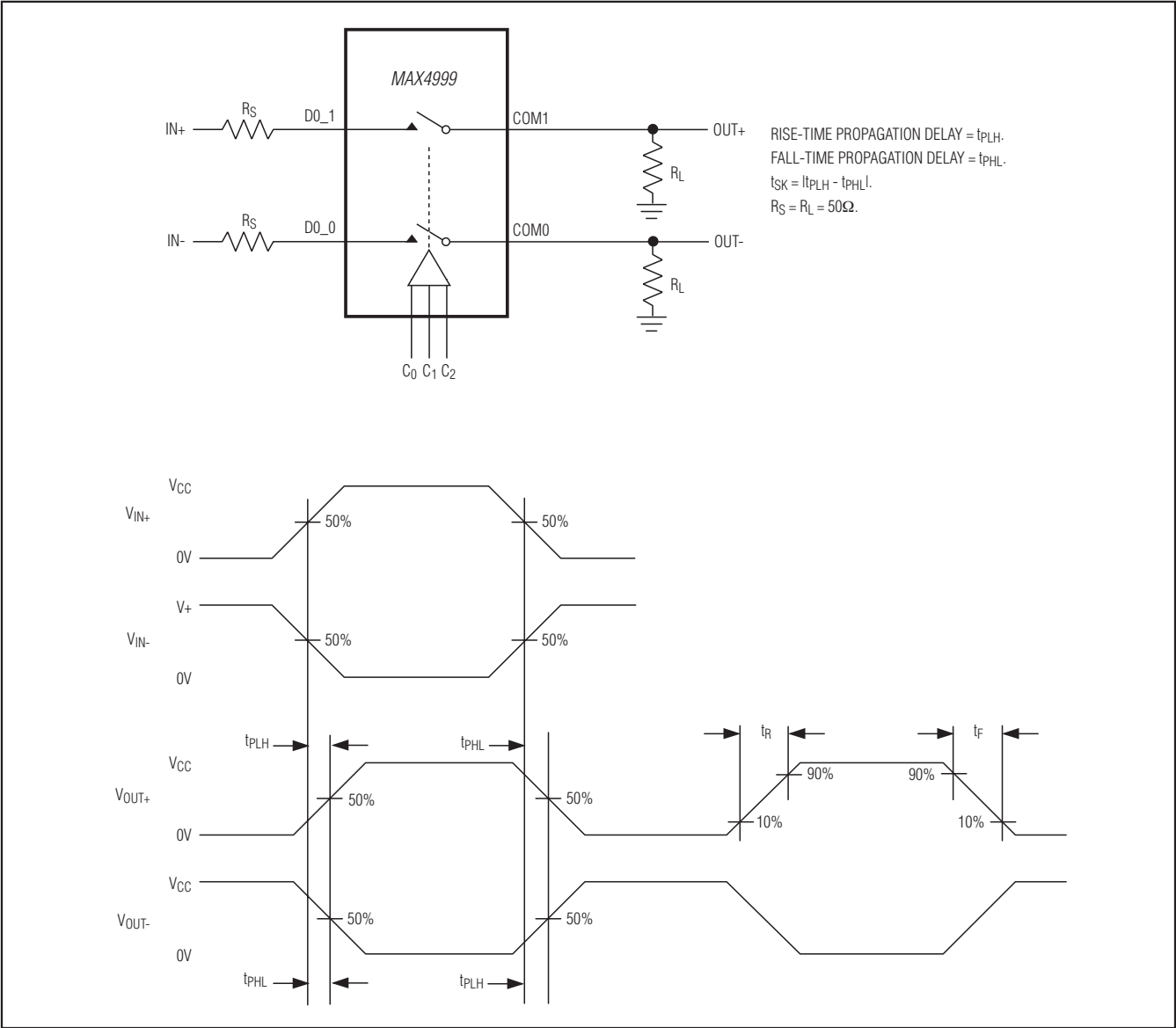


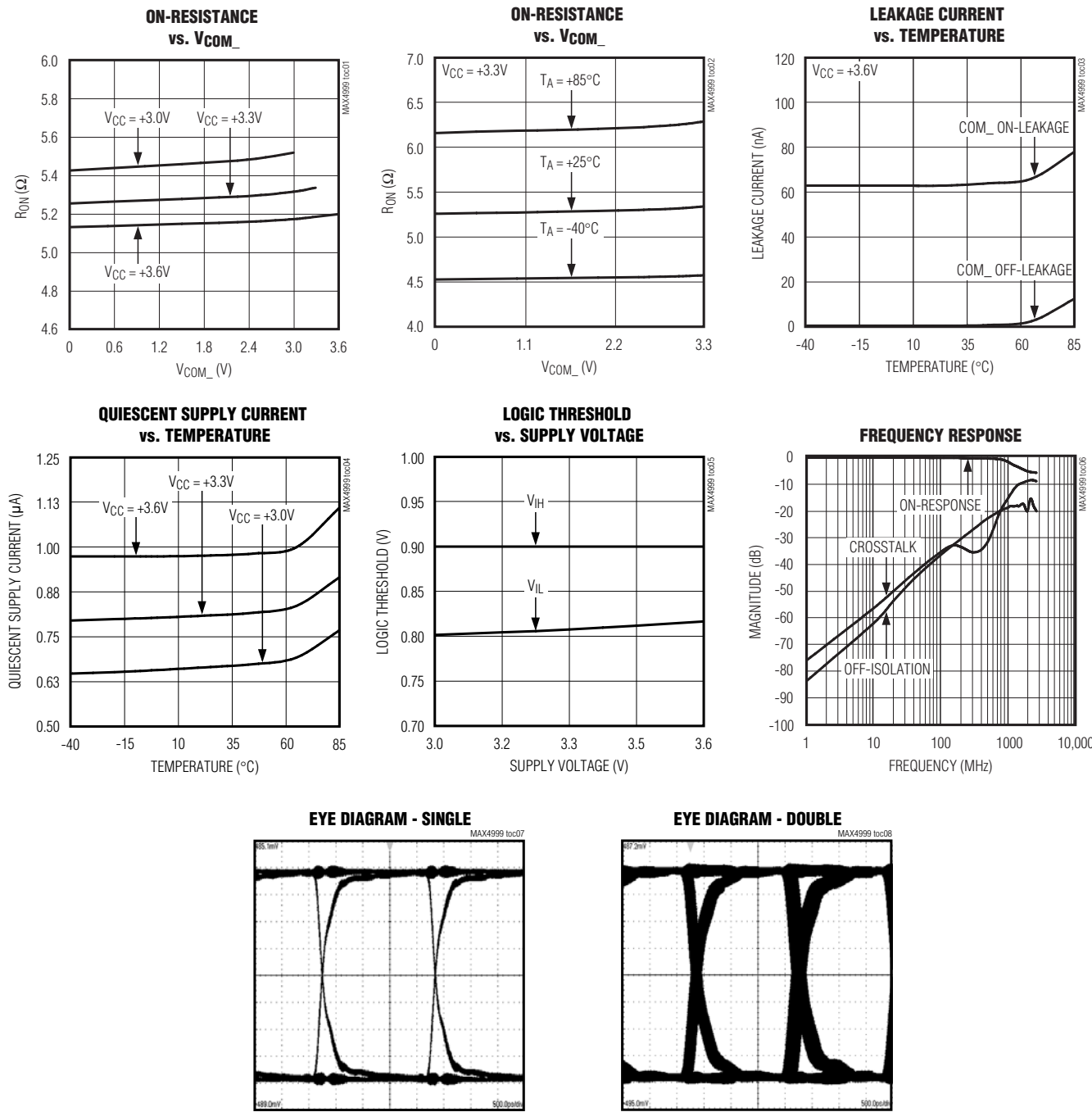
Figure 2. Propagation Delay and Skew

MEASUREMENTS ARE STANDARDIZED AGAINST SHORT AT SOCKET TERMINALS.
 OFF-ISOLATION IS MEASURED BETWEEN COM_ AND "OFF" USB_ TERMINAL ON EACH SWITCH.
 ON-LOSS IS MEASURED BETWEEN COM_ AND "ON" USB_ TERMINAL ON EACH SWITCH.
 CROSSTALK IS MEASURED FROM ONE USB_ CHANNEL TO ANOTHER USB_ CHANNEL.
 SIGNAL DIRECTION THROUGH SWITCH IS REVERSED; WORST VALUES ARE RECORDED.

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Typical Operating Characteristics

($V_{CC} = +3.3V$, $T_A = +25^{\circ}C$, unless otherwise noted.)



Pin Description

PIN	NAME	FUNCTION
1, 11, 14, 17, 21, 24, 27, 30	GND	Ground
2, 20	V _{CC}	Power-Supply Input. Bypass V _{CC} to GND with a 0.1μF capacitor placed as close to V _{CC} as possible.
3	EN	Enable Input
4	COM0	Analog Switch Common D- Terminal
5	COM1	Analog Switch Common D+ Terminal
6	C0	Control Input 0
7	C1	Control Input 1
8	C2	Control Input 2
9	D0_0	Analog Switch 0 D- Terminal
10	D0_1	Analog Switch 0 D+ Terminal
12	D1_0	Analog Switch 1 D- Terminal
13	D1_1	Analog Switch 1 D+ Terminal
15	D2_0	Analog Switch 2 D- Terminal
16	D2_1	Analog Switch 2 D+ Terminal
18	D3_0	Analog Switch 3 D- Terminal
19	D3_1	Analog Switch 3 D+ Terminal
22	D4_1	Analog Switch 4 D+ Terminal
23	D4_0	Analog Switch 4 D- Terminal
25	D5_1	Analog Switch 5 D+ Terminal
26	D5_0	Analog Switch 5 D- Terminal
28	D6_1	Analog Switch 6 D+ Terminal
29	D6_0	Analog Switch 6 D- Terminal
31	D7_1	Analog Switch 7 D+ Terminal
32	D7_0	Analog Switch 7 D- Terminal
—	EP	Exposed Pad. Connect EP to GND or leave unconnected.

Detailed Description

The MAX4999 differential Hi-Speed USB analog multiplexer features low on-capacitance (C_{ON}) and low on-resistance (R_{ON}) necessary for high-performance switching applications. The low C_{ON} is designed for USB server/mass storage devices. This device is ideal for USB 2.0 Hi-Speed applications at 480Mbps, while also meeting the requirements for USB low-/full-speed applications.

Digital Control Inputs (C0, C1, C2)

The MAX4999 provides three digital control inputs (C0, C1, C2) to select the analog signal path between the COM₋ and D-/D+ channels. The truth table for the MAX4999 is shown in the *Functional Diagram/Truth Table*. Driving the control inputs rail-to-rail minimizes power consumption.

Enable Input (EN)

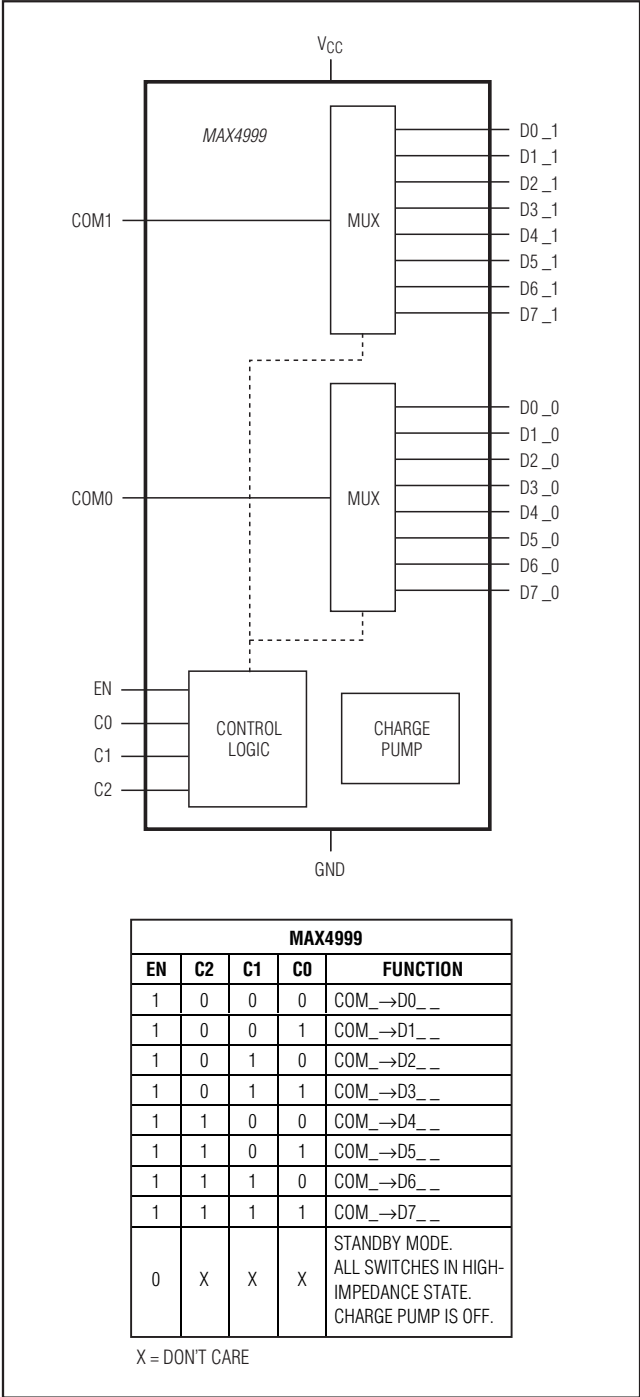
The MAX4999 features an enable input that when driven low, places the device in standby mode. In standby mode, all channels are high impedance and the internal charge pump is disabled, thus minimizing the quiescent supply current. For normal operation, drive EN high.

Analog Signal Levels

Signals applied to COM1 are routed to D₋_1 terminals. Signals applied to COM0 are routed to D₋_0 terminals. This multiplexer is bidirectional, allowing COM₋ and D-/D+ terminals to be configured as either inputs or outputs. Additionally, the MAX4999 can be used for non-USB signals if the signals fall within the normal operating range.

The MAX4999 features an internal charge pump that allows signal levels greater than the supply voltage. Limit the analog input/output signal level to no more than the *Absolute Maximum Ratings*.

Functional Diagram/Truth Table



Applications Information

Increasing USB Channels

The MAX4999 features an enable input that allows two MAX4999s to be connected, allowing multiplexing between 16 USB channels. Figure 4 shows the typical application with a single USB common terminal multiplexed to eight channels (8:1). See the Eye Diagram - Single graph in the *Typical Operating Characteristics*. Figure 5 shows two MAX4999 devices configured with the USB common terminal multiplexed to 16 USB channels (16:1). See the Eye Diagram - Double graph in the *Typical Operating Characteristics*. The MAX4999 was designed to be symmetrical so that the two common ports may be wired in parallel with very short wiring to create a 16:1 configuration. When operating in 16:1 configuration, interchange COM0 and COM1 on the second device to reverse the D+ and D- pins. This minimizes vias and crossovers (Figure 5).

USB Switching

The MAX4999 analog multiplexers are fully compliant with the USB 2.0 specification. The low on-resistance and low on-capacitance of the MAX4999 make it ideal for high-performance switching applications.

Board Layout

Hi-Speed switches require proper layout and design procedures for optimum performance. Keep design-controlled impedance PCB traces as short as possible. Ensure that high-quality bypass ceramic capacitors (X7R, X5R or better) are placed as close to the device as possible and use large ground planes where possible.



Chip Information

PROCESS: CMOS

Package Information

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
32 TQFN	T3255+4	21-0140	90-0012

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	5/08	Initial release	—
1	6/11	Added <i>Package Thermal Characteristics</i> ; renamed pins in Figure 4; changed pin references in <i>Electrical Characteristics</i> , Figures 3 and 5, TOCs, and <i>Functional Diagram</i> .	2, 5, 6, 8, 9
2	3/15	Updated <i>Benefits and Features</i> section	1

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Телефон: 8 (812) 309-75-97 (многоканальный)

Факс: 8 (812) 320-03-32

Электронная почта: ocean@oceanchips.ru

Web: <http://oceanchips.ru/>

Адрес: 198099, г. Санкт-Петербург, ул. Калинина, д. 2, корп. 4, лит. А