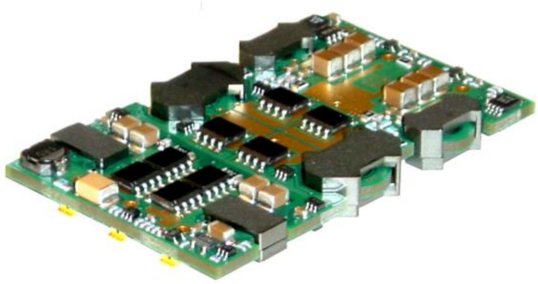
QD48S033050

Quarter-Brick DC-DC Converter



The **QD48S033050** dual output surface mounted DC-DC converter offers unprecedented performance in a quarter brick package by providing two independently regulated high current outputs with total power of 100 W. This is accomplished by the use of patent pending circuit and packaging techniques to achieve ultra-high efficiency, excellent thermal performance and a very low body profile.

In telecommunications applications the **QD48** converters provide up to 15 A @ 3.3 V and 10 A @ 5 V simultaneously – with thermal performance far exceeding existing dual quarter bricks and comparable to dual half-bricks. Low body profile and the preclusion of heat sinks minimize airflow shadowing, thus enhancing cooling for downstream devices. The use of 100% surface-mount technologies for assembly, coupled with Power Bel Solutions advanced electric and thermal circuitry and packaging, results in a product with extremely high quality and reliability.

Key Features & Benefits

- RoHS lead-free solder and lead-solder-exempted products are available
- Delivers simultaneously up to 15 A on 3.3 VDC and up to 10 A on 5.0 VDC output
- Can replace two single output quarter-bricks
- Minimal cross-channel interference
- High efficiency: 88% @ full load, 89% @ half load
- Start-up into pre-biased output
- No minimum load required
- No heat sink required
- Low profile: 0.26” [6.6 mm]
- Low weight: 1 oz [28 g] typical
- Industry-standard footprint: 1.45” x 2.30”
- Meets Basic Insulation Requirements of EN60950
- Withstands 100 V input transient for 100 ms
- On-board LC input filter
- Fixed-frequency operation
- Fully protected
- Output voltage trim range: ±10% for both outputs
- Trim resistor via industry-standard equations
- High reliability: MTBF 2.6 million hours, calculated per Telcordia TR-332, Method I Case 1
- Positive or negative logic ON/OFF option
- Approved to the latest edition and amendment of ITE Safety standards, UL/CSA 60950-1 and IEC60950-1
- Meets conducted emissions requirements of FCC
- Class B and EN55022 Class B with external filter
- All materials meet UL94, V-0 flammability rating

1. ELECTRICAL SPECIFICATIONS

Conditions: T_A = 25°C, Airflow = 300 LFM (1.5 m/s), Vin = 48 VDC, unless otherwise specified.

PARAMETER	CONDITIONS / DESCRIPTION	MIN	TYP	MAX	UNITS
Absolute Maximum Ratings					
Input Voltage	Continuous	0		80	VDC
Operating Ambient Temperature		-40		85	°C
Storage Temperature		-55		125	°C
Input Characteristics					
Operating Input Voltage Range		36	48	75	VDC
Input Under Voltage Lockout	Non-latching				
Turn-on Threshold		33	34	35	VDC
Turn-off Threshold		31	32	33	VDC
Input Transient Withstand (Susceptibility)	100 ms			100	VDC
Output Characteristics					
External Load Capacitance					
3.3 V	Plus full load (resistive)			10,000	µF
5.0 V	Plus full load (resistive)			4,700	µF
Output Current Range					
3.3 V	At nominal output voltage 3.3 V	0		15	ADC
5.0 V	At nominal output voltage 5.0 V	0		10	ADC
Current Limit Inception					
3.3V	Non-latching	15.75	18	19.5	ADC
5.0 V	Non-latching	10.5	13	15	ADC
Peak Short-Circuit Current					
3.3 V	Non-latching. Short=10mΩ.		20	30	A
5.0 V	Non-latching. Short=10mΩ.		15	30	A
RMS Short-Circuit Current					
3.3 V	Non-latching			4	Arms
5.0 V	Non-latching			4	Arms
Isolation Characteristics					
I/O Isolation		2000			VDC
Isolation Capacitance			1.3		pF
Isolation Resistance		10			MΩ
Feature Characteristics					
Switching Frequency			435		kHz
Output Voltage Trim Range[1]					
3.3 V	See section: Output Voltage Adjust/TRIM	-10		+10	%
5.0 V	Simultaneous with 3.3 V output	-10		+10	%
Output Over-Voltage Protection					
3.3 V	Non-latching	3.85	4.125	4.25	V
5.0 V	Non-latching	5.85	6.15	6.4	V
Over-Temperature Shutdown (PCB)	Non-latching		120		°C
Auto-Restart Period	Applies to all protection features		100		ms
Turn-On Time 5.0 V	3.3 V tracks 5.0 V		4		ms
ON/OFF Control (Positive Logic)					
Converter Off		-20		0.8	VDC
Converter On		2.4		20	VDC
ON/OFF Control (Negative Logic)					
Converter Off		2.4		20	VDC
Converter On		-20		0.8	VDC

Input Characteristics					
Maximum Input Current	3.3 VDC @ 15 ADC, 5.0 VDC @ 10 ADC, Vin = 36 V			3.2	ADC
Input Stand-by Current	Vin = 48 V, converter disabled		2.6		mAdc
Input No Load Current (0 load on the output)	Vin = 48 V, converter enabled		72		mAdc
Input Reflected-Ripple Current	See Figure 36 - 25MHz bandwidth		6		mAPK-PK
Input Voltage Ripple Rejection	120Hz		TBD		dB
Output Characteristics					
Output Voltage Set Point (no load)					
3.3 V	-40°C to 85°C	3.267	3.300	3.333	VDC
5.0 V	-40°C to 85°C	4.950	5.000	5.050	VDC
Output Regulation					
Over Line					
3.3 V			±2		mV
5.0 V			±2		mV
Over Load[2]					
3.3 V			-10		mV
5.0 V			-6		mV
Cross Regulation[3]					
3.3 V	For Iout2 (5.0 V) change from 0 to 10 A		-3		mV
5.0 V	For Iout1 (3.3 V) change from 0 to 15 A		-5		mV
Output Voltage Range					
3.3 V	Over line, load and cross regulation	3.234		3.366	VDC
5.0 V	Over line, load and cross regulation	4.9		5.100	VDC
Output Ripple and Noise - 25MHz bandwidth					
3.3 V	Full load + 1 µF ceramic		20	30	mVPK-PK
5.0 V	Full load + 1 µF ceramic		25	35	mVPK-PK
Dynamic Response					
Load Change: 50% to 75% to 50%	ΔIout = 25% of IoutMax				
di/dt = 0.1 A/µS					
3.3 V	Co = 10 µF tant. + 1 µF ceramic (Fig.23)		40		mV
5.0 V	Co = 10 µF tant. + 1 µF ceramic (Fig.24)		50		mV
Setting Time to 1%					
3.3 V			100		µs
5.0 V			20		µs
di/dt = 5 A/µS					
3.3V	Co = 300 µF tant. + 1 µF ceramic (Fig.25)		90		mV
5.0 V	Co = 300 µF tant. + 1 µF ceramic (Fig.26)		90		mV
Setting Time to 1%					
3.3 V			60		µs
5.0 V			60		µs
Efficiency					
3.3 V 100% Load, 5.0 V 100% Load			88		%
3.3 V 50% Load, 5.0 V 50% Load			89		%

1) Vout1 and Vout2 can be simultaneously increased or decreased up to 10% via the Trim function. When trimming up, in order not to exceed the converter's maximum allowable output power capability equal to the product of the nominal output voltage and the allowable output current for the given conditions, the designer must, if necessary, decrease the maximum current (originally obtained from the derating curves) by the same percentage to ensure the converter's actual output power remains at or below the maximum allowable output power.

2) Load regulation is affected with resistance of the output pins (approximately 0.3 mΩ) since there is no remote sense.

3) Cross regulation is affected with resistance of the RETURN pin (approximately 0.3 mΩ) since there is no remote sense.

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2. OPERATIONS

2.1 INPUT AND OUTPUT IMPEDANCE

These power converters have been designed to be stable with no external capacitors when used in low inductance input and output circuits.
However, in many applications, the inductance associated with the distribution from the power source to the input of the converter can affect the stability of the converter. The addition of a 33 μF electrolytic capacitor with an ESR < 1 Ω across the input helps ensure stability of the converter. In many applications, the user has to use decoupling capacitance at the load. The converter will exhibit stable operation with external load capacitance up to 10,000 μF on 3.3 V and 4,700uF on 5 V output.

2.2 ON/OFF (Pin 2)

The ON/OFF pin is used to turn the power converter on or off remotely via a system signal. There are two remote control options available, positive logic and negative logic and both are referenced to Vin(-). Typical connections are shown in Fig. 1.

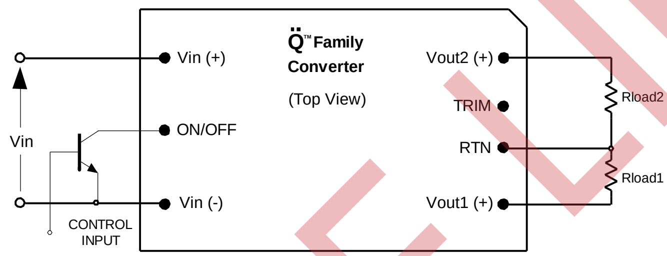


Figure 1. Circuit configuration for ON/OFF function.

The positive logic version turns on when the ON/OFF pin is at logic high and turns off when at logic low. The converter is on when the ON/OFF pin is left open.
The negative logic version turns on when the pin is at logic low and turns off when the pin is at logic high. The ON/OFF pin can be hard wired directly to Vin(-) to enable automatic power up of the converter without the need of an external control signal.
ON/OFF pin is internally pulled-up to 5 V through a resistor. A mechanical switch, open collector transistor, or FET can be used to drive the input of the ON/OFF pin. The device must be capable of sinking up to 0.2 mA at a low level voltage of ≤ 0.8 V. An external voltage source of ±20 V max. may be connected directly to the ON/OFF input, in which case it should be capable of sourcing or sinking up to 1 mA depending on the signal polarity. See the Start-up Information section for system timing waveforms associated with use of the ON/OFF pin.

2.3 OUTPUT VOLTAGE ADJUST/TRIM (PIN 6)

The converter's output voltages can be adjusted simultaneously up 10% or down 10% relative to the rated output voltages by the addition of an externally connected resistor.
The TRIM pin should be left open if trimming is not being used. To minimize noise pickup, a 0.1 μF capacitor is connected internally between the TRIM and RETURN pins.

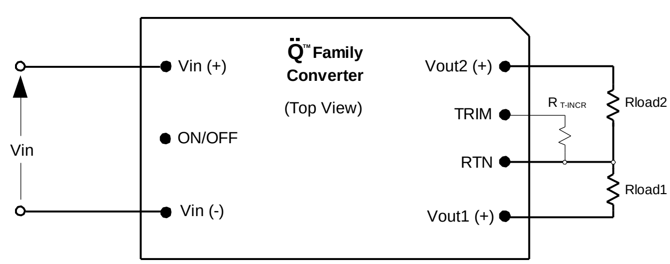


Figure 2. Configuration for increasing output voltage.

To increase the output voltage (refer to Fig. 2), a trim resistor, $R_{T\text{-}INCR}$, should be connected between the TRIM (Pin 6) and RETURN (Pin 5), with a value from the table below.

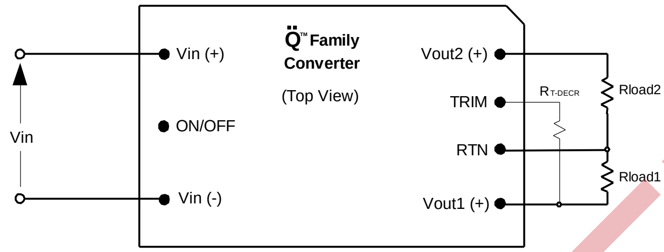


Figure 3. Configuration for decreasing output voltage.

To decrease the output voltage, a trim resistor $R_{T\text{-}DECR}$, (Fig. 3) should be connected between the TRIM (Pin 6) and Vout1(+) pin (Pin 4), with a value from the table below, where:
Δ = percentage of increase or decrease Vout (NOM).

Note 1:
Both outputs are trimmed up or down simultaneously.

TRIM RESISTOR (VOUT INCREASE)	
Δ [%]	*$R_{T\text{-}INCR}$ [kΩ]*
1	54.9
2	24.9
3	14.3
4	9.31
5	6.34
6	4.32
7	2.80
8	1.69
9	0.825
10	0

TRIM RESISTOR (VOUT DECREASE)	
Δ [%]	*$R_{T\text{-}DECR}$ [kΩ]*
-1	68.1
-2	30.1
-3	17.8
-4	11.5
-5	7.68
-6	5.36
-7	3.48
-8	2.10
-9	1.05
-10	0

Note 2: The above trim resistor values match those typically used in industry-standard dual quarter bricks.

3. PROTECTION FEATURES

3.1 INPUT UNDERVOLTAGE LOCKOUT

Input under-voltage lockout is standard with this converter. The converter will shut down when the input voltage drops below a pre-determined voltage.
The input voltage must be at least 35 V for the converter to turn on. Once the converter has been turned on, it will shut off when the input voltage drops below 31 V. This feature is beneficial in preventing deep discharging of batteries used in telecom applications.

3.2 OUTPUT OVERCURRENT PROTECTION (OCP)

The converter is protected against overcurrent or short circuit conditions on both outputs. Upon sensing an overcurrent condition, the converter will switch to constant current operation and thereby begin to reduce output voltages. If, due to current limit, the output voltage Vout1 (3.3 V) drops, than Vout2 (5.0 V) will follow Vout1 with less than 1 V difference. Drop on Vout2 output due to current limit will not affect voltage on Vout1. For further load increase, if either Vout1 drops below 1 Vdc or Vout2 drops below 2 Vdc, the converter will shut down (Figs. 29 and 30).
Once the converter has shut down, it will attempt to restart nominally every 100 ms with a 2% duty cycle (Figs. 33 and 34). The attempted restart will continue indefinitely until the overload or short circuit conditions are removed or the output voltage Vout1 rises above 1 Vdc and Vout2 above 2 Vdc.

3.3 OUTPUT OVERVOLTAGE PROTECTION (OVP)

The converter will shut down if the output voltage across either Vout1(+) (Pin 4) or Vout2(+) (Pin 7) and RETURN (Pin 5) exceeds the threshold of the OVP circuitry. The OVP protection is separate for Vout1 and Vout2 with their own reference independent of the output voltage regulation loops. Once the converter has shut down, it will attempt to restart every 100 ms until the OVP condition is removed.

3.4 OVERTEMPERATURE PROTECTION (OTP)

The converter will shut down under an over temperature condition to protect itself from overheating caused by operation outside the thermal derating curves, or operation in abnormal conditions such as system fan failure. After the converter has cooled to a safe operating temperature, it will automatically restart.

3.5 SAFETY REQUIREMENTS

The converters meet North American and International safety regulatory requirements per UL60950 and EN60950. Basic Insulation is provided between input and output.
To comply with safety agencies requirements, an input line fuse must be used external to the converter. A 5-A fuse is recommended for use with this product.

3.6 ELECTROMAGNETIC COMPATIBILITY (EMC)

EMC requirements must be met at the end-product system level, as no specific standards dedicated to EMC characteristics of board mounted component dc-dc converters exist. However, Power Bel Solutions tests its converters to several system level standards, primary of which is the more stringent EN55022, Information technology equipment - Radio disturbance characteristics - Limits and methods of measurement.
With the addition of a simple external filter (see application notes), all versions of the QD48S converters pass the requirements of Class B conducted emissions per EN55022 and FCC, and meet at a minimum, Class A radiated emissions per EN 55022 and Class B per FCC Title 47CFR, Part 15-J. Please contact Power Bel Solutions Applications Engineering for details of this testing.

3.7 INPUT TRANSIENT WITHSTAND

This family of converters withstands 100V input transient for 100ms.

3.8 STARTUP INFORMATION (USING NEGATIVE ON/OFF)

Scenario #1: Initial Startup From Bulk Supply
ON/OFF function enabled, converter started via application of V_{IN}. See Figure 4.

Time	Comments
t_0	ON/OFF pin is ON; system front-end power is toggled on, V_{IN} to converter begins to rise.
t_1	V_{IN} crosses Under-Voltage Lockout protection circuit threshold; converter enabled.
t_2	Converter begins to respond to turn-on command (converter turn-on delay).
t_3	Output voltage $V_{OUT}1$ reaches 100% of nominal value
t_4	Output voltage $V_{OUT}2$ reaches 100% of nominal value.

For this example, the total converter startup time (t_4- t_1) is typically 4 ms.

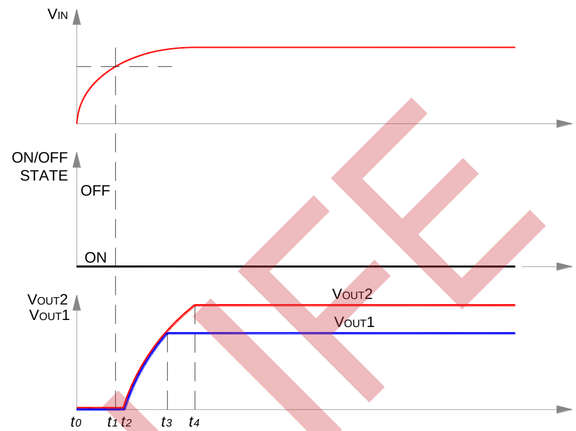


Figure 4. Start-up scenario #1.

Scenario #2: Initial Startup Using ON/OFF Pin
With V_{IN} previously powered, converter started via ON/OFF pin. See Figure 5.

Time	Comments
t_0	V_{INPUT} at nominal value.
t_1	Arbitrary time when ON/OFF pin is enabled (converter enabled).
t_2	End of converter turn-on delay.
t_3	Output voltage V_{OUT1} reaches 100% of nominal value.
t_4	Output voltage V_{OUT2} reaches 100% of nominal value.

For this example, the total converter startup time (t_4- t_1) is typically 4 ms.

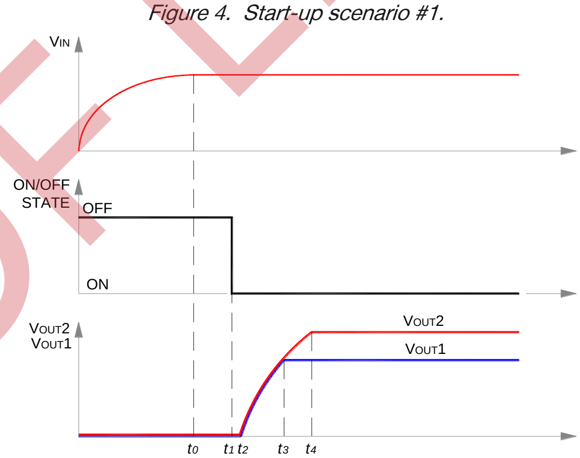


Figure 5. Startup scenario #2.

Scenario #3: Turn-off and Restart Using ON/OFF Pin
With V_{IN} previously powered, converter is disabled and then enabled via ON/OFF pin. See Figure 6.

Time	Comments
t_0	V_{IN} and V_{OUT} are at nominal values; ON/OFF pin ON.
t_1	ON/OFF pin arbitrarily disabled; converter output falls to zero; turn-on inhibit delay period (100 ms typical) is initiated, and ON/OFF pin action is internally inhibited.
t_2	ON/OFF pin is externally re-enabled. **If (t_2- t_1) ≤ 100 ms**, external action of ON/OFF pin is locked out by startup inhibit timer. **If (t_2- t_1) > 100 ms**, ON/OFF pin action is internally enabled.
t_3	Turn-on inhibit delay period ends. If ON/OFF pin is ON, converter begins turn-on; if off, converter awaits ON/OFF pin ON signal; see Figure 5.
t_4	End of converter turn-on delay.
t_5	Output voltage V_{OUT1} reaches 100% of nominal value.
t_6	Output voltage V_{OUT2} reaches 100% of nominal value.

For the condition, **(t_2- t_1) ≤ 100 ms**, the total converter startup time (t_6- t_2) is typically 103 ms. For **(t_2- t_1) > 100 ms**, startup will be typically 4 ms after release of ON/OFF pin.

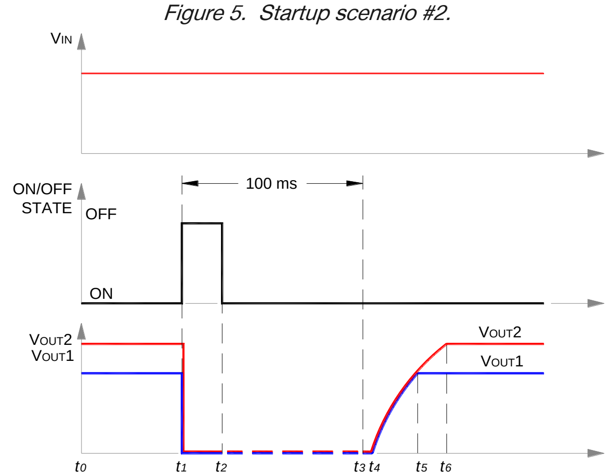


Figure 6. Startup scenario #3.

4. CHARACTERIZATION

4.1 GENERAL INFORMATION

The converter has been characterized for many operational aspects, to include thermal derating (maximum load current as a function of ambient temperature and airflow) for vertical and horizontal mounting, efficiency, start-up and shutdown parameters, output ripple and noise, transient response to load step-change, overload and short circuit.
The following pages contain specific plots or waveforms associated with the converter. Additional comments for specific data are provided below.

4.2 TEST CONDITIONS

All data presented were taken with the converter soldered to a test board, specifically a 0.060" thick printed wiring board (PWB) with four layers. The top and bottom layers were not metalized. The two inner layers, comprising two-ounce copper, were used to provide traces for connectivity to the converter.
The lack of metalization on the outer layers as well as the limited thermal connection ensured that heat transfer from the converter to the PWB was minimized. This provides a worst-case but consistent scenario for thermal derating purposes.
All measurements requiring airflow were made in Power Bel Solutions vertical and horizontal wind tunnel facilities using infrared (IR) thermography and thermocouples for thermometry.
Ensuring that the components on the converter do not exceed their ratings is important to maintaining high reliability. If one anticipates operating the converter at or close to the maximum loads specified in the derating curves, it is prudent to check actual operating temperatures in the application. Thermographic imaging is preferable; if this capability is not available, then thermocouples may be used. Power Bel Solutions recommends the use of AWG #40 gauge thermocouples to ensure measurement accuracy. Careful routing of the thermocouple leads will further minimize measurement error. Refer to Figure 37 for optimum measuring thermocouple location.

4.3 THERMAL DERATING

Available output power and load current vs. ambient temperature and airflow rates are given in Figs. 7-14. Ambient temperature was varied between 25°C and 85°C, with airflow rates from 30 to 500 LFM (0.15 to 2.5 m/s), and vertical and horizontal converter mounting.
For each set of conditions, the maximum load current was defined as the lowest of:

(i) The output current at which either any FET junction temperature did not exceed a maximum specified temperature (120°C) as indicated by the thermographic image, or
(ii) The nominal rating of the converter (15 A on Vout1 and 10 A on Vout2.)

During normal operation, derating curves with maximum FET temperature less than or equal to 120°C should not be exceeded. Temperature on the PCB at the thermocouple location shown in Fig. 37 should not exceed 118°C in order to operate inside the derating curves.

4.4 EFFICIENCY

Efficiency vs. load current plots are shown in Figs. 14-19 for ambient temperature of 25ºC, airflow rate of 300 LFM (1.5 m/s), both vertical and horizontal orientations, and input voltages of 36 V, 48 V and 72 V, for different combinations of the loads on outputs Vout1 and Vout2.

4.5 START-UP

Output voltage waveforms during the turn-on transient using the ON/OFF pin, are shown without and with full rated load currents (resistive load) in Figs. 21 and 22, respectively.

4.6 RIPPLE AND NOISE

Figure 31 shows the output voltage ripple waveform, measured at full rated load current on both outputs with a 1 μF ceramic capacitor across both outputs. Note that all output voltage waveforms are measured across a 1 μF ceramic capacitor. The input reflected ripple current waveforms are obtained using the test setup shown in Fig. 32. The corresponding waveforms are shown in Figs. 35 and 36.

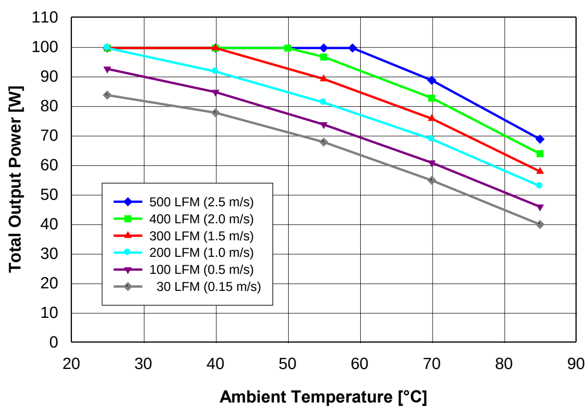


Figure 7. Available output power for balanced load current (Iout1 = 1.5 Iout2) vs. ambient air temperature and airflow rates for converter mounted vertically with Vin = 48 V, air flowing from pin 3 to pin 1 and maximum FET temperature ≤ 120 °C.

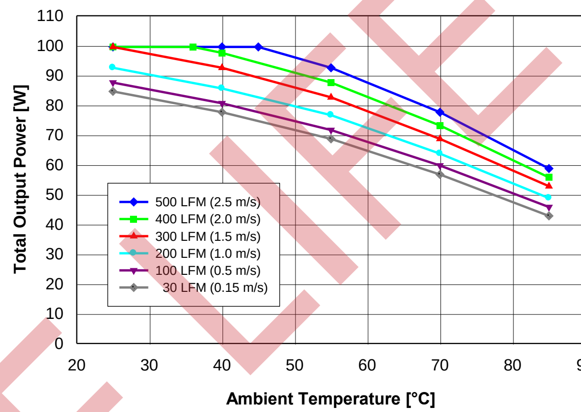


Figure 8. Available output power for balanced load current (Iout1 = 1.5 Iout2) vs. ambient air temperature and airflow rates for converter mounted horizontally with Vin = 48 V, air flowing from pin 3 to pin 4 and maximum FET temperature ≤ 120 °C.

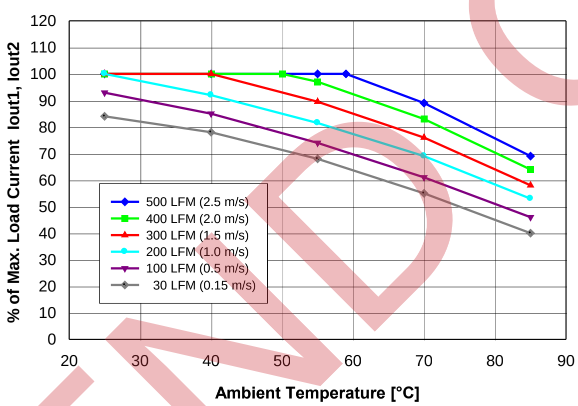


Figure 9. Available balanced load current (Iout1 = 1.5 Iout2) vs. ambient air temperature and airflow rates for converter mounted vertically with Vin = 48 V, air flowing from pin 3 to pin 1 and maximum FET temperature ≤ 120 °C.

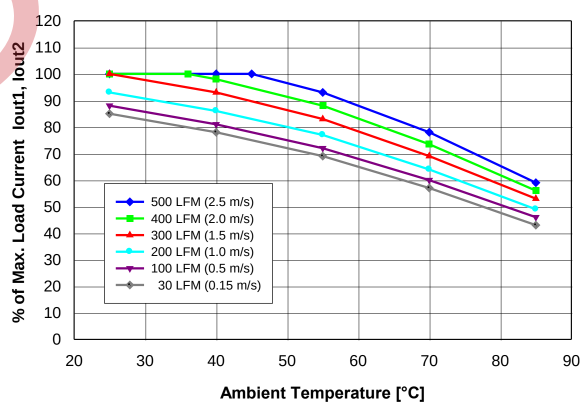


Figure 10. Available balanced load current (Iout1 = 1.5 Iout2) vs. ambient temperature and airflow rates for converter mounted horizontally with Vin = 48 V, air flowing from pin 3 to pin 4 and maximum FET temperature ≤ 120 °C.

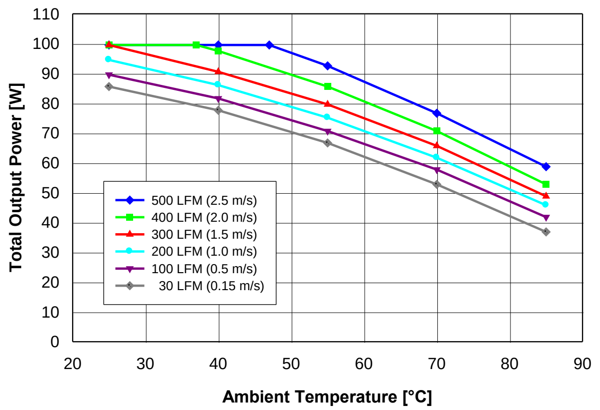


Figure 11. Available output power for balanced load current (Iout1 = 1.5·Iout2) vs. ambient air temperature and airflow rates for converter mounted vertically with Vin = 48 V, air flowing from pin 3 to pin 4 and maximum FET temperature ≤ 120 °C.

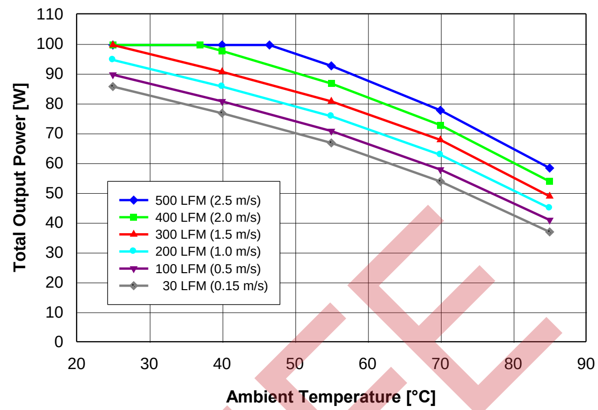


Figure 12. Available output power for balanced load current (Iout1 = 1.5·Iout2) vs. ambient air temperature and airflow rates for converter mounted vertically with Vin = 48 V, air flowing from pin 4 to pin 3 and maximum FET temperature ≤ 120 °C.

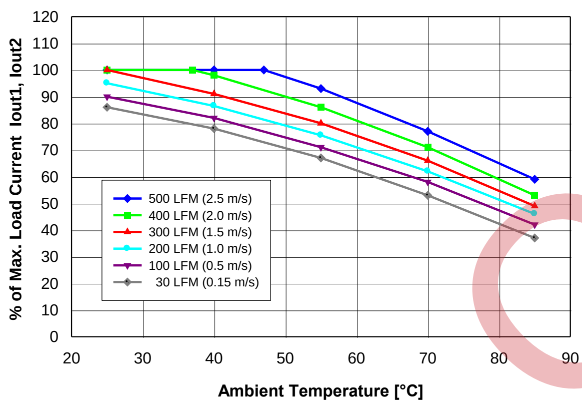


Figure 13. Available balanced load current (Iout1 = 1.5·Iout2) vs. ambient air temperature and airflow rates for converter mounted vertically with Vin = 48 V, air flowing from pin 3 to pin 4 and maximum FET temperature ≤ 120 °C.

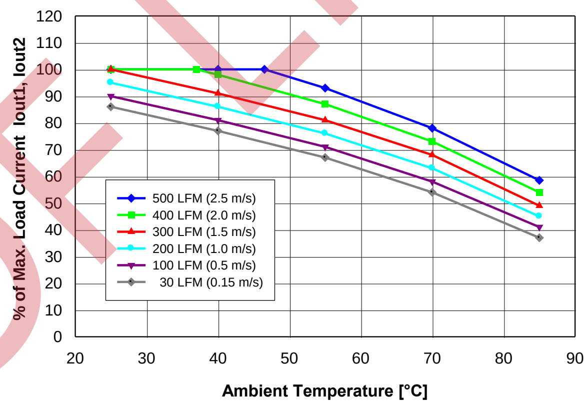


Figure 14. Available balanced load current (Iout1 = 1.5·Iout2) vs. ambient air temperature and airflow rates for converter mounted vertically with Vin = 48 V, air flowing from pin 4 to pin 3 and maximum FET temperature ≤ 120 °C.

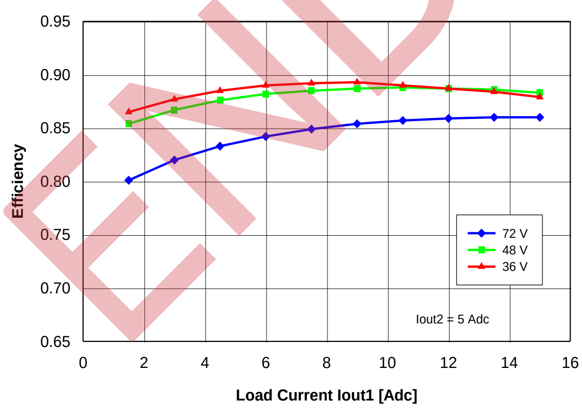


Figure 15. Efficiency vs. load current Iout1 and input voltage for converter mounted vertically with air flowing from pin 3 to pin 1 at a rate of 300 LFM (1.5 m/s), for Iout2 = 5 A and Ta = 25 °C.

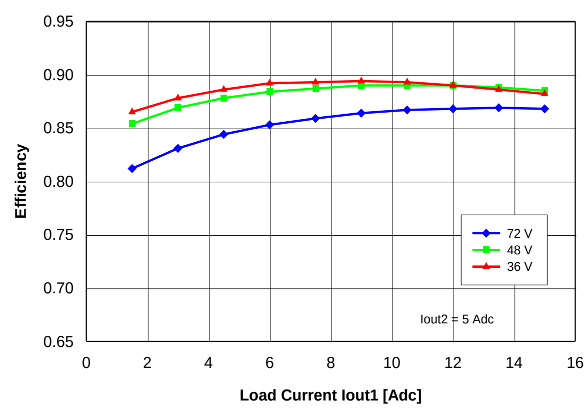


Figure 16. Efficiency vs. load current Iout1 and input voltage for converter mounted horizontally with air flowing from pin 3 to pin 4 at a rate of 300 LFM (1.5 m/s), for Iout2 = 5 A and Ta = 25 °C.

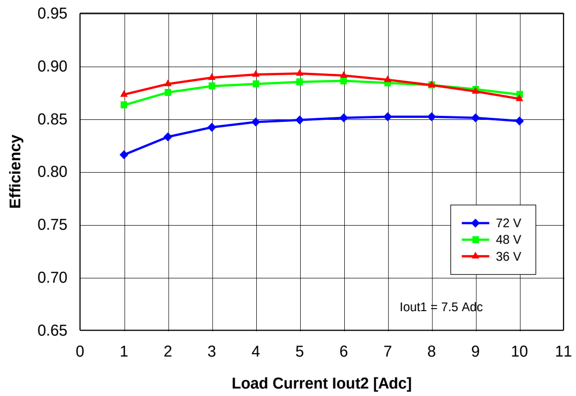


Figure 17. Efficiency vs. load current Iout2 and input voltage for converter mounted vertically with air flowing from pin 3 to pin 1 at a rate of 300 LFM (1.5 m/s), for Iout1 = 7.5 A and Ta = 25 °C.

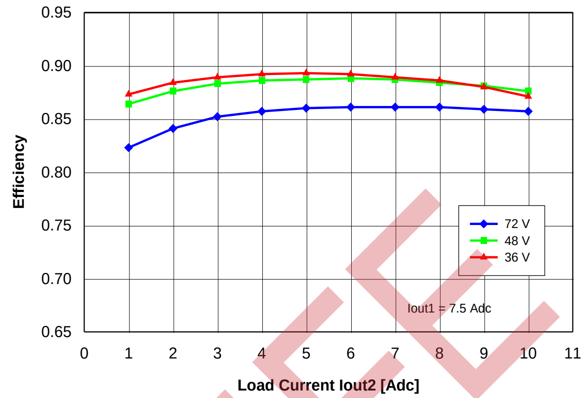


Figure 18. Efficiency vs. load current Iout2 and input voltage for converter mounted horizontally with air flowing from pin 3 to pin 4 at a rate of 300 LFM (1.5 m/s), for Iout1 = 7.5 A and Ta = 25 °C.

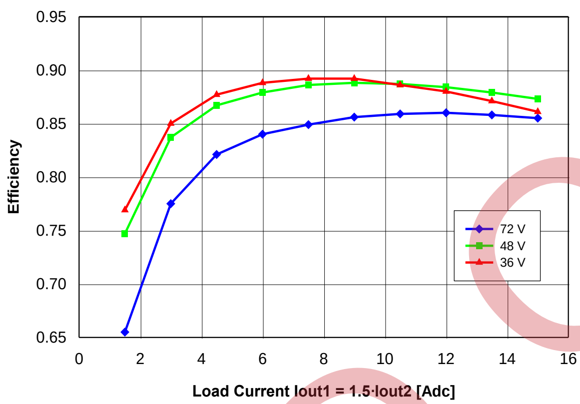


Figure 19. Efficiency vs. balanced load current (Iout1 = 1.5·Iout2) and input voltage for converter mounted vertically with air flowing from pin 3 to pin 1 at a rate of 300 LFM (1.5 m/s) and Ta = 25 °C.

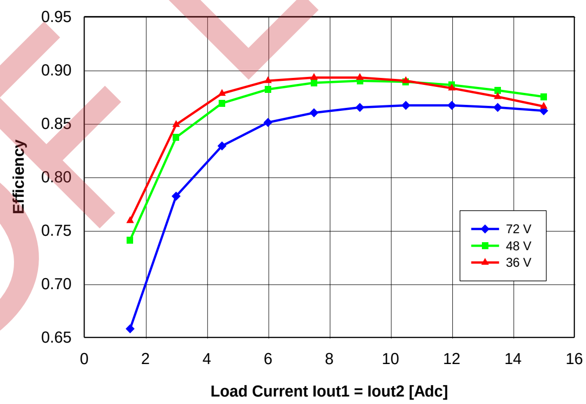


Figure 20. Efficiency vs. balanced load current (Iout1/Iout2 = const.) and input voltage for converter mounted horizontally with air flowing from pin 3 to pin 4 at a rate of 300 LFM (1.5 m/s) and Ta = 25 °C.

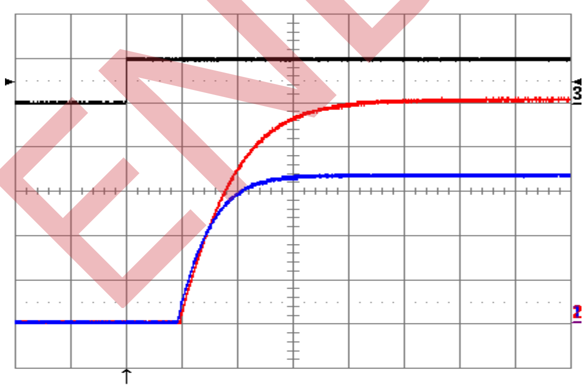


Figure 21. Turn-on transient waveforms at no load current and Vin = 48 V, triggered via ON/OFF pin. Top trace: ON/OFF signal (5 V/div.). Bottom traces: Vout1 (blue, 1 V/div.), Vout2 (red, 1 V/div.). Time scale: 1 ms/div.

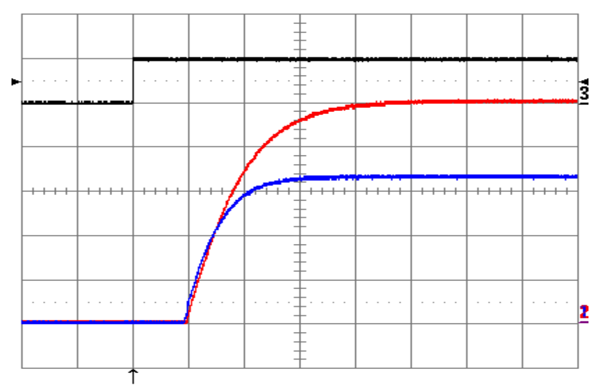


Figure 22. Turn-on transient waveforms at full rated load current (resistive) and Vin = 48 V, triggered via ON/OFF pin. Top trace: ON/OFF signal (5 V/div.). Bottom traces: Vout1 (blue, 1 V/div.), Vout2 (red, 1 V/div.). Time scale: 1 ms/div.

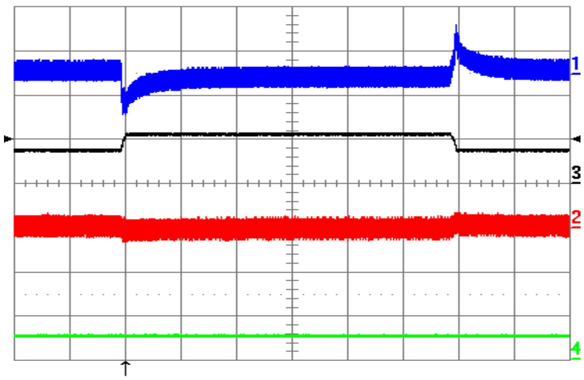


Figure 23. Output voltage response to Iout1 load current step-change of 3.75 A (50%-75%-50%) at Iout2 = 5 A and Vin = 48 V. Ch1 = Vout1 (50 mV/div), Ch2 = Vout2 (50 mV/div), Ch3 = Iout1 (10 A/div.), Ch4 = Iout2 (10 A/div.). Current slew rate: 0.1 A/ µs, Co = 10 µF tantalum + 1 µF ceramic. Time scale: 0.5 ms/div.

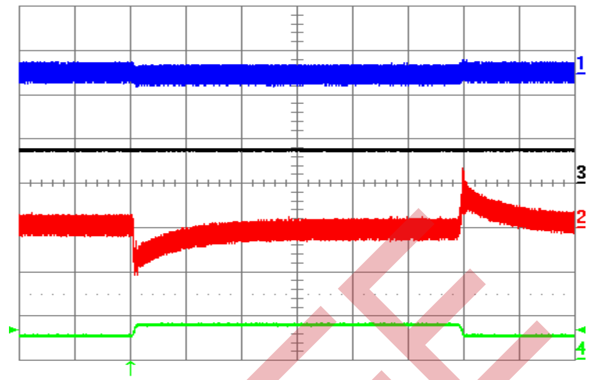


Figure 24. Output voltage response to Iout2 load current step-change of 2.5 A (50%-75%-50%) at Iout1 = 7.5 A and Vin = 48 V. Ch1 = Vout1 (50 mV/div), Ch2 = Vout2 (50 mV/div), Ch3 = Iout1 (10 A/div.), Ch4 = Iout2 (10 A/div.). Current slew rate: 0.1 A/ µs, Co = 10 µF tantalum + 1 µF ceramic. Time scale: 0.5 ms/div.

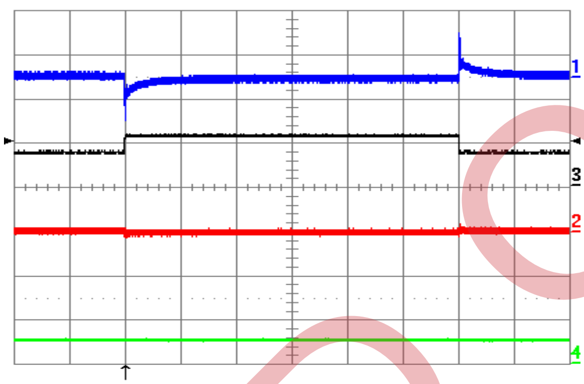


Figure 25. Output voltage response to Iout1 load current step-change of 3.75 A (50%-75%-50%) at Iout2 = 5 A and Vin = 48 V. Ch1 = Vout1 (100 mV/div), Ch2 = Vout2 (100 mV/div), Ch3 = Iout1 (10 A/div.), Ch4 = Iout2 (10 A/div.). Current slew rate: 5 A/µs, Co = 300 µF tantalum + 1 µF ceramic. Time scale: 0.5 ms/div.

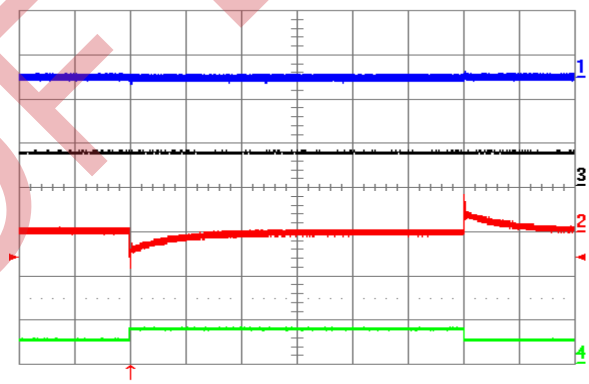


Figure 26. Output voltage response to Iout2 load current step-change of 2.5 A (50%-75%-50%) at Iout1 = 7.5 A and Vin = 48 V. Ch1 = Vout1 (100 mV/div), Ch2 = Vout2 (100 mV/div), Ch3 = Iout1 (10 A/div.), Ch4 = Iout2 (10 A/div.). Current slew rate: 5 A/µs, Co = 300 µF tantalum + 1 µF ceramic. Time scale: 0.5 ms/div.

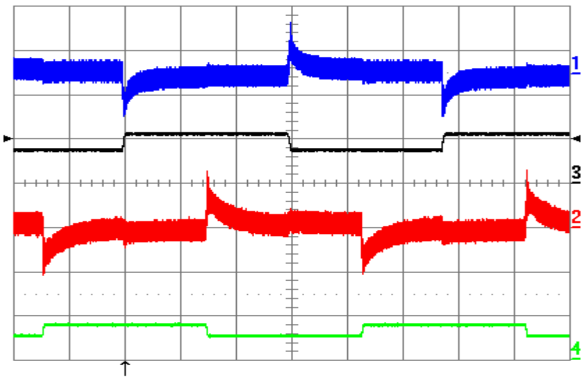


Figure 27. Output voltage response to both Iout1 and Iout2 (out of phase) load current step-change of 3.75 A (Iout1) and 2.5 A (Iout2) (50%-75%-50%) at Vin = 48 V. Ch1 = Vout1 (50 mV/div), Ch2 = Vout2 (50 mV/div), Ch3 = Iout1 (10 A/div.), Ch4 = Iout2 (10 A/div.). Current slew rate: 0.1 A/ µs, Co = 10 µF tantalum + 1 µF ceramic. Time scale: 1.0 ms/div.

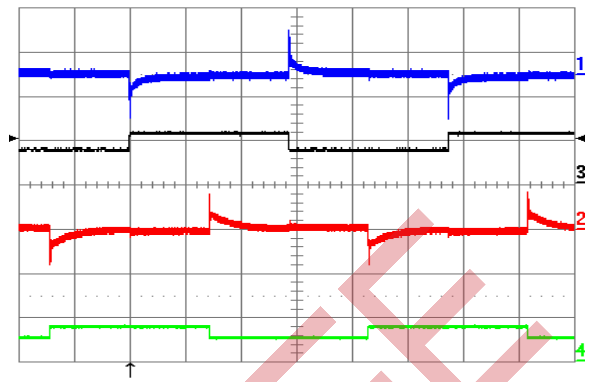


Figure 28. Output voltage response to both Iout1 and Iout2 (out of phase) load current step-change of 3.75 A (Iout1) and 2.5 A (Iout2) (50%-75%-50%) at Vin = 48 V. Ch1 = Vout1 (100 mV/div), Ch2 = Vout2 (100 mV/div), Ch3 = Iout1 (10 A/div.), Ch4 = Iout2 (10 A/div.) Current slew rate: 5 A/ µs, Co = 300 µF tantalum + 1 µF ceramic. Time scale: 1.0 ms/div.

Note: The only cross-talk during transient is due to the common RETURN pin for both outputs.

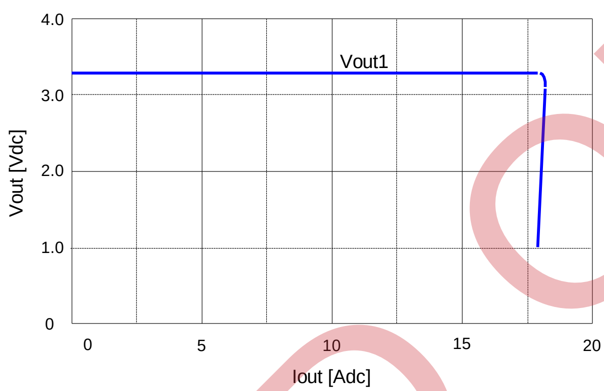


Figure 29. Output voltage Vout1 vs. load current Iout1 showing current limit point and converter shutdown point. When Vout1 is in current limit, Vout2 is not affected until Vout1 reaches the shut-down threshold of 1 V. Input voltage has almost no effect on Vout1 current limit characteristic.

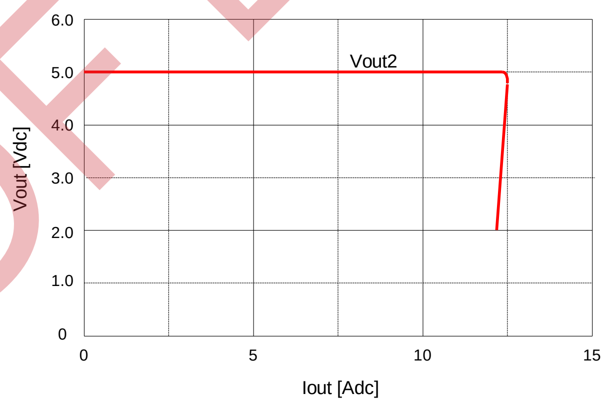


Figure 30. Output voltage Vout2 vs. load current Iout2 showing current limit point and converter shutdown point. When Vout2 is in current limit, Vout1 will follow with less than 1 V difference until Vout2 reaches shut-down threshold of 2 V. Input voltage has almost no effect onVout1 current limit characteristic.

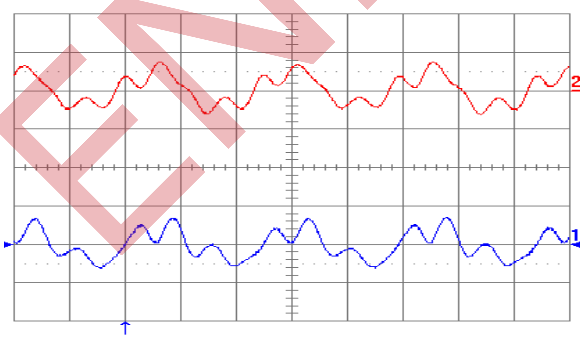


Figure 31. Output voltage ripple at full rated load current into a resistive load on both outputs with Co = 1uF (ceramic) and Vin = 48 V. Ch2 = Vout2, Ch1 = Vout1 (both 20 mV/div). Time scale: 1 µs/div.

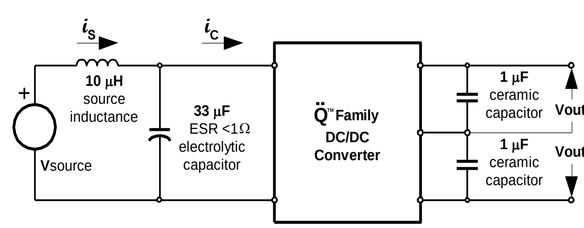


Figure 32. Test setup for measuring input reflected ripple currents, i_c and i_s.

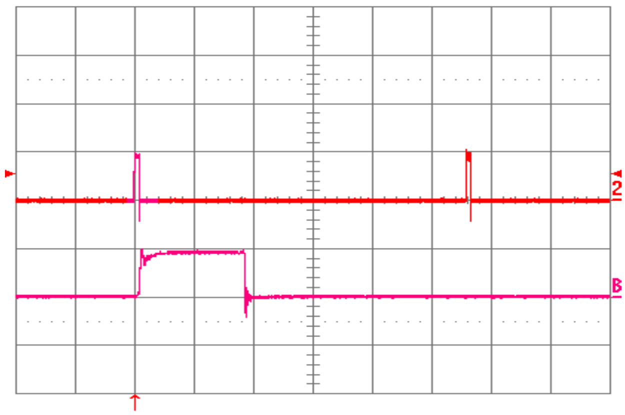


Figure 33. Load current Iout1 into a 10 mΩ short circuit on Vout1 during re-start, with Vout2 open (no load), at Vin = 48 V. Ch2 = Iout1 (20 A/div, 20 ms/div). ChB = Iout1 (20 A/div, 1 ms/div) is an expansion of the on-time portion of Iout1.

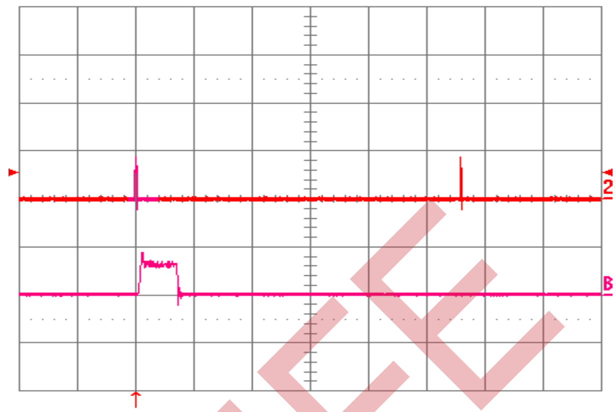


Figure 34. Load current Iout2 into a 10 mΩ short circuit on Vout2 during re-start, with Vout1 open (no load), at Vin = 48 V. Ch2 = Iout2 (20 A/div, 20 ms/div). ChB = Iout2 (20 A/div, 1 ms/div) is an expansion of the on-time portion of Iout2.

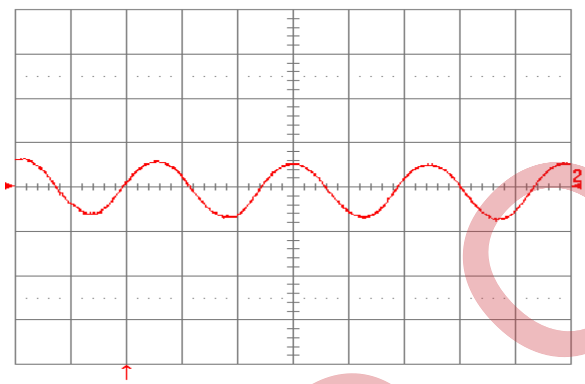


Figure 35. Input reflected ripple current, ic (100 mA/div), measured at input terminals at full rated load current on both outputs and Vin = 48 V. Refer to Fig. 34 for test setup. Time scale: 1 μs/div.

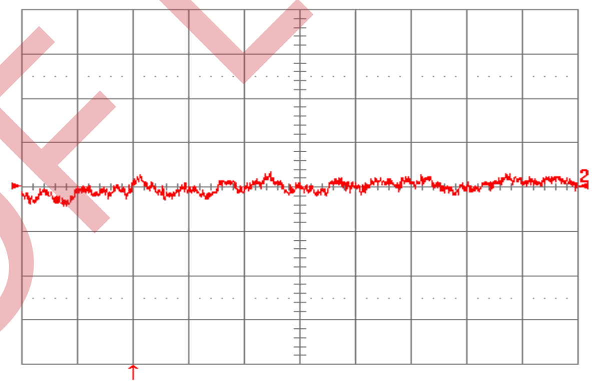


Figure 36. Input reflected ripple current, is (10 mA/div), measured through 10 μH at the source at full rated load current on both outputs and Vin = 48 V. Refer to Fig. 34 for test setup. Time scale: 1 μs/div.

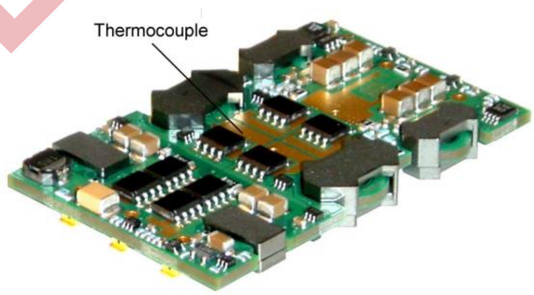
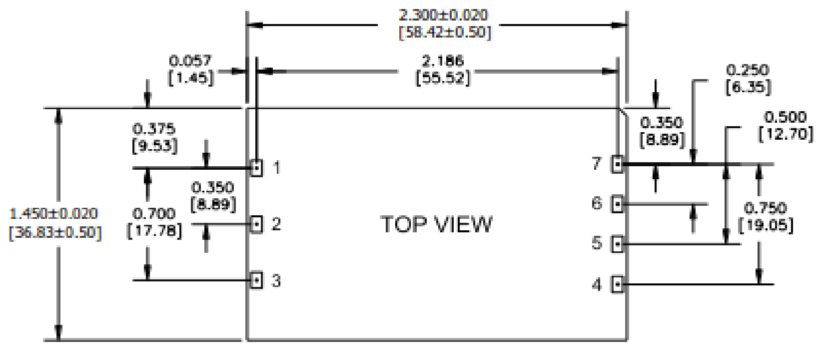


Figure 37. Location of the thermocouple for thermal testing.

5. MECHANICAL PARAMETERS



PAD/PIN CONNECTIONS	
Pad/Pin #	**Function**
1	Vin (+)
2	ON/OFF
3	Vin (-)
4	Vout1 (-)
5	RTN [Vo1(-) +Vo2(-)]
6	TRIM
7	Vout2 (+)

- All dimensions are in inches [mm]
- Connector material: Copper
- Connector Finish: Gold over Nickel
- Converter Weight: 1 oz. [28 g] typical
- Recommended Surface-Mount Pads:
  Min. 0.080" x 0.112" [2.03 x 2.84]
  Max. 0.092" x 0.124" [2.34 x 3.15]

6. ORDERING INFORMATION

Product Series	Input Voltage	Mounting Scheme	Output Voltage 1 (Vout1)	Output Voltage 2 (Vout2)		ON/OFF Logic	Maximum Height [HT]	Pin Length [PL]	Special Features	RoHS
QD	48	S	033	050	-	N	S	0	0	G
Dual Quarter-Brick Format	36-75 V	Surface Mount	033 ⇒ 3.3 V Note: Always specify Vout2 as the higher of the two output voltages.	050 ⇒ 5.0 V		N ⇒ Negative P ⇒ Positive	S ⇒ 0.273"	0 ⇒ 0.00"	0 ⇒ STD	No Suffix ⇒ RoHS lead-solder-exemption compliant G ⇒ RoHS compliant for all six substances

The example above describes P/N QD48S033050-NS00G: 36-75 V input, dual output, surface mounting, 3.3 V @ 15 A and 5.0 V @ 10 A, negative ON/OFF logic and RoHS compliant for all six substances. Please consult factory regarding availability of a specific version.

For more information on these products consult: tech.support@psbel.com

NUCLEAR AND MEDICAL APPLICATIONS - Products are not designed or intended for use as critical components in life support systems, equipment used in hazardous environments, or nuclear control systems.
TECHNICAL REVISIONS - The appearance of products, including safety agency certifications pictured on labels, may change depending on the date manufactured. Specifications are subject to change without notice.

