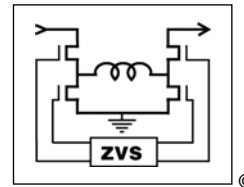


PRM™ Regulator

- 24 V input V•I Chip™ PRM
- Vin range 18 – 36 Vdc
- High density – 407 W/in³
- Small footprint – 103 W/in²
- Low weight – 0.5 oz (15 g)
- Adaptive Loop feedback
- ZVS buck-boost regulator
- 1.33 MHz switching frequency
- 95% efficiency
- 125°C operation (Tj)



Vin = 18 – 36 V
Vf = 26 – 55 V
Pf = 120 W
If = 2.5 A



Product Description

The V•I Chip regulator is a very efficient non-isolated regulator capable of both boosting and bucking a wide range input voltage. It is specifically designed to provide a controlled Factorized Bus distribution voltage for powering downstream VTM™ Transformer — fast, efficient, isolated low noise Point-of-Load (POL) converters. In combination, PRMs and VTMs™ form a complete DC-DC converter subsystem offering all of the unique benefits of Vicor's Factorized Power Architecture™ (FPA)™: high density and efficiency; low noise operation; architectural flexibility; extremely fast transient response; and elimination of bulk capacitance at the Point-of-Load (POL).

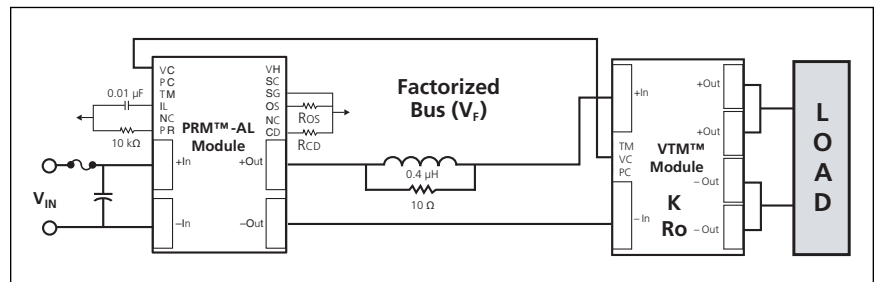
In FPA systems, the POL voltage is the product of the Factorized Bus voltage delivered by a PRM and the "K-factor" (the fixed voltage transformation ratio) of a downstream VTM. The PRM controls the Factorized Bus voltage to provide regulation at the POL. Because VTMs perform true voltage division and current multiplication, the Factorized Bus voltage may be set to a value that is substantially higher than the bus voltages typically found in "intermediate bus" systems, reducing distribution losses and enabling use of narrower distribution bus traces. A PRM-VTM chip set can provide up to 100 A, or 115 W, at a FPA system density of 169 A/in³, or 195 W/in³ — and because the PRM can be located, or "factorized," remotely from the POL, these power densities can effectively be doubled.

The PRM described in this data sheet features a unique "Adaptive Loop" compensation feedback: a single wire alternative to traditional remote sensing and feedback loops that enables precise control of an isolated POL voltage without the need for either a direct connection to the load or for noise sensitive, bandwidth limiting, isolation devices in the feedback path.

Absolute Maximum Ratings

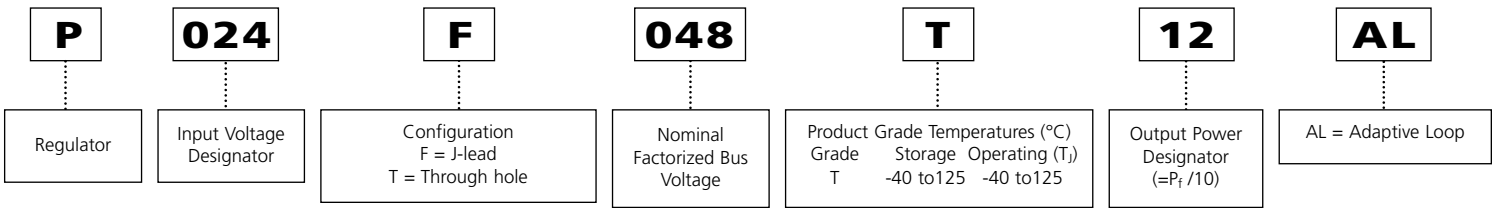
| Parameter | Values | Unit | Notes |
|--------------------------------|--------------|------|---------|
| +In to -In | -1.0 to 60.0 | Vdc | |
| PC to -In | -0.3 to 6.0 | Vdc | |
| PR to -In | -0.3 to 9.0 | Vdc | |
| IL to -In | -0.3 to 6.0 | Vdc | |
| VC to -In | -0.3 to 18.0 | Vdc | |
| +Out to -Out | -0.3 to 59 | Vdc | |
| SC to -Out | -0.3 to 3.0 | Vdc | |
| VH to -Out | -0.3 to 9.5 | Vdc | |
| OS to -Out | -0.3 to 9.0 | Vdc | |
| CD to -Out | -0.3 to 9.0 | Vdc | |
| SG to -Out | 100 | mA | |
| Continuous output current | 2.5 | Adc | |
| Continuous output power | 120 | W | |
| Case temperature during reflow | 225 | °C | MSL 5 |
| | 245 | °C | MSL 6 |
| Operating junction temperature | -40 to 125 | °C | T-Grade |
| Storage temperature | -40 to 125 | °C | T-Grade |

DC-DC Converter



The P024F048T12AL is used with any 048 input series VTM to provide a regulated and isolated output.

Part Numbering



Overview of Adaptive Loop Compensation

Adaptive Loop compensation, illustrated in Figure 1, contributes to the bandwidth and speed advantage of Factorized Power. The PRM monitors its output current and automatically adjusts its output voltage to compensate for the voltage drop in the output resistance of the VTM. R_{OS} sets the desired value of VTM output voltage, V_{out}; R_{CD} is set to a value that compensates for the output resistance of the VTM (which, ideally, is located at the point of load). For selection of R_{OS} and R_{CD}, refer to Table 1 below or Page 9.

The V•I Chip’s bi-directional VC port :

1. Provides a wake up signal from the PRM to the VTM that synchronizes the rise of the VTM output voltage to that of the PRM.
2. Provides feedback from the VTM to the PRM to enable the PRM to compensate for the voltage drop in VTM output resistance, R_O.

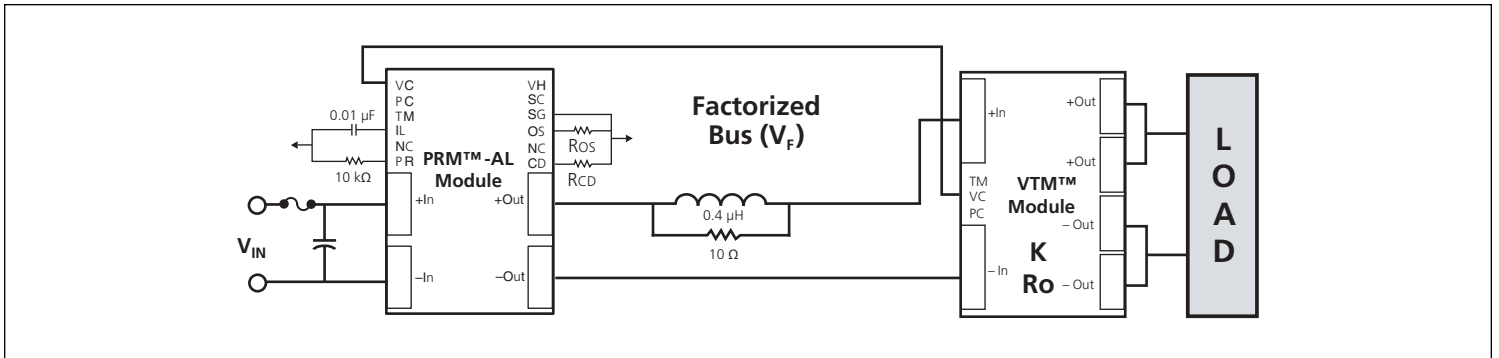


Figure 1 — With Adaptive Loop control the output of the VTM is regulated over the load current range with only a single interconnect between the PRM and VTM and without the need for isolation in the feedback path.

| Desired Load Voltage (Vdc) | VTM P/N ⁽¹⁾ | Max VTM Output Current (A) ⁽²⁾ | R _{OS} (kΩ) ⁽³⁾ | R _{CD} (Ω) ⁽³⁾ |
|----------------------------|------------------------|---|-------------------------------------|------------------------------------|
| 1.0 | V048F015T100 | 100 | 3.57 | 26.1 |
| 1.2 | V048F015T100 | 100 | 2.94 | 32.4 |
| 1.5 | V048F015T100 | 100 | 2.37 | 39.2 |
| 1.8 | V048F020T080 | 80 | 2.61 | 35.7 |
| 2.0 | V048F020T080 | 80 | 2.37 | 39.2 |
| 3.0 | V048F030T070 | 70 | 2.37 | 39.2 |
| 3.3 | V048F040T050 | 50 | 2.89 | 32.6 |
| 5.0 | V048F060T040 | 40 | 2.87 | 33.2 |
| 8.0 | V048F080T030 | 30 | 2.37 | 32.9 |
| 9.6 | V048F096T025 | 25 | 2.37 | 32.9 |
| 10 | V048F120T025 | 25 | 2.86 | 32.9 |
| 12 | V048F120T025 | 25 | 2.37 | 39.2 |
| 15 | V048F160T015 | 15 | 2.49 | 37.4 |
| 24 | V048F240T012 | 12.5 | 2.37 | 39.2 |
| 28 | V048F320T009 | 9.4 | 2.74 | 35.7 |
| 36 | V048F480T006 | 6.3 | 3.16 | 30.1 |
| 48 | V048F480T006 | 6.3 | 2.37 | 39.2 |

Note:
 (1) See Table 2 on page 9 for nominal V_{out} range and K factors.
 (2) See “PRM output power vs. VTM output power” on Page 10
 (3) 1% precision resistors recommended

Table 1 — Configure your Chip Set using the PRM-AL

Input Specs (Conditions are at 24 Vin, 48 Vf, full load, and 25°C ambient unless otherwise specified)

| Parameter | Min | Typ | Max | Unit | Note |
|--|------|-------|------|--------|--|
| Input voltage range | 18 | 24 | 36 | Vdc | |
| Input dV/dt | | | 1 | V/μs | |
| Input undervoltage turn-on | | 15.8 | 16.5 | Vdc | Increases as temp. increases to 17.3 max |
| Input undervoltage turn-off | 13.5 | 14.1 | | Vdc | |
| Input overvoltage turn-on | 36.3 | 37.1 | | Vdc | |
| Input overvoltage turn-off | | 37.8 | 38.9 | Vdc | |
| Input quiescent current | | 0.5 | 1 | mA | PC low |
| Input current | | 5.2 | | Adc | |
| Input reflected ripple current | | 284 | | mA p-p | See Figures 4 & 5 |
| No load power dissipation | | 3.82 | 7.65 | W | |
| Internal input capacitance | | 5 | | μF | Ceramic |
| Recommended external input capacitance | | 1,000 | | μF | See Figure 5 for input filter circuit. Source impedance dependent |

Input Waveforms

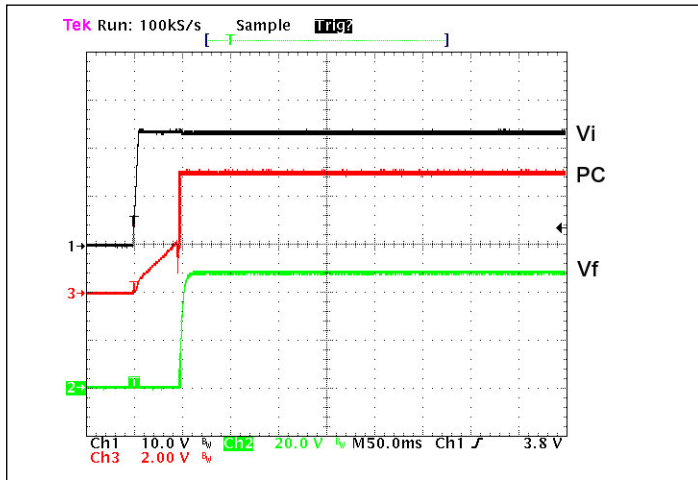


Figure 2 — Vf and PC response from power up

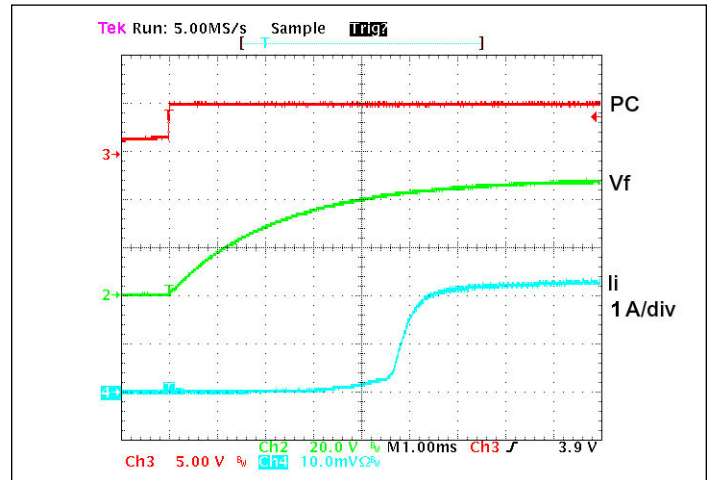


Figure 3 — Vf turn-on waveform with inrush current – PC enabled electronic load set constant R

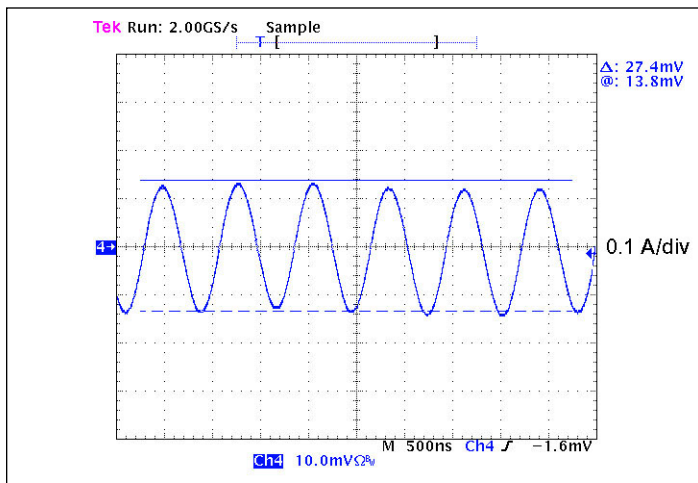


Figure 4 — Input reflected ripple current

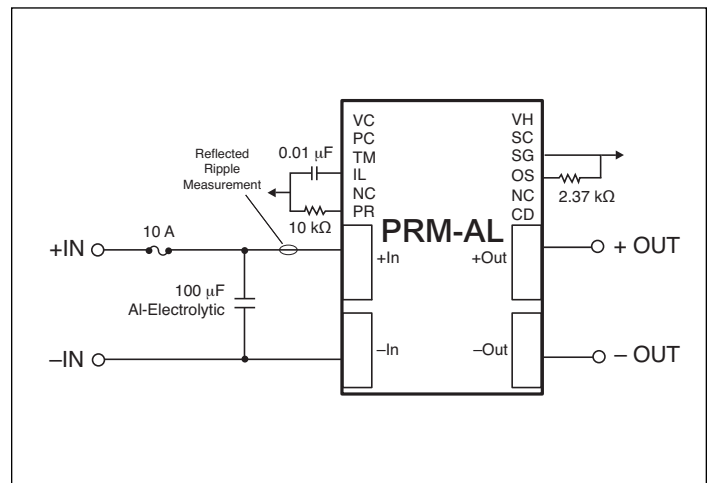


Figure 5 — Input filter capacitor recommendation

Output Specs (Conditions are at 24 V_{in}, 48 V_f, full load, and 25°C ambient unless otherwise specified)

| Parameter | Min | Typ | Max | Unit | Note |
|---------------------------------|------|------|------|------|---|
| Output voltage range | 26 | 48 | 55 | Vdc | Factorized Bus voltage (V _f) set by R _{OS} |
| Output power | 0 | | 120 | W | |
| Output current | 0 | | 2.5 | Adc | |
| DC current limit | 2.6 | 3.0 | 3.3 | Adc | I _L pin floating |
| Average short circuit current | | | 0.5 | A | Auto recovery |
| Set point accuracy | | 1.5 | | % | |
| Line regulation | | 0.1 | 0.2 | % | Low line to high line |
| Load regulation | | 0.1 | 0.2 | % | No CD resistor |
| Load regulation (at VTM output) | | 1.0 | 2.0 | % | Adaptive Loop |
| Current share accuracy | | 5 | 10 | % | |
| Efficiency | | | | | |
| Full load | | 95 | | % | See Figure 6,7 & 8 |
| Output overvoltage set point | 56 | | 59.4 | Vdc | |
| Output ripple voltage | | | | | |
| No external bypass | | 1.0 | 2.0 | % | Factorized Bus, see Figure 13 |
| With 10 μF capacitor | | 0.5 | 1.0 | % | Factorized Bus, see Figure 14 |
| Switching frequency | 1.24 | 1.33 | 1.45 | MHz | Fixed frequency |
| Output turn-on delay | | | | | |
| From application of power | | 55 | 105 | ms | See Figure 2 |
| From PC pin high | | 100 | | μs | See Figure 3, consult Applications Engineering if powering loads other than VTMs. |
| Internal output capacitance | | 5 | | μF | Ceramic |
| Factorized Bus capacitance | | | 47 | μF | |

Efficiency Graphs

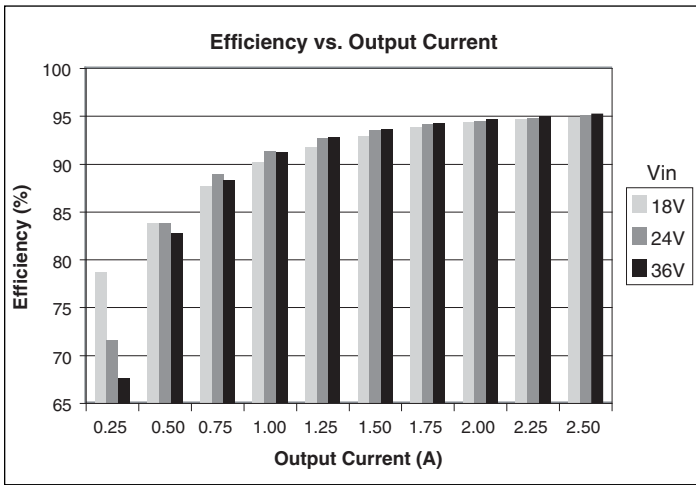


Figure 6 — Efficiency vs. output current at 48 Vf

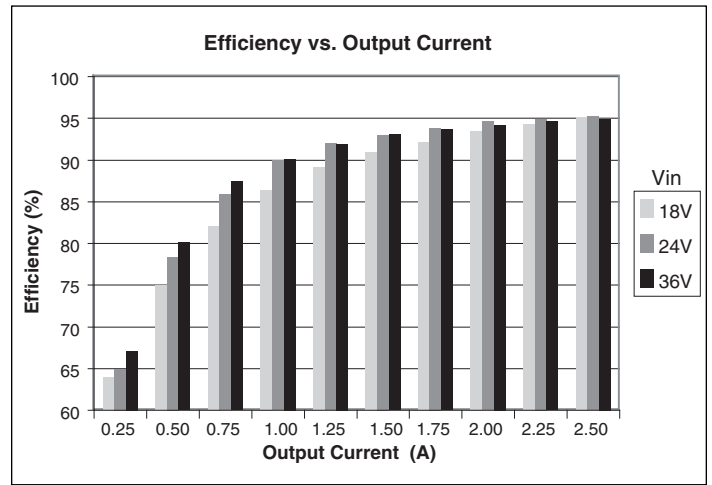


Figure 7 — Efficiency vs. output current at 36 Vf

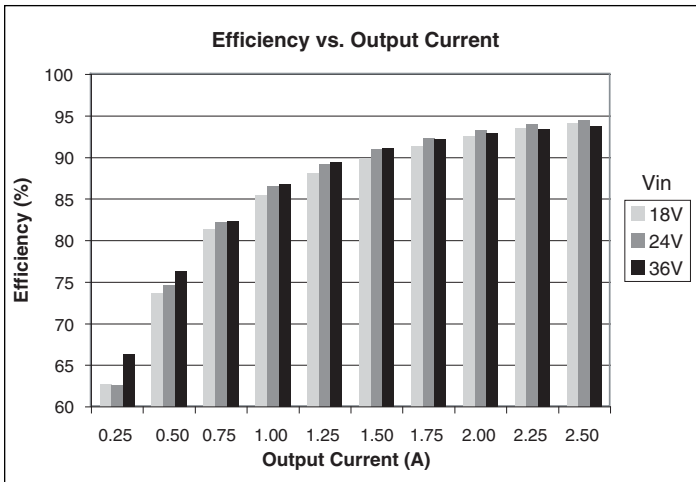


Figure 8 — Efficiency vs. output current at 26 Vf

Output Waveforms

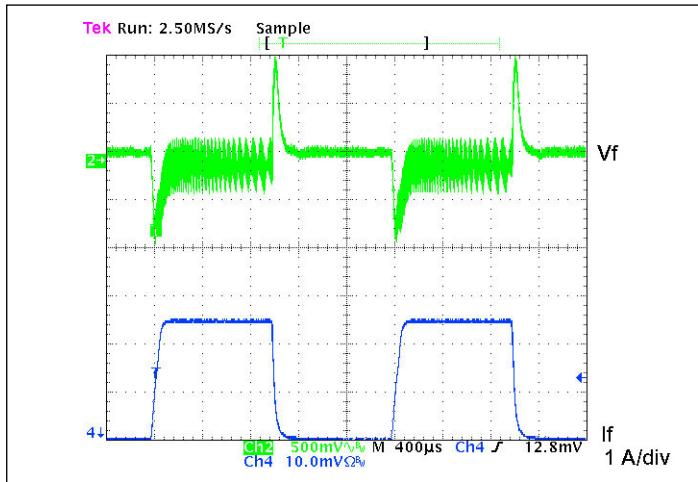


Figure 9 — Transient response; PRM alone 24 Vin, 0–2.5–0 A no load capacitance, local loop

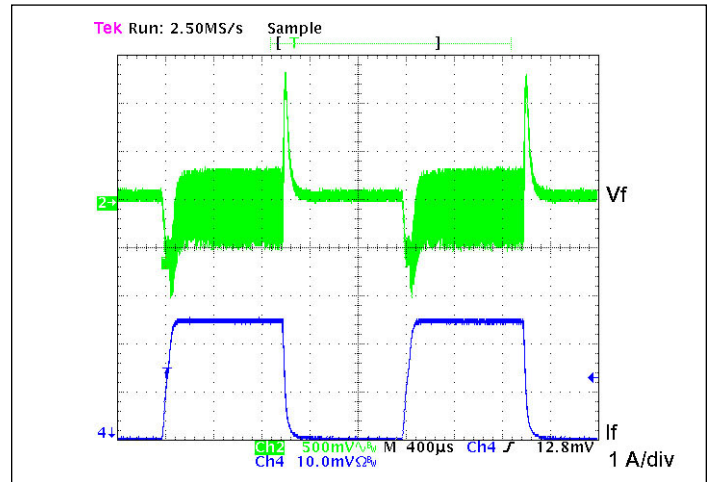


Figure 10 — Transient response; PRM alone, 18 Vin, 0–2.5–0 A no load capacitance, local loop

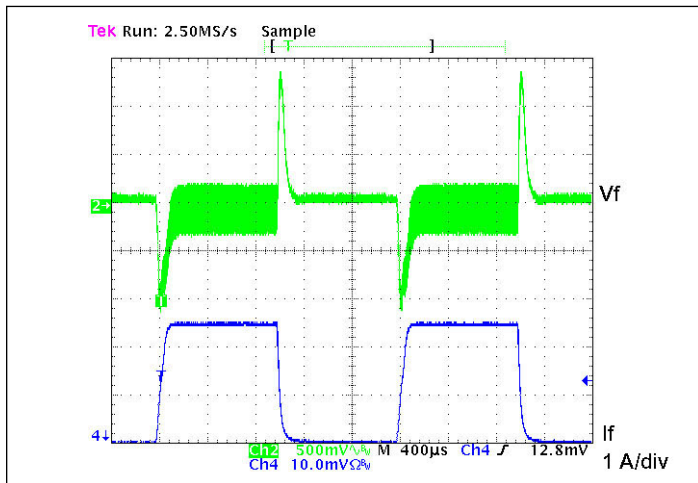


Figure 11 — Transient response; PRM alone 36 Vin, 0–2.5–0 A no load capacitance, local loop

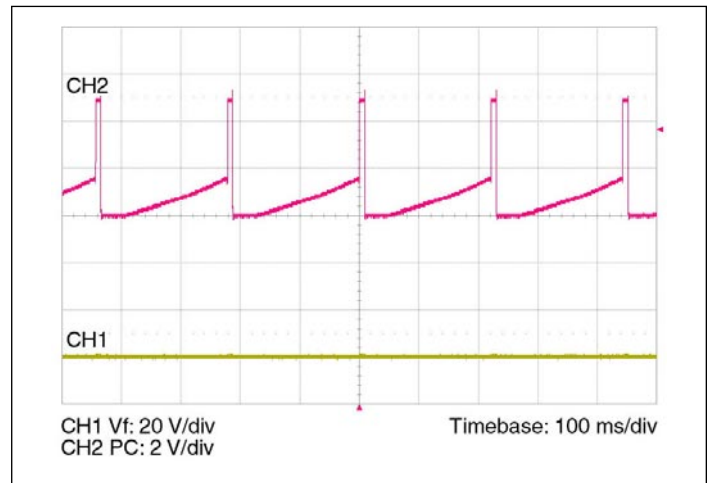


Figure 12 — PC during fault – frequency will vary as a function of line voltage

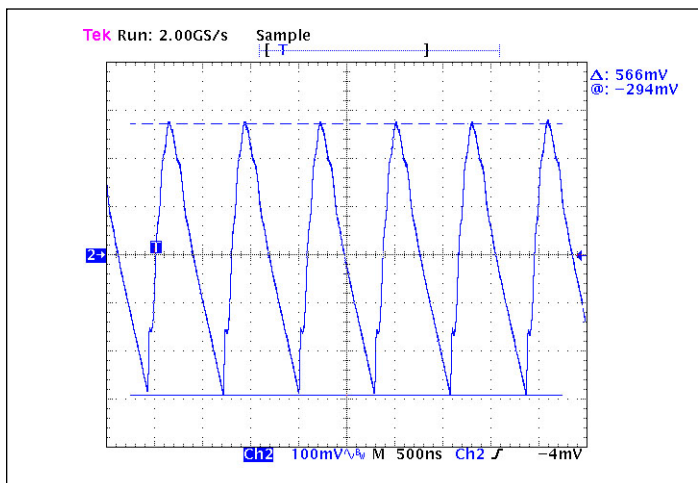


Figure 13 — Output ripple full load no bypass capacitance

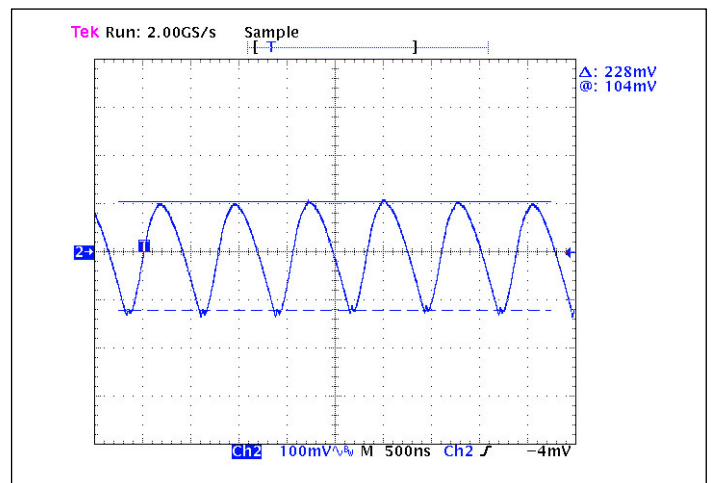


Figure 14 — Output ripple full load 10 µF bypass capacitance

Auxiliary Pins (Conditions are at 24 Vin, 48 Vf, full load, and 25°C ambient unless otherwise specified)

| Parameter | Min | Typ | Max | Unit | Note |
|---------------------------|------|-------|------|------|---|
| VC (VTM Control) | | | | | |
| Pulse width | 8 | 12 | 18 | ms | |
| Peak voltage | 12 | 14 | 18 | V | Referenced to –Out |
| PC (Primary Control) | | | | | |
| DC voltage | 4.8 | 5.0 | 5.2 | Vdc | Referenced to –In |
| Module disable voltage | 2.3 | 2.4 | | Vdc | Referenced to –In |
| Module enable voltage | | 2.5 | 2.6 | Vdc | |
| Disable hysteresis | | 100 | | mV | |
| Current limit | | 1.75 | 1.90 | mA | Source only after start up; not to be used for aux. supply; 100 kΩ minimum load impedance to assure start up. |
| Enable delay time | | 100 | | μs | |
| Disable delay time | | 1 | | μs | |
| IL (Current Limit Adjust) | | | | | |
| Voltage | 0.95 | 1 | 1.05 | V | |
| Accuracy | | ± 15 | | % | Based on DC current limit set point |
| PR (Parallel Port) | | | | | |
| Voltage | 1.5 | | 3 | V | Referenced to SG; See description Page 8 |
| Source current | 1 | | | mA | |
| External capacitance | | | 100 | pF | |
| VH (Auxiliary Voltage) | | | | | |
| Range | 8.7 | 9.0 | 9.3 | Vdc | Typical internal bypass C=0.1 μF Maximum external C=0.1 μF, referenced to SG |
| Regulation | | 0.04 | | %/mA | |
| Current | | | 5 | mA p | |
| SC (Secondary Control) | | | | | |
| Voltage | 1.23 | 1.24 | 1.25 | Vdc | Referenced to SG |
| Internal capacitance | | 0.22 | | μF | |
| External capacitance | | | 0.7 | μF | |
| OS (Output Set) | | | | | |
| Set point accuracy | | ± 1.5 | | % | Includes 1% external resistor |
| Reference offset | | ± 4 | | mV | |
| CD (Compensation Device) | | | | | |
| External resistance | 20 | | | Ω | Omit resistor for regulation at output of PRM |

General Specs

| Parameter | Min | Typ | Max | Unit | Note |
|---|-----|------------|-----|--------|--|
| MTBF | | | | | |
| MIL-HDBK-217F | | 2.2 | | Mhrs | 25°C, GB |
| Agency approvals | | cTUVus | | | UL/CSA 60950-1, EN60950-1 |
| | | | | | CE Marked for Low Voltage Directive and RoHS Recast Directive, as applicable |
| Mechanical parameters | | | | | |
| Weight | | 0.53 / 15 | | oz / g | See Mechanical Drawings, Figures 19 – 22 |
| Dimensions | | | | | |
| Length | | 1.28/32,5 | | in/mm | |
| Width | | 0.87/22,0 | | in/mm | |
| Height | | 0.265/6,73 | | in/mm | |
| Thermal | | | | | |
| Over temperature shutdown | 130 | 135 | 140 | °C | Junction temperature |
| Thermal capacity | | 9.3 | | Ws/°C | |
| Junction-to-case thermal impedance (R _{θJC}) | | 1.1 | | °C/W | |
| Junction-to-board thermal impedance (R _{θJB}) | | 2.1 | | °C/W | |
| Case-to-ambient | | 3.7 | | °C/W | With 0.25" heat sink @ 300 LFM |

+In / -In DC Voltage Ports

The V•I Chip maximum input voltage should not be exceeded. PRMs have internal over / undervoltage lockout functions that prevent operation outside of the specified input range. PRMs will turn on when the input voltage rises above its undervoltage lockout. If the input voltage exceeds the overvoltage lockout, PRMs will shut down until the overvoltage fault clears. PC will toggle indicating an out of bounds condition.

+Out / -Out Factorized Voltage Output Ports

These ports provide the Factorized Bus voltage output. The –Out port is connected internally to the –In port through a current sense resistor. The PRM has a maximum power and a maximum current rating and is protected if either rating is exceeded. Do not short –Out to –In.

VC – VTM Control

The VTM Control (VC) port supplies an initial V_{CC} voltage to downstream VTMs, enabling the VTMs and synchronizing the rise of the VTM output voltage to that of the PRM. The VC port also provides feedback to the PRM to compensate for voltage drop due to the VTM output resistance. The PRM's VC port should be connected to the VTM VC port. A PRM VC port can drive a maximum of two (2) VTM VC ports.

PC – Primary Control

The PRM voltage output is enabled when the PC pin is open circuit (floating). To disable the PRM output voltage, the PC pin is pulled low. Open collector optocouplers, transistors, or relays can be used to control the PC pin. When using multiple PRMs in a high power array, the PC ports must be tied together to synchronize their turn on. During an abnormal condition the PC pin will pulse (Fig.12) as the PRM initiates a restart cycle. This will continue until the abnormal condition is rectified. The PC should not be used as an auxiliary voltage supply, nor should it be switched at a rate greater than 1 Hz.

TM – Factory Use Only**IL – Current Limit Adjust**

The PRM has a preset, maximum, current limit set point. The IL port may be used to reduce the current limit set point to a lower value. See "Adjusting Current Limits" on page 10.

PR – Parallel Port

The PR port signal, which is proportional to the PRM output power, supports current sharing of two PRMs. To enable current sharing, PR ports should be interconnected. Steps should be taken to minimize coupling noise into the interconnecting bus. Terminate this port with a 10 k equivalent resistance to SG, e.g. 10 k for a single PRM, 20 k each for 2 PRMs in parallel, 30 k each for 3 PRMs in parallel etc.. Please consult Vicor Applications Engineering regarding additional considerations when paralleling more than two PRMs.

VH – Auxiliary Voltage

VH is a gated (e.g. mirrors PC), non-isolated, nominally 9 Volt, regulated DC voltage (see "Auxiliary Pins" specifications, on Page 7) that is referenced to SG. VH may be used to power external circuitry having a total current consumption of no more than 5 mA under either transient or steady state conditions including turn-on.

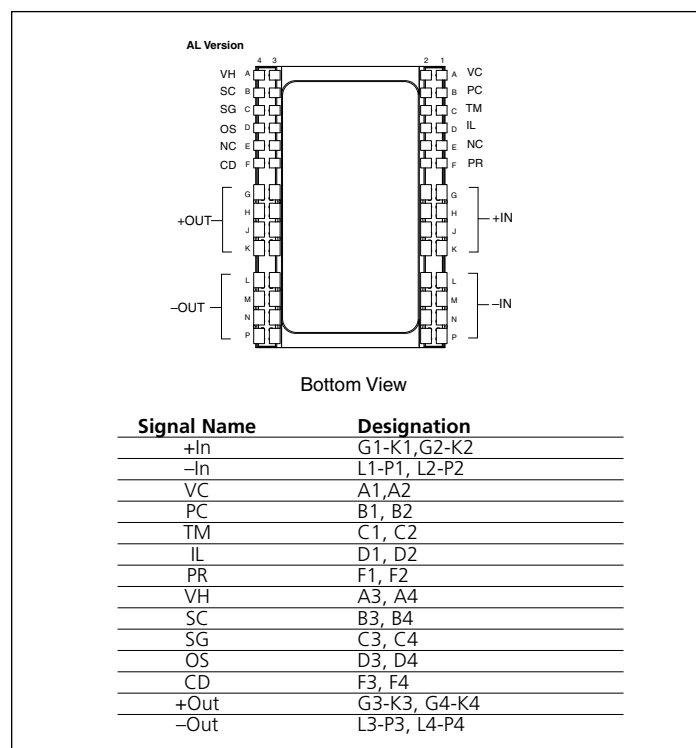


Figure 15 — PRM pin configuration

SC – Secondary Control

The load voltage may be controlled by connecting a resistor or voltage source to the SC port referenced to SG. The slew rate of the output voltage may be controlled by controlling the rate-of-rise of the voltage at the SC port (e.g., to limit inrush current into a capacitive load).

SG – Signal Ground

This port provides a low inductance Kelvin connection to –In and should be used as reference for the OS, CD, SC, VH and IL ports.

OS – Output Set

The application-specific value of the Factorized Bus voltage (V_f) is set by connecting a resistor between OS and SG. Resistor value selection is shown in Table 1 on Page 2, and described on Page 9. If no resistor is connected, the PRM output will be approximately one volt. If set resistor is not collocated with the PRM, a local bypass capacitor of ~200 pF may be required.

CD – Compensation Device

Adaptive Loop control is configured by connecting an external resistor between the CD port and SG. Selection of an appropriate resistor value (see Equation 2 on Page 9 and Table 1 on Page 2) configures the PRM to compensate for voltage drops in the equivalent output resistance of the VTM and the PRM-VTM distribution bus. If no resistor is connected to CD, the PRM will be in Local Loop mode and will regulate the +Out/–Out voltage to a fixed value.

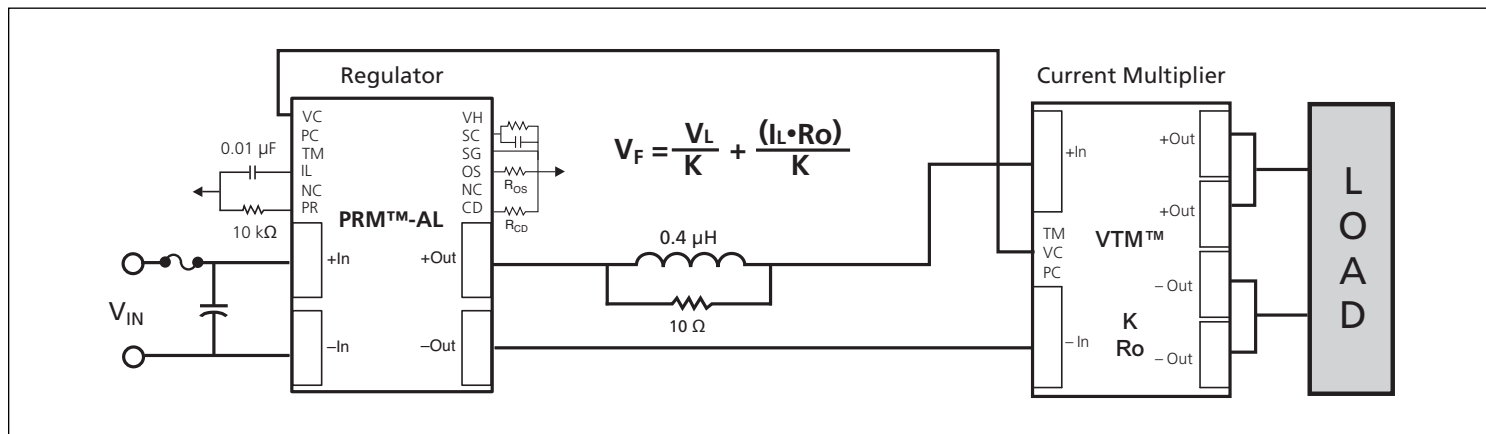


Figure 16 — Adaptive Loop compensation with soft start using the SC port.

Output Voltage Setting with Adaptive Loop

The equations for calculating R_{OS} and R_{CD} to set a VTM output voltage are:

$$R_{OS} = \frac{93100}{\left(\frac{V_L \cdot 0.8395}{K}\right) - 1} \quad (1)$$

$$R_{CD} = \frac{91238}{R_{OS}} + 1 \quad (2)$$

V_L = Desired load voltage

V_{OUT} = VTM output voltage

K = VTM transformation ratio
(available from appropriate VTM data sheet)

V_f = PRM output voltage, the Factorized Bus (see Figure 16)

R_o = VTM output resistance
(available from appropriate VTM data sheet)

I_L = Load Current
(actual current delivered to the load)

Output Voltage Trimming (optional)

After setting the output voltage from the procedure above the output may be margined down (26 V_f min) by a resistor from SC-SCG using this formula:

$$R_d \Omega = \frac{10000 V_{fd}}{V_{fs} - V_{fd}}$$

Where V_{fd} is the desired factorized bus and V_{fs} is the set factorized bus.

A low voltage source can be applied to the SC port to margin the load voltage in proportion to the SC reference voltage.

An external capacitor can be added to the SC port as shown in Figure 16 to control the output voltage slew rate for soft start.

| Nominal Vout Range (Vdc) | VTM K Factor |
|--------------------------|--------------|
| 0.8 ↔ 1.6 | 1/32 |
| 1.1 ↔ 2.2 | 1/24 |
| 1.6 ↔ 3.3 | 1/16 |
| 2.2 ↔ 4.4 | 1/12 |
| 3.3 ↔ 6.6 | 1/8 |
| 4.3 ↔ 8.8 | 1/6 |
| 6.5 ↔ 13.4 | 1/4 |
| 8.7 ↔ 17.9 | 1/3 |
| 13.0 ↔ 26.9 | 1/2 |
| 17.4 ↔ 36.0 | 2/3 |
| 26.0 ↔ 54.0 | 1 |

Table 2 — 048 input series VTM K factor selection guide

OVP – Overvoltage Protection

The output Overvoltage Protection set point of the P024F048T12AL is factory preset for 56 V. If this threshold is exceeded the output shuts down and a restart sequence is initiated. If the condition that causes OVP is still present, the unit will again shut down. This cycle will be repeated until the fault condition is removed. The OVP set point may be set at the factory to meet unique high voltage requirements.

PRM Output Power Versus VTM Output Power

As shown in Figure 17 the P024F048T12AL is rated to deliver 2.5 A maximum, when it is delivering an output voltage in the range from 26 V to 48 V, and 120 W, maximum, when delivering an output voltage in the range from 48 V to 55 V. When configuring a PRM for use with a specific VTM, refer to the appropriate VTM data sheet. The VTM input power can be calculated by dividing the VTM output power by the VTM efficiency (available from the VTM data sheet). The input power required by the VTM should not exceed the output power rating of the PRM.

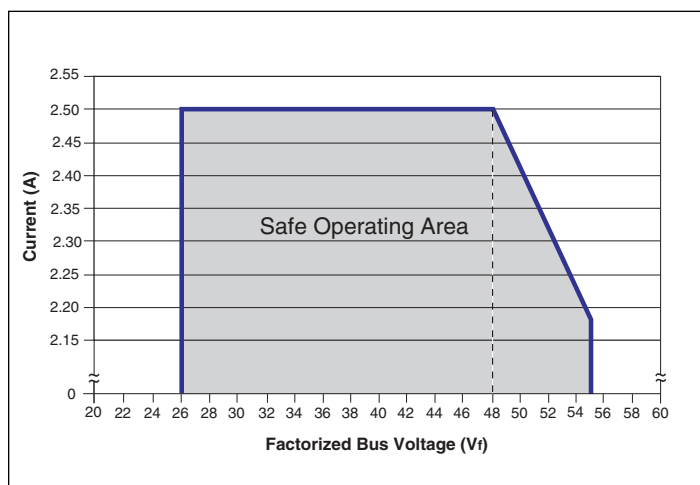


Figure 17 — P024F048T12AL rating based on Factorized Bus voltage

The Factorized Bus voltage should not exceed an absolute limit of 55 V, including steady state, ripple and transient conditions. Exceeding this limit may cause the internal OVP set point to be exceeded.

Parallel Considerations

The PR port is used to connect two PRMs in parallel to form a higher power array. When configuring arrays, PR port interconnection terminating impedance is 10 k to SG. See note Page 8 and refer to Application Note AN002. Additionally one PRM should be designated as the master while all other PRMs are set as slaves by shorting their SC pin to SG. The PC pins must be directly connected (no diodes) to assure a uniform start up sequence. Consult Vicor applications engineering for applications requiring more than two PRMs.

Adjusting Current Limit

The current limit can be lowered by placing an external resistor between the I_L and SG ports (see Figure 18 for resistor values). With the I_L port open-circuit, the current limit is preset to be within the range specified in the output specifications table on Page 4.

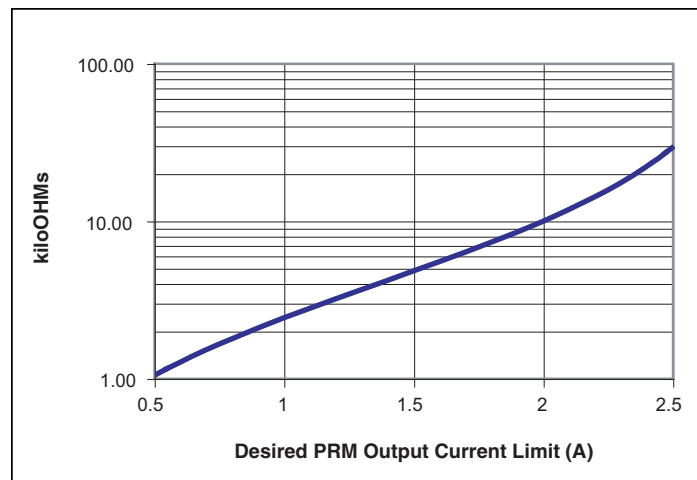


Figure 18 — External resistor value for adjusting current limit

Input Fuse Recommendations

A fuse should be incorporated at the input to the PRM, in series with the +In port. A fast acting fuse, NANO2 FUSE 451/453 Series 10 A 125 V, or equivalent, may be required to meet certain safety agency Conditions of Acceptability. Always ascertain and observe the safety, regulatory, or other agency specifications that apply to your specific application.

Product Safety Considerations

If the input of the PRM is connected to SELV or ELV circuits, the output of the PRM can be considered SELV or ELV respectively.

Application Notes

For PRM and V•I Chip application notes on soldering, board layout, and system design please click on the link below:

http://www.vicorpower.com/technical_library/application_information/chips/

Applications Assistance

Please contact Vicor Applications Engineering for assistance, 1-800-927-9474, or email at apps@vicorpower.com.

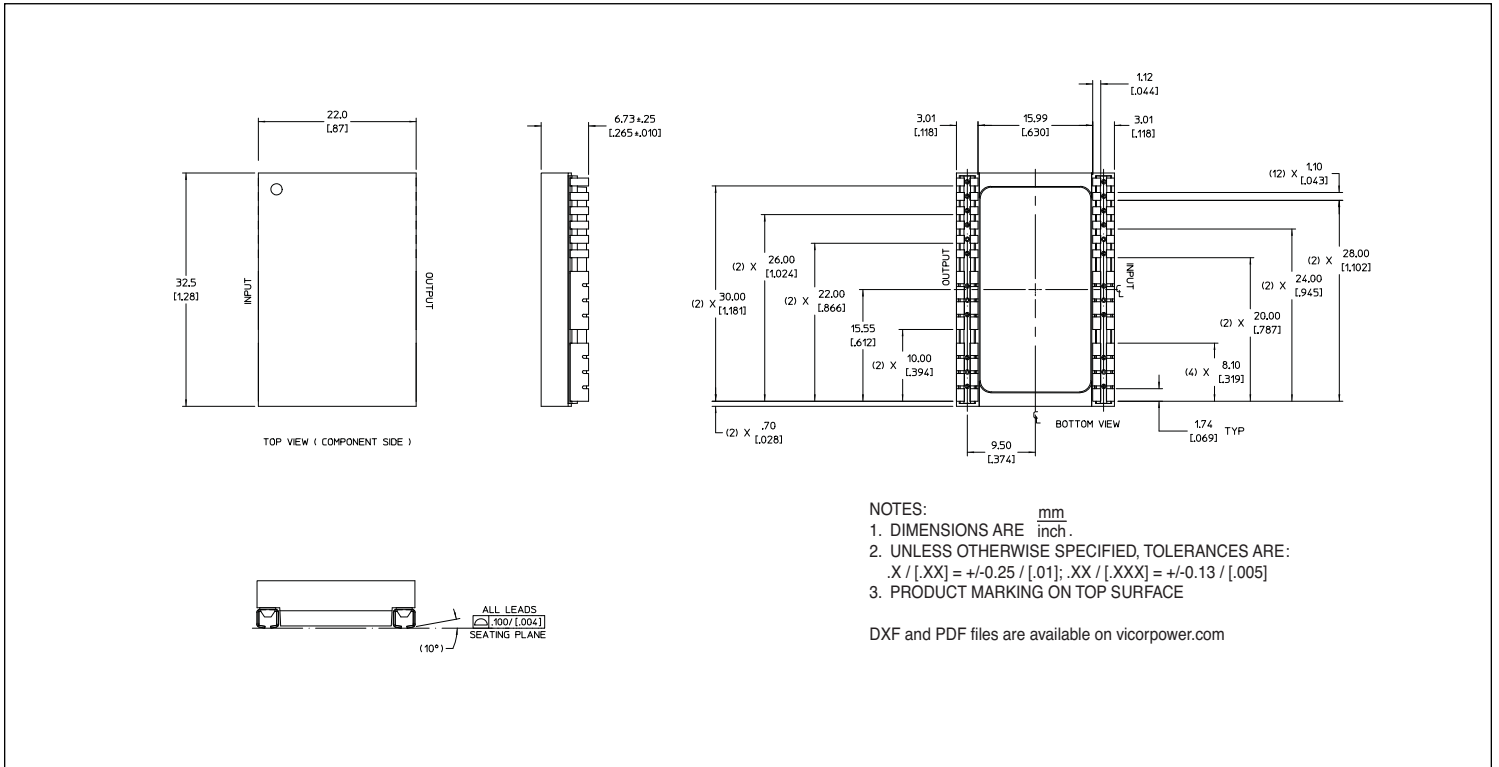


Figure 19 — PRM J-Lead mechanical outline; Onboard mounting

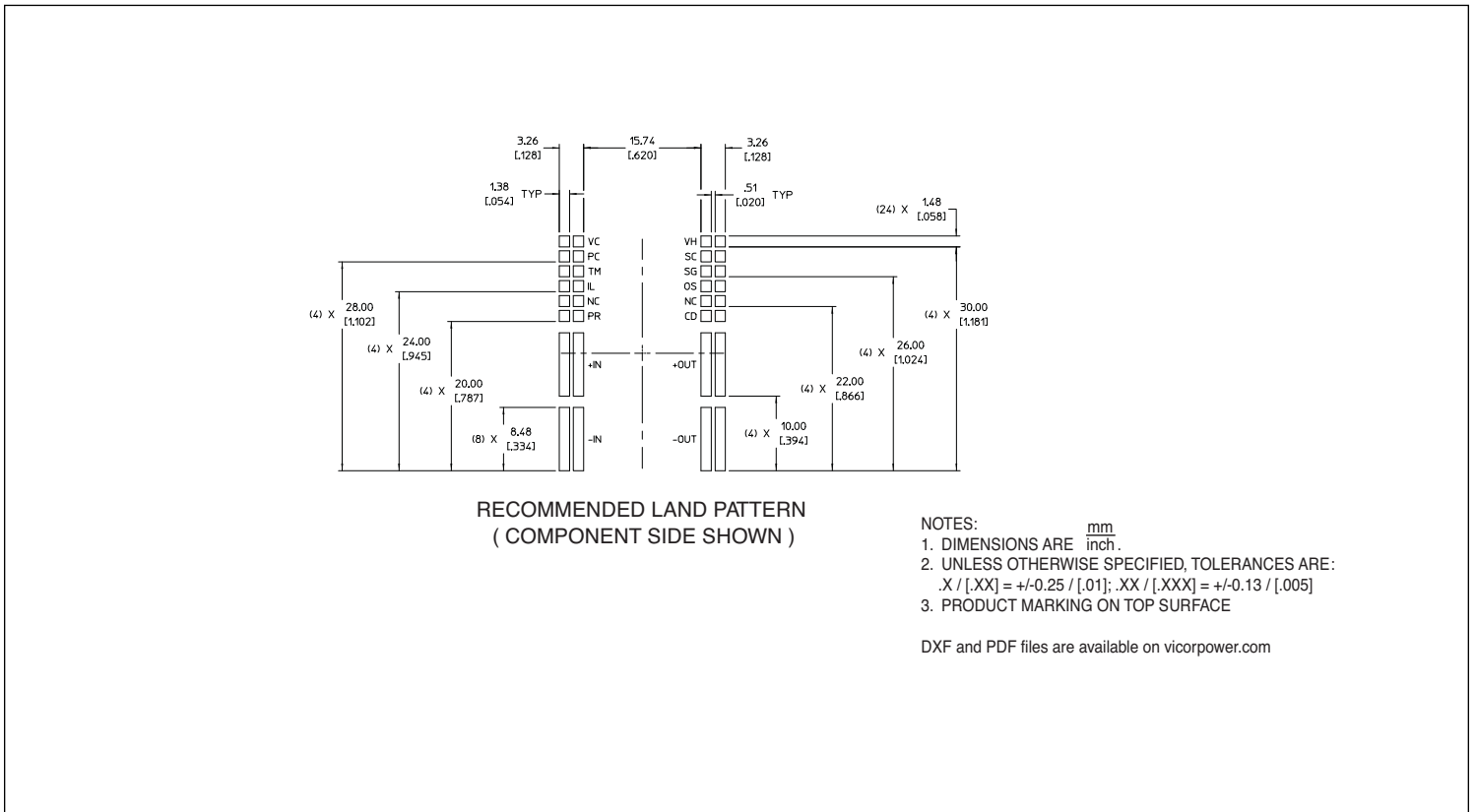


Figure 20 — PRM J-Lead PCB land layout information; Onboard mounting

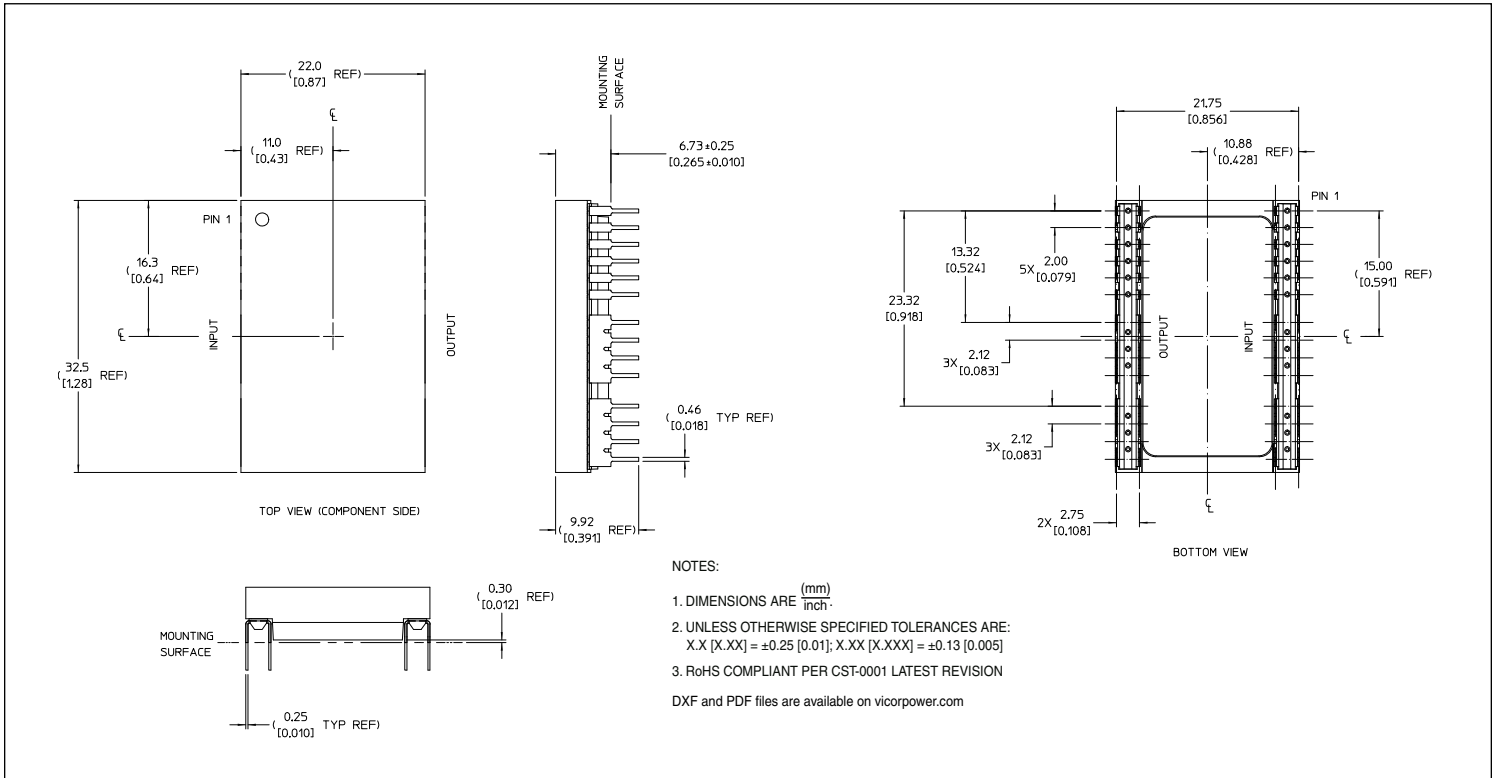


Figure 21 — PRM Through-hole mechanical outline

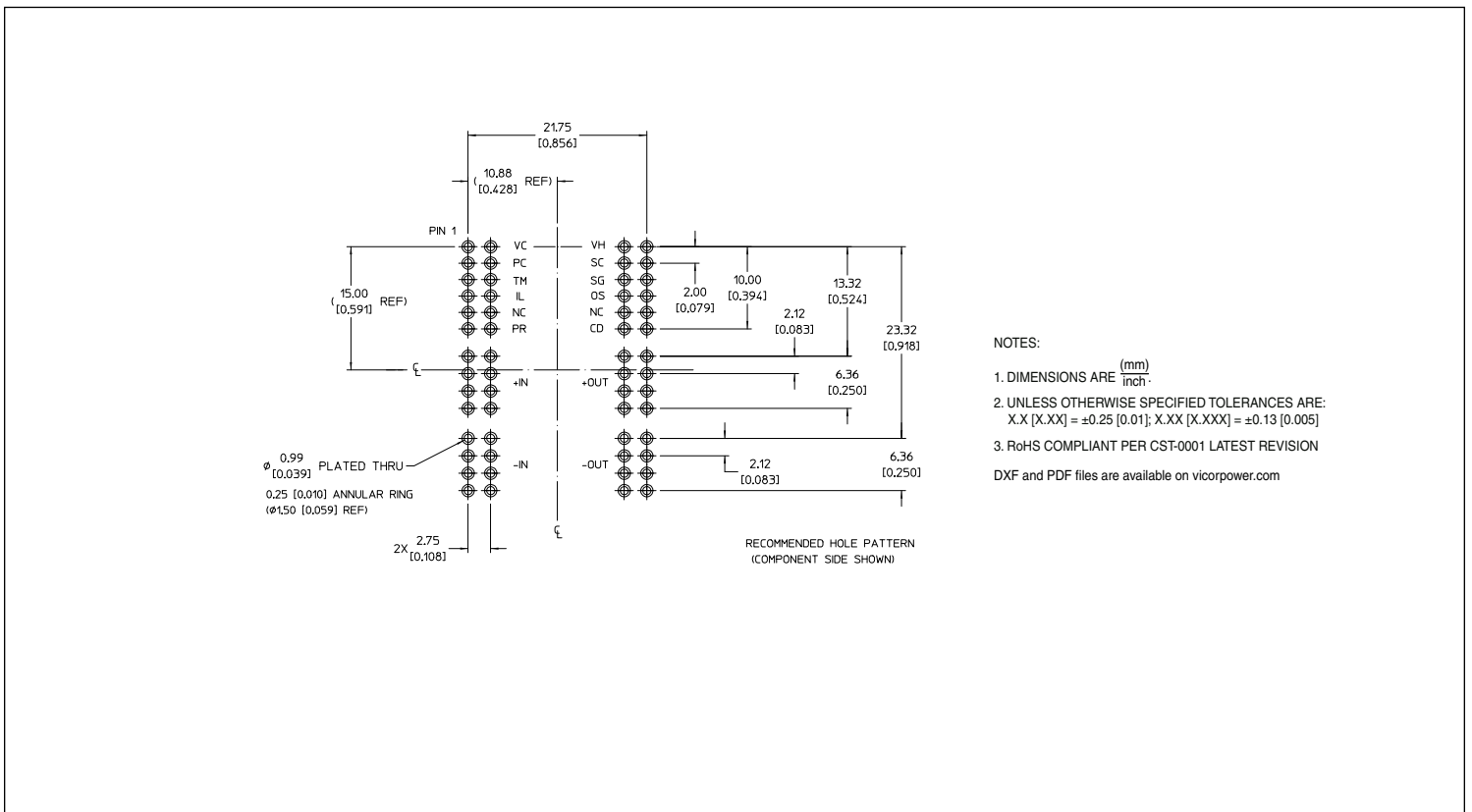


Figure 22 — PRM Through-hole PCB layout information

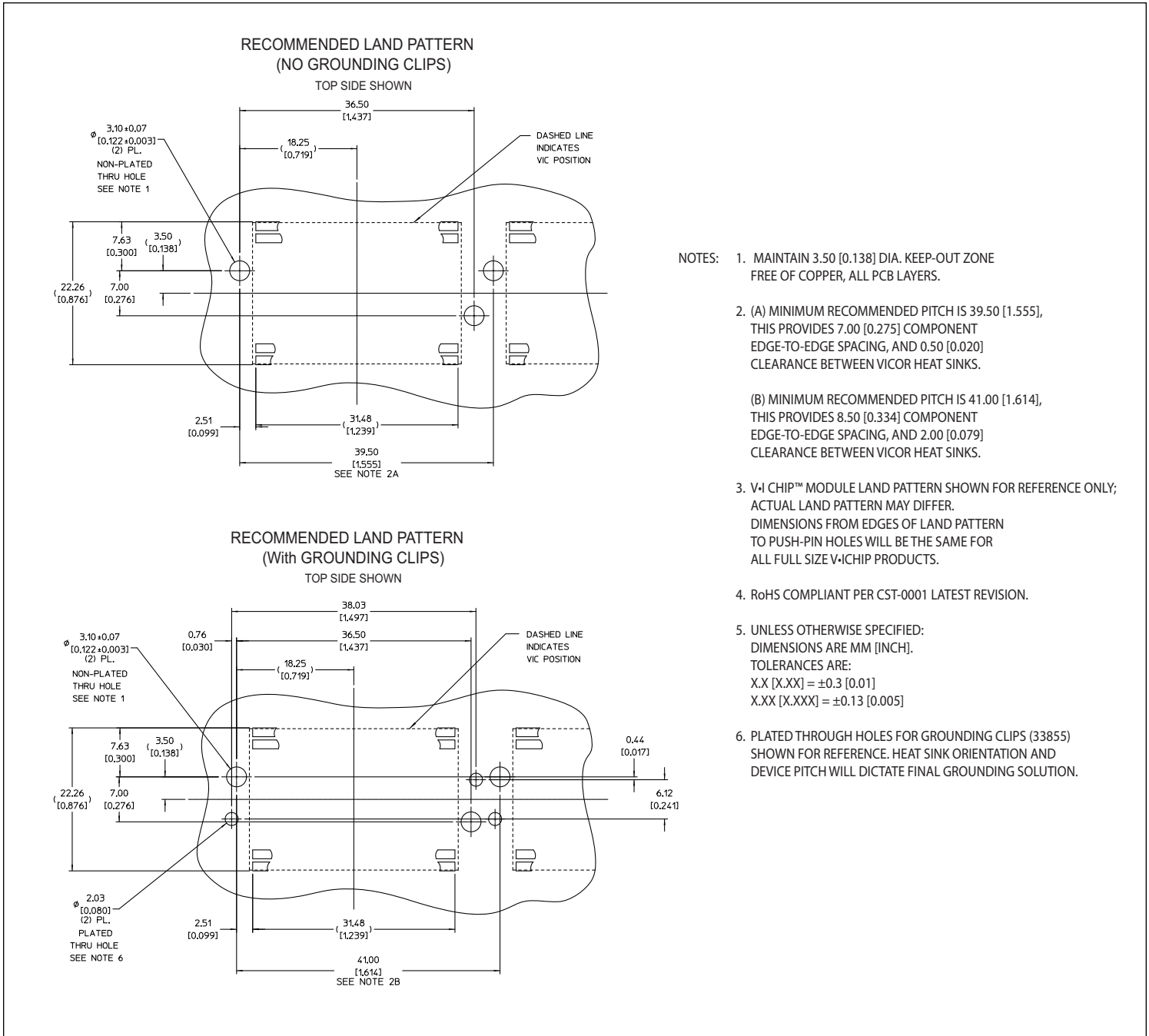


Figure 23 — Hole location for push pin heat sink relative to V•I Chip

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