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Renesas Electronics Corporation

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1. Overview

This MCU is built using the high-performance silicon gate CMOS process using a R8C/Tiny Series CPU core and is packaged in a 32-pin plastic molded LQFP. This MCU operates using sophisticated instructions featuring a high level of instruction efficiency. With 1M bytes of address space, it is capable of executing instructions at high speed.

1.1 Applications

Electric household appliance, office equipment, housing equipment (sensor, security), general industrial equipment, audio, etc.

1.2 Performance Overview

Table 1.1. lists the performance outline of this MCU.

Table 1.1 Performance outline

| Item | | Performance |
|-------------------------------|-------------------------------------|---|
| CPU | Number of basic instructions | 89 instructions |
| | Minimum instruction execution time | 50 ns ($f(X_{IN}) = 20$ MHz, $V_{CC} = 3.0$ to 5.5 V) 100 ns ($f(X_{IN}) = 10$ MHz, $V_{CC} = 2.7$ to 5.5 V) |
| | Operating mode | Single-chip |
| | Address space | 1M bytes |
| | Memory capacity | See Table 1.2. |
| Peripheral function | Port | Input/Output: 22 (including LED drive port), Input: 2 |
| | LED drive port | I/O port: 8 |
| | Timer | Timer X: 8 bits x 1 channel, Timer Y: 8 bits x 1 channel, Timer Z: 8 bits x 1 channel (Each timer equipped with 8-bit prescaler) Timer C: 16 bits x 1 channel (Circuits of input capture and output compare) |
| | Serial Interface | •1 channel Clock synchronous, UART •1 channel UART |
| | A/D converter | 10-bit A/D converter: 1 circuit, 12 channels |
| | Watchdog timer | 15 bits x 1 (with prescaler) |
| | Interrupt | Internal: 11 factors, External: 5 factors, Software: 4 factors, Priority level: 7 levels |
| | Clock generation circuit | 2 circuits •Main clock generation circuit (Equipped with a built-in feedback resistor) •On-chip oscillator (high speed, low speed) On High-speed on-chip oscillator the frequency adjustment function is usable. |
| | Oscillation stop detection function | Main clock oscillation stop detection function |
| | Voltage detection circuit | Included |
| | Power on reset circuit | Included |
| Electrical characteristics | Supply voltage | $V_{CC} = 3.0$ to 5.5 V ($f(X_{IN}) = 20$ MHz) $V_{CC} = 2.7$ to 5.5 V ($f(X_{IN}) = 10$ MHz) |
| | Power consumption | Typ. 9 mA ($V_{CC} = 5.0$ V, ($f(X_{IN}) = 20$ MHz) Typ. 5 mA ($V_{CC} = 3.0$ V, ($f(X_{IN}) = 10$ MHz) Typ. 35 μ A ($V_{CC} = 3.0$ V, Wait mode, Peripheral clock off) Typ. 0.7 μ A ($V_{CC} = 3.0$ V, Stop mode) |
| Flash memory | Program/erase supply voltage | $V_{CC} = 2.7$ to 5.5 V |
| | Program/erase endurance | 100 times |
| Operating ambient temperature | | -20 to 85 °C -40 to 85 °C (D-version) |
| Package | | 32-pin plastic mold LQFP |

1.3 Block Diagram

Figure 1.1 shows this MCU block diagram.

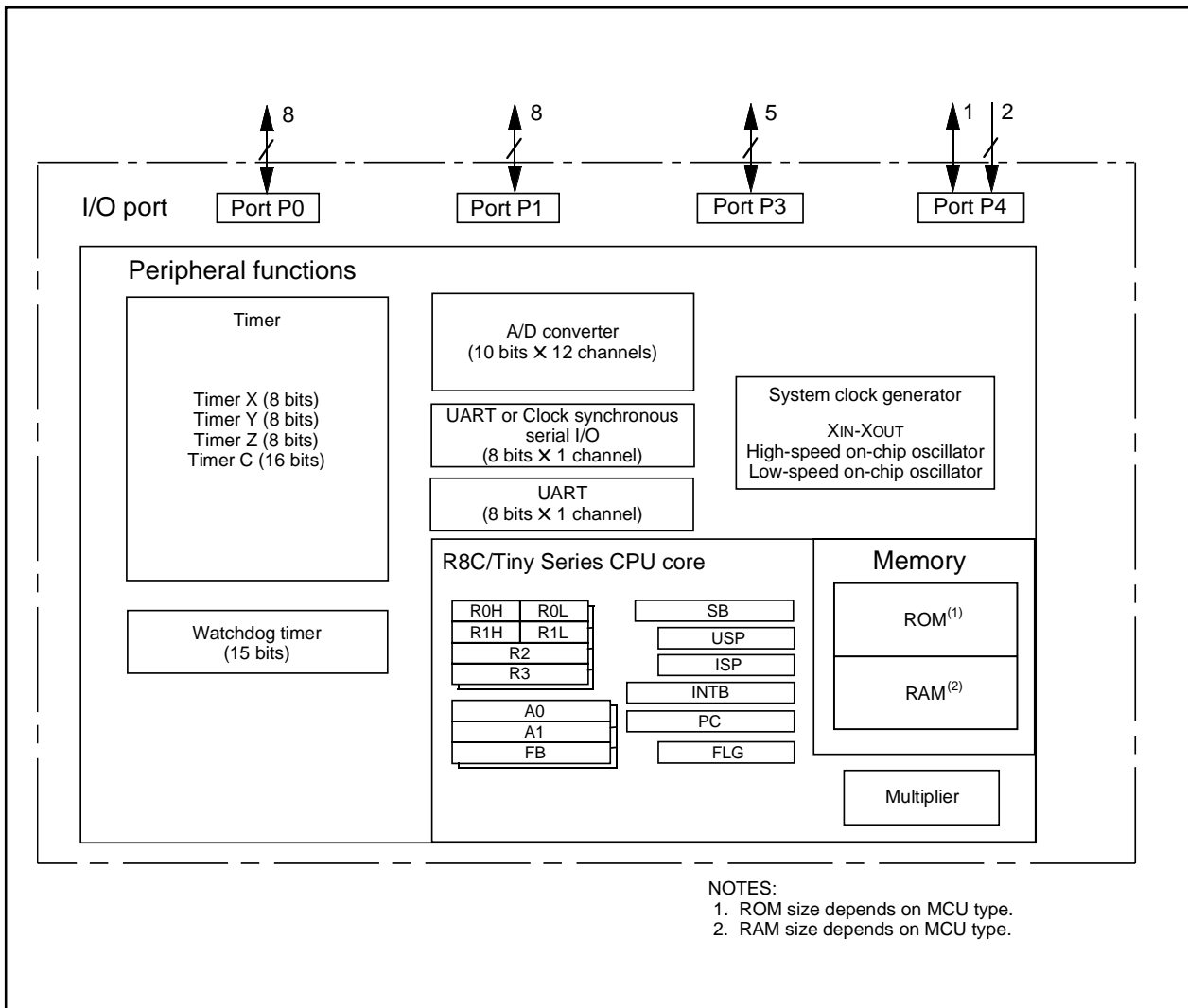


Figure 1.1 Block Diagram

1.4 Product Information

Table 1.2 lists the product information.

Table 1.2 Product Information

As of January 2006

| Type No. | ROM capacity | RAM capacity | Package type | Remarks |
|-------------|--------------|--------------|--------------|----------------------|
| R5F21112FP | 8K bytes | 512 bytes | PLQP0032GB-A | Flash memory version |
| R5F21113FP | 12K bytes | 768 bytes | PLQP0032GB-A | |
| R5F21114FP | 16K bytes | 1K bytes | PLQP0032GB-A | |
| R5F21112DFP | 8K bytes | 512 bytes | PLQP0032GB-A | D version |
| R5F21113DFP | 12K bytes | 768 bytes | PLQP0032GB-A | |
| R5F21114DFP | 16K bytes | 1K bytes | PLQP0032GB-A | |

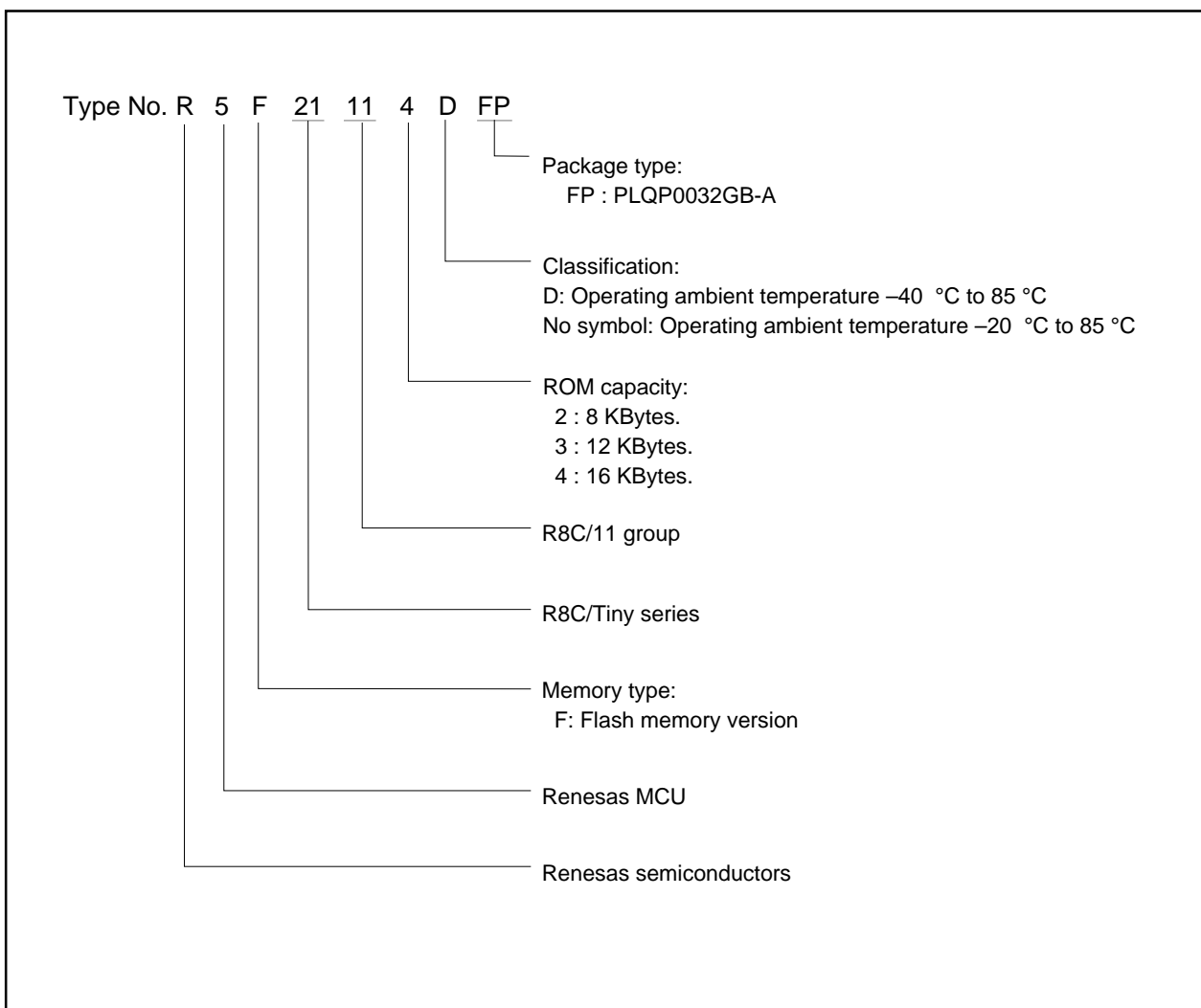


Figure 1.2 Type No., Memory Size, and Package

1.5 Pin Assignments

Figure 1.3 shows the pin configuration (top view).

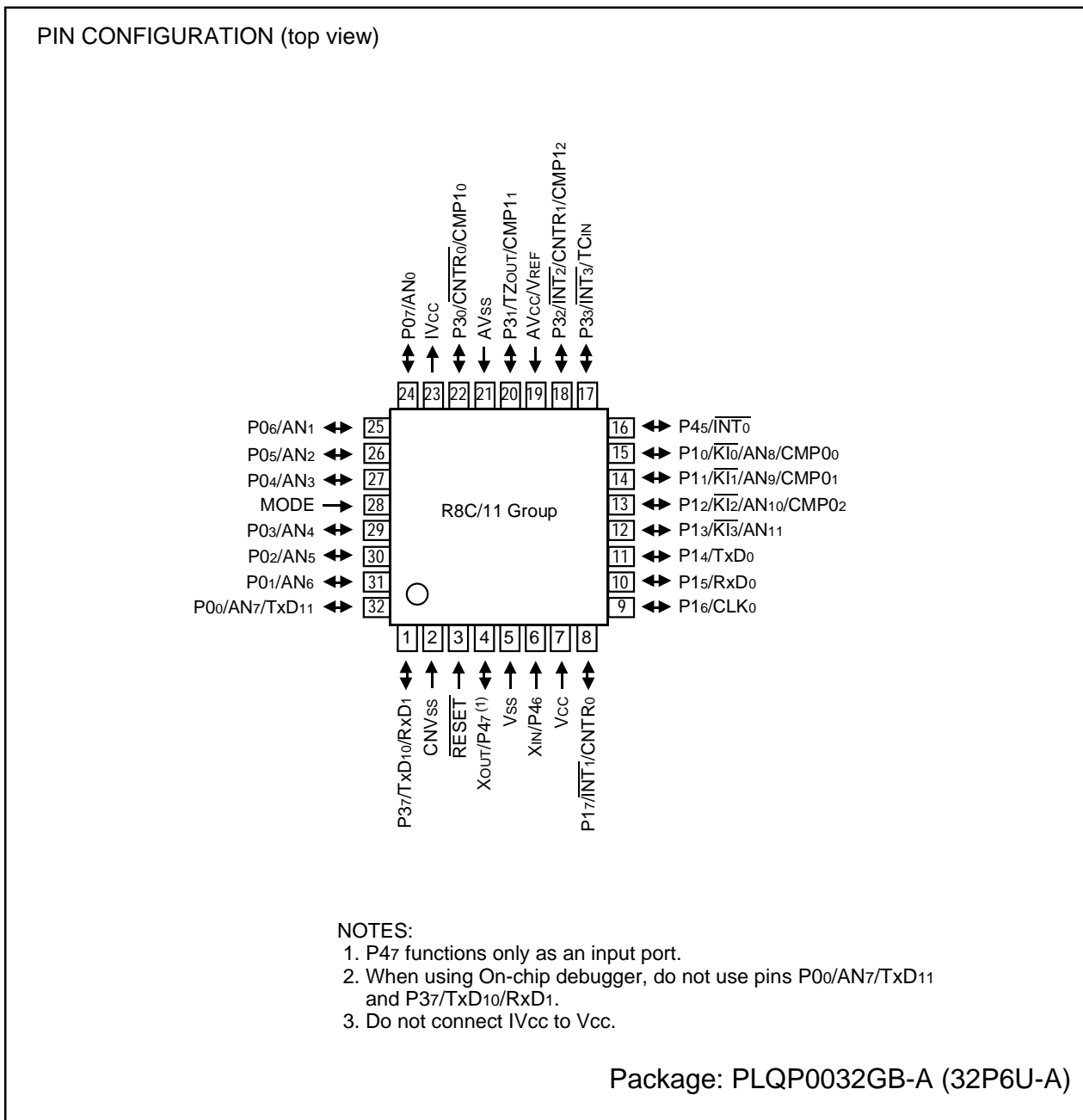


Figure 1.3 Pin Assignments (Top View)

1.6 Pin Description

Table 1.3 shows the pin description

Table 1.3 Pin description

| Signal name | Pin name | I/O type | Function |
|---------------------------|---|----------|--|
| Power supply input | Vcc, Vss | I | Apply 2.7 V to 5.5 V to the Vcc pin. Apply 0 V to the Vss pin. |
| IVcc | IVcc | O | This pin is to stabilize internal power supply. Connect this pin to Vss via a capacitor (0.1 μ F). Do not connect to Vcc. |
| Analog power supply input | AVcc, AVss | I | Power supply input pins for A/D converter. Connect the AVcc pin to Vcc. Connect the AVss pin to Vss. Connect a capacitor between pins AVcc and AVss. |
| Reset input | RESET | I | Input "L" on this pin resets the MCU. |
| CNVss | CNVss | I | Connect this pin to Vss via a resistor. |
| MODE | MODE | I | Connect this pin to Vcc via a resistor. |
| Main clock input | XIN | I | These pins are provided for the main clock generating circuit I/O. Connect a ceramic resonator or a crystal oscillator between the XIN and XOUT pins. To use an externally derived clock, input it to the XIN pin and leave the XOUT pin open. |
| Main clock output | XOUT | O | |
| INT interrupt input | INT $\bar{0}$ to INT $\bar{3}$ | I | INT interrupt input pins. |
| Key input interrupt | KI $\bar{0}$ to KI $\bar{3}$ | I | Key input interrupt pins. |
| Timer X | CNTR $\bar{0}$ | I/O | Timer X I/O pin |
| | CNTR $\bar{0}$ | O | Timer X output pin |
| Timer Y | CNTR $\bar{1}$ | I/O | Timer Y I/O pin |
| Timer Z | TZOUT | O | Timer Z output pin |
| Timer C | TCIN | I | Timer C input pin |
| | CMP $\bar{0}$ to CMP $\bar{0}$ ₂ , CMP $\bar{1}$ ₀ to CMP $\bar{1}$ ₂ | O | Timer C output pins |
| Serial interface | CLK $\bar{0}$ | I/O | Transfer clock I/O pin. |
| | RxD $\bar{0}$, RxD $\bar{1}$ | I | Serial data input pins. |
| | TxD $\bar{0}$, TxD $\bar{1}$ ₀ , TxD $\bar{1}$ ₁ | O | Serial data output pins. |
| Reference voltage input | VREF | I | Reference voltage input pin for A/D converter. Connect the VREF pin to Vcc. |
| A/D converter | AN $\bar{0}$ to AN $\bar{1}$ ₁ | I | Analog input pins for A/D converter |
| I/O port | P $\bar{0}$ to P $\bar{7}$, P $\bar{1}$ ₀ to P $\bar{1}$ ₇ , P $\bar{3}$ ₀ to P $\bar{3}$ ₃ , P $\bar{3}$ ₇ , P $\bar{4}$ ₅ | I/O | These are 8-bit CMOS I/O ports. Each port has an I/O select direction register, allowing each pin in that port to be directed for input or output individually. Any port set to input can select whether to use a pull-up resistor or not by program. P $\bar{1}$ ₀ to P $\bar{1}$ ₇ also function as LED drive ports. |
| Input port | P $\bar{4}$ ₆ , P $\bar{4}$ ₇ | I | Port for input-only |

2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU registers. The CPU has 13 registers. Of these, R0, R1, R2, R3, A0, A1 and FB comprise a register bank. Two sets of register banks are provided.

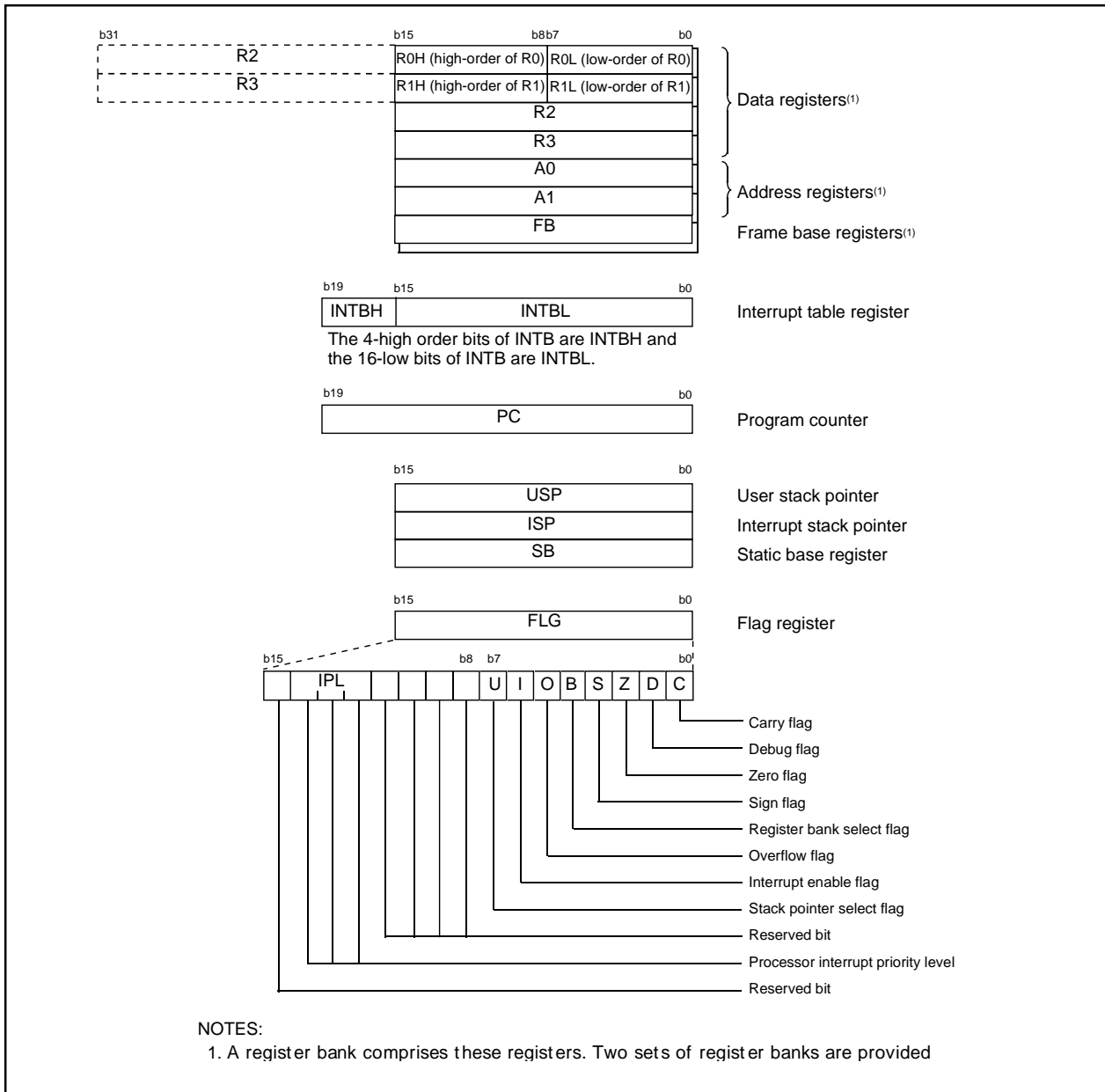


Figure 2.1 CPU Register

2.1 Data Registers (R0, R1, R2 and R3)

R0 is a 16-bit register for transfer, arithmetic and logic operations. The same applies to R1 to R3. The R0 can be split into high-order bit (R0H) and low-order bit (R0L) to be used separately as 8-bit data registers. The same applies to R1H and R1L as R0H and R0L. R2 can be combined with R0 to be used as a 32-bit data register (R2R0). The same applies to R3R1 as R2R0.

2.2 Address Registers (A0 and A1)

A0 is a 16-bit register for address register indirect addressing and address register relative addressing. They also are used for transfer, arithmetic and logic operations. The same applies to A1 as A0. A0 can be combined with A1 to be used as a 32-bit address register (A1A0).

2.3 Frame Base Register (FB)

FB is a 16-bit register for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB is a 20-bit register indicates the start address of an interrupt vector table.

2.5 Program Counter (PC)

PC, 20 bits wide, indicates the address of an instruction to be executed.

2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

The stack pointer (SP), USP and ISP, are 16 bits wide each.

The U flag of FLG is used to switch between USP and ISP.

2.7 Static Base Register (SB)

SB is a 16-bit register for SB relative addressing.

2.8 Flag Register (FLG)

FLG is a 11-bit register indicating the CPU state.

2.8.1 Carry Flag (C)

The C flag retains a carry, borrow, or shift-out bit that has occurred in the arithmetic logic unit.

2.8.2 Debug Flag (D)

The D flag is for debug only. Set to "0".

2.8.3 Zero Flag (Z)

The Z flag is set to "1" when an arithmetic operation resulted in 0; otherwise, "0".

2.8.4 Sign Flag (S)

The S flag is set to "1" when an arithmetic operation resulted in a negative value; otherwise, "0".

2.8.5 Register Bank Select Flag (B)

The register bank 0 is selected when the B flag is "0". The register bank 1 is selected when this flag is set to "1".

2.8.6 Overflow Flag (O)

The O flag is set to "1" when the operation resulted in an overflow; otherwise, "0".

2.8.7 Interrupt Enable Flag (I)

The I flag enables a maskable interrupt.

An interrupt is disabled when the I flag is set to "0", and are enabled when the I flag is set to "1". The I flag is set to "0" when an interrupt request is acknowledged.

2.8.8 Stack Pointer Select Flag (U)

ISP is selected when the U flag is set to "0", USP is selected when the U flag is set to "1".

The U flag is set to "0" when a hardware interrupt request is acknowledged or the INT instruction of software interrupt numbers 0 to 31 is executed.

2.8.9 Processor Interrupt Priority Level (IPL)

IPL, 3 bits wide, assigns processor interrupt priority levels from level 0 to level 7.

If a requested interrupt has greater priority than IPL, the interrupt is enabled.

2.8.10 Reserved Bit

When write to this bit, set to "0". When read, its content is indeterminate.

3. Memory

Figure 3.1 is a memory map of this MCU. This MCU provides 1-Mbyte address space from addresses 00000₁₆ to FFFFF₁₆.

The internal ROM is allocated lower addresses beginning with address 0FFFF₁₆. For example, a 16-Kbyte internal ROM is allocated addresses from 0C000₁₆ to 0FFFF₁₆.

The fixed interrupt vector table is allocated addresses 0FFDC₁₆ to 0FFFF₁₆. They store the starting address of each interrupt routine.

The internal RAM is allocated higher addresses beginning with address 00400₁₆. For example, a 1-Kbyte internal RAM is allocated addresses 00400₁₆ to 007FF₁₆. The internal RAM is used not only for storing data, but for calling subroutines and stacks when interrupt request is acknowledged.

Special function registers (SFR) are allocated addresses 00000₁₆ to 002FF₁₆. The peripheral function control registers are located them. All addresses, which have nothing allocated within the SFR, are reserved area and cannot be accessed by users.

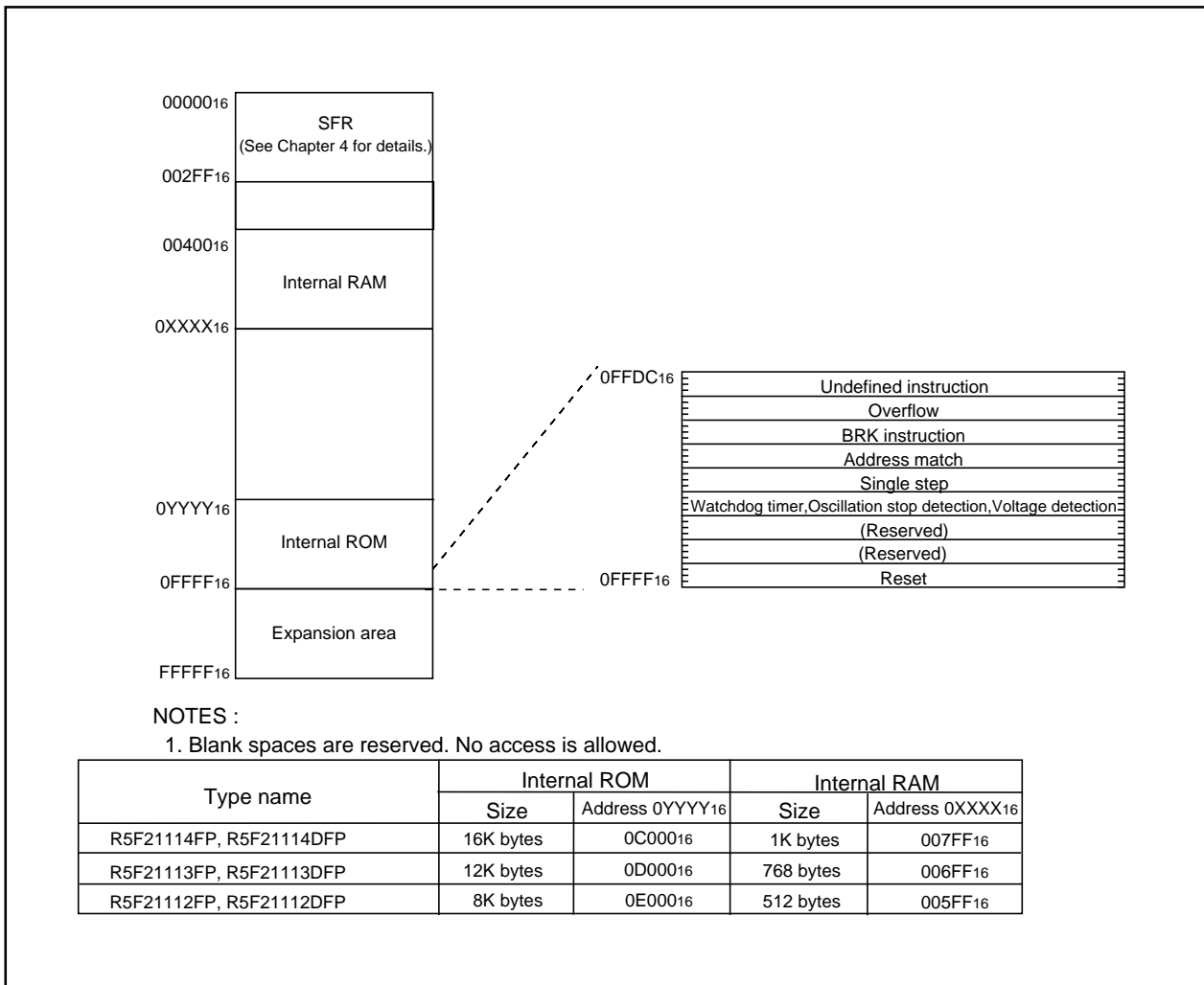


Figure 3.1 Memory Map

4. Special Function Register (SFR)

SFR(Special Function Register) is the control register of peripheral functions. Tables 4.1 to 4.4 list the SFR information

Table 4.1 SFR Information(1)(1)

| Address | Register | Symbol | After reset |
|--------------------|---|--------|---|
| 0000 ₁₆ | | | |
| 0001 ₁₆ | | | |
| 0002 ₁₆ | | | |
| 0003 ₁₆ | | | |
| 0004 ₁₆ | Processor mode register 0 | PM0 | 0016 |
| 0005 ₁₆ | Processor mode register 1 | PM1 | 0016 |
| 0006 ₁₆ | System clock control register 0 | CM0 | 011010002 |
| 0007 ₁₆ | System clock control register 1 | CM1 | 001000002 |
| 0008 ₁₆ | High-speed on-chip oscillator control register 0 | HR0 | 0016 |
| 0009 ₁₆ | Address match interrupt enable register | AIER | XXXXXX002 |
| 000A ₁₆ | Protect register | PRCR | 00XXX0002 |
| 000B ₁₆ | High-speed on-chip oscillator control register 1 | HR1 | 4016 |
| 000C ₁₆ | Oscillation stop detection register | OCD | 000001002 |
| 000D ₁₆ | Watchdog timer reset register | WDTR | XX16 |
| 000E ₁₆ | Watchdog timer start register | WDTS | XX16 |
| 000F ₁₆ | Watchdog timer control register | WDC | 000111112 |
| 0010 ₁₆ | Address match interrupt register 0 | RMAD0 | 0016 |
| 0011 ₁₆ | | | 0016 |
| 0012 ₁₆ | | | X016 |
| 0013 ₁₆ | | | |
| 0014 ₁₆ | Address match interrupt register 1 | RMAD1 | 0016 |
| 0015 ₁₆ | | | 0016 |
| 0016 ₁₆ | | | X016 |
| 0017 ₁₆ | | | |
| 0018 ₁₆ | | | |
| 0019 ₁₆ | Voltage detection register 1 ⁽²⁾ | VCR1 | 000010002 |
| 001A ₁₆ | Voltage detection register 2 ⁽²⁾ | VCR2 | 0016 ⁽³⁾ 10000002 ⁽⁴⁾ |
| 001B ₁₆ | | | |
| 001C ₁₆ | | | |
| 001D ₁₆ | | | |
| 001E ₁₆ | INT0 input filter select register | INT0F | XXXXX0002 |
| 001F ₁₆ | Voltage detection interrupt register ⁽²⁾ | D4INT | 0016 ⁽³⁾ 010000012 ⁽⁴⁾ |
| 0020 ₁₆ | | | |
| 0021 ₁₆ | | | |
| 0022 ₁₆ | | | |
| 0023 ₁₆ | | | |
| 0024 ₁₆ | | | |
| 0025 ₁₆ | | | |
| 0026 ₁₆ | | | |
| 0027 ₁₆ | | | |
| 0028 ₁₆ | | | |
| 0029 ₁₆ | | | |
| 002A ₁₆ | | | |
| 002B ₁₆ | | | |
| 002C ₁₆ | | | |
| 002D ₁₆ | | | |
| 002E ₁₆ | | | |
| 002F ₁₆ | | | |
| 0030 ₁₆ | | | |
| 0031 ₁₆ | | | |
| 0032 ₁₆ | | | |
| 0033 ₁₆ | | | |
| 0034 ₁₆ | | | |
| 0035 ₁₆ | | | |
| 0036 ₁₆ | | | |
| 0037 ₁₆ | | | |
| 0038 ₁₆ | | | |
| 0039 ₁₆ | | | |
| 003A ₁₆ | | | |
| 003B ₁₆ | | | |
| 003C ₁₆ | | | |
| 003D ₁₆ | | | |
| 003E ₁₆ | | | |
| 003F ₁₆ | | | |

X : Undefined

NOTES:

- Blank spaces are reserved. No access is allowed.
- Software reset or the watchdog timer reset does not affect this register.
- Owing to Reset input.
- In the case of RESET pin = H retaining.

Table 4.2 SFR Information(2)⁽¹⁾

| Address | Register | Symbol | After reset |
|--------------------|---|--------|-------------|
| 0040 ₁₆ | | | |
| 0041 ₁₆ | | | |
| 0042 ₁₆ | | | |
| 0043 ₁₆ | | | |
| 0044 ₁₆ | | | |
| 0045 ₁₆ | | | |
| 0046 ₁₆ | | | |
| 0047 ₁₆ | | | |
| 0048 ₁₆ | | | |
| 0049 ₁₆ | | | |
| 004A ₁₆ | | | |
| 004B ₁₆ | | | |
| 004C ₁₆ | | | |
| 004D ₁₆ | Key input interrupt control register | KUPIC | XXXXX0002 |
| 004E ₁₆ | AD conversion interrupt control register | ADIC | XXXXX0002 |
| 004F ₁₆ | | | |
| 0050 ₁₆ | Compare 1 interrupt control register | CMP1IC | XXXXX0002 |
| 0051 ₁₆ | UART0 transmit interrupt control register | S0TIC | XXXXX0002 |
| 0052 ₁₆ | UART0 receive interrupt control register | S0RIC | XXXXX0002 |
| 0053 ₁₆ | UART1 transmit interrupt control register | S1TIC | XXXXX0002 |
| 0054 ₁₆ | UART1 receive interrupt control register | S1RIC | XXXXX0002 |
| 0055 ₁₆ | INT2 interrupt control register | INT2IC | XXXXX0002 |
| 0056 ₁₆ | Timer X interrupt control register | TXIC | XXXXX0002 |
| 0057 ₁₆ | Timer Y interrupt control register | TYIC | XXXXX0002 |
| 0058 ₁₆ | Timer Z interrupt control register | TZIC | XXXXX0002 |
| 0059 ₁₆ | INT1 interrupt control register | INT1IC | XXXXX0002 |
| 005A ₁₆ | INT3 interrupt control register | INT3IC | XXXXX0002 |
| 005B ₁₆ | Timer C interrupt control register | TCIC | XXXXX0002 |
| 005C ₁₆ | Compare 0 interrupt control register | CMP0IC | XXXXX0002 |
| 005D ₁₆ | INT0 interrupt control register | INT0IC | XX00X0002 |
| 005E ₁₆ | | | |
| 005F ₁₆ | | | |
| 0060 ₁₆ | | | |
| 0061 ₁₆ | | | |
| 0062 ₁₆ | | | |
| 0063 ₁₆ | | | |
| 0064 ₁₆ | | | |
| 0065 ₁₆ | | | |
| 0066 ₁₆ | | | |
| 0067 ₁₆ | | | |
| 0068 ₁₆ | | | |
| 0069 ₁₆ | | | |
| 006A ₁₆ | | | |
| 006B ₁₆ | | | |
| 006C ₁₆ | | | |
| 006D ₁₆ | | | |
| 006E ₁₆ | | | |
| 006F ₁₆ | | | |
| 0070 ₁₆ | | | |
| 0071 ₁₆ | | | |
| 0072 ₁₆ | | | |
| 0073 ₁₆ | | | |
| 0074 ₁₆ | | | |
| 0075 ₁₆ | | | |
| 0076 ₁₆ | | | |
| 0077 ₁₆ | | | |
| 0078 ₁₆ | | | |
| 0079 ₁₆ | | | |
| 007A ₁₆ | | | |
| 007B ₁₆ | | | |
| 007C ₁₆ | | | |
| 007D ₁₆ | | | |
| 007E ₁₆ | | | |
| 007F ₁₆ | | | |

X : Undefined

NOTES:

- Blank spaces are reserved. No access is allowed.

Table 4.3 SFR Information(3)(1)

| Address | Register | Symbol | After reset |
|--------------------|---|--------|---------------------|
| 0080 ₁₆ | Timer Y, Z mode register | TYZMR | 0016 |
| 0081 ₁₆ | Prescaler Y register | PREY | FF16 |
| 0082 ₁₆ | Timer Y secondary register | TYSC | FF16 |
| 0083 ₁₆ | Timer Y primary register | TYPR | FF16 |
| 0084 ₁₆ | Timer Y, Z waveform output control register | PUM | 0016 |
| 0085 ₁₆ | Prescaler Z register | PREZ | FF16 |
| 0086 ₁₆ | Timer Z secondary register | TZSC | FF16 |
| 0087 ₁₆ | Timer Z primary register | TZPR | FF16 |
| 0088 ₁₆ | | | |
| 0089 ₁₆ | | | |
| 008A ₁₆ | Timer Y, Z output control register | TYZOC | 0016 |
| 008B ₁₆ | Timer X mode register | TXMR | 0016 |
| 008C ₁₆ | Prescaler X register | PREX | FF16 |
| 008D ₁₆ | Timer X register | TX | FF16 |
| 008E ₁₆ | Timer count source set register | TCSS | 0016 |
| 008F ₁₆ | | | |
| 0090 ₁₆ | Timer C register | TC | 0016 |
| 0091 ₁₆ | | | 0016 |
| 0092 ₁₆ | | | |
| 0093 ₁₆ | | | |
| 0094 ₁₆ | | | |
| 0095 ₁₆ | | | |
| 0096 ₁₆ | External input enable register | INTEN | 0016 |
| 0097 ₁₆ | | | |
| 0098 ₁₆ | Key input enable register | KIEN | 0016 |
| 0099 ₁₆ | | | |
| 009A ₁₆ | Timer C control register 0 | TCC0 | 0016 |
| 009B ₁₆ | Timer C control register 1 | TCC1 | 0016 |
| 009C ₁₆ | Capture, compare 0 register | TM0 | 0016 |
| 009D ₁₆ | | | 0016 ⁽²⁾ |
| 009E ₁₆ | Compare 1 register | TM1 | FF16 |
| 009F ₁₆ | | | FF16 |
| 00A0 ₁₆ | UART0 transmit/receive mode register | U0MR | 0016 |
| 00A1 ₁₆ | UART0 bit rate register | U0BRG | XX16 |
| 00A2 ₁₆ | UART0 transmit buffer register | U0TB | XX16 |
| 00A3 ₁₆ | | | XX16 |
| 00A4 ₁₆ | UART0 transmit/receive control register 0 | U0C0 | 000010002 |
| 00A5 ₁₆ | UART0 transmit/receive control register 1 | U0C1 | 000000102 |
| 00A6 ₁₆ | UART0 receive buffer register | U0RB | XX16 |
| 00A7 ₁₆ | | | XX16 |
| 00A8 ₁₆ | UART1 transmit/receive mode register | U1MR | 0016 |
| 00A9 ₁₆ | UART1 bit rate register | U1BRG | XX16 |
| 00AA ₁₆ | UART1 transmit buffer register | U1TB | XX16 |
| 00AB ₁₆ | | | XX16 |
| 00AC ₁₆ | UART1 transmit/receive control register 0 | U1C0 | 000010002 |
| 00AD ₁₆ | UART1 transmit/receive control register 1 | U1C1 | 000000102 |
| 00AE ₁₆ | UART1 receive buffer register | U1RB | XX16 |
| 00AF ₁₆ | | | XX16 |
| 00B0 ₁₆ | UART transmit/receive control register 2 | UCON | 0016 |
| 00B1 ₁₆ | | | |
| 00B2 ₁₆ | | | |
| 00B3 ₁₆ | | | |
| 00B4 ₁₆ | | | |
| 00B5 ₁₆ | | | |
| 00B6 ₁₆ | | | |
| 00B7 ₁₆ | | | |
| 00B8 ₁₆ | | | |
| 00B9 ₁₆ | | | |
| 00BA ₁₆ | | | |
| 00BB ₁₆ | | | |
| 00BC ₁₆ | | | |
| 00BD ₁₆ | | | |
| 00BE ₁₆ | | | |
| 00BF ₁₆ | | | |

X : Undefined

NOTES:

- Blank spaces are reserved. No access is allowed.
- When output compare mode (the TCC13 bit in the TCC1 register = 1) is selected, the value after reset is set to "FFFF16".

Table 4.4 SFR Information(4)(1)

| Address | Register | Symbol | After reset |
|--------------------|---|--------|-------------------------|
| 00C0 ₁₆ | AD register | AD | XX ₁₆ |
| 00C1 ₁₆ | | | XX ₁₆ |
| 00C2 ₁₆ | | | |
| 00C3 ₁₆ | | | |
| 00C4 ₁₆ | | | |
| 00C5 ₁₆ | | | |
| 00C6 ₁₆ | | | |
| 00C7 ₁₆ | | | |
| 00C8 ₁₆ | | | |
| 00C9 ₁₆ | | | |
| 00CA ₁₆ | | | |
| 00CB ₁₆ | | | |
| 00CC ₁₆ | | | |
| 00CD ₁₆ | | | |
| 00CE ₁₆ | | | |
| 00CF ₁₆ | | | |
| 00D0 ₁₆ | | | |
| 00D1 ₁₆ | | | |
| 00D2 ₁₆ | | | |
| 00D3 ₁₆ | | | |
| 00D4 ₁₆ | AD control register 2 | ADCON2 | 00 ₁₆ |
| 00D5 ₁₆ | | | |
| 00D6 ₁₆ | AD control register 0 | ADCON0 | 00000XX ₂ |
| 00D7 ₁₆ | AD control register 1 | ADCON1 | 00 ₁₆ |
| 00D8 ₁₆ | | | |
| 00D9 ₁₆ | | | |
| 00DA ₁₆ | | | |
| 00DB ₁₆ | | | |
| 00DC ₁₆ | | | |
| 00DD ₁₆ | | | |
| 00DE ₁₆ | | | |
| 00DF ₁₆ | | | |
| 00E0 ₁₆ | Port P0 register | P0 | XX ₁₆ |
| 00E1 ₁₆ | Port P1 register | P1 | XX ₁₆ |
| 00E2 ₁₆ | Port P0 direction register | PD0 | 00 ₁₆ |
| 00E3 ₁₆ | Port P1 direction register | PD1 | 00 ₁₆ |
| 00E4 ₁₆ | | | |
| 00E5 ₁₆ | Port P3 register | P3 | XX ₁₆ |
| 00E6 ₁₆ | | | |
| 00E7 ₁₆ | Port P3 direction register | PD3 | 00 ₁₆ |
| 00E8 ₁₆ | Port P4 register | P4 | XX ₁₆ |
| 00E9 ₁₆ | | | |
| 00EA ₁₆ | Port P4 direction register | PD4 | 00 ₁₆ |
| 00EB ₁₆ | | | |
| 00EC ₁₆ | | | |
| 00ED ₁₆ | | | |
| 00EE ₁₆ | | | |
| 00EF ₁₆ | | | |
| 00F0 ₁₆ | | | |
| 00F1 ₁₆ | | | |
| 00F2 ₁₆ | | | |
| 00F3 ₁₆ | | | |
| 00F4 ₁₆ | | | |
| 00F5 ₁₆ | | | |
| 00F6 ₁₆ | | | |
| 00F7 ₁₆ | | | |
| 00F8 ₁₆ | | | |
| 00F9 ₁₆ | | | |
| 03FA ₁₆ | | | |
| 00FB ₁₆ | | | |
| 00FC ₁₆ | Pull-up control register 0 | PUR0 | 00XX0000 ₂ |
| 00FD ₁₆ | Pull-up control register 1 | PUR1 | XXXXXXXX0X ₂ |
| 00FE ₁₆ | Port P1 drive capacity control register | DRR | 00 ₁₆ |
| 00FF ₁₆ | Timer C output control register | TCOUT | 00 ₁₆ |
| 01B3 ₁₆ | Flash memory control register 4 | FMR4 | 01000000 ₂ |
| 01B4 ₁₆ | | | |
| 01B5 ₁₆ | Flash memory control register 1 | FMR1 | 0100XX0X ₂ |
| 01B6 ₁₆ | | | |
| 01B7 ₁₆ | Flash memory control register 0 | FMR0 | 00000001 ₂ |

X : Undefined

NOTES:

1. Blank columns, 0100₁₆ to 01B2₁₆ and 01B8₁₆ to 02FF₁₆ are all reserved. No access is allowed.

5. Electrical Characteristics

Table 5.1 Absolute Maximum Ratings

| Symbol | Parameter | Condition | Rated value | Unit |
|------------------|-------------------------------|-----------------------------------|-----------------------------------|------|
| V _{CC} | Supply voltage | V _{CC} =AV _{CC} | -0.3 to 6.5 | V |
| AV _{CC} | Analog supply voltage | V _{CC} =AV _{CC} | -0.3 to 6.5 | V |
| V _I | Input voltage | | -0.3 to V _{CC} +0.3 | V |
| V _O | Output voltage | | -0.3 to V _{CC} +0.3 | V |
| P _d | Power dissipation | T _{opr} =25 °C | 300 | mW |
| T _{opr} | Operating ambient temperature | | -20 to 85 / -40 to 85 (D version) | °C |
| T _{stg} | Storage temperature | | -65 to 150 | °C |

Table 5.2 Recommended Operating Conditions

| Symbol | Parameter | Conditions | Standard | | | Unit | |
|------------------------|--|---|---------------------|---------------------|--------------------|------|----|
| | | | Min. | Typ. | Max. | | |
| V _{CC} | Supply voltage | | 2.7 | — | 5.5 | V | |
| AV _{CC} | Analog supply voltage | | — | V _{CC} (3) | — | V | |
| V _{SS} | Supply voltage | | — | 0 | — | V | |
| AV _{SS} | Analog supply voltage | | — | 0 | — | V | |
| V _{IH} | "H" input voltage | | 0.8V _{CC} | — | V _{CC} | V | |
| V _{IL} | "L" input voltage | | 0 | — | 0.2V _{CC} | V | |
| I _{OH} (sum) | "H" peak all output currents | Sum of all pins' IOH (peak) | — | — | -60.0 | mA | |
| I _{OH} (peak) | "H" peak output current | | — | — | -10.0 | mA | |
| I _{OH} (avg) | "H" average output current | | — | — | -5.0 | mA | |
| I _{OL} (sum) | "L" peak all output currents | Sum of all pins' IOL (peak) | — | — | 60 | mA | |
| I _{OL} (peak) | "L" peak output current | Except P1 ₀ to P1 ₇ | — | — | 10 | mA | |
| | | P1 ₀ to P1 ₇ | Drive capacity HIGH | — | — | 30 | mA |
| | | | Drive capacity LOW | — | — | 10 | mA |
| I _{OL} (avg) | "L" average output current | Except P1 ₀ to P1 ₇ | — | — | 5 | mA | |
| | | P1 ₀ to P1 ₇ | Drive capacity HIGH | — | — | 15 | mA |
| | | | Drive capacity LOW | — | — | 5 | mA |
| f (XIN) | Main clock input oscillation frequency | 3.0V ≤ V _{CC} ≤ 5.5V | 0 | — | 20 | MHz | |
| | | 2.7V ≤ V _{CC} < 3.0V | 0 | — | 10 | MHz | |

NOTES:

1. V_{CC} = AV_{CC} = 2.7 to 5.5V at T_{opr} = -20 to 85 °C / -40 to 85 °C, unless otherwise specified.
2. The typical values when average output current is 100ms.
3. Hold V_{CC}=AV_{CC}.

Table 5.3 A/D Conversion Characteristics

| Symbol | Parameter | | Measuring condition | Standard | | | Unit |
|--------------|--|-----------------------|---|----------|----------------|-----------|---------------|
| | | | | Min. | Typ. | Max. | |
| — | Resolution | | $V_{ref} = V_{CC}$ | — | — | 10 | Bit |
| — | Absolute accuracy | 10 bit mode | $\phi_{AD} = 10 \text{ MHz}$, $V_{ref} = V_{CC} = 5.0 \text{ V}$ | — | — | ± 3 | LSB |
| | | 8 bit mode | $\phi_{AD} = 10 \text{ MHz}$, $V_{ref} = V_{CC} = 5.0 \text{ V}$ | — | — | ± 2 | LSB |
| | | 10 bit mode | $\phi_{AD} = 10 \text{ MHz}$, $V_{ref} = V_{CC} = 3.3 \text{ V}^{(3)}$ | — | — | ± 5 | LSB |
| | | 8 bit mode | $\phi_{AD} = 10 \text{ MHz}$, $V_{ref} = V_{CC} = 3.3 \text{ V}^{(3)}$ | — | — | ± 2 | LSB |
| R_{LADDER} | Ladder resistance | | $V_{REF} = V_{CC}$ | 10 | — | 40 | $k\Omega$ |
| t_{CONV} | Conversion time | 10 bit mode | $\phi_{AD} = 10 \text{ MHz}$, $V_{ref} = V_{CC} = 5.0 \text{ V}$ | 3.3 | — | — | μs |
| | | 8 bit mode | $\phi_{AD} = 10 \text{ MHz}$, $V_{ref} = V_{CC} = 5.0 \text{ V}$ | 2.8 | — | — | μs |
| V_{REF} | Reference voltage | | | — | $V_{CC}^{(4)}$ | — | V |
| V_{IA} | Analog input voltage | | | 0 | — | V_{ref} | V |
| — | A/D operating clock frequency ⁽²⁾ | Without sample & hold | | 0.25 | — | 10 | MHz |
| | | With sample & hold | | 1.0 | — | 10 | MHz |

NOTES:

- $V_{CC} = AV_{CC} = 2.7$ to 5.5 V at $T_{opr} = -20$ to $85 \text{ }^\circ\text{C}$ / -40 to $85 \text{ }^\circ\text{C}$, unless otherwise specified.
- If f_{AD} exceeds 10 MHz more, divide the f_{AD} and hold A/D operating clock frequency (ϕ_{AD}) 10 MHz or below.
- If the AV_{CC} is less than 4.2V, divide the f_{AD} and hold A/D operating clock frequency (ϕ_{AD}) $f_{AD}/2$ or below.
- Hold $V_{CC} = V_{ref}$.

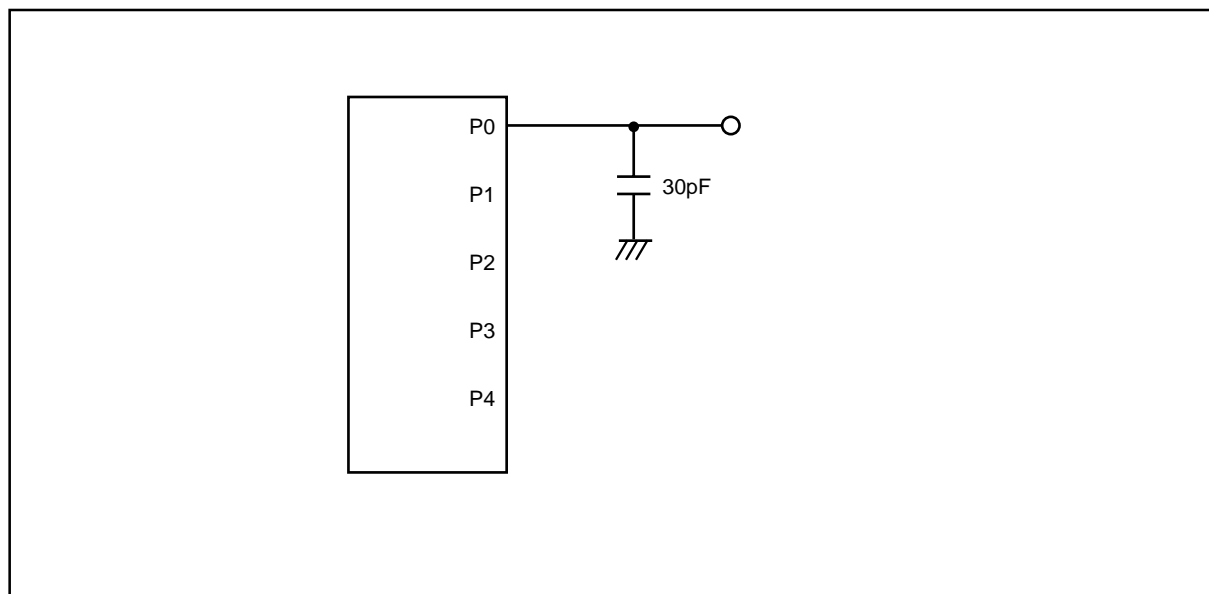


Figure 5.1 Port P0 to P4 measurement circuit

Table 5.4 Flash Memory Version Electrical Characteristics

| Symbol | Parameter | Measuring condition | Standard | | | Unit |
|-----------|---|---------------------------|----------|------|------|-------|
| | | | Min. | Typ. | Max. | |
| — | Program/erase endurance | | 100 | — | — | times |
| — | Byte program time | | — | 50 | 400 | μs |
| — | Block erase time | | — | 0.4 | 9 | s |
| td(SR-ES) | Time delay from suspend request until erase suspend | | — | — | 8 | ms |
| — | Erase Suspend Request Interval | | 10 | — | — | ms |
| — | Program, Erase voltage | | 2.7 | — | 5.5 | V |
| — | Read voltage | | 2.7 | — | 5.5 | V |
| — | Program, Erase temperature | | 0 | — | 60 | °C |
| — | Data hold time ⁽²⁾ | Ambient temperature=55 °C | 20 | — | — | year |

NOTES:

1. Referenced to $V_{CC1}=AV_{CC}=2.7$ to $5.5V$ at $T_{opr} = 0$ to 60 °C unless otherwise specified.
2. The data hold time includes time that the power supply is off or the clock is not supplied.

Table 5.5 Voltage Detection Circuit Electrical Characteristics

| Symbol | Parameter | Measuring condition | Standard | | | Unit |
|---------|---|---------------------|----------|------|------|------|
| | | | Min. | Typ. | Max. | |
| Vdet | Voltage detection level | | 3.3 | 3.8 | 4.3 | V |
| — | Voltage detection interrupt request generating time ⁽²⁾ | | — | 40 | — | μs |
| — | Voltage detection circuit self consumption current | VC27=1, VCC=5.0V | — | 600 | — | nA |
| td(E-A) | Waiting time till voltage detection circuit operation starts ⁽³⁾ | | — | — | 20 | μs |
| Vccmin | Minimum value of microcomputer operation voltage | | 2.7 | — | — | V |

NOTES:

1. The measuring condition is $V_{CC}=AV_{CC}=2.7V$ to $5.5V$ and $T_{opr} = -40$ °C to 85 °C.
2. This shows the time until the voltage detection interrupt request is generated since the voltage passes Vdet.
3. This shows the required time until the voltage detection circuit operates when setting to "1" again after setting the VC27 bit in the VCR2 register to "0".

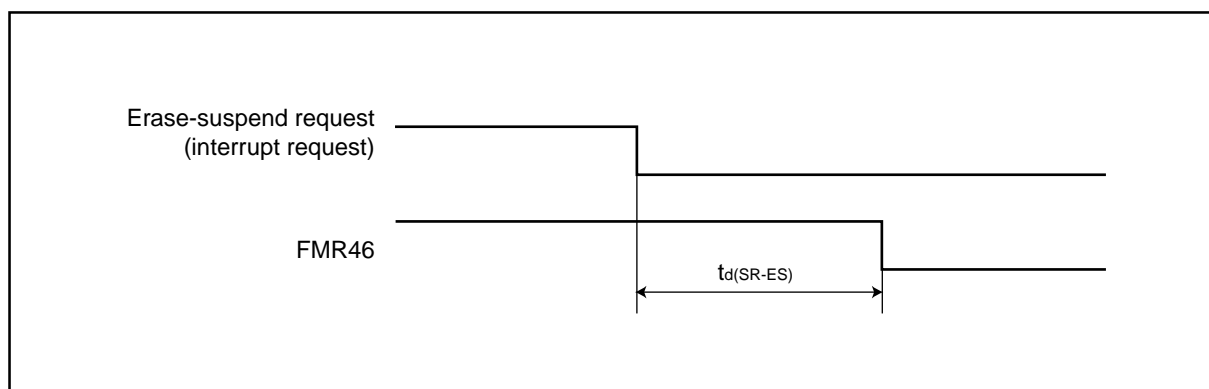
**Figure 5.2 Time delay from Suspend Request until Erase Suspend**

Table 5.6 Reset Circuit Electrical Characteristics (When Using Hardware Reset 2^(1, 3))

| Symbol | Parameter | Measuring condition | Standard | | | Unit |
|----------------|---|---|----------|------|------|------|
| | | | Min. | Typ. | Max. | |
| Vpor2 | Power-on reset valid voltage | -20°C ≤ Topr < 85°C | — | — | Vdet | V |
| tw(Vpor2-Vdet) | Supply voltage rising time when power-on reset is canceled ⁽²⁾ | -20°C ≤ Topr < 85°C, tw(por2) ≥ 0s ⁽⁴⁾ | — | — | 100 | ms |

NOTES:

1. The voltage detection circuit which is embedded in a microcomputer is a factor to generate the hardware reset 2. Refer to 5.1.2 Hardware Reset 2 of Hardware Manual for details.
2. This condition is not applicable when using with Vcc ≥ 1.0V.
3. When turning power on after the external power has been held below the valid voltage (Vpor1) for greater than 10 seconds, refer to Table 5.7 Reset Circuit Electrical Characteristics (When Not Using Hardware Reset 2).
4. tw(por2) is time to hold the external power below effective voltage (Vpor2).

Table 5.7 Reset Circuit Electrical Characteristics (When Not Using Hardware Reset 2)

| Symbol | Parameter | Measuring condition | Standard | | | Unit |
|----------------|--|---|----------|------|------|------|
| | | | Min. | Typ. | Max. | |
| Vpor1 | Power-on reset valid voltage | -20°C ≤ Topr < 85°C | — | — | 0.1 | V |
| tw(Vpor1-Vdet) | Supply voltage rising time when power-on reset is canceled | 0°C ≤ Topr ≤ 85°C, tw(por1) ≥ 10s ⁽²⁾ | — | — | 100 | ms |
| tw(Vpor1-Vdet) | Supply voltage rising time when power-on reset is canceled | -20°C ≤ Topr < 0°C, tw(por1) ≥ 30s ⁽²⁾ | — | — | 100 | ms |
| tw(Vpor1-Vdet) | Supply voltage rising time when power-on reset is canceled | -20°C ≤ Topr < 0°C, tw(por1) ≥ 10s ⁽²⁾ | — | — | 1 | ms |
| tw(Vpor1-Vdet) | Supply voltage rising time when power-on reset is canceled | 0°C ≤ Topr ≤ 85°C, tw(por1) ≥ 1s ⁽²⁾ | — | — | 0.5 | ms |

NOTES:

1. When not using hardware reset 2, use with Vcc ≥ 2.7V.
2. tw(por1) is time to hold the external power below effective voltage (Vpor1).

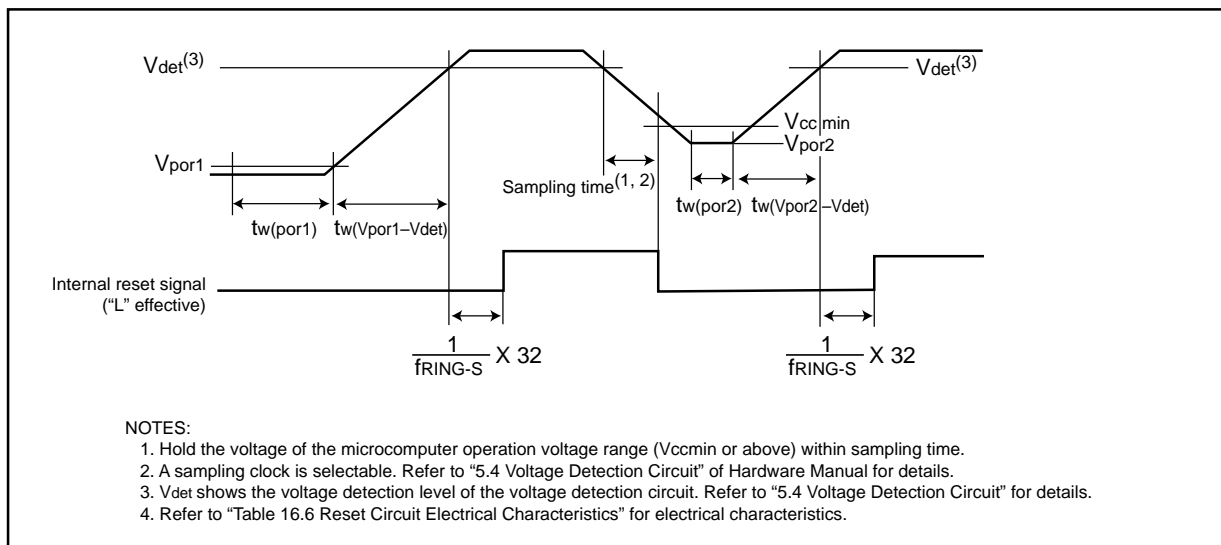
**Figure 5.3 Reset Circuit Electrical Characteristics**

Table 5.8 High-speed On-Chip Oscillator Circuit Electrical Characteristics

| Symbol | Parameter | Measuring condition | Standard | | | Unit |
|--------------|--|---|----------|------|------|------|
| | | | Min. | Typ. | Max. | |
| — | High-speed on-chip oscillator frequency 1 / (td(HRoffset)+td(HR)) when the reset is released | VCC=5.0V, Topr=25 °C Set "4016" in the HR1 register | 6 | 8 | 10 | MHz |
| td(HRoffset) | Settable high-speed on-chip oscillator minimum period | VCC=5.0V, Topr=25 °C Set "0016" in the HR1 register | — | 61 | — | ns |
| td(HR) | High-speed on-chip oscillator period adjusted unit | Differences when setting "0116" and "0016" in the HR register | — | 1 | — | ns |
| — | High-speed on-chip oscillator frequency temperature dependence(1) | Frequency fluctuation in temperature range of -10 °C to 50 °C | — | ±5 | — | % |
| — | High-speed on-chip oscillator frequency temperature dependence(2) | Frequency fluctuation in temperature range of -40 °C to 85 °C | — | ±10 | — | % |

NOTES:

1. The measuring condition is Vcc=AVcc=5.0 V and Topr=25 °C.

Table 5.9 Power Circuit Timing Characteristics

| Symbol | Parameter | Measuring condition | Standard | | | Unit |
|---------|--|---------------------|----------|------|------|------|
| | | | Min. | Typ. | Max. | |
| td(P-R) | Time for internal power supply stabilization during powering-on ⁽²⁾ | | 1 | — | 2000 | μs |
| td(R-S) | STOP release time ⁽³⁾ | | — | — | 150 | μs |

NOTES:

1. The measuring condition is Vcc=AVcc=2.7 to 5.5 V and Topr=25 °C.
2. This shows the wait time until the internal power supply generating circuit is stabilized during power-on.
3. This shows the time until BCLK starts from the interrupt acknowledgement to cancel stop mode.

Table 5.10 Electrical Characteristics (1) [Vcc=5V]

| Symbol | Parameter | | Measuring condition | Standard | | | Unit | |
|---------------------|--|---|--------------------------|--------------------------|---------|------|------|---|
| | | | | Min. | Typ. | Max. | | |
| VOH | "H" output voltage | Except XOUT | I _{OH} =-5mA | Vcc-2.0 | — | Vcc | V | |
| | | | I _{OH} =-200μA | Vcc-0.3 | — | Vcc | V | |
| | | XOUT | Drive ability HIGH | I _{OH} =-1 mA | Vcc-2.0 | — | Vcc | V |
| | | | Drive ability LOW | I _{OH} =-500μA | Vcc-2.0 | — | Vcc | V |
| VOL | "L" output voltage | Except P10 to P17, XOUT | I _{OL} = 5 mA | — | — | 2.0 | V | |
| | | | I _{OL} = 200 μA | — | — | 0.45 | V | |
| | | P10 to P17 | Drive capacity HIGH | I _{OL} = 15 mA | — | — | 2.0 | V |
| | | | Drive capacity LOW | I _{OL} = 5 mA | — | — | 2.0 | V |
| | | | Drive capacity LOW | I _{OL} = 200 μA | — | — | 0.45 | V |
| | | XOUT | Drive capacity HIGH | I _{OL} = 1 mA | — | — | 2.0 | V |
| | | | Drive capacity LOW | I _{OL} =500 μA | — | — | 2.0 | V |
| VT+·VT- | Hysteresis | INT0, INT1, INT2, INT3, KI0, KI1, KI2, KI3, CNTR0, CNTR1, TCIN, RxD0, RxD1, P45 | | 0.2 | — | 1.0 | V | |
| | | RESET | | 0.2 | — | 2.2 | V | |
| I _{IH} | "H" input current | | V _I =5V | — | — | 5.0 | μA | |
| I _{IL} | "L" input current | | V _I =0V | — | — | -5.0 | μA | |
| R _{PULLUP} | Pull-up resistance | | V _I =0V | 30 | 50 | 167 | kΩ | |
| R _{XIN} | Feedback resistance | XIN | | — | 1.0 | — | MΩ | |
| f _{RING-S} | Low-speed on-chip oscillator frequency | | | 40 | 125 | 250 | kHz | |
| V _{RAM} | RAM retention voltage | | At stop mode | 2.0 | — | — | V | |

NOTES:

1. Referenced to Vcc = AVcc = 4.2 to 5.5V at Topr = -20 to 85 °C / -40 to 85 °C, f(XIN)=20MHz unless otherwise specified.

Table 5.11 Electrical Characteristics (2) [Vcc=5V]

| Symbol | Parameter | Measuring condition | Standard | | | Unit | |
|-----------------|--|---|--|------|------|------|----|
| | | | Min. | Typ. | Max. | | |
| I _{CC} | Power supply current (V _{CC} =3.3 to 5.5V) In single-chip mode, the output pins are open and other pins are V _{SS} | High-speed mode X _{IN} =20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz No division | — | 9 | 15 | mA | |
| | | | X _{IN} =16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz No division | — | 8 | 14 | mA |
| | | | X _{IN} =10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz No division | — | 5 | — | mA |
| | | Medium-speed mode | X _{IN} =20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz Division by 8 | — | 4 | — | mA |
| | | | X _{IN} =16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz Division by 8 | — | 3 | — | mA |
| | | | X _{IN} =10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz Division by 8 | — | 2 | — | mA |
| | | High-speed on-chip oscillator mode | Main clock off High-speed on-chip oscillator on=8 MHz Low-speed on-chip oscillator on=125 kHz No division | — | 4 | 8 | mA |
| | | | Main clock off High-speed on-chip oscillator on=8 MHz Low-speed on-chip oscillator on=125 kHz Division by 8 | — | 1.5 | — | mA |
| | | Low-speed on-chip oscillator mode | Main clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz Division by 8 | — | 470 | 900 | μA |
| | | Wait mode | Main clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz When a WAIT instruction is executed ⁽¹⁾ Peripheral clock operation VC27="0" | — | 40 | 80 | μA |
| | | Wait mode | Main clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz When a WAIT instruction is executed ⁽¹⁾ Peripheral clock off VC27="0" | — | 38 | 76 | μA |
| | | Stop mode | Main clock off, Topr = 25 °C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10="1" Peripheral clock off VC27="0" | — | 0.8 | 3.0 | μA |

NOTES:

1. Timer Y is operated with timer mode.
2. Referenced to V_{CC} = AV_{CC} = 4.2 to 5.5V at Topr = -20 to 85 °C / -40 to 85 °C, f(X_{IN})=20MHz unless otherwise specified.

Timing requirements (Unless otherwise noted: $V_{CC} = 5V$, $V_{SS} = 0V$ at $T_{opr} = 25\text{ }^{\circ}C$) [$V_{CC}=5V$]**Table 5.12 XIN input**

| Symbol | Parameter | Standard | | Unit |
|----------|----------------------------|----------|------|------|
| | | Min. | Max. | |
| tC(XIN) | XIN input cycle time | 50 | – | ns |
| tWH(XIN) | XIN input HIGH pulse width | 25 | – | ns |
| tWL(XIN) | XIN input LOW pulse width | 25 | – | ns |

Table 5.13 CNTR0 input, CNTR1 input, $\overline{INT2}$ input

| Symbol | Parameter | Standard | | Unit |
|------------|------------------------------|----------|------|------|
| | | Min. | Max. | |
| tC(CNTR0) | CNTR0 input cycle time | 100 | – | ns |
| tWH(CNTR0) | CNTR0 input HIGH pulse width | 40 | – | ns |
| tWL(CNTR0) | CNTR0 input LOW pulse width | 40 | – | ns |

Table 5.14 TCIN input, $\overline{INT3}$ input

| Symbol | Parameter | Standard | | Unit |
|-----------|-----------------------------|--------------------|------|------|
| | | Min. | Max. | |
| tC(TCIN) | TCIN input cycle time | 400 ⁽¹⁾ | – | ns |
| tWH(TCIN) | TCIN input HIGH pulse width | 200 ⁽²⁾ | – | ns |
| tWL(TCIN) | TCIN input LOW pulse width | 200 ⁽²⁾ | – | ns |

NOTES:

1. When using the Timer C input capture mode, adjust the cycle time above (1/ Timer C count source frequency x 3).
2. When using the Timer C input capture mode, adjust the pulse width above (1/ Timer C count source frequency x 1.5).

Table 5.15 Serial Interface

| Symbol | Parameter | Standard | | Unit |
|----------|-----------------------------|----------|------|------|
| | | Min. | Max. | |
| tC(CK) | CLKi input cycle time | 200 | – | ns |
| tW(CKH) | CLKi input HIGH pulse width | 100 | – | ns |
| tW(CKL) | CLKi input LOW pulse width | 100 | – | ns |
| td(C-Q) | TxDi output delay time | – | 80 | ns |
| th(C-Q) | TxDi hold time | 0 | – | ns |
| tsu(D-C) | RxDi input setup time | 35 | – | ns |
| th(C-D) | RxDi input hold time | 90 | – | ns |

Table 5.16 External interrupt $\overline{INT0}$ input

| Symbol | Parameter | Standard | | Unit |
|---------|--|--------------------|------|------|
| | | Min. | Max. | |
| tW(INH) | $\overline{INT0}$ input HIGH pulse width | 250 ⁽¹⁾ | – | ns |
| tW(INL) | $\overline{INT0}$ input LOW pulse width | 250 ⁽²⁾ | – | ns |

NOTES:

1. When selecting the digital filter by the $\overline{INT0}$ input filter select bit, use the $\overline{INT0}$ input HIGH pulse width to the greater value, either (1/ digital filter clock frequency x 3) or the minimum value of standard.
2. When selecting the digital filter by the $\overline{INT0}$ input filter select bit, use the $\overline{INT0}$ input LOW pulse width to the greater value, either (1/ digital filter clock frequency x 3) or the minimum value of standard.

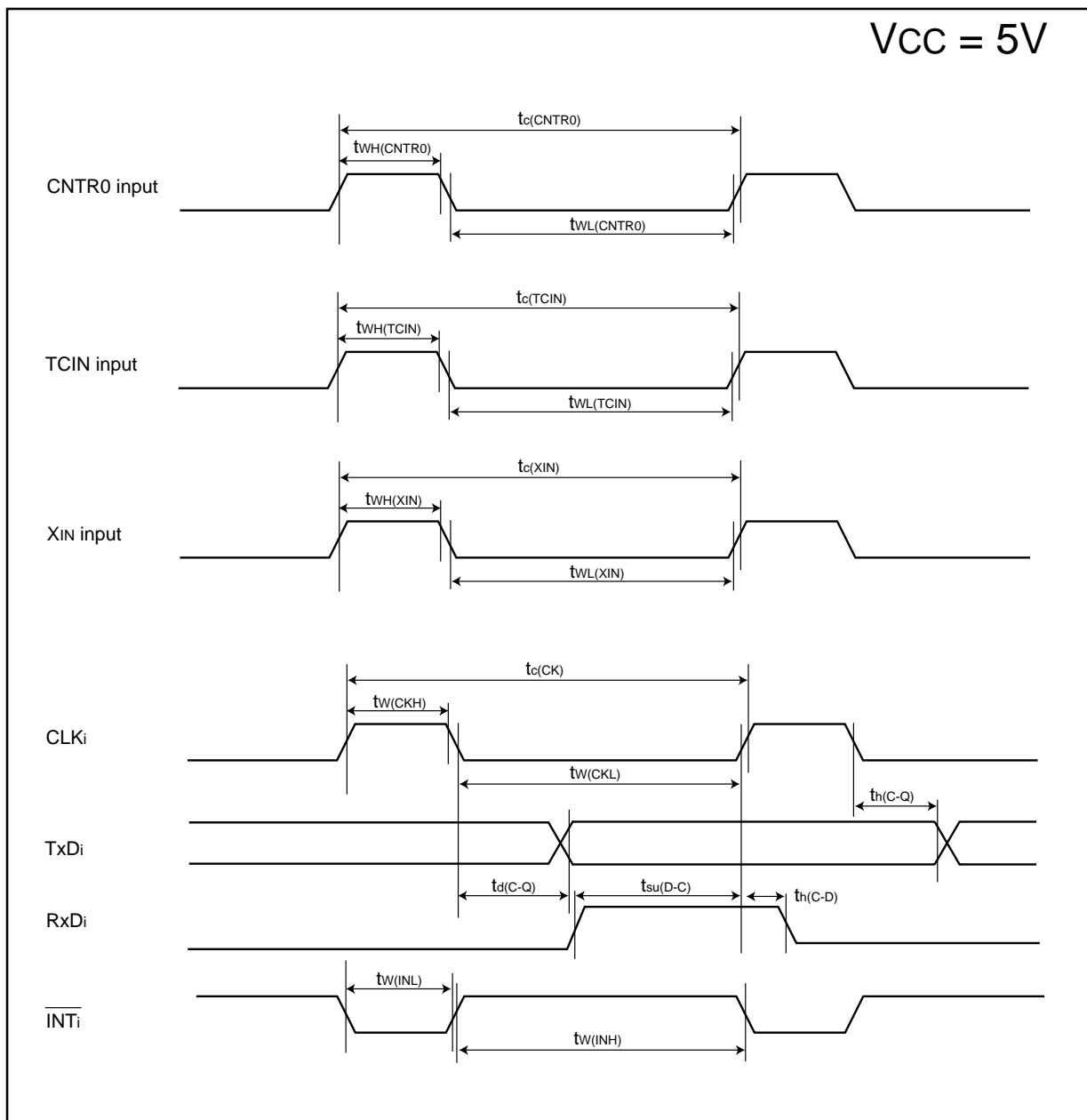


Figure 5.4 Vcc=5V timing diagram

Table 5.17 Electrical Characteristics (3) [Vcc=3V]

| Symbol | Parameter | | Measuring condition | | Standard | | | Unit |
|------------------|--|---|---------------------|-------------|----------|------|------|------|
| | | | | | Min. | Typ. | Max. | |
| VOH | "H" output voltage | Except XOUT | IOH=-1mA | | Vcc-0.5 | — | Vcc | V |
| | | XOUT | Drive capacity HIGH | IOH=-0.1 mA | Vcc-0.5 | — | Vcc | v |
| | | | Drive capacity LOW | IOH=-50 μA | Vcc-0.5 | — | Vcc | v |
| VOL | "L" output voltage | Except P10 to P17, XOUT | IOL= 1 mA | | — | — | 0.5 | V |
| | | P10 to P17 | Drive capacity HIGH | IOL= 2 mA | — | — | 0.5 | V |
| | | | Drive capacity LOW | IOL= 1 mA | — | — | 0.5 | v |
| | | XOUT | Drive capacity HIGH | IOL= 0.1 mA | — | — | 0.5 | v |
| | | | Drive capacity LOW | IOL=50 μA | — | — | 0.5 | v |
| VT+-VT- | Hysteresis | INT0, INT1, INT2, INT3, K10, K11, K12, K13, CNTR0, CNTR1, TCIN, RxD0, RxD1, P45 | | | 0.2 | — | 0.8 | v |
| | | RESET | | | 0.2 | — | 1.8 | v |
| IiH | "H" input current | | | Vi=3V | — | — | 4.0 | μA |
| IiL | "L" input current | | | Vi=0V | — | — | -4.0 | μA |
| RPULLUP | Pull-up resistance | | | Vi=0V | 66 | 160 | 500 | kΩ |
| RiXIN | Feedback resistance | XIN | | | — | 3.0 | — | MΩ |
| fRING-S | Low-speed on-chip oscillator frequency | | | | 40 | 125 | 250 | kHz |
| V _{RAM} | RAM retention voltage | | At stop mode | | 2.0 | — | — | V |

NOTES:

1. Referenced to Vcc = AVcc = 2.7 to 3.3V at Topr = -20 to 85 °C / -40 to 85 °C, f(XIN)=10MHz unless otherwise specified.

Table 5.18 Electrical Characteristics (4) [Vcc=3V]

| Symbol | Parameter | Measuring condition | Standard | | | Unit | |
|---|--|---|--|--|------|------|----|
| | | | Min. | Typ. | Max. | | |
| I _{cc} | Power supply current (V _{cc} =2.7 to 3.3V) In single-chip mode, the output pins are open and other pins are V _{ss} | High-speed mode X _{IN} =20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz No division | — | 8 | 13 | mA | |
| | | | X _{IN} =16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz No division | — | 7 | 12 | mA |
| | | | | X _{IN} =10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz No division | — | 5 | — |
| | | Medium-speed mode X _{IN} =20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz Division by 8 | — | | 3 | — | mA |
| | | | X _{IN} =16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz Division by 8 | — | 2.5 | — | mA |
| | | | | X _{IN} =10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz Division by 8 | — | 1.6 | — |
| | | High-speed on-chip oscillator mode Main clock off High-speed on-chip oscillator on=8 MHz Low-speed on-chip oscillator on=125 kHz No division | — | | 3.5 | 7.5 | mA |
| | | | Main clock off High-speed on-chip oscillator on=8 MHz Low-speed on-chip oscillator on=125 kHz Division by 8 | — | 1.5 | — | mA |
| | | Low-speed on-chip oscillator mode Main clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz Division by 8 | | — | 420 | 800 | μA |
| | | Wait mode Main clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz When a WAIT instruction is executed ⁽¹⁾ Peripheral clock operation VC27="0" | — | 37 | 74 | μA | |
| Wait mode Main clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on=125 kHz When a WAIT instruction is executed ⁽¹⁾ Peripheral clock off VC27="0" | — | | 35 | 70 | μA | | |
| | Stop mode Main clock off, T _{opr} = 25 °C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10="1" Peripheral clock off VC27="0" | — | 0.7 | 3.0 | μA | | |

NOTES:

1. Timer Y is operated with timer mode.
2. Referenced to V_{cc} = AV_{cc} = 2.7 to 3.3V at T_{opr} = -20 to 85 °C / -40 to 85 °C, f(X_{IN})=10MHz unless otherwise specified.

Timing requirements (Unless otherwise noted: Vcc = 3V, Vss = 0V at Topr = 25 °C) [Vcc=3V]**Table 5.19 XIN input**

| Symbol | Parameter | Standard | | Unit |
|----------|----------------------------|----------|------|------|
| | | Min. | Max. | |
| tC(XIN) | XIN input cycle time | 100 | – | ns |
| tWH(XIN) | XIN input HIGH pulse width | 40 | – | ns |
| tWL(XIN) | XIN input LOW pulse width | 40 | – | ns |

Table 5.20 CNTR0 input, CNTR1 input, INT2 input

| Symbol | Parameter | Standard | | Unit |
|------------|------------------------------|----------|------|------|
| | | Min. | Max. | |
| tC(CNTR0) | CNTR0 input cycle time | 300 | – | ns |
| tWH(CNTR0) | CNTR0 input HIGH pulse width | 120 | – | ns |
| tWL(CNTR0) | CNTR0 input LOW pulse width | 120 | – | ns |

Table 5.21 TCIN input, INT3 input

| Symbol | Parameter | Standard | | Unit |
|-----------|-----------------------------|---------------------|------|------|
| | | Min. | Max. | |
| tC(TCIN) | TCIN input cycle time | 1200 ⁽¹⁾ | – | ns |
| tWH(TCIN) | TCIN input HIGH pulse width | 600 ⁽²⁾ | – | ns |
| tWL(TCIN) | TCIN input LOW pulse width | 600 ⁽²⁾ | – | ns |

NOTES:

1. When using the Timer C input capture mode, adjust the cycle time above (1/ Timer C count source frequency x 3).
2. When using the Timer C input capture mode, adjust the pulse width above (1/ Timer C count source frequency x 1.5).

Table 5.22 Serial Interface

| Symbol | Parameter | Standard | | Unit |
|----------|-----------------------------|----------|------|------|
| | | Min. | Max. | |
| tC(CK) | CLKi input cycle time | 300 | – | ns |
| tW(CKH) | CLKi input HIGH pulse width | 150 | – | ns |
| tW(CKL) | CLKi input LOW pulse width | 150 | – | ns |
| td(C-Q) | TxDi output delay time | – | 160 | ns |
| th(C-Q) | TxDi hold time | 0 | – | ns |
| tsu(D-C) | RxDi input setup time | 55 | – | ns |
| th(C-D) | RxDi input hold time | 90 | – | ns |

Table 5.23 External interrupt INT0 input

| Symbol | Parameter | Standard | | Unit |
|---------|-----------------------------|--------------------|------|------|
| | | Min. | Max. | |
| tW(INH) | INT0 input HIGH pulse width | 380 ⁽¹⁾ | – | ns |
| tW(INL) | INT0 input LOW pulse width | 380 ⁽²⁾ | – | ns |

NOTES:

1. When selecting the digital filter by the INT0 input filter select bit, use the INT0 input HIGH pulse width to the greater value, either (1/ digital filter clock frequency x 3) or the minimum value of standard.
2. When selecting the digital filter by the INT0 input filter select bit, use the INT0 input LOW pulse width to the greater value, either (1/ digital filter clock frequency x 3) or the minimum value of standard.

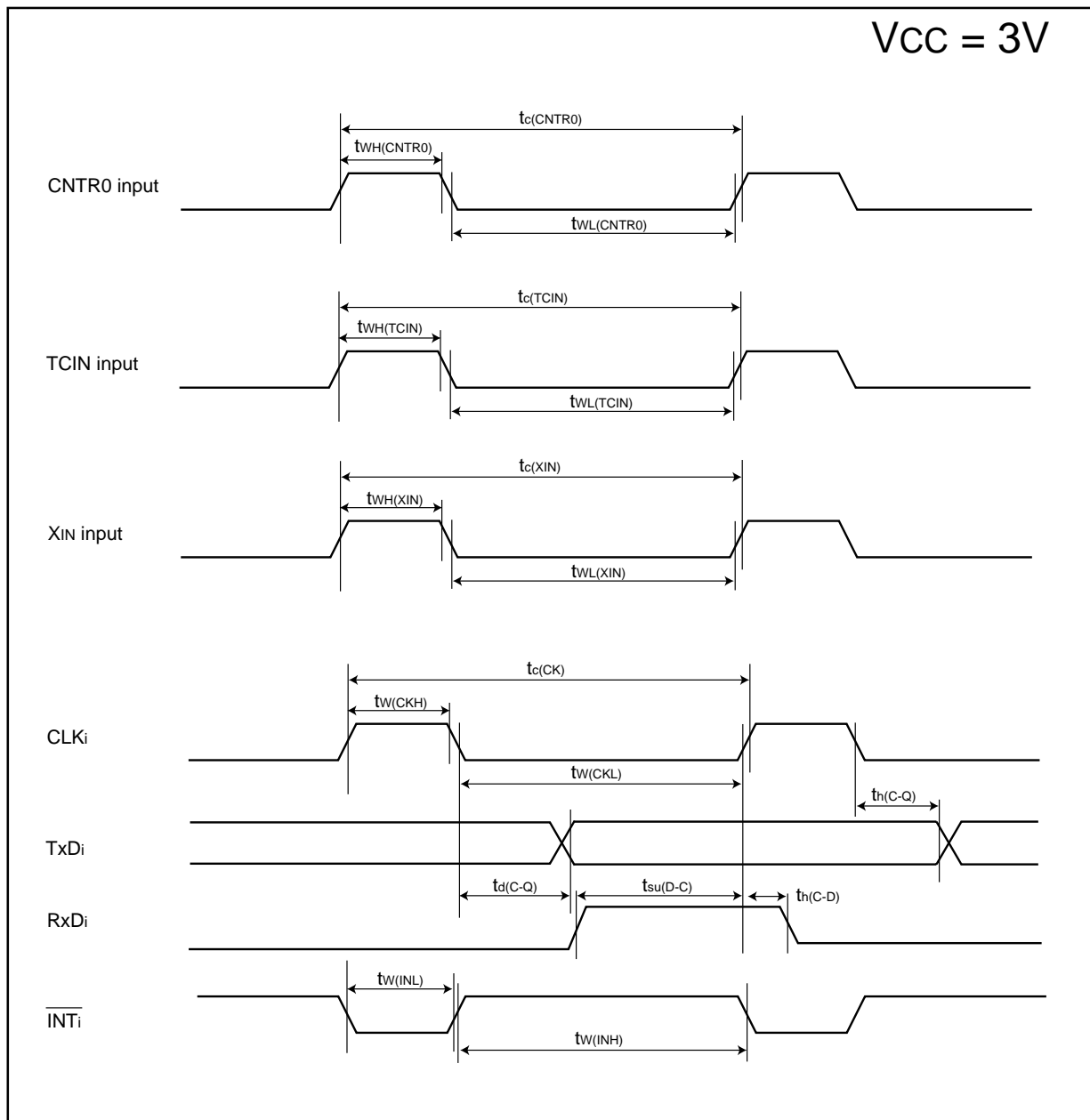
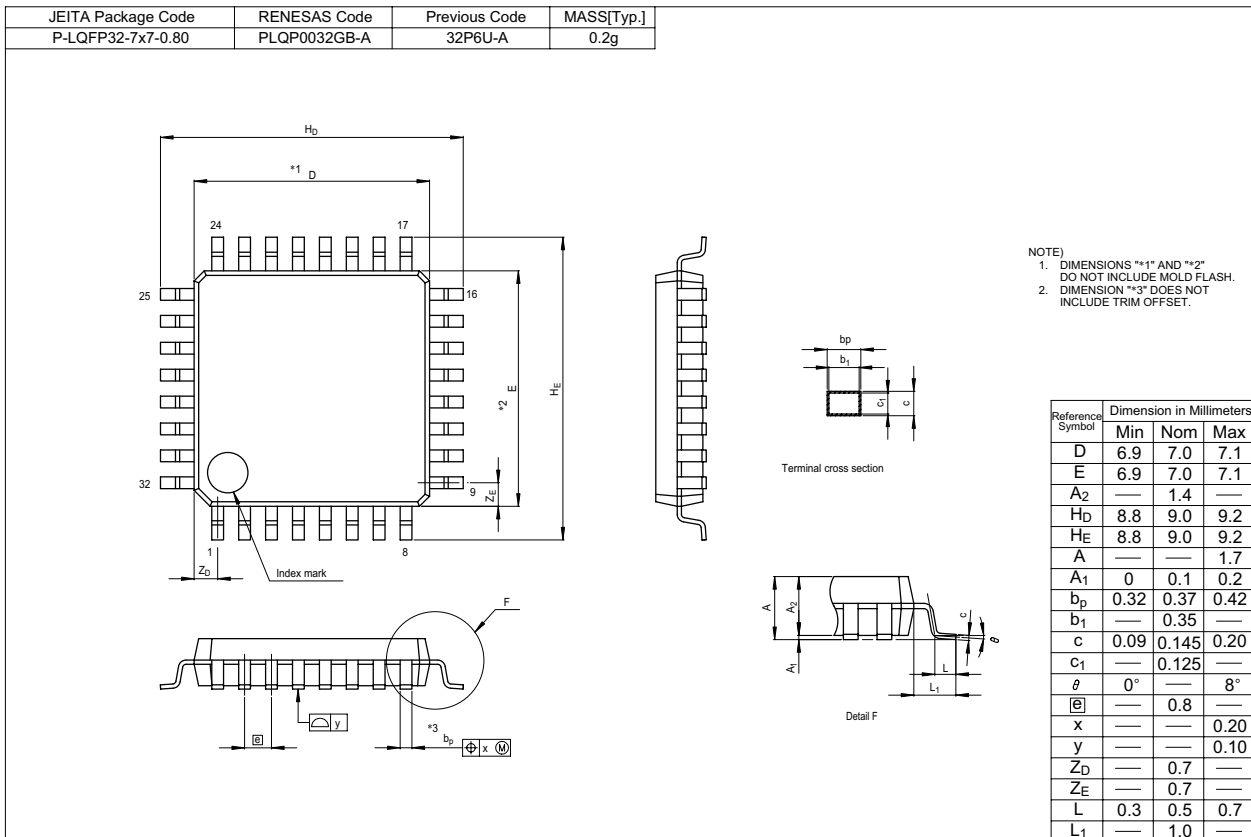


Figure 5.5 Vcc=3V timing diagram

Package Dimensions



REVISION HISTORY

R8C/11 Group Datasheet

| Rev. | Date | Description | |
|------|---------------|--|--|
| | | Page | Summary |
| 1.00 | Jun. 19, 2003 | | First edition issued |
| 1.10 | Sep. 08, 2003 | 2 5 6 10 12 14 | Table 1.1: Shortest instruction execution time and $f(XIN)$ changed Figure 1.3: Pin name changed from TXOUT to $CNTR\bar{0}$ Table 1.3: Pin name changed from TXOUT to $CNTR\bar{0}$ The value of HR1 register after reset changed The value of TC register after reset changed Chapter "5. Electrical Characteristics" added |
| 1.20 | Oct. 31, 2003 | 2 6 11 14 15 17 19 20 21 22 23 24 25 | Table 1.1: Power consumption values added Table 1.3: Resistor value for CNV_{SS} and MODE deleted Register name of address 0050 ₁₆ modified from CMP2IC to CMP1IC, register name of address 005C ₁₆ modified from CMP1IC to CMP0IC Table 5.2: Note 3 and Note 4 deleted t_{samp} in Table 5.3 deleted Figure 5.1 added Table 5.10: V_{CC} changed from "4.2 to 5.5V" to "3.3V to 5.5V", low-power on-chip oscillator changed from "on 100kHz" to "125kHz", $XIN=5MHz$ deleted and $XIN=10MHz$ added in high-speed mode and medium-speed mode, $VC27="0"$ added in stop mode measuring condition, data added and modified Table 11 to Table 15 added Figure 5.2 added Table 5.16: Note 1, $f(BCLK)=5 MHz$ changed to 10 MHz Table 5.17: low-power ring oscillator changed from "on 100kHz" to "125kHz", $XIN=5MHz$ deleted and $XIN=10MHz$ added in high-speed mode and medium-speed mode, $VC27="0"$ added in stop mode measuring condition, data added and modified Table 5.18 to Table 5.22 added Figure 5.3 added |
| 1.30 | Dec 05, 2003 | 4 15 | Table 1.2 : ** deleted Table 5.4 revised |
| 1.40 | Sep 30, 2004 | all pages 2 5 6 9 10-13 12 14 15 16 17 18 | Words standardized (on-chip oscillator, serial interface, A/D) Table 1.1 revised Figure 1.3, NOTES 3 added Table 1.3 revised Figure 3.1, NOTES added One body sentence in chapter 4 added ; Title of Table 4.1 to 4.4 added Table 4.3 revised ; Table 4.4 revised Table 5.2 revised Table 5.3 revised Table 5.4 revised ; Table 16.5 revised Table 5.6, 5.7 adn 5.8 revised ; Figure 5.3 revised Table 5.9 revised ; Table 5.10 revised |

REVISION HISTORY

R8C/11 Group Datasheet

| Rev. | Date | Description | |
|------|----------------------------|-------------|--|
| | | Page | Summary |
| 1.40 | Sep 30, 2004 | 20 | Table 5.12 revised ; Table 5.16 revised |
| | | 22 | Table 16.17 revised |
| | | 24 | Table 16.19 revised |
| 1.50 | Apr.27.2005 | 4 | Table 1.2, Figure 1.2 package name revised |
| | | 5 | Figure 1.3 package name revised |
| | | 10 | Table 4.1 revised |
| | | 12 | Table 4.3 revised |
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| | | 18 | Table 5.9, Table 10 partly revised |
| | | 22 | Table 5.17 partly revised |
| 26 | Package Dimensions revised | | |
| 1.60 | Jan.27.2006 | 2 | Table 1.1 Performance outline revised |
| | | 3 | Figure 1.1 Block diagram partly revised |
| | | 4 | 1.4 Product Information, title of Table 1.2 "Product List" → "Product Informaton" revised |
| | | | Figure 1.2 Type No., Memory Size, and Package partly revised |
| | | 6 | Table 1.3 Pin description revised |
| | | 7-8 | 2 Central Processing Unit (CPU) revised |
| | | | Figure 2.1 CPU register revised |
| | | 10 | Table 4.1 SFR Information(1) NOTES:1 revised |
| | | 11 | Table 4.2 SFR Information(2) NOTES:1 revised |
| | | 12 | Table 4.3 SFR Information(3); 0081 ₁₆ : "Prescaler Y" → "Prescaler Y Register" 0082 ₁₆ : "Timer Y Secondary" → "Timer Y Secondary Register" 0083 ₁₆ : "Timer Y Primary" → "Timer Y Primary Register" 0085 ₁₆ : "Prescaler Z" → "Prescaler Z Register" 0086 ₁₆ : "Timer Z Secondary" → "Timer Z Secondary Register" 0087 ₁₆ : "Timer Z Primary" → "Timer Z Primary Register" 008C ₁₆ : "Prescaler X" → "Prescaler X Register" revised NOTES:1, 2 revised |
| | | 13 | Table 4.4 SFR Information(4) NOTES:1 revised |
| | | 14 | Table 5.2 Recommended Operating Conditions; NOTES: 1, 2, 3 revised |
| | | 15 | Table 5.3 A/D Conversion Characteristics; "A/D operation clock frequency" → "A/D operating clock frequency" revised NOTES: 1, 2, 3, 4 revised |
| | | 16 | Table 5.4 Flash Memory (Program ROM) Electrical Characteristics; "Topr" → "Ambient temperature" revised Measuring condition of byte program time and block erase time deleted |
| | | 17 | Table 5.6 Reset Circuit Electrical Characteristics (When Using Hardware Reset 2) NOTES: 3 revised |
| | | 18 | Table 5.8 High-speed On-Chip Oscillator Circuit Electrical Characteristics; "High-speed on-chip oscillator temperature dependence" → "High-speed on-chip oscillator frequency temperature dependence" revised Table 5.10 Electrical Characteristics (1) [V _{CC} =5V]; "P1 ₀ to P1 ₇ Except Xout" → "Except P1 ₀ to P1 ₇ , Xout" revised |

REVISION HISTORY

R8C/11 Group Datasheet

| Rev. | Date | Description | |
|------|-------------|-------------|---|
| | | Page | Summary |
| 1.60 | Jan.27.2006 | 19 | Table 5.11 Electrical Characteristics (2) [Vcc=5V] NOTES: 1, 2 revised Measuring condition Stop mode: "Topr = 25 °C" |
| | | 22 | Table 5.17 Electrical Characteristics (3) [Vcc=3V] "P1 ₀ to P1 ₇ Except X _{OUT} " → "Except P1 ₀ to P1 ₇ , X _{OUT} " revised |
| | | 23 | Table 5.18 Electrical Characteristics (4) [Vcc=3V] NOTES: 1, 2 revised Measuring condition Stop mode: "Topr = 25 °C" |
| | | | |

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