

TOSHIBA Multi-chip Device  
Silicon PNP Epitaxial Transistor , Field Effect Transistor Silicon N Channel MOS Type

# TPCP8F01

- Switching Applications
- Load Switch Applications
- Multi-chip discrete device; built-in PNP Transistor for main switch and N-ch MOS FET for drive

- High DC current gain:  $h_{FE} = 200$  to  $500$  ( $I_C = -0.5$  A)  
(PNP Transistor)
- Low collector-emitter saturation:  $V_{CE(sat)} = -0.19$  V (max)  
(PNP Transistor)
- High-speed switching:  $t_f = 40$  ns (typ.) (PNP Transistor)

## Absolute Maximum Ratings ( $T_a = 25^\circ\text{C}$ )

### Transistor

Characteristics		Symbol	Rating	Unit
Collector-base voltage		$V_{CBO}$	-30	V
Collector-emitter voltage		$V_{CEO}$	-20	V
Emitter-base voltage		$V_{EBO}$	-7	V
Collector current	DC	$I_C$	-3.0	A
	Pulse	$I_{CP}$	-5.0	
Base current		$I_B$	-250	mA
Collector power dissipation		$P_C$ (Note 1)	1.0	W
Junction temperature		$T_j$	150	$^\circ\text{C}$

### MOS FET

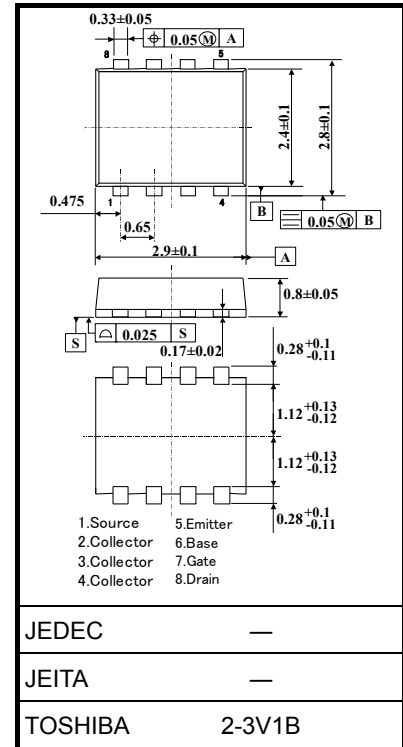
Characteristics		Symbol	Rating	Unit
Drain-source voltage		$V_{DSS}$	20	V
Gate-source voltage		$V_{GSS}$	$\pm 10$	V
Drain current	DC	$I_D$	100	mA
	Pulse	$I_{DP}$	200	
Channel temperature		$T_j$	150	$^\circ\text{C}$

Note 1: Mounted on FR4 board (glass epoxy, 1.6mm thick, Cu area: 645mm<sup>2</sup>)

Note 2: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/Derating Concept and Methods) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Unit: mm

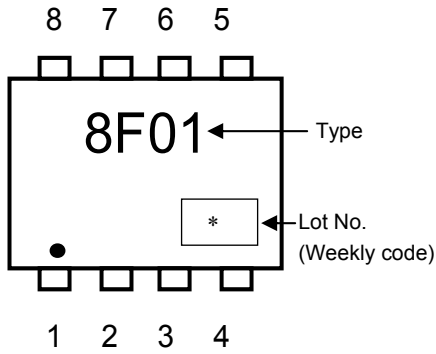


Weight : 0.017g (Typ.)

## Common Absolute Maximum Rating (Ta = 25°C)

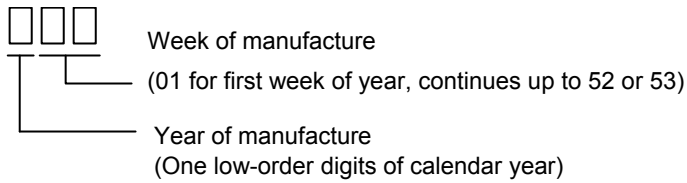
Characteristics	Symbol	Rating	Unit
Storage temperature range	T <sub>stg</sub>	-55 to 150	°C

### Figure 2 Marking (Note 3)



Note 3 : Black round marking " • " located on the left lower side of parts number marking "8F01" indicates terminal No.1

\* Weekly code: (Three digits)

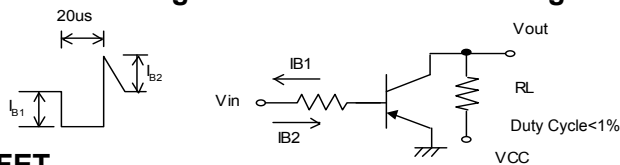


## Electrical Characteristics (Ta = 25°C)

### Transistor

Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Collector cut-off current		$I_{CBO}$	$V_{CB} = -30\text{ V}, I_E = 0$	—	—	-100	nA
Emitter cut-off current		$I_{EBO}$	$V_{EB} = -7\text{ V}, I_C = 0$	—	—	-100	nA
Collector-emitter breakdown voltage		$V_{(BR)CEO}$	$I_C = -10\text{ mA}, I_B = 0$	-20	—	—	V
DC current gain	$h_{FE}(1)$		$V_{CE} = -2\text{ V}, I_C = -0.5\text{ A}$	200	—	500	
	$h_{FE}(2)$		$V_{CE} = -2\text{ V}, I_C = -1.6\text{ A}$	100	—	—	
Collector-emitter saturation voltage		$V_{CE(sat)}$	$I_C = -1.6\text{ A}, I_B = -53\text{ mA}$	—	—	-0.19	V
Base-emitter saturation voltage		$V_{BE(sat)}$	$I_C = -1.6\text{ A}, I_B = -53\text{ mA}$	—	—	-1.10	V
Collector Output Capacitance		$C_{ob}$	$V_{CB} = -10\text{ V}, I_E = 0, f = 1\text{ MHz}$	—	28	—	pF
Switching time	Rise time	$t_r$	See Figure 3 circuit diagram $V_{CC} \approx -12\text{ V}, R_L = 7.5\ \Omega$ $-I_{B1} = I_{B2} = -53\text{ mA}$	—	70	—	ns
	Storage time	$t_{stg}$		—	150	—	
	Fall time	$t_f$		—	40	—	

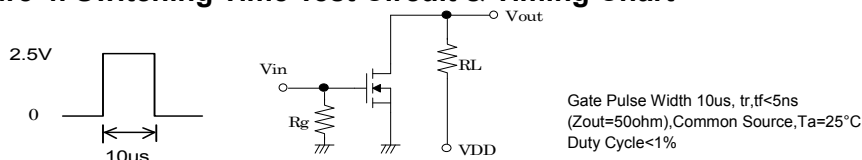
**Figure 3. Switching Time Test Circuit & Timing Chart**



### MOS FET

Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		$I_{GSS}$	$V_{GS} = -10\text{ V}, V_{DS} = 0$	—	—	±1	µA
Drain-source breakdown voltage		$V_{(BR)DSS}$	$I_D = 0.1\text{ mA}, V_{GS} = 0$	20	—	—	V
Drain cut-off current		$I_{DSS}$	$V_{DS} = 20\text{ V}, V_{GS} = 0$	—	—	1	µA
Gate Threshold voltage		$V_{th}$	$V_{DS} = 3\text{ V}, I_D = 0.1\text{ mA}$	0.6	—	1.1	V
Forward Transfer Admittance		$ Y_{fs} $	$V_{DS} = 3\text{ V}, I_D = 10\text{ mA}$	40	—	—	mS
Drain-source ON resistance	$R_{DS(ON)}$		$I_D = 10\text{ mA}, V_{GS} = 4.0\text{ V}$	—	1.5	3	Ω
			$I_D = 10\text{ mA}, V_{GS} = 2.5\text{ V}$	—	2.2	4	
			$I_D = 1\text{ mA}, V_{GS} = 1.5\text{ V}$	—	5.2	15	
Input capacitance		$C_{iss}$	$V_{DS} = 3\text{ V}, V_{GS} = 0, f = 1\text{ MHz}$	—	9.3	—	pF
Reverse transfer capacitance		$C_{rss}$		—	4.5	—	
Output capacitance		$C_{oss}$		—	9.8	—	
Switching time	Turn-on time	$t_{on}$	$V_{DD} \approx -3\text{ V}, R_L = 300\ \Omega$ $V_{GS} = 0\text{ to }2.5\text{ V}$	—	70	—	ns
	Turn-off time	$t_{off}$		—	125	—	

**Figure 4. Switching Time Test Circuit & Timing Chart**



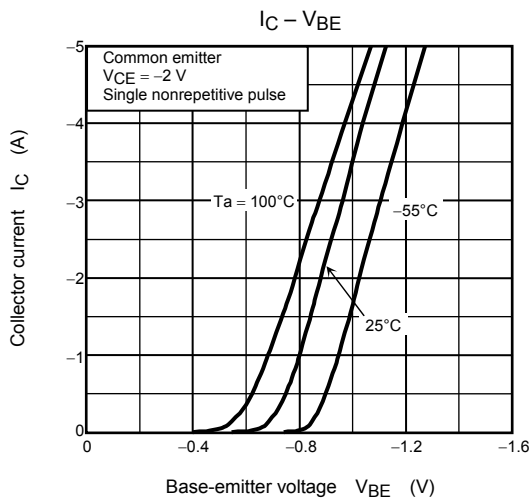
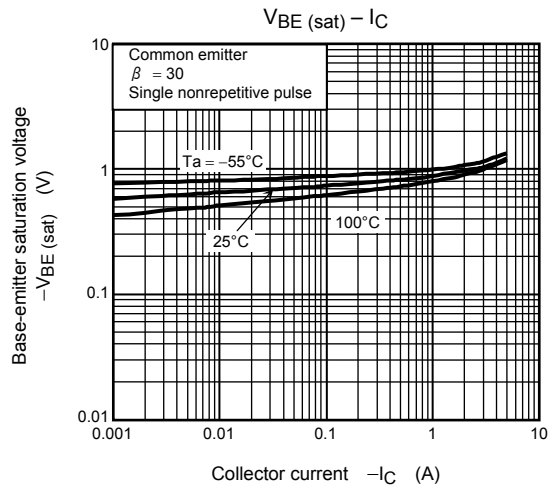
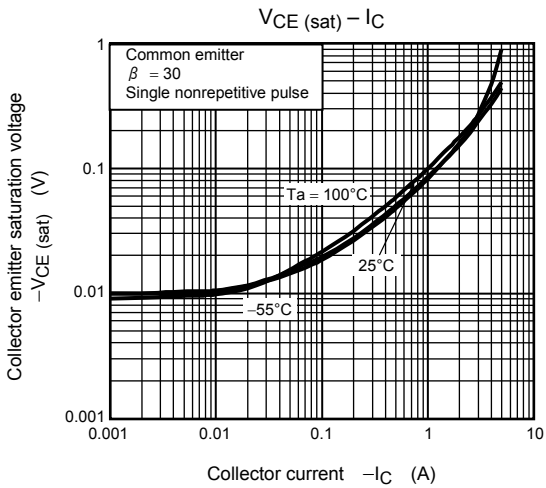
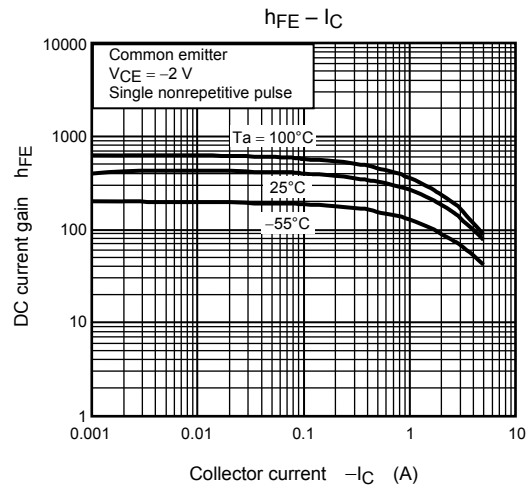
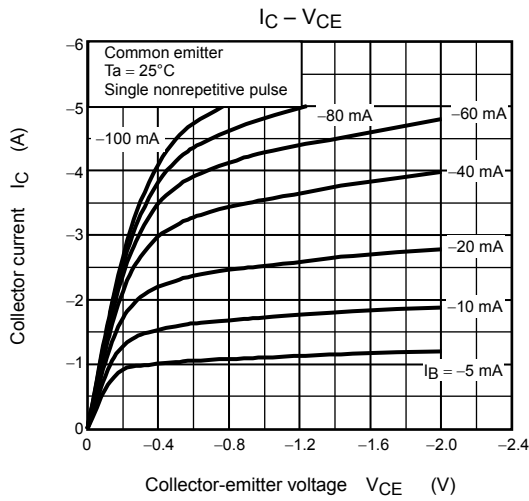
### Precautions

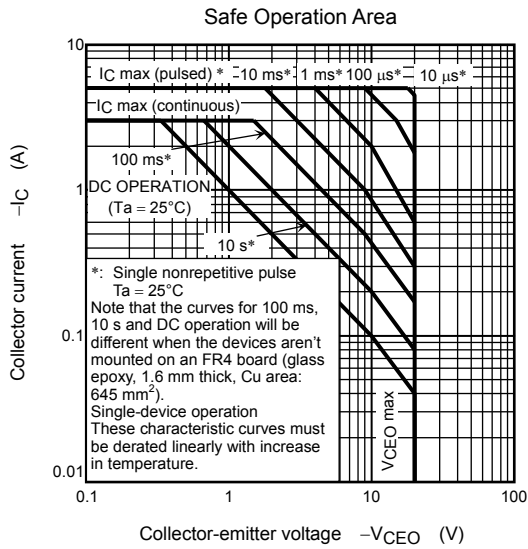
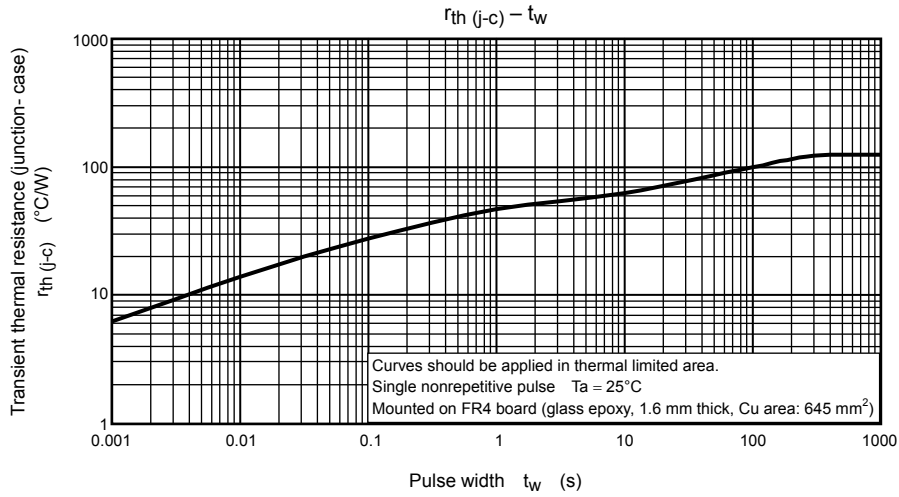
$V_{th}$  can be expressed as voltage between gate and source when low operating current value is  $I_D = 100\ \mu\text{A}$  for this product. For normal switching operation,  $V_{GS(ON)}$  requires higher voltage than  $V_{th}$  and  $V_{GS(OFF)}$  requires lower voltage than  $V_{th}$ . (relationship can be established as follows:  $V_{GS(OFF)} < V_{th} < V_{GS(ON)}$ )

Please take this into consideration for using the device.

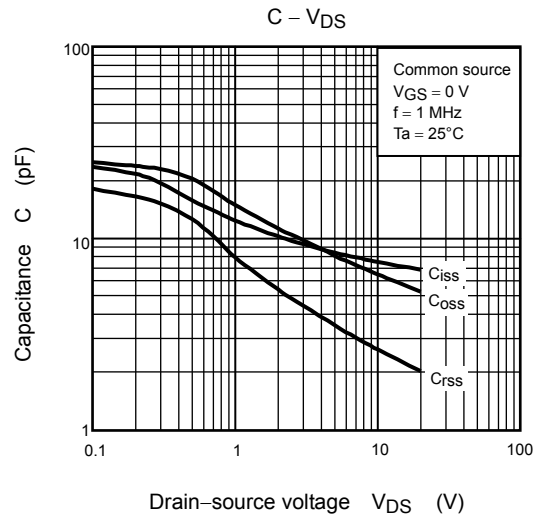
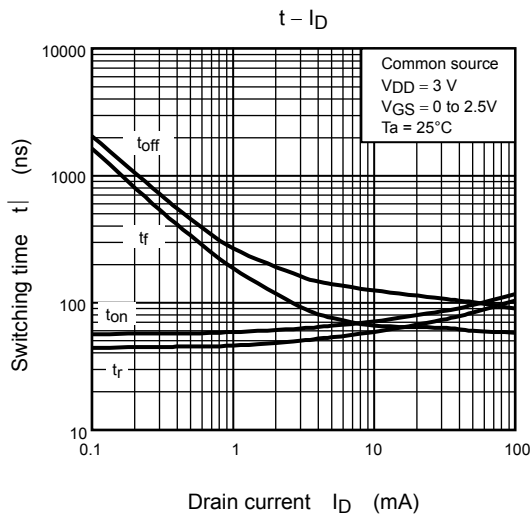
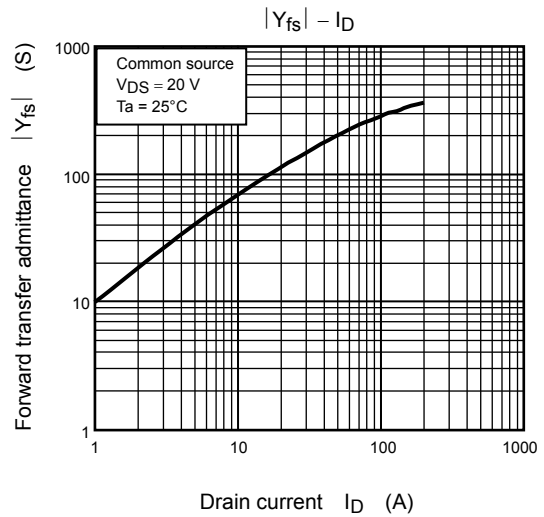
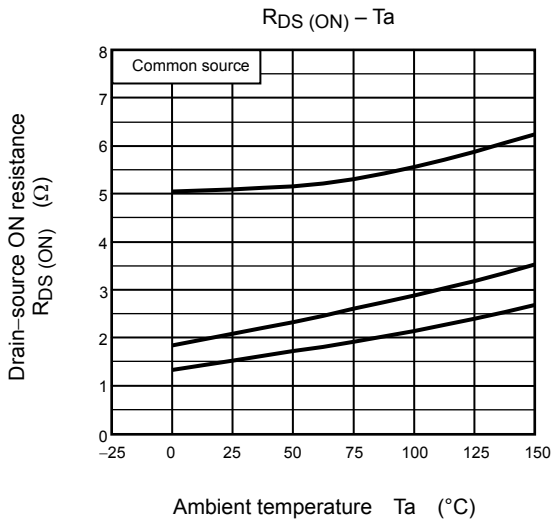
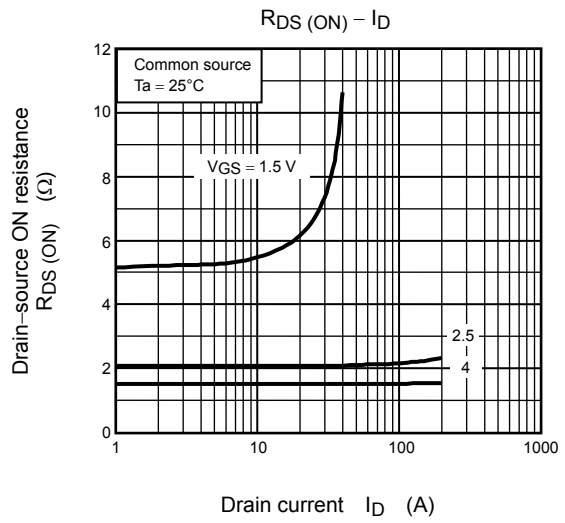
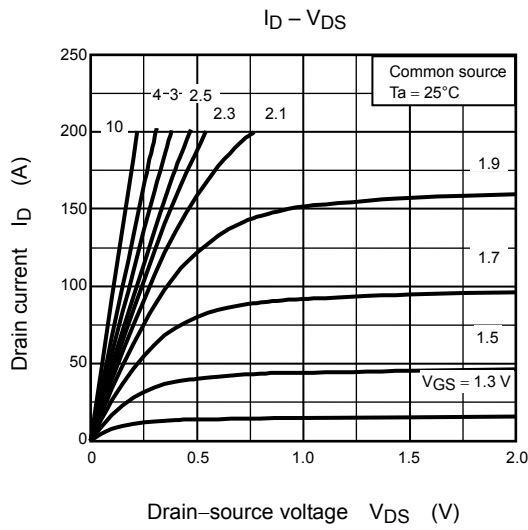
$V_{GS}$  recommended voltage of 2.5V or higher to turn on this product.

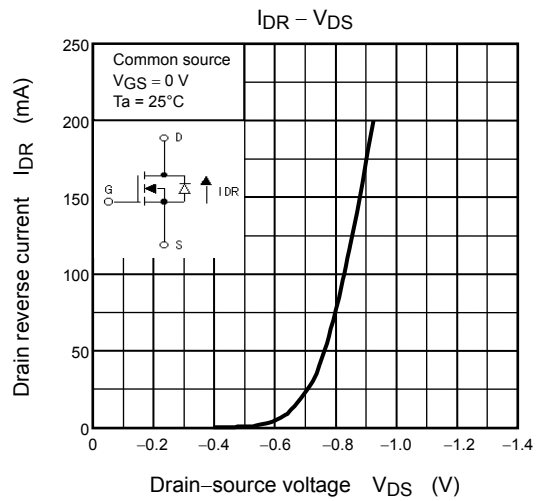
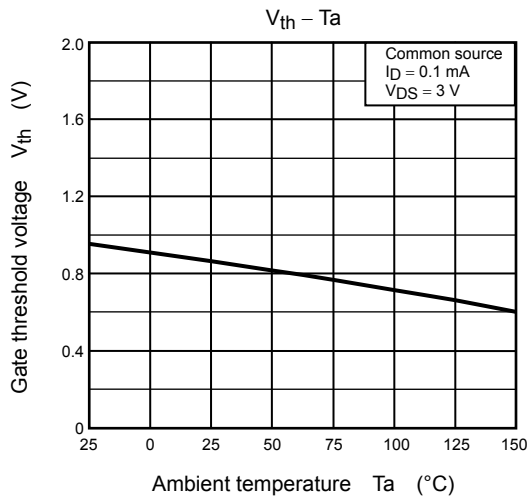
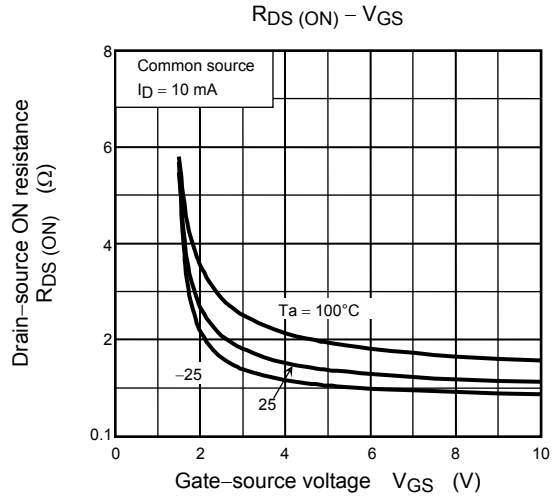
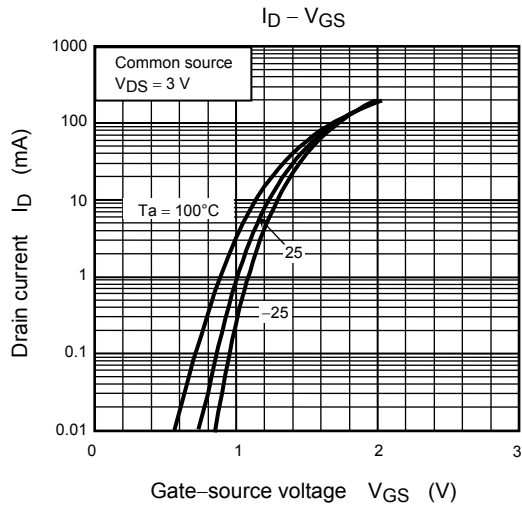
**PNP**





## Nch-MOS





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