# HEF4077B-Q100

# Quad 2-input EXCLUSIVE-NOR gate Rev. 1 — 14 March 2017

**Product data sheet** 

# **General description**

The HEF4077B-Q100 is a quad 2-input EXCLUSIVE-NOR gate. The outputs are fully buffered for the highest noise immunity and pattern insensitivity to output impedance.

The HEF4077B-Q100 operates over a recommended V<sub>DD</sub> power supply range of 3 V to 15 V referenced to V<sub>SS</sub> (usually ground). Unused inputs must be connected to V<sub>DD</sub>, V<sub>SS</sub>, or another input.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 3) and is suitable for use in automotive applications.

#### **Features and benefits**

- Automotive product qualification in accordance with AEC-Q100 (Grade 3)
  - Specified from -40 °C to +85 °C
- Fully static operation
- 5 V, 10 V, and 15 V parametric ratings
- Standardized symmetrical output characteristics
- ESD protection:
  - MIL-STD-883, method 3015 exceeds 2000 V
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V (C = 200 pF, R = 0  $\Omega$ )
- Complies with JEDEC standard JESD 13-B

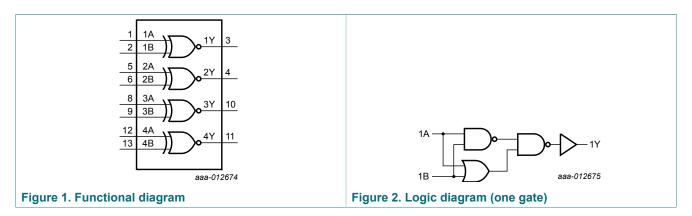
# **Ordering information**

#### **Table 1. Ordering information**

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Type number	Package				
	Temperature range	Name	Description	Version	
HEF4077BT-Q100	-40 °C to +85 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1	

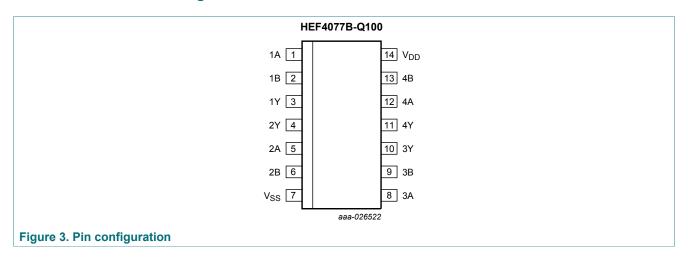


# 4 Functional diagram



# 5 Pinning information

#### 5.1 Pinning



# 5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
1A to 4A	1, 5, 8, 12	input
1B to 4B	2, 6, 9, 13	input
1Y to 4Y	3, 4, 10, 11	output
V <sub>SS</sub>	7	ground (0 V)
$V_{DD}$	14	supply voltage

# 6 Functional description

Table 3. Functional table [1]

Input		Output
nA	nB	nY
L	L	Н
L	Н	L
Н	L	L
Н	Н	Н

<sup>[1]</sup> H = HIGH voltage level;

# 7 Limiting values

#### Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to  $V_{\rm SS}$  = 0 V (ground).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DD}$	supply voltage		-0.5	+18	V
I <sub>IK</sub>	input clamping current	$V_{I} < -0.5 \text{ V or } V_{I} > V_{DD} + 0.5 \text{ V}$	-	±10	mA
VI	input voltage		-0.5	V <sub>DD</sub> + 0.5	V
lok	output clamping current	$V_{O} < -0.5 \text{ V or } V_{O} > V_{DD} + 0.5 \text{ V}$	-	±10	mA
I <sub>I/O</sub>	input/output current		-	±10	mA
I <sub>DD</sub>	supply current		-	50	mA
T <sub>stg</sub>	storage temperature		-65	+150	°C
T <sub>amb</sub>	ambient temperature		-40	+85	°C
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> = -40 °C to +85 °C			
		SO14 package [1]	-	500	mW
Р	power dissipation	per output	-	100	mW

<sup>[1]</sup> For SO14 package:  $P_{tot}$  derates linearly with 8 mW/K above 70 °C.

# 8 Recommended operating conditions

**Table 5. Operating conditions** 

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DD}$	supply voltage		3	15	V
VI	input voltage		0	$V_{DD}$	V
T <sub>amb</sub>	ambient temperature	in free air	-40	+85	°C
Δt/ΔV	Δt/ΔV input transition rise and fall rate	V <sub>DD</sub> = 5 V	-	3.75	μs/V
		V <sub>DD</sub> = 10 V	-	0.5	μs/V
		V <sub>DD</sub> = 15 V	-	0.08	μs/V

HEF4077B\_Q100

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L = LOW voltage level

# 9 Static characteristics

#### **Table 6. Static characteristics**

 $V_{SS} = 0 \ V$ ;  $V_I = V_{SS}$  or  $V_{DD}$  unless otherwise specified.

Symbol	Parameter	Conditions	V <sub>DD</sub>	T <sub>amb</sub> =	-40 °C	T <sub>amb</sub> =	25 °C	T <sub>amb</sub> =	85 °C	Unit
				Min	Max	Min	Max	Min	Max	
V <sub>IH</sub>	HIGH-level	I <sub>O</sub>   < 1 μΑ	5 V	3.5	-	3.5	-	3.5	-	V
	input voltage		10 V	7.0	-	7.0	-	7.0	-	V
			15 V	11.0	-	11.0	-	11.0	-	V
V <sub>IL</sub>	LOW-level	I <sub>O</sub>   < 1 μΑ	5 V	-	1.5	-	1.5	-	1.5	V
	input voltage		10 V	-	3.0	-	3.0	-	3.0	V
			15 V	-	4.0	-	4.0	-	4.0	V
V <sub>OH</sub>	HIGH-level	I <sub>O</sub>   < 1 μA	5 V	4.95	-	4.95	-	4.95	-	V
	output voltage		10 V	9.95	-	9.95	-	9.95	-	V
			15 V	14.95	-	14.95	-	14.95	-	V
V <sub>OL</sub>	V <sub>OL</sub> LOW-level output voltage	I <sub>O</sub>   < 1 μA	5 V	-	0.05	-	0.05	-	0.05	V
			10 V	-	0.05	-	0.05	-	0.05	V
			15 V	-	0.05	-	0.05	-	0.05	V
I <sub>OH</sub>	HIGH-level	V <sub>O</sub> = 2.5 V	5 V	-	-1.7	-	-1.4	-	-1.1	mA
	output current	V <sub>O</sub> = 4.6 V	5 V	-	-0.52	-	-0.44	-	-0.36	mA
		V <sub>O</sub> = 9.5 V	10 V	-	-1.3	-	-1.1	-	-0.9	mA
		V <sub>O</sub> = 13.5 V	15 V	-	-3.6	-	-3.0	-	-2.4	mA
I <sub>OL</sub>	LOW-level	V <sub>O</sub> = 0.4 V	5 V	0.52	-	0.44	-	0.36	-	mA
	output current	V <sub>O</sub> = 0.5 V	10 V	1.3	-	1.1	-	0.9	-	mA
		V <sub>O</sub> = 1.5 V	15 V	3.6	-	3.0	-	2.4	-	mA
I <sub>I</sub>	input leakage current		15 V	-	±0.3	-	±0.3	-	±3.0	μΑ
I <sub>DD</sub>	supply current	all valid input	5 V	-	1.0	-	1.0	-	7.5	μA
		combinations; I <sub>O</sub> = 0 A	10 V	-	2.0	-	2.0	-	15.0	μA
		10 - 0 7	15 V	-	4.0	-	4.0	-	30.0	μA
Cı	input capacitance		-	-	-	-	7.5	-	-	pF

# 10 Dynamic characteristics

# Table 7. Dynamic characteristics [1]

 $T_{amb}$  = 25 °C; unless otherwise specified; for waveform see Figure 4; for test circuit see Figure 5.

Symbol	Parameter	Conditions	V <sub>DD</sub>	Extrapolation formula	Min	Тур	Max	Unit
t <sub>PHL</sub>	HIGH to LOW	nA or nB to nY	5 V	48 ns + (0.55 ns/pF)C <sub>L</sub>	-	75	150	ns
	propagation delay		10 V	24 ns + (0.23 ns/pF)C <sub>L</sub>	-	35	70	ns
			15 V	22 ns + (0.16 ns/pF)C <sub>L</sub>	-	30	55	ns
t <sub>PLH</sub>	LOW to HIGH	nA or nB to nY	5 V	43 ns + (0.55 ns/pF)C <sub>L</sub>	-	70	145	ns
	propagation delay		10 V	19 ns + (0.23 ns/pF)C <sub>L</sub>	-	30	60	ns
			15 V	17 ns + (0.16 ns/pF)C <sub>L</sub>	-	25	50	ns
t <sub>t</sub>	transition time	nY	5 V <sup>[2]</sup>	10 ns + (1.00 ns/pF)C <sub>L</sub>	-	60	120	ns
			10 V	9 ns + (0.42 ns/pF)C <sub>L</sub>	-	30	60	ns
			15 V	6 ns + (0.28 ns/pF)C <sub>L</sub>	-	20	40	ns

<sup>[1]</sup> The typical value of the propagation delay and output transition time can be calculated with the extrapolation formula (C<sub>L</sub> in pF).

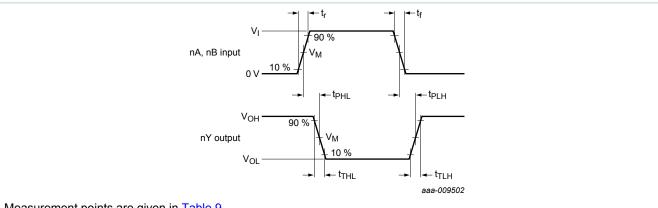
#### **Table 8. Dynamic power dissipation**

 $V_{SS} = 0 \ V; \ t_r = t_f \le 20 \ ns; \ T_{amb} = 25 \ ^{\circ}C.$ 

Symbol	Parameter	$V_{DD}$	Typical formula	where:
$P_{D}$	dynamic power dissipation	5 V		f <sub>i</sub> = input frequency in MHz;
		10 V	$P_D = 4500 \times f_i + \Sigma (f_0 \times C_L) \times V_{DD}^2 (\mu W)$	f <sub>o</sub> = output frequency in MHz; C <sub>L</sub> = output load capacitance in pF;
		15 V	$P_{D} = 114700 \times f_{i} + \Sigma (f_{o} \times C_{L}) \times V_{DD}^{2}$ (µW)	$\Sigma(f_o \times C_L)$ = sum of the outputs; $V_{DD}$ = supply voltage in V.

<sup>[2]</sup> t<sub>t</sub> is the same as t<sub>THL</sub> and t<sub>TLH</sub>.

#### 10.1 Waveform and test circuit



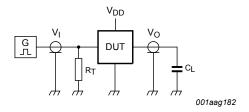
Measurement points are given in Table 9.

Logic levels:  $V_{\text{OL}}$  and  $V_{\text{OH}}$  are typical output voltage levels that occur with the output load.

Figure 4. Input to output propagation delay and output transition times

**Table 9. Measurement points** 

Supply voltage	Input	Output
$V_{DD}$	V <sub>M</sub>	V <sub>M</sub>
5 V to 15 V	0.5V <sub>DD</sub>	0.5V <sub>DD</sub>



Test data is given in Table 10.

Definitions for test circuit:

C<sub>L</sub> = load capacitance including jig and probe capacitance.

 $R_T$  = termination resistance should be equal to the output impedance  $Z_0$  of the pulse generator.

Figure 5. Test circuit

Table 10. Test data

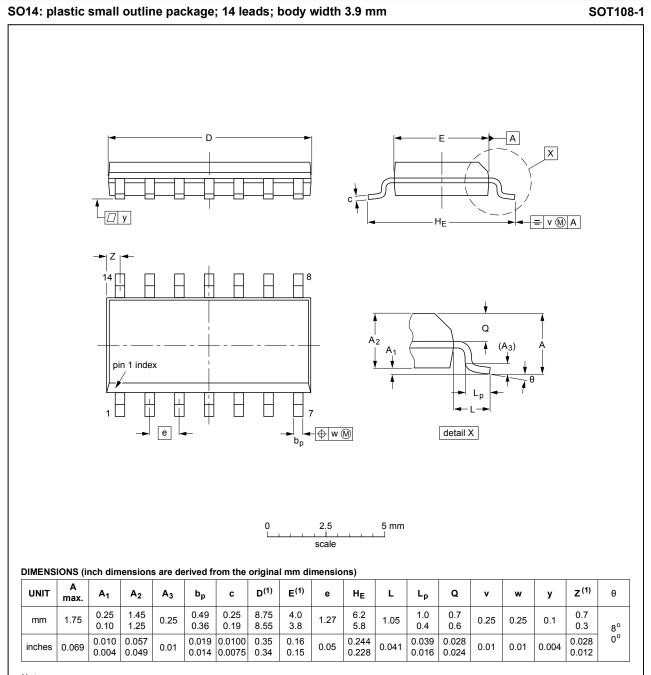
Supply voltage	Input	Load	
$V_{DD}$	VI	t <sub>r</sub> , t <sub>f</sub>	CL
5 V to 15 V	V <sub>SS</sub> or V <sub>DD</sub>	≤ 20 ns	50 pF

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# 11 Package outline



#### Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE REFERENCES				EUROPEAN	ISSUE DATE	
VERSION	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE
SOT108-1	076E06	MS-012				<del>99-12-27</del> 03-02-19

Figure 6. Package outline SOT108-1 (SO14)

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# 12 Abbreviations

#### **Table 11. Abbreviations**

Acronym	Description
DUT	Device Under Test
ESD	ElectroStatic Discharge
НВМ	Human Body Model
MIL	Military
MM	Machine Model

# 13 Revision history

#### **Table 12. Revision history**

Document ID	Release date	Data sheet status	Change notice	Supersedes
HEF4077_Q100 v.1	20170314	Product data sheet	-	-

### 14 Legal information

#### 14.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
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# HEF4077B-Q100

# Quad 2-input EXCLUSIVE-NOR gate

#### **Contents**

1	General description	1
2	Features and benefits	
3	Ordering information	1
4	Functional diagram	
5	Pinning information	
5.1	Pinning	
5.2	Pin description	
6	Functional description	
7	Limiting values	
8	Recommended operating conditions	
9	Static characteristics	
10	Dynamic characteristics	
10.1	Waveform and test circuit	
11	Package outline	7
12	Abbreviations	
13	Revision history	
14	Legal information	

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Date of release: 14 March 2017 Document identifier: HEF4077B\_Q100



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