# ISL78302

Dual LDO with Low Noise, High Performance and Low IQ

FN7696
Rev 6.00
November 6, 2014

ISL78302 is a high performance dual LDO capable of sourcing 300mA current from each output. It has a low standby current and is stable with an output capacitance of 1µF to 10µF and an ESR of up to 200mΩ.

The device integrates an individual Power-On-Reset (POR) function for each output. The POR delay for VO2 can be externally programmed by connecting a timing capacitor to the CPOR pin. The POR delay for VO1 is internally fixed at approximately 2ms. A reference bypass pin is also provided for connecting a noise filtering capacitor for low noise and high-PSRR applications.

The quiescent current is typically only 47µA with both LDOs enabled and active. Separate enable pins control each individual LDO output. When both enable pins are low, the device is in shutdown, typically drawing less than 0.5µA.

The part operates down to 2.3V and up to 6.5V input. The typical output voltage can be as low as 1.2V and as high as 3.3V for each regulator. Please refer to the “Ordering Information” on page 3 for standard options.

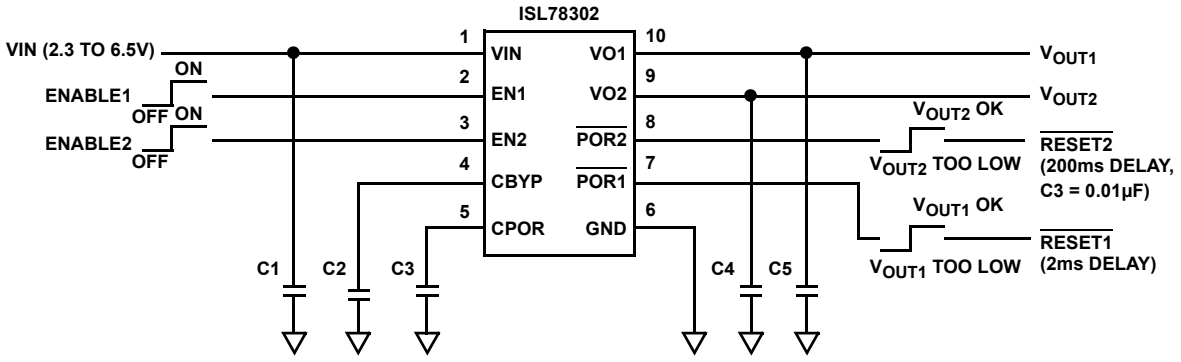
The ISL78302 is AEC-Q100 qualified at the automotive temperature range of -40°C to +105°C.

## Features

- Integrates two 300mA high performance LDOs
- Excellent transient response to large current steps
- ±1.8% Accuracy over all operating conditions
- Excellent load regulation: <0.1% voltage change across full range of load current
- Extremely low quiescent current: 47µA (both LDOs active)
- Wide input voltage capability: 2.3V to 6.5V
- Low dropout voltage: typically 300mV at 300mA
- Low output noise: typically 37µ$V_{RMS}$ at 100µA (1.5V)
- Stable with 1µF to 10µF ceramic capacitors
- Separate enable and POR pins for each LDO
- Soft-start and staged turn-on to limit input current surge during enable
- Current limit and over-temperature protection
- Tiny 10 Lead 3mm x 3mm DFN package
- AEC-Q100 qualified
- Pb-free (RoHS Compliant)

## Applications

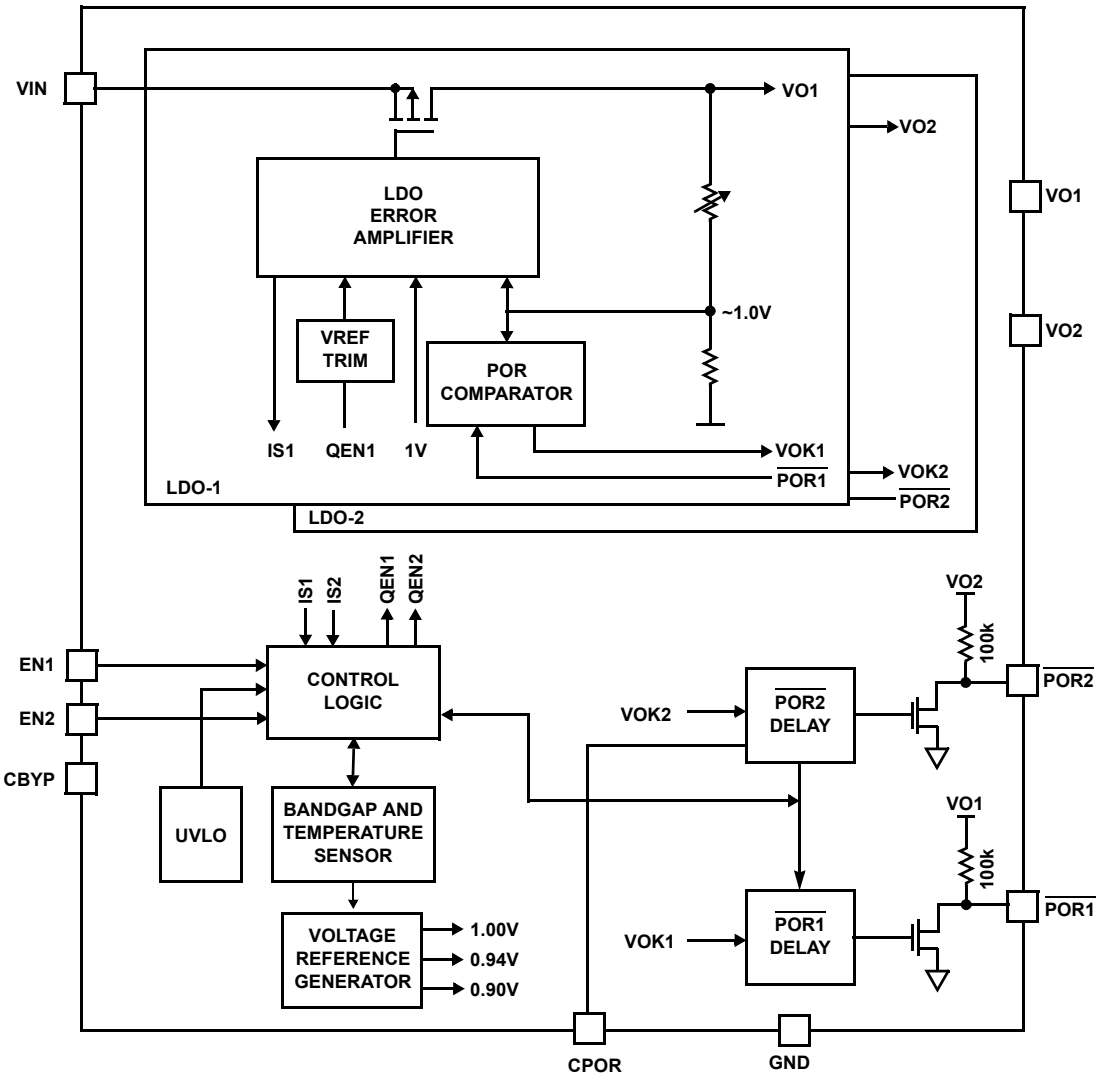
- Radio receivers
- Camera modules
- GPS/navigation
- Infotainment systems




C1, C4, C5: 1µF X5R CERAMIC CAPACITOR
C2: 0.01µF X7R CERAMIC CAPACITOR
C3: 0.01µF X7R CERAMIC CAPACITOR

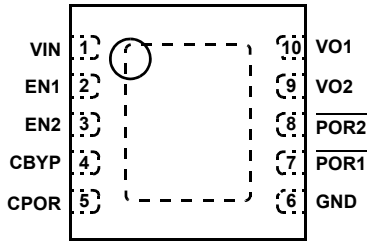
FIGURE 1. TYPICAL APPLICATION

# Block Diagram



# Pin Configuration

ISL78302
(10 LD 3x3 DFN)
TOP VIEW




# Pin Descriptions

| PIN NUMBER | PIN NAME | TYPE | DESCRIPTION |
|---|---|---|---|
| 1 | VIN | Analog I/O | Supply Voltage/LDO Input. Connect a 1µF capacitor to GND. |
| 2 | EN1 | Low Voltage Compatible CMOS Input | LDO-1 Enable. ENABLE = HIGH |
| 3 | EN2 | Low Voltage Compatible CMOS Input | LDO-2 Enable. ENABLE = HIGH |
| 4 | CBYP | Analog I/O | Reference Bypass Capacitor Pin. Recommended to connect capacitor of value 0.01µF between this pin and GND for optimum noise and PSRR performance. |
| 5 | CPOR | Analog I/O | POR2 Delay Setting Capacitor Pin. Connect a capacitor between this pin and GND to delay the $\overline{\text{POR2}}$ output release after LDO-2 output reaches 94% of its specified voltage level. (200ms delay per 0.01µF). |
| 6 | GND | Ground | GND is the connection to system ground. Connect to PCB Ground plane. |
| 7 | $\overline{\text{POR1}}$ | Open-Drain Output (1mA) | Open-drain POR Output for LDO-1 (active-low). Internally connected to VO1 through 100kΩ resistor. |
| 8 | $\overline{\text{POR2}}$ | Open-Drain Output (1mA) | Open-drain POR Output for LDO-2 (active-low). Internally connected to VO2 through 100kΩ resistor. |
| 9 | VO2 | Analog I/O | LDO-2 Output. Connect capacitor of value 1µF to 10µF to GND (1µF recommended). |
| 10 | VO1 | Analog I/O | LDO-1 Output. Connect capacitor of value 1µF to 10µF to GND (1µF recommended). |

# Ordering Information

| PART NUMBER (Notes 1, 2, 3) | PART MARKING | VO1 VOLTAGE (V) | VO2 VOLTAGE (V) | TEMP RANGE (°C) | PACKAGE (Pb-Free) | PKG DWG. # |
|---|---|---|---|---|---|---|
| ISL78302ARFBZ | DNAB | 2.5 | 1.5 | -40 to +105 | 10 Ld 3x3 DFN | L10.3x3C |
| ISL78302ARBFZ | DNAC | 1.5 | 2.5 | -40 to +105 | 10 Ld 3x3 DFN | L10.3x3C |
| ISL78302ARNBZ | DNAD | 3.3 | 1.5 | -40 to +105 | 10 Ld 3x3 DFN | L10.3x3C |
| ISL78302ARBNZ | DNAE | 1.5 | 3.3 | -40 to +105 | 10 Ld 3x3 DFN | L10.3x3C |
| ISL78302ARNWZ | DNAF | 3.3 | 1.2 | -40 to +105 | 10 Ld 3x3 DFN | L10.3x3C |
| ISL78302ARWCZ | DNAG | 1.2 | 1.8 | -40 to +105 | 10 Ld 3x3 DFN | L10.3x3C |
| ISL78302ARFWZ | DNAH | 2.5 | 1.2 | -40 to +105 | 10 Ld 3x3 DFN | L10.3x3C |
| ISL78302ARCWZ | DNAJ | 1.8 | 1.2 | -40 to +105 | 10 Ld 3x3 DFN | L10.3x3C |
| ISL78302AR1AZ | DNAV | 1.25 | 3.3 | -40 to +105 | 10 Ld 3x3 DFN | L10.3x3C |

NOTES:

1. Add "-T*"suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL78302. For more information on MSL please see techbrief TB363.

## Absolute Maximum Ratings

Supply Voltage ($V_{IN}$) . . . . . +7.1V
$V_O1$, $V_O2$ Pins . . . . . +3.6V
All Other Pins . . . . . -0.3 to ($V_{IN}$ + 0.3)V
ESD Ratings
Human Body Model (Tested per JESD22-A114E) . . . . . 3kV
Machine Model (Tested per JESD-A115-A) . . . . . 200V
Charge Device Model (Tested Per AEC-Q100-011) . . . . . 2kV

## Thermal Information

| Thermal Resistance (Notes 4, 5) | $\theta_{JA}$ (°C/W) | $\theta_{JC}$ (°C/W) |
|---|---|---|
| 10 Ld 3x3 DFN Package | 59 | 18.5 |

Junction Temperature Range . . . . . -40°C to +125°C
Operating Temperature Range . . . . . -40°C to +105°C
Storage Temperature Range . . . . . -65°C to +150°C
Pb-Free Reflow Profile . . . . . see TB493

## Recommended Operating Conditions

Ambient Temperature Range ($T_A$) . . . . . -40°C to +105°C
Supply Voltage ($V_{IN}$) . . . . . 2.3V to 6.5V

*CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.*

NOTES:

4. $\theta_{JA}$ is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
5. For $\theta_{JC}$, the "case temp" location is the center of the exposed metal pad on the package underside.

## Electrical Specifications

Unless otherwise noted, all parameters are guaranteed over the operational supply voltage and temperature range of the device as follows: $T_A$ = -40°C to +105°C; $V_{IN}$ = ($V_O$ + 0.5V) to 6.5V with a minimum $V_{IN}$ of 2.3V; $C_{IN}$ = 1µF; $C_O$ = 1µF; $C_{BYP}$ = 0.01µF; $C_{POR}$ = 0.01µF. **Boldface limits apply across the operating temperature range, -40°C to +105°C.**

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN (Note 7) | TYP | MAX (Note 7) | UNITS |
|---|---|---|---|---|---|---|
| **DC CHARACTERISTICS** | | | | | | |
| Supply Voltage | $V_{IN}$ | | **2.3** | | **6.5** | V |
| Ground Current | | Quiescent condition: $I_{O1}$ = 0µA; $I_{O2}$ = 0µA | | | | |
| | $I_{DD1}$ | One LDO active | | 30 | **36** | µA |
| | $I_{DD2}$ | Both LDO active | | 47 | **55** | µA |
| Shutdown Current | $I_{DDS}$ | | | 0.3 | **2.1** | µA |
| UVLO Threshold | $V_{UV+}$ | | **1.9** | 2.1 | **2.3** | V |
| | $V_{UV-}$ | | **1.6** | 1.8 | **2.0** | V |
| Regulation Voltage Accuracy | | $V_{IN}$ = $V_O$ + 0.5V to 5.5V, $I_O$ = 10µA to 300mA, $T_J$ = +25°C | -0.8 | | +0.8 | % |
| | | $V_{IN}$ = $V_O$ + 0.5V to 5.5V, $I_O$ = 10µA to 300mA, $T_J$ = -40°C to +105°C | -1.8 | | +1.8 | % |
| Maximum Output Current | $I_{MAX}$ | Continuous | **300** | | | mA |
| Internal Current Limit | $I_{LIM}$ | | **320** | 475 | **650** | mA |
| Dropout Voltage (Note 6) | $V_{DO}$ | $I_O$ = 300mA | | 300 | | mV |
| | | $I_O$ = 150mA | | 150 | **250** | mV |
| Thermal Shutdown Temperature | $T_{SD+}$ | | | 145 | | °C |
| | $T_{SD-}$ | | | 110 | | °C |
| **AC CHARACTERISTICS** | | | | | | |
| Ripple Rejection | | $I_O$ = 10mA, $V_{IN}$ = 2.8V(min), $V_O$ = 1.5V, $C_{BYP}$ = 0.01µF | | | | |
| | | at 1kHz | | 64 | | dB |
| | | at 10kHz | | 51 | | dB |
| | | at 100kHz | | 38 | | dB |

**Electrical Specifications** Unless otherwise noted, all parameters are guaranteed over the operational supply voltage and temperature range of the device as follows: $T_A$ = -40°C to +105°C; $V_{IN}$ = ($V_O$ + 0.5V) to 6.5V with a minimum $V_{IN}$ of 2.3V; $C_{IN}$ = 1µF; $C_O$ = 1µF; $C_{BYP}$ = 0.01µF; $C_{POR}$ = 0.01µF. **Boldface limits apply across the operating temperature range, -40°C to +105°C. (Continued)**

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN (Note 7) | TYP | MAX (Note 7) | UNITS |
|---|---|---|---|---|---|---|
| Output Noise Voltage | | $I_O$ = 100µA, $V_O$ = 1.5V, $T_A$ = +25°C, $C_{BYP}$ = 0.01µF BW = 10Hz to 100kHz | | 37 | | $µV_{RMS}$ |
| **DEVICE START-UP CHARACTERISTICS** | | | | | | |
| Device Enable Time | $t_{EN}$ | Time from assertion of the ENx pin to when the output voltage reaches 95% of the VO(nom) | | 250 | **500** | µs |
| LDO Soft-start Ramp Rate | $t_{SSR}$ | Slope of linear portion of LDO output voltage ramp during start-up, $V_{OUT}$ > 1.25V | | 30 | **60** | µs/V |
| | | Slope of linear portion of LDO output voltage ramp during start-up, $V_{OUT}$ ≤ 1.25V | | 40 | **80** | µs/V |
| **EN1, EN2 PIN CHARACTERISTICS** | | | | | | |
| Input Low Voltage | $V_{IL}$ | | **-0.3** | | **0.5** | V |
| Input High Voltage | $V_{IH}$ | | **1.35** | | **$V_{IN}$ + 0.3** | V |
| Input Leakage Current | $I_{IL}$, $I_{IH}$ | | | | **0.1** | µA |
| Pin Capacitance | $C_{PIN}$ | Informative | | 5 | | pF |
| **$\overline{POR1}$, $\overline{POR2}$ PIN CHARACTERISTICS** | | | | | | |
| $\overline{POR1}$, $\overline{POR2}$ Thresholds | $V_{POR+}$ | As a percentage of nominal output voltage | **91** | 94 | **97** | % |
| | $V_{POR-}$ | | **87** | 90 | **93** | % |
| $\overline{POR1}$ Delay | $t_{P1LH}$ | | **0.5** | 2.0 | **3.2** | ms |
| | $t_{P1HL}$ | | | 25 | | µs |
| $\overline{POR2}$ Delay | $t_{P2LH}$ | $C_{POR}$ = 0.01µF | **100** | 200 | **300** | ms |
| | $t_{P2HL}$ | | | 25 | | µs |
| $\overline{POR1}$, $\overline{POR2}$ Pin Output Low Voltage | $V_{OL}$ | at $I_{OL}$ = 1.0mA | | | **0.2** | V |
| $\overline{POR1}$, $\overline{POR2}$ Pin Internal Pull-up Resistance | $R_{POR}$ | | **78** | 100 | **180** | kΩ |

NOTES:

6. VOx = 0.98*VOx(NOM); Valid for VOx greater than 1.85V.
7. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

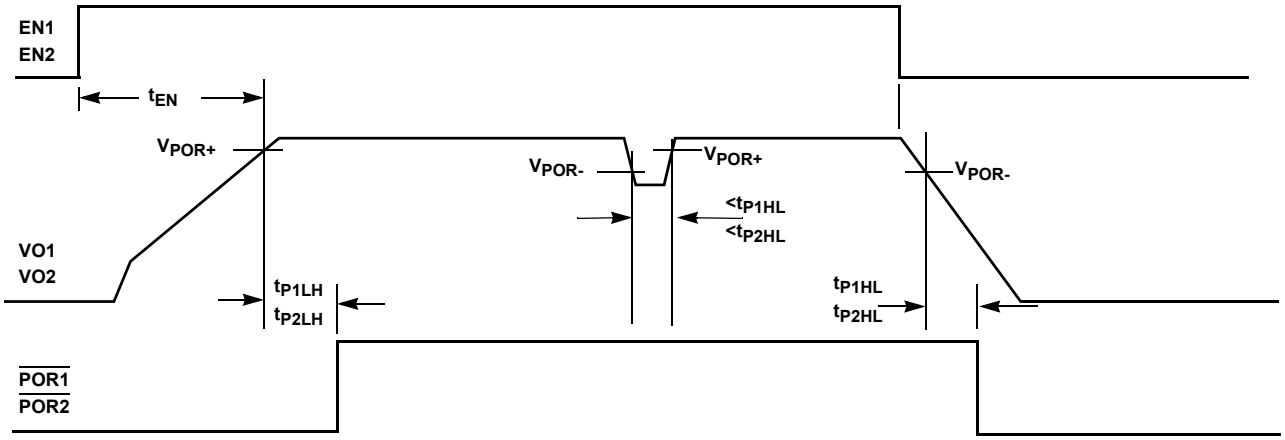



**FIGURE 2. TIMING PARAMETER DEFINITION**

# Typical Performance Curves

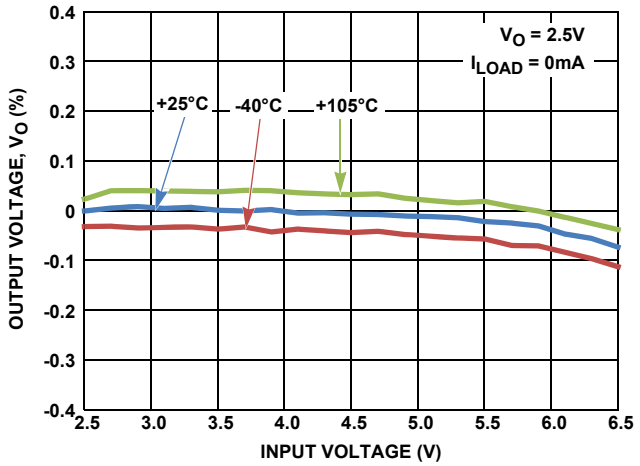



FIGURE 3. LINE REGULATION (2.5V OUTPUT)

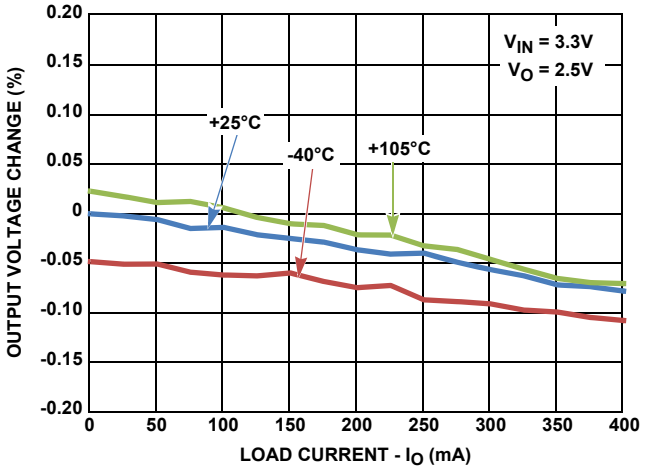



FIGURE 4. LOAD REGULATION

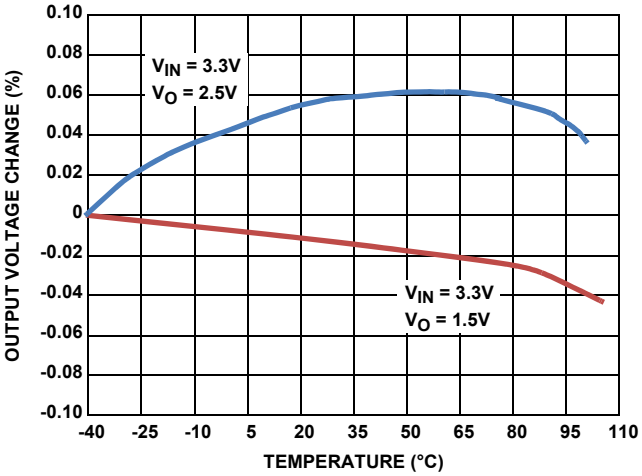



FIGURE 5. OUTPUT VOLTAGE CHANGE vs TEMPERATURE

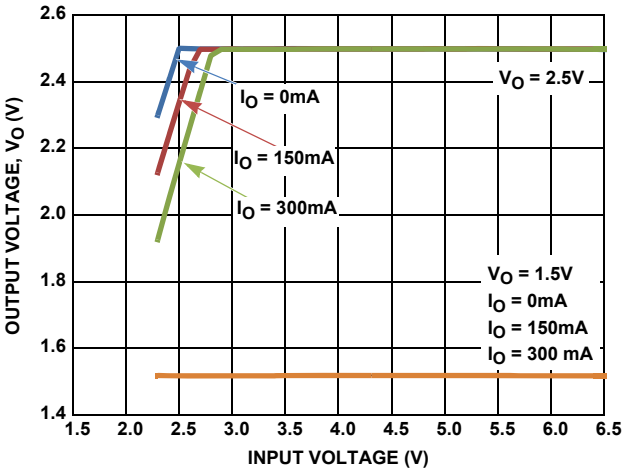



FIGURE 6. OUTPUT VOLTAGE vs INPUT VOLTAGE (2.5V AND 1.5V OUTPUT)

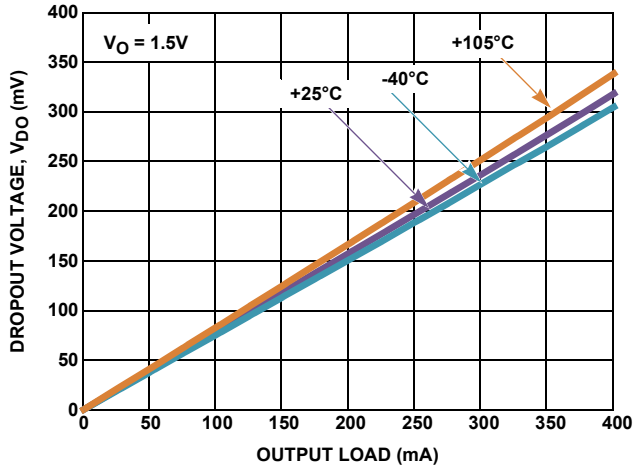



FIGURE 7. DROPOUT VOLTAGE vs LOAD CURRENT

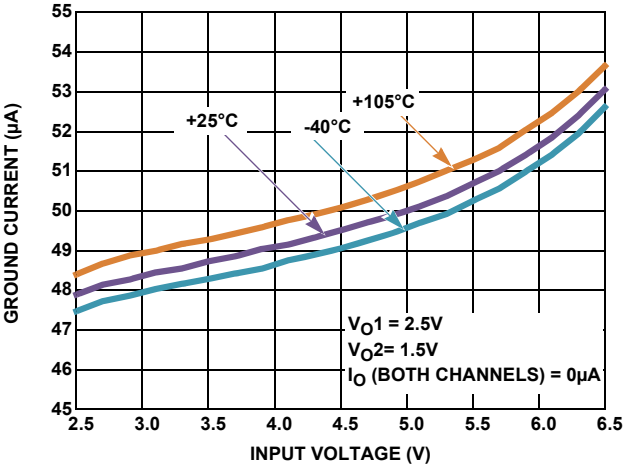



FIGURE 8. GROUND CURRENT vs INPUT VOLTAGE

## Typical Performance Curves (Continued)

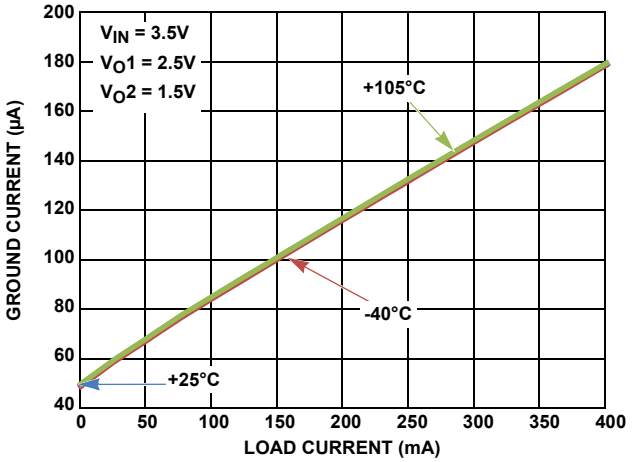



FIGURE 9. GROUND CURRENT vs LOAD

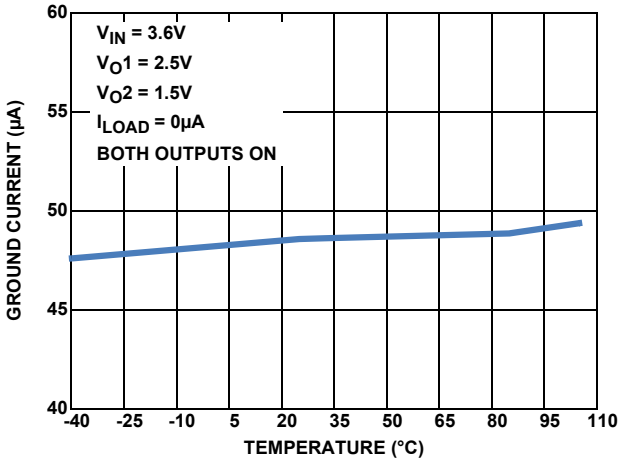



FIGURE 10. GROUND CURRENT vs TEMPERATURE

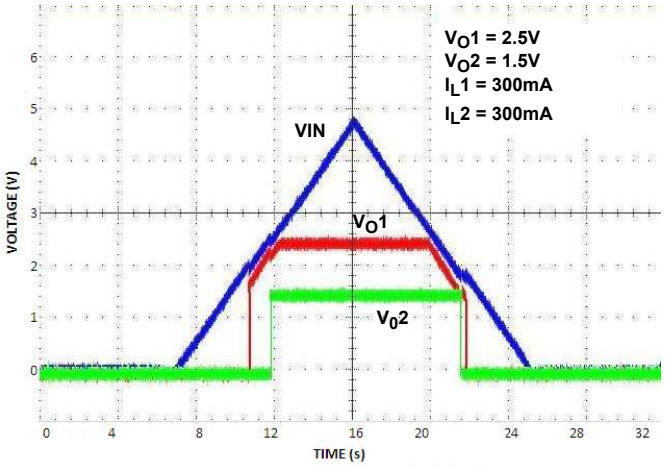



FIGURE 11. POWER-UP/POWER-DOWN

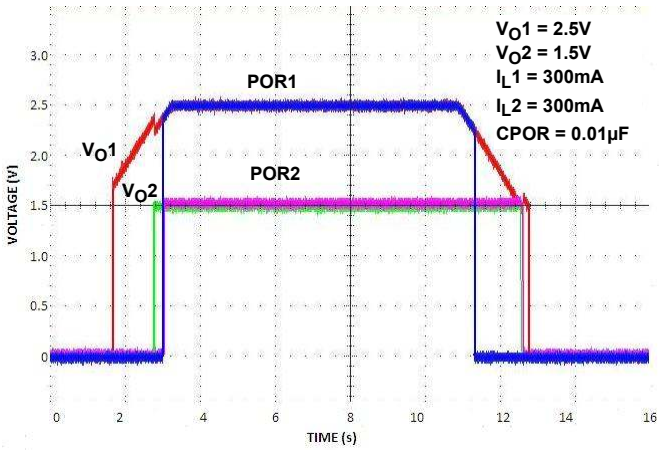



FIGURE 12. POWER-UP/POWER-DOWN WITH POR SIGNALS

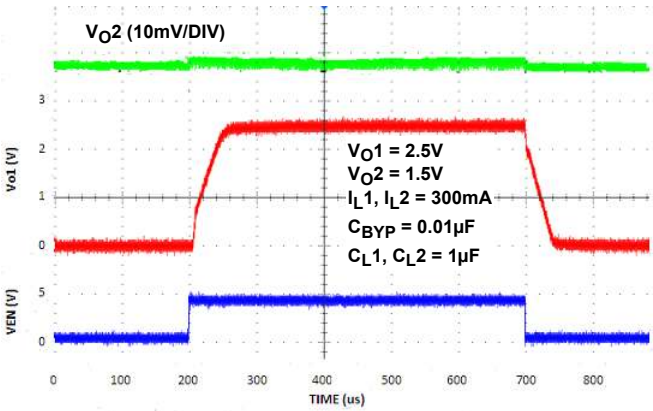



FIGURE 13. TURN-ON/TURN-OFF RESPONSE

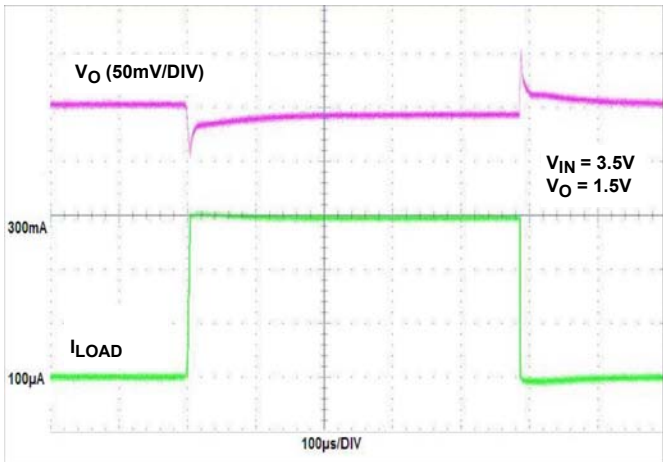



FIGURE 14. LOAD TRANSIENT RESPONSE

## Typical Performance Curves (Continued)

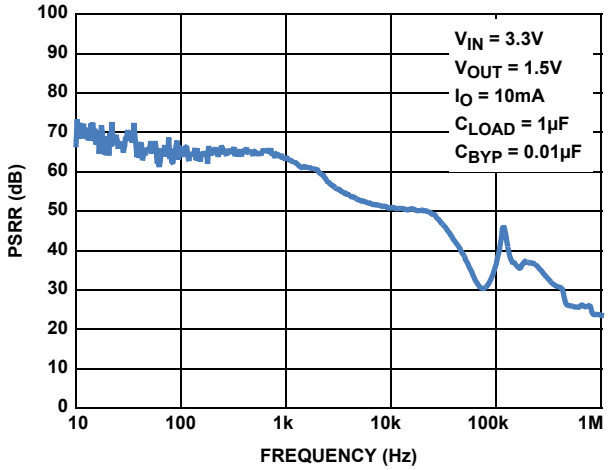



FIGURE 15. PSRR vs FREQUENCY

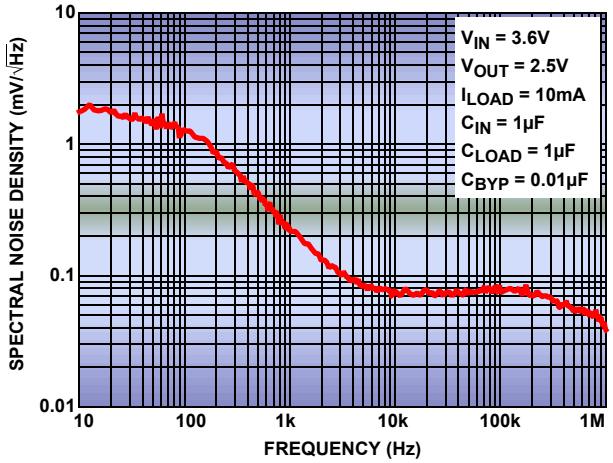



FIGURE 16. SPECTRAL NOISE DENSITY vs FREQUENCY (2.5V OUTPUT, 10mA LOAD)

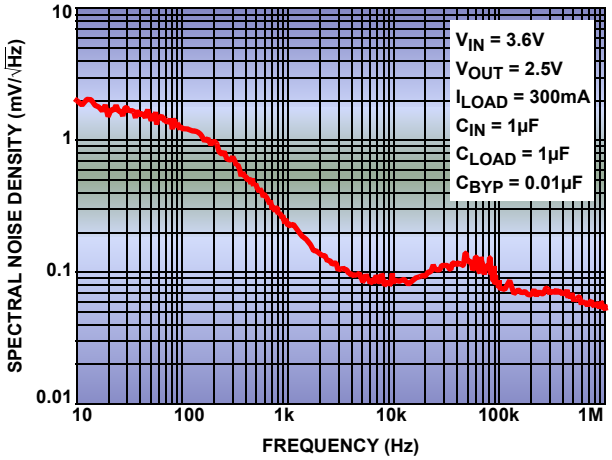



FIGURE 17. SPECTRAL NOISE DENSITY vs FREQUENCY (2.5V OUTPUT, 300mA LOAD)

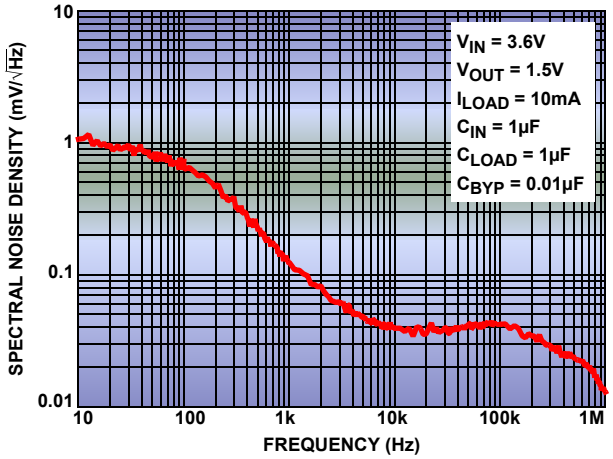



FIGURE 18. SPECTRAL NOISE DENSITY vs FREQUENCY (1.5V OUTPUT, 10mA LOAD)

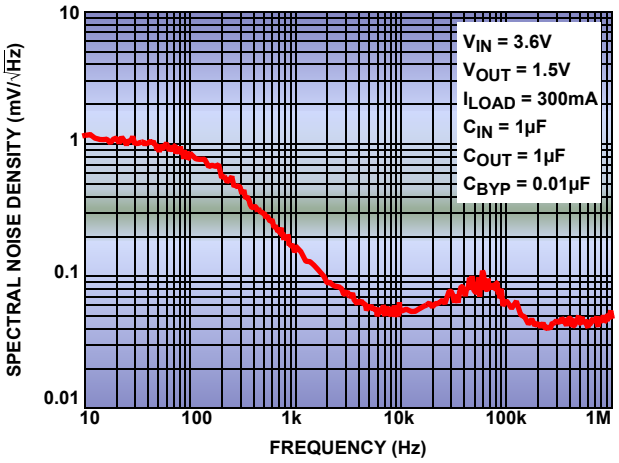



FIGURE 19. SPECTRAL NOISE DENSITY vs FREQUENCY (1.5V OUTPUT, 300mA LOAD)

# Functional Description

The ISL78302 contains two high performance LDOs. High performance is achieved through a circuit that delivers fast transient response to varying load conditions. In a quiescent condition, the ISL78302 adjusts its biasing to achieve the lowest standby current consumption.

The device also integrates current limit protection, smart thermal shutdown protection, staged turn-on and soft-start. Smart thermal shutdown protects the device against overheating. Staged turn-on and soft-start minimize start-up input current surges without causing excessive device turn-on time.

## Power Control

The ISL78302 has two separate enable pins (EN1 and EN2) to individually control power to each of the LDO outputs. When both EN1 and EN2 are low, the device is in shutdown mode. During this condition, all on-chip circuits are off, and the device draws minimum current, typically less than 0.5µA.

When one or both of the enable pins is asserted, the device first polls the output of the UVLO detector to ensure that VIN voltage is at least about 2.1V. Once verified, the device initiates a start-up sequence. During the start-up sequence, trim settings are first read and latched. Then, sequentially, the bandgap, reference voltage and current generation circuitry power-up. Once the references are stable, a fast-start circuit quickly charges the external reference bypass capacitor (connected to the CBYP pin) to the proper operating voltage. After the bypass capacitor has been charged, the LDOs power-up in their specified sequence.

Soft-start circuitry integrated into each LDO limits the initial ramp-up rate to about 30µs/V to minimize current surge.

If EN1 is brought high and EN2 goes high before the VO1 output stabilizes, the ISL78302 delays the VO2 turn-on until the VO1 output reaches its target level.

If EN2 is brought high and EN1 goes high before VO2 starts its output ramp, then VO1 turns on first and, the ISL78302 delays the VO2 turn-on until the VO1 output reaches its target level.

If EN2 is brought high and EN1 goes high after VO2 starts its output ramp, then the ISL78302 immediately starts to ramp up the VO1 output.

If both EN1 and EN2 are brought high at the same time, the VO1 output has priority and is always powered up first.

During operation, whenever the VIN voltage drops below 1.8V, the ISL78302 immediately disables both LDO outputs. When VIN rises back above 2.1V, the device reinitiates its start-up sequence, and LDO operation will resume automatically.

## Reference Generation

The reference generation circuitry includes a trimmed bandgap, a trimmed voltage reference divider, a trimmed current reference generator, and an RC noise filter. The filter includes the external capacitor connected to the CBYP pin. A 0.01µF (capacitor connected CBYP) implements a 100Hz lowpass filter and is recommended for most high-performance applications. Capacitor values above 0.01µF are not recommended for the CBYP pin.

The bandgap generates a zero temperature coefficient (TC) voltage for the reference divider. The reference divider provides the regulation reference, POR detection thresholds, and other voltage references required for current generation and over-temperature detection.

The current generator provides the references required for adaptive biasing as well as references for LDO output current limit and thermal shutdown determination.

## LDO Regulation and Programmable Output Divider

The LDO regulator is implemented with a high-gain operational amplifier driving a PMOS pass transistor. The design of the ISL78302 provides a regulator that has low quiescent current, fast transient response, and overall stability across all operating and load current conditions. LDO stability is guaranteed for a 1µF to 10µF output capacitor that has a tolerance better than 20% and an ESR less than 200mΩ. The design is performance-optimized for a 1µF capacitor. Unless limited by the application, use of an output capacitor value above 4.7µF is not normally needed, as LDO performance improvement is minimal.

Each LDO uses an independently trimmed 1V reference. An internal resistor divider drops the LDO output voltage down to 1V. This is compared to the 1V reference for regulation. The resistor division ratio is programmed in the factory to the output voltages of 1.2V, 1.5V, 1.8V, 2.5V and 3.3V.

## Power-On Reset Generation

Each LDO has a separate Power-on Reset signal generation circuit, which outputs to the respective $\overline{\text{POR}}$ pins. The POR signal is generated as follows.

A POR comparator continuously monitors the output of each LDO. The LDO enters a power-good state when the output voltage is above 94% of the expected output voltage for a period exceeding the LDO PGOOD entry delay time. In the power-good state, the open-drain $\overline{\text{PORx}}$ output is in a high-impedance state. An internal 100kΩ pull-up resistor pulls the pin up to the respective LDO output voltage. An external resistor can be added between the $\overline{\text{PORx}}$ output and the LDO output for a faster rise time; however, the $\overline{\text{PORx}}$ output should not connect through an external resistor to a supply greater than the associated LDO voltage.

The ISL78302 offers 1.2V and 1.5V regulated outputs in several options. On these low output voltage versions, it has been found that the internal pull-ups on POR outputs do not always function correctly above $V_{IN}$ = 3.9V. For this reason, it is recommended to use an external 100kΩ pull-up resistor for either POR pin if its associated output is either 1.2V or 1.5V. For outputs higher than 1.5V, no external resistor is required over the full input range from 2.3V to 6.5V.

The power-good state is exited when the LDO output falls below 90% of the expected output voltage for a period longer than the PGOOD exit delay time. While power-good is false, the ISL78302 pulls the respective $\overline{\text{POR}}$ pin low.

For LDO-1, the PGOOD entry delay time is fixed at about 2ms, while the PGOOD exit delay is about 25µs. For LDO-2, the PGOOD entry and exit delays are determined by the value of the external

capacitor connected to the CPOR pin. For a 0.01µF capacitor, the entry and exit delays are 200ms and 25µs, respectively. Larger or smaller capacitor values will yield proportionately longer or shorter delay times. The POR exit delay should never be allowed to be less than 10µs to ensure sufficient immunity against transient induced false POR triggering.

## Over-Temperature Detection

The bandgap provides a proportional-to-temperature current that indicates the temperature of the silicon. This current is compared with references to determine whether the device is in danger of damage from overheating. When the die temperature reaches about +145°C, one or both of the LDOs momentarily shuts down until the die cools sufficiently. In the overheat condition, only the LDO sourcing more than 50mA is shut off. This shutoff does not affect the operation of the other LDO. If both LDOs source more than 50mA and an overheat condition occurs, both LDO outputs are disabled. Once the die temperature falls back below about +110°C and disabled LDOs are re-enabled, the soft-start automatically takes place.

The ISL78302 provides short-circuit protection by limiting the output current to about 475mA. If short circuited, an output current of 475mA causes die heating. If the short circuit lasts long enough, the overheat detection circuit turns off the output.

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# Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest revision.

| DATE | REVISION | CHANGE |
|---|---|---|
| November 6, 2014 | FN7696.6 | Changed Testing information for Charged Device Model<br>from: Charged Device Model(Tested Per JESD22-C101C)...2kv<br>to: with Charged Device Model(Tested Per AEC-Q100-011)..2kv |
| December 4, 2013 | FN7696.5 | Page 1:<br>Changed last paragraph in description from:<br>"The ISL78302 is rated for the automotive temperature range (-40°C to +105°C)."<br>to:<br>"The ISL78302 is AEC-Q100 rated. The ISL78302 is rated for the automotive temperature range (-40°C to +105°C)."<br>Features bullet changed from: "Qualified for automotive applications" to: "AEC-Q100 Tested" |
| November 5, 2013 | FN7696.4 | Page 1 - Added the words "Qualified for Automotive Applications" under the Features section<br>Page 13 - Updated L10.3x3C POD from rev 2 to rev 3. Changes from rev 2:<br>Removed package outline and included center to center distance between lands on recommended land pattern.<br>Removed Note 4 "Dimension b applies to the metallized terminal and is measured between 0.18mm and 0.30mm from the terminal tip." |
| July 31, 2013 | FN7696.3 | Added Part Number ISL78302AR1AZ to “Ordering Information” on page 3<br>Electrical Spec Table changed LDO Soft-Start Ramp Rate Test Conditions under Device Start-up Characteristics on page 5<br>From: $V_{OUT}$ > 1.2V to $V_{OUT}$ > 1.25V<br>From: $V_{OUT}$ = 1.2V to $V_{OUT}$ <= 1.25V |
| March 15, 2012 | FN7696.2 | Removed "Other voltage selections are available upon request." from page 1.<br>Corrected "VO2" to "VO1" (tied to POR1#) in “Block Diagram” on page 2.<br>Corrected "VO4" to VO2" (tied to POR2#) in “Block Diagram” on page 2.<br>Removed Note 2 "For other output voltages, contact Intersil." from “Ordering Information” on page 3.<br>Corrected part marking for ISL78302ARCWZ from DANJ to DNAJ.<br>Added “$V_{OUT}$ > 1.2V” to conditions of “LDO Soft-start Ramp Rate” on page 5 where Typ/Max are 30/60µs/V.<br>Added line for $V_{OUT}$ = 1.2V with Typ/Max specs of 40/80µs/V.<br>Added paragraph to “Power-On Reset Generation” on page 10 ("The ISL78302 offers ... is required over the full input range from 2.3V to 6.5V."). |
| December 5, 2011 | FN7696.1 | Removed “Coming Soon” from parts in “Ordering Information” on page 3. |
| January 28, 2011 | FN7696.0 | Initial Release. |

# About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

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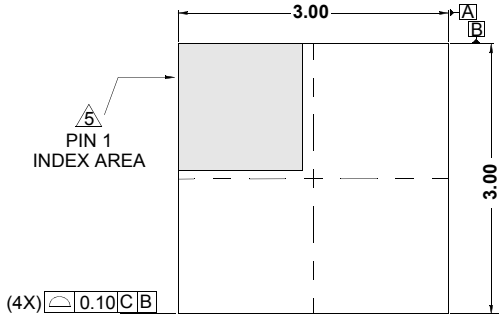
# Package Outline Drawing

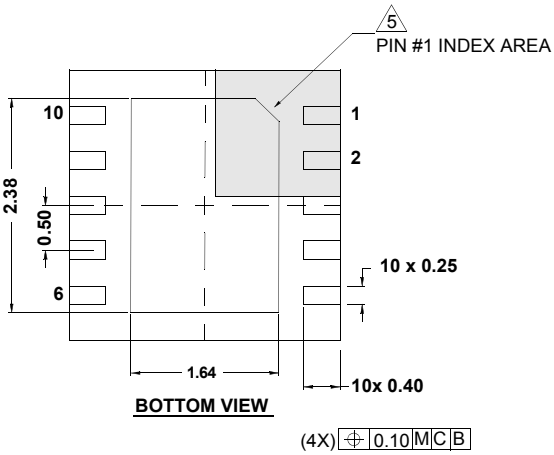
## L10.3x3C

**10 LEAD DUAL FLAT PACKAGE (DFN)**

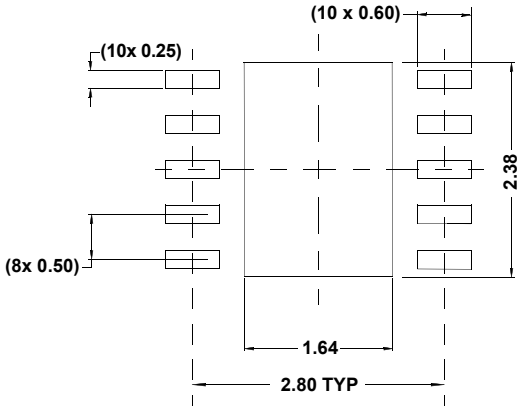
**Rev 3, 10/11**



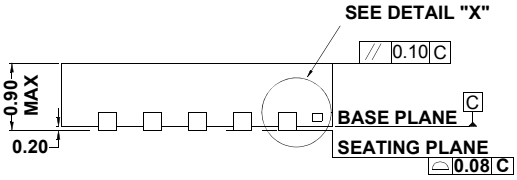

TOP VIEW



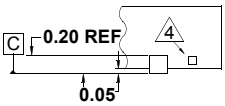

BOTTOM VIEW




TYPICAL RECOMMENDED LAND PATTERN




SIDE VIEW




DETAIL "X"

**NOTES:**

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Tiebar shown (if present) is a non-functional feature.
5. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
6. COMPLIANT TO JEDEC MO-229-WEED-3 except for E-PAD dimensions.

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