

Z86C91

# CMOS Z8<sup>®</sup> ROMLess Microcontrollers

**Product Specification** 

PS018501-1002



This publication is subject to replacement by a later edition. To determine whether a later edition exists, or to request copies of publications, contact:

## **ZiLOG Worldwide Headquarters**

532 Race Street Campbell, CA 95126-3432 Telephone: 408.558.8500

Fax: 408.558.8300 www.ZiLOG.com

ZiLOG is a registered trademark of ZiLOG Inc. in the United States and in other countries. All other products and/or service names mentioned herein may be trademarks of the companies with which they are associated.

### **Document Disclaimer**

© 2002 by ZiLOG, Inc. All rights reserved. Information in this publication concerning the devices, applications, or technology described is intended to suggest possible uses and may be superseded. ZiLOG, INC. DOES NOT ASSUME LIABILITY FOR OR PROVIDE A REPRESENTATION OF ACCURACY OF THE INFORMATION, DEVICES, OR TECHNOLOGY DESCRIBED IN THIS DOCUMENT. ZiLOG ALSO DOES NOT ASSUME LIABILITY FOR INTELLECTUAL PROPERTY INFRINGEMENT RELATED IN ANY MANNER TO USE OF INFORMATION, DEVICES, OR TECHNOLOGY DESCRIBED HEREIN OR OTHERWISE. Except with the express written approval ZiLOG, use of information, devices, or technology as critical components of life support systems is not authorized. No licenses or other rights are conveyed, implicitly or otherwise, by this document under any intellectual property rights.

PS018501-1002



## Table of Contents

Z86C91 Features
Pin Description
Pin Functions
Functional Description
Control Registers
Electrical Characteristics36Absolute Maximum Ratings36Standard Test Conditions36Capacitance37DC Electrical Characteristics37AC Electrical Characteristics39
Packaging
Ordering Information
Document Information
Customer Feedback Form50Z86C91 Product Specification50Customer Information50
Product Information
Problem Description or Suggestion



## List of Figures

Figure 1.	Z86C91 Functional Block Diagram	3
Figure 2.	40-Pin DIP Pin Configuration	4
Figure 3.	44-Pin PQFP Pin Configuration	6
Figure 4.	44-Pin PLCC Configuration	8
Figure 5.	Port 0 Configuration	]
Figure 6.	Port 1 Configuration	2
Figure 7.	Port 2 Configuration	3
Figure 8.	Port 3 Configuration	4
Figure 9.	Transmitted Data (No Parity)	4
Figure 10.	Transmitted Data (With Parity) 1	5
Figure 11.	Received Data (No Parity)	5
Figure 12.	Received Data (With Parity)	4
Figure 13.	Program Memory Map	8
Figure 14.	Data Memory Map	9
Figure 15.	Register File	2(
Figure 16.	Register Pointer Register	2]
Figure 17.	Register Pointer—Detail	2]
Figure 18.	Counter/Timer Block Diagram	23
Figure 19.	Interrupt Block Diagram	2.5
Figure 20.	Oscillator Configuration	26
Figure 21.	Serial I/O Register (F0h: Read/Write)	?
Figure 22.	Timer Mode Register (F1h: Read/Write)	3.5
Figure 23.	Counter Timer 1 Register (F2h: Read/Write)	3.5
Figure 24.	Prescaler 1 Register (F3h: Write Only)	29
Figure 25.	Counter/Timer 0 Register (F4h: Read/Write)	29
Figure 26.	Prescaler 0 Register (F5h: Write Only)	3(
Figure 27.	Port 2 Mode Register (F6h: Write Only)	3(
Figure 28.	Port 3 Mode Register (F7h: Write Only)	; ]
Figure 29.	Port 0 and 1 Mode Register (F8h: Write Only)	32
Figure 30.	Interrupt Priority Register (F9h: Write Only)	13
Figure 31.	Interrupt Request Register (FAh: Read/Write)	33
Figure 32.	Interrupt Mask Register (FBh: Read/Write)	<b>;</b> ∠
Figure 33.	Flags Register (FCh: Read/Write)	<b>;</b> ∠
Figure 34.	Register Pointer Register (FDh: Read/Write)	35

# Z86C91 | CMOS Z8® ROMLess Microcontrollers



Figure 35.	Stack Pointer Register (FEh: Read/Write)
Figure 36.	Stack Pointer Register (FFh: Read/Write)
Figure 37.	Test Load Diagram
Figure 38.	External I/O or Memory Read and Write Timing
Figure 39.	Additional Timing
Figure 40.	Input Handshake Timing
Figure 41.	Output Handshake Timing
Figure 42.	40-Pin DIP Package Diagram
Figure 43.	44-Pin PLCC Package Diagram
Figure 44.	44-Pin PQFP Package Diagram



### vi

## List of Tables

Table 1.	40-Pin DIP Pin Identification
Table 2.	44-Pin PQFP Pin Identification
Table 3.	44-Pin PLCC Configuration
Table 4.	Port 3 Pin Assignments
Table 5.	Absolute Maximum Ratings
Table 6.	DC Electrical Characteristics at Standard and External Temperatures 37
Table 7.	External I/O or Memory Read/Write Timing—Standard/Extended Tempera-
	ture
Table 8.	Clock Dependent Formulas
Table 9.	Additional Timing (Standard and Extended Temperature) 42
Table 10.	Handshake Timing (Standard and Extended Temperatures)
Table 11.	Ordering Information

## **Architectural Overview**

ZiLOG's large Z8<sup>®</sup> family of 8-bit ROMless microcontrollers includes the Z86C91 product with 236 bytes of RAM. Each of these devices offer fast execution, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, and easy hardware/software system expansion along with low cost and low power consumption.

For applications demanding powerful I/O capabilities, the Z86C91 offers 24 pins dedicated to input and output. These lines are grouped into four ports. Each port consists of eight lines and is configurable under software control to proviide timing, status signals, serial or parallel I/O with or without handshake and an address/data bus for interfacing external memory. The Z86C91 MCU features three basic address spaces to support this wide range of configurations: Program Memory, Data Memory, and 236 General Purposes Registers.

The Z86C91 operates at 16 MHz with a voltage range of 4.5 to 5.5 VDC.

To unburden the system from coping with real-time tasks such as counting/timing and data communication, the Z86C91 offers two on-chip counter/timers with a large number of user-selectable modes and a full-duplex hardware UART.

The Z86C91 is a ROMless part and offers the use of external memory, which enables this  $Z8^{\text{®}}$  MCU to be used in high-volume applications, or where code flexibility is required.



**Note:** All signals with an overline are active Low. For example,  $B/\overline{W}$ , for which WORD is active Low, and  $\overline{B}/W$ , for which BYTE is active Low.

Power connections follow these conventional descriptions:

Connection	Circuit	Device
Power	$V_{CC}$	$V_{DD}$
Ground	GND	$V_{SS}$

#### **Z86C91 Features**

- Asynchronous receiver/transmitter UART
- 40-Pin DIP and 44-Pin PLCC and QFP Packages
- 4.5- to 5.5-Volt Operating Range
- Operating Temperature Ranges:

Standard: 0°C to 70°C

Extended: -40°C to 105°C

• 24 Input/Output Lines

- Six Vectored, Prioritized Interrupts from Eight Different Sources
- Two Programmable 8-Bit Counter/Timers, each with two 6-Bit Programmable Prescalers
- On-Chip Oscillator that accepts a Crystal, Ceramic Resonator, LC, or External Clock
- Two Standby Modes: STOP and HALT
- Auto Latches

ZiLOG

## **Functional Block Diagrams**

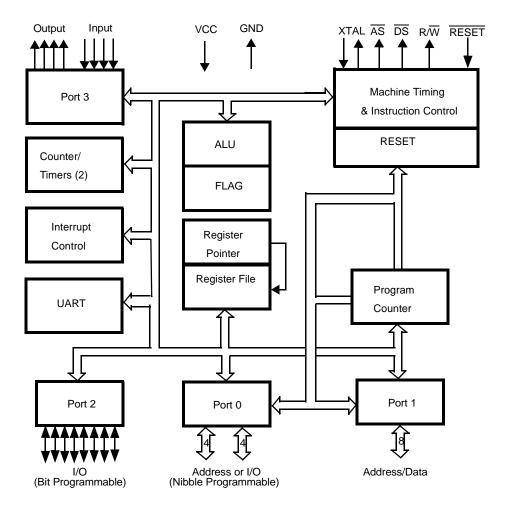


Figure 1. Z86C91 Functional Block Diagram

## **Pin Description**

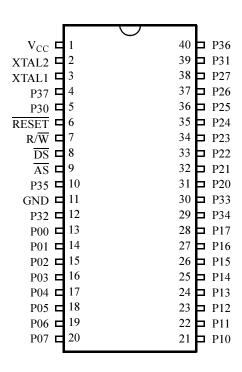


Figure 2. 40-Pin DIP Pin Configuration

Table 12. 40-Pin DIP Pin Identification

Pin #	Symbol	Function	Direction
1	$V_{CC}$	Power Supply	Input
2	XTAL2	Crystal, Oscillator Clock	Output
3	XTAL1	Crystal, Oscillator Clock	Input
4	P37	Port 3, Pin 7	Output
5	P30	Port 3, Pin 0	Input
6	RESET	Reset	Input
7	R/W	Read/Write	Output
8	DS	Data Strobe	Output
9	ĀS	Address Strobe	Output
10	P35	Port 3, Pin 5	Output



Table 12. 40-Pin DIP Pin Identification (Continued)

Pin #	Symbol	Function	Direction
11	GND	Ground, V <sub>SS</sub>	Output
12	P32	Port 3, Pin 2	Input
13-20	P00-P07	Port 0, Pins 0-7	Input/Output
21-28	P10-P17	Port 3, Pins 0-7	Input/Output
29	P34	Port 3, Pin 4	Output
30	P33	Port 3, Pin 3	Input
31-38	P20-P27	Port 2, Pins 0-7	Input/Output
39	P31	Port 3, Pin 1	Input
40	P36	Port 3, Pin 6	Output

ZiLOG

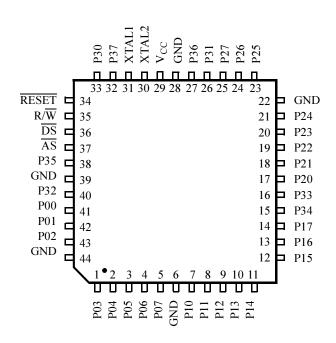


Figure 3. 44-Pin PQFP Pin Configuration

Table 13. 44-Pin PQFP Pin Identification

Pin #	Symbol	Function	Direction
1-5	P03-P07	Port 0, Bits 3-7	Input/Output
6	GND	Ground	Output
7-14	P10-P17	Port 1, Bits 0-7	Input/Output
15	P34	Port 3, Bit 4	Output
16	P33	Port 3, Bit 3	Intput
17-21	P20-P24	Port 2, Bits 0-4	Input/Output
22	GND	Ground	Output
23-25	P25-P27	Port 2, Bits 5-7	Input/Output
26	P31	Port 3, Bit 1	Input
27	P36	Port 3, Bit 6	Output
28	GND	Ground	Output

Table 13. 44-Pin PQFP Pin Identification (Continued)

Pin # Symbol		Function	Direction	
29	V <sub>CC</sub>	Power Supply	Input	
30	XTAL2	Crystal, Oscillator Clock	Output	
31	XTAL1	Crystal, Oscillator Clock	Input	
32	P37	Port 3, Bit 7	Output	
33	P30	Port 3, Bit 0	Intput	
34	RESET	Reset	Input	
35	R/W	Read/Write	Output	
36	DS	Data Strobe	Output	
37	ĀS	Address Strobe	Output	
38	P35	Port 3, Bit 5	Output	
39	GND	Ground	Output	
40	P32	Port 3, Bit 2	Input	
41-43	P00-P02	Port 0, Bits 0-2	Input/Output	
44	GND	Ground	Output	

ZiLOG

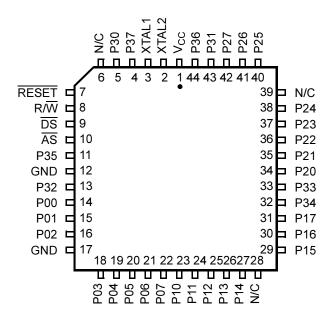


Figure 4. 44-Pin PLCC Configuration

Table 14. 44-Pin PLCC Configuration

Pin #	Symbol	Function	Direction
1	V <sub>CC</sub>	Power Supply	Input
2	XTAL2	Crystal, Oscillator Clock	Output
3	XTAL1	Crystal, Oscillator Clock	Input
4	P37	Port 3, Pin 7	Output
5	P30	Port 3, Pin 0	Input
6	N/C	Not Connected	
7	RESET	Reset	Input
8	R/W	Read/Write	Output
9	DS	Data Strobe	Output
10	ĀS	Address Strobe	Output
11	P35	Port 3, Pin 5	Output
12	GND	Ground V <sub>SS</sub>	Output



Table 14. 44-Pin PLCC Configuration (Continued)

Pin #	Symbol	Function	Direction	
13	P32	Port 3, Pin 2	Input	
14-16	P00-P02	Port 0, Pins 0-2	Input/Output	
17	GND	Ground	Output	
18-22	P03-P07	Port 0, Pins 3-7	Input/Output	
23-27	P10-P14	Port 1, Pins 0-4	Input/Output	
28	N/C	Not Connected		
29-31	P15-P17	Port 1, Pins 5-7	Input/Output	
32	P34	Port 3, Pin 4	Output	
33	P33	Port 3, Pin 3	Input	
34-38	P20-P24	Port 2, Pins 0-4	Input/Output	
39	N/C	Not Connected		
40-42	P25-P27	Port 2, Pins 5-7	Input/Output	
43	P31	Port 3, Pin 1	Input	
44	P36	Port 3, Pin 6	Output	

## **Pin Functions**

The following paragraphs describe the function of each available Z86C91 pin.

 $\overline{DS}$  (output, active Low). The Data Strobe is activated one time for each external memory transfer. For a READ operation, data must be available prior to the trailing edge of  $\overline{DS}$ . For WRITE operations, the falling edge of  $\overline{DS}$  indicates that output data is valid.

 $\overline{\text{AS}}$  (output, active Low). The Address Strobe is pulsed one time at the beginning of each machine cycle for external memory transfer. Address output is through Port 1 for all external programs. Memory address transfers are valid at the trailing edge of  $\overline{\text{AS}}$ . Under program control,  $\overline{\text{AS}}$  is placed in the high-impedance state along with Ports 0 and 1, Data Strobe, and READ/WRITE.

**XTAL1** (Crystal 1)Time-Based Oscillator Input. This pin connects a parallel-resonant crystal, ceramic resonator, LC network, or an external single-phase clock to the on-chip oscillatorand buffer.

**XTAL2 (Crystal 2) Time-Based Oscillator Output.** This pin connects a parallel-resonant crystal, ceramic resonant, LC network to the on-chip oscillator and buffer.

R/W (output, WRITE Low). The READ/WRITE signal is Low when the Z8 writes to external data memory.

 $\overline{\text{RESET}}$  (input, Low). To avoid asynchronous and noisy reset problems, the Z8 is equipped with a reset filter of four external XTAL clocks (4TpC). If the external  $\overline{\text{RESET}}$  signal is less than 4TpC in duration, reset does not occur.

On the fifth clock after  $\overline{RESET}$  is detected, an internal RST signal is latched and held for an internal register count of 18 external clocks, or for the duration of the external  $\overline{RESET}$ , whichever is longer. During the reset cycle,  $\overline{DS}$  is held active Low while  $\overline{AS}$  cycles at a rate of TpC/2. When  $\overline{RESET}$  is deactivated, program execution begins at location 000Ch. Power-Up reset time must be held Low for 50 ms, or until  $V_{CC}$  is stable, whichever is longer.

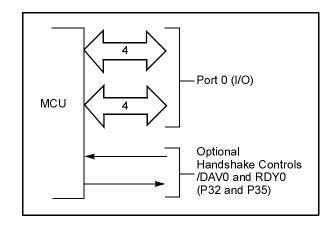
Port 0 (P00–P07). Port 0 is an 8-bit, nibble programmable, bidirectional, TTL-compatible port. These eight I/O lines are configured under software control as a nibble I/O port (P03–P00 input/output and P07–P04 input/output), or as an address port for interfacing external memory. When used as an I/O port, Port 0 may be placed under handshake control. In this configuration, Port 3, lines P32 and P35 are used as the handshake control DAV0 and RDY0. Handshake signal direction is dictated by the I/O direction (input or output) of Port 0 of the upper nibble P04–P07. The lower nibble must indicate the same direction as the upper nibble.

For external memory references, Port 1 provides address bits A7–A0 (lower nibble) and Port 0 provides address bits A15–A8 (upper nibble) depending on the required address space. If the address range requires 12 bits or less, the upper nibble of Port 0 is programmed independently as I/O while the lower nibble is used for addressing. If one or

both nibbles are required for I/O operation, they are configured by writing to the Port 01 mode register (P01M).

After a hardware RESET, Port 0 is configured as address lines A15–A8, and extended timing is set to accommodate slow memory access. The initialization routine can include reconfiguration to eliminate this extended timing mode.

Port 0 can be placed in a high-impedance state along with Port 1,  $\overline{AS}$ ,  $\overline{DS}$  and  $R/\overline{W}$ , allowing the Z8 to share common resources in multiprocessor and DMA applications (Figure 5). A hardware RESET is required to exit this high-impedance state.



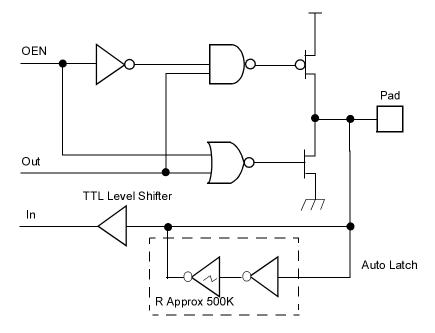
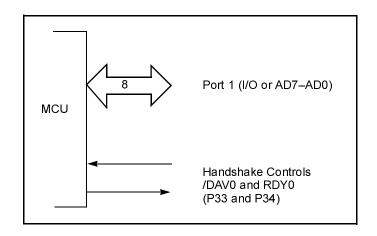


Figure 5. Port 0 Configuration

**Port 1 (P17–P10).** Port 1 is an 8-bit, TTL- compatible port (Figure 6), with multiplexed Address (A7–A0) and Data (D7–D0) ports for interfacing external memory. If more than 256 external locations are required, Port 0 outputs the additional lines.

Port 1 can be placed in the high-impedance state along with Port 0,  $\overline{AS}$ ,  $\overline{DS}$ , and  $R/\overline{W}$ , allowing the Z8 to share common resources in multiprocessor and DMA applications (Figure 6). A hardware RESET is required to exit this high-impedance state.



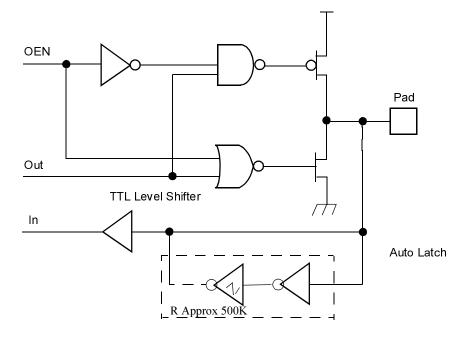
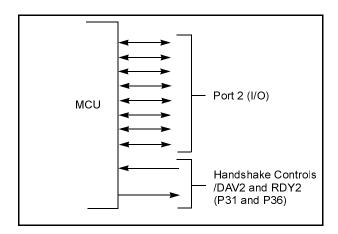


Figure 6. Port 1 Configuration

Port 2 (P27–P20). Port 2 is an 8-bit programmable, bidirectional, TTL-compatible I/O port. These eight I/O lines are configured under software control as an input or output, independently or globally as an open-drain output. Port 2 is always available for I/O operation. When used as an I/O port, Port 2 is placed under handshake control. In this configuration, Port 3 lines P31 and P36 are used as the handshake control lines  $\overline{DAV2}$  and RDY2. The handshake signal assignment for Port 3 lines P31 and P36 is dictated by the direction (input or output) assigned to P27 (Figure 7). After a RESET, Port 2 is configured as an input port. The Port 2 output portion of the circuit has open-drain as it's default configuration.



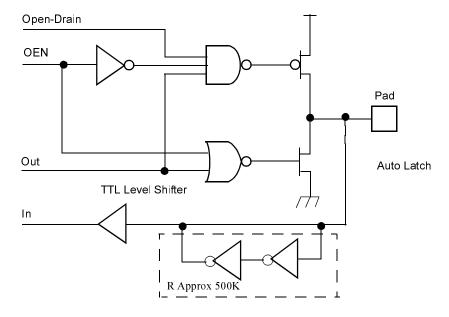


Figure 7. Port 2 Configuration

Port 3 (P37–P30). Port 3 is an 8-bit, TTL-compatible port, with four fixed inputs (P33–P30) and four fixed outputs (P34–P37). Port 3 is configured under software control for Input/Output, Counter/Timers, interrupt, UART, port handshake, and data Memory functions. Port 3, when used as serial I/O are programmed as serial in and serial out respectively (Figure 8).

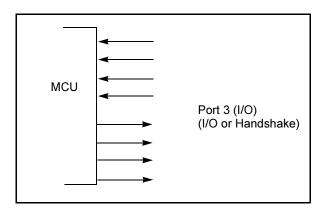


Figure 8. Port 3 Configuration

For interrupt functions, Port 3 inputs are falling-edge interrupt inputs. Access to Counter/Timer 1 is made through P31 ( $T_{\rm IN}$ ) and P36 ( $T_{\rm OUT}$ ). Handshake lines for Ports 0, 1, and 2 are available on P31 through P36.

Port 3 also provides the following control functions: handshake for Ports 0, 1, and 2 ( $\overline{DAV}$  and RDY); four external interrupt request signals (IRQ3–IRQ0); timer input and output signals ( $T_{IN}$  and  $T_{OUT}$ ); Data Memory Select.

P34 output is software-programmed to function as a Data Memory Select ( $\overline{DM}$ ). The Port 3 Mode Register (P3M) bit D3,D4 selects this function. When accessing external data memory, P34 goes active Low; when accessing external program memory, P34 goes High.

An onboard UART is enabled by software setting bit D5 of the Port 3 Mode Register P3M. When enabled, P30 is the receive input and P37 is the transmit output.

Port 3, lines P30 and P37 are programmed as serial I/O for full-duplex serial asynchronous receiver/transmitter operation. The bit rate is controlled by Counter/Timer0.

The Z8 automatically adds a start bit and two stop bits to transmitted data. Serial Data formats are shown in Figure 9 and Figure 10. Odd parity is also available by setting bit D7 in the P3M register. Eight data bits are always transmitted, regardless of parity selection. If parity is enabled, the eighth bit is the odd parity bit. An interrupt request (IRQ4) is generated on all transmitted characters.

Received data must have a start bit, eight data bits and at least one stop bit. If parity is on, bit 7 of the received data is replaced by a parity error flag. Received characters generate the IRQ3 interrupt request.

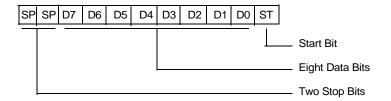


Figure 9. Transmitted Data (No Parity)

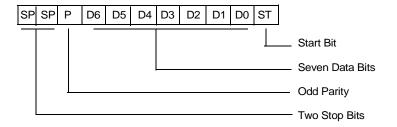


Figure 10. Transmitted Data (With Parity)

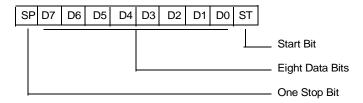


Figure 11. Received Data (No Parity)

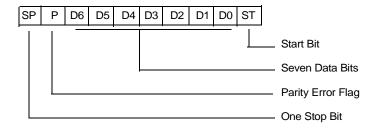


Figure 12. Received Data (With Parity)

Table 15. Port 3 Pin Assignments

Pin	I/O	Control Times	r Interrupt	P0 HS	P2 HS	Ext	UART
P30	IN		IRQ3				Serial In
P31	IN	T <sub>IN</sub>	IRQ2		D/R		
P32	IN		IRQ0	D/R			
P33	IN		IRQ1				
P34	OUT					$\overline{\mathrm{DM}}$	
P35	OUT			R/D			
P36	OUT	T <sub>OUT</sub>			R/D		
P37	OUT						Serial Out
Notes:							

HS = Handshake Signals

 $D = \overline{DAV}$  (Data Available)

R = RDY (Ready)

**Autolatch.** The autolatch places valid CMOS levels on all inputs that are not externally driven. Whether this level is 0 or 1 cannot be determined. A valid CMOS level, rather than a floating node, reduces excessive supply current flow in the input buffer. Autolatches are available on Port 0, Port 1, Port 2, and P3 inputs.

RESET (input, Low). Initializes the MCU. RESET occurs through external reset only. During Power-On Reset, the externally-generated reset drives the RESET pin Low for the POR time. Pull-up is provided internally.



RESET depends on oscillator operation to achieve full reset conditions. **Caution:** 

 $\overline{RESET}$  is a Schmitt-triggered input. During the RESET cycle,  $\overline{DS}$  is held active Low while  $\overline{AS}$  cycles at a rate of  $T_pC \div 2$ . Program execution begins at location 000Ch, after the  $\overline{RESET}$  is released.

When program execution begins,  $\overline{AS}$  and  $\overline{DS}$  toggles only for external memory accesses. The Z8 can only exit Stop Mode by using the RESET pin. The Z8 does reset all registers on a Stop-Mode Recovery operation out of STOP mode.

## **Functional Description**

The Z8 MCU incorporates the following functions that enhance the standard Z8<sup>®</sup> architecture and provide the user with increased design flexibility:

- Reset
- Program Memory
- Data Memory
- Working Register
- General-Purpose Registers
- Stack Pointer
- Counter/Timers
- Interrupts
- Clock
- HALT and STOP Modes
- Port Configuration Register

**RESET.** The device is reset in the following condition:

External Reset

Automatic Power-On Reset circuitry is not built into this Z8. This Z8 requires an external reset circuit to reset upon power-up. The internal pull-up resistor is on the  $\overline{\text{RESET}}$  pin, so a pull-up resistor is not required; however, in a high-EMI (noisy) environment, it is recommended that a low-value pull-up resistor be used.

**Program Memory.** The Z86C91 can address up to 64 KB of external program memory. The first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain six 16-bit vectors that correspond to the six available interrupts. Program execution begins at external location 000Ch after reset. See Figure 13.

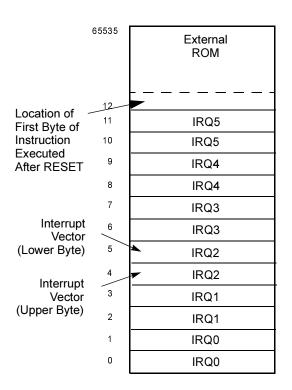


Figure 13. Program Memory Map

**Data Memory** ( $\overline{DM}$ ). The Z86C91addresses up to 64 KB of external data memory. External data memory may be included with, or separated from, the external program memory space.  $\overline{DM}$ , an optional I/O function that is programmed to appear on pin P34, is used to distinguish between data and program memory space (Figure 14). The state of the  $\overline{DM}$  signal is controlled by the type of instruction being executed. An LDC Op Code references PROGRAM ( $\overline{DM}$  inactive) memory, and an LDE instruction references data ( $\overline{DM}$  active Low) memory. The user must configure Port 3 Mode Register (P3M) bits D3 and D4 for this mode.

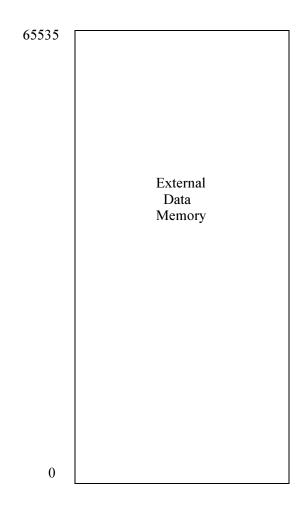


Figure 14. Data Memory Map

Register File. The register file contains three I/O port registers, 236 general-purpose registers, and 16 control and status registers (Figure 15). The instructions can access registers directly or indirectly via an 8-bit address field. The Z86C91 also allows short 4-bit register addressing using the Register Pointer (Figure 16). In the 4-bit mode, the register file is divided into 16 working register groups, each occupying 16 continuous locations. The Register Pointer addresses the starting location of the active working register group.

Location		Identifiers
255	Stack Pointer (Bits 7-0)	SPL
254	Stack Pointer (Bits 15-8)	SPH
253	Register Pointer	RP
252	Program Control Flags	FLAGS
251	Interrupt Mask Register	IMR
250	Interrupt Request Register	IRQ
249	Interrupt Priority Register	IPR
248	Ports 0-1 Mode	P01M
247	Port 3 Mode	P3M
246	Port 2 Mode	P2M
245	T0 Prescaler	PRE0
244	Timer/Counter 0	Т0
243	T1 Prescaler	PRE1
242	Timer/Counter 1	T1
241	Timer Mode	TMR
240	Serial I/O	SIO
239	General Purpose Registers	
4		
3	Port 3	P3
2	Port 2	P2
1	Reserved	Reserved
0	Port 0	P0
U	1 011 0	] 10

Figure 15. Register File

**Note:** Register Bank E0-EF is only accessed through working register and indirect addressing modes.

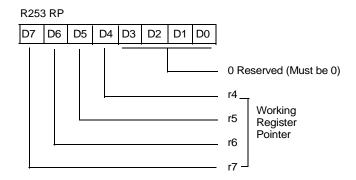


Figure 16. Register Pointer Register

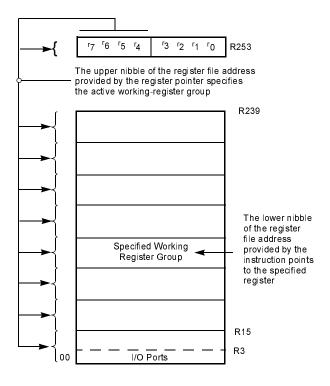


Figure 17. Register Pointer—Detail

General-Purpose Registers (GPR). General-purpose registers are undefined after the device is powered up. These registers keep the most recent value after any RESET, as long as the RESET occurs in the  $V_{CC}$  voltage-specified operating range. General-purpose registers are not guaranteed to keep their most recent state from if  $V_{CC}$  drops below the minimum  $V_{CC}$  operating range.

**Stack Pointer.** The Z86C91 has a 16-bit Stack Pointer (SPH and SPL) used for the external stack, that resides anywhere in the data memory. An 8-bit Stack Pointer (SPL) is used for the internal stack that resides within the 236 general-purpose registers. Stack Pointer High (SPH) is used as a general-purpose register only when using an internal stack.

**Counter/Timers.** There are two 8-bit programmable counter/timers (T0 and T1), each driven by its own 6-bit programmable prescaler. The T1 prescaler is driven by internal or external clock sources; however, the T0 prescaler is driven by the internal clock only (Figure 17).

The 6-bit prescalers can divide the input frequency of the clock source by any integer number from 1 to 64. Each prescaler drives its counter, which decrements the value (1 to 256) that is loaded into the counter. When both the counter and prescaler reach the end of the count, a timer interrupt request, IRQ4 (T0) or IRQ5 (T1), is generated.

The counters are programmed to START, STOP, restart to CONTINUE, or restart from the initial value. The counters can also be programmed to STOP upon reaching 1 (SIN-GLE-PASS mode) or to automatically reload the initial value and continue counting (MODULO–N CONTINUOUS mode).

The counters, but not the prescalers, are read at any time without disturbing their value or count mode. Reading the prescalers returns the value FFh. The clock source for T1 is user-definable and is either the internal micro controller clock divide-by-four, or an external signal input through Port 3. The maximum frequency of the external timer signal is the XTAL clock signal divided by 8. The Timer Mode Register configures the external timer input (P31) as an external clock, a trigger input that is retriggerable or nonretriggerable, or as a gate input for the internal clock. Port 3 line P36 also serves as an output ( $T_{\rm OUT}$ ) through which T0, T1, or the internal clock is output. The counter/timers are cascaded by connecting the T0 output to the input of T1.

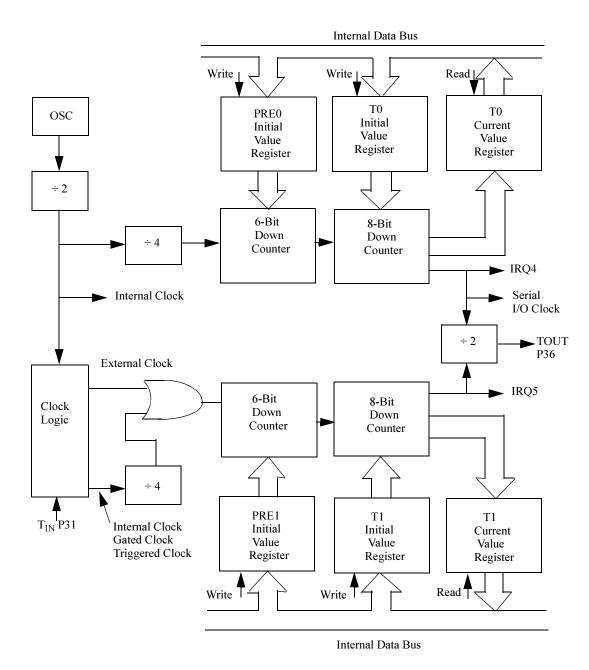


Figure 18. Counter/Timer Block Diagram

Interrupts. The Z8 has six different interrupts from eight different sources. These interrupts are maskable and prioritized. The 8 sources are divided as follows: 4 sources are claimed by Port 3 lines P33–P30, one in Serial Out, one in Serial In, and 2 are claimed by counter/timers. The Interrupt Mask Register globally or individually enables or disables the six interrupt requests. When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority register

All interrupts are vectored through locations in Program Memory. When an interrupt request is granted, the interrupt machine cycle is activated. This resets the interrupt request flag and disables all of the subsequent interrupts, except Program Counter and Status Flags, and branches to the program memory vector location reserved for that interrupt. This memory location and the next byte contain the 16 bit address of the interrupt service routine for that particular interrupt request.

To accommodate polled interrupt systems, interrupt inputs are masked and the Interrupt Request register is polled to determine which of the interrupt requests need service. Software initiated interrupts are supported by setting the appropriate bit in the Interrupt Request Register (IRQ).

Nested interrupts are supported by enabling interrupts in the interrupt service routine.

Internal interrupt requests are sampled on the falling edge of the last cycle of every instruction, and the interrupt request must be valid 5TpC before the falling edge of the last clock cycle of the currently executing instruction.

When the device samples a valid interrupt request, the next 48TpC (external XTAL clock cycles) are used to prioritize the interrupt, and push the two PC bytes and the FLAG register on the stack. The following nine cycles are used to fetch the interrupt vector from external memory. The first byte of the interrupt service routine is fetched beginning on the 58th TpC cycle following the internal sample point, which corresponds to the 63rd TpC cycle following the external interrupt sample point.

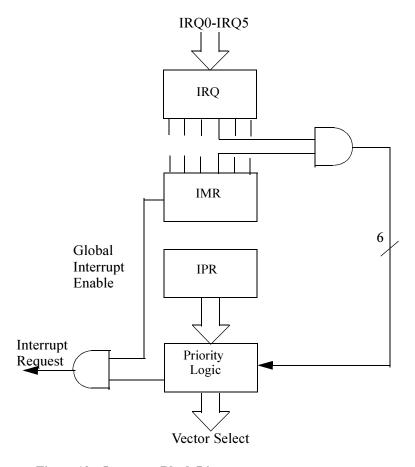


Figure 19. Interrupt Block Diagram

Clock. The on-chip oscillator has a high-gain, parallel-resonant amplifier for connection to a crystal, LC, ceramic resonator, or any suitable external clock source (XTAL1 = INPUT, XTAL2 = OUTPUT). The crystal should be AT-cut, 1MHz to 20 MHz maximum, with a series resistance (RS) of less than or equal to  $100\,\Omega$  when oscillating from 1MHz to  $16\,\text{MHz}$ .

The crystal should be connected across XTAL1 and XTAL2 using the oscillator manufacturer's recommended capacitor (10 pF<CL<300pF) from each pin to ground (Figure 20).

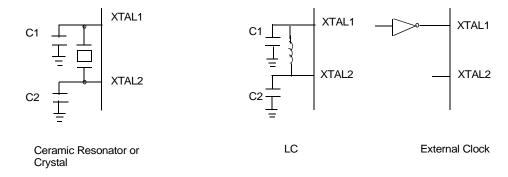


Figure 20. Oscillator Configuration

**HALT.** HALT turns off the internal CPU clock, but not the XTAL oscillation or the peripheral clock. The counter/timers and external interrupts IRQ0, IRQ1, IRQ2, and IRQ3 remain active. The devices are recovered by interrupts either externally or internally generated.

**STOP.** This instruction turns off the internal clock and external crystal oscillation and reduces the standby current to 10 microamperes or less. The STOP mode is terminated by a reset, which causes the processor to restart the application program at location 000Ch.

In order to enter STOP (or HALT) mode, it is necessary to first flush the instruction pipeline to avoid suspending execution in mid-instruction. Therefore, the user must execute a NOP (Op Code = FFh) immediately before the appropriate sleep instruction. For example:

FF NOP ; clear the pipeline 6F STOP ; enter STOP mode

or

FF NOP ; clear the pipeline 7F HALT ; enter HALT mode

## **Control Registers**

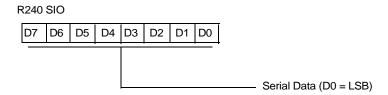


Figure 21. Serial I/O Register (F0h: Read/Write)



**Caution:** 

The majority of the control registers are read/write. The rest of the control are write only. The write-only registers are not readable. Attempting to read write-only registers will result in reading non-valid data. Any attempt to use logical or boolean types of instructions on these registers may corrupt the contents in the registers involved. Emulator operations on these write-only registers also reflect what is found on the Z8 device.

## **Timer Mode Register**

The Timer Mode Register, TMR, controls timing and counter functions and shown.in Figure 22.

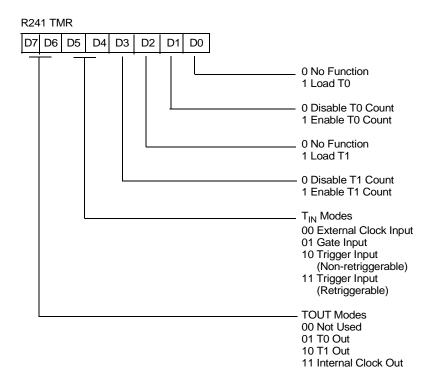


Figure 22. Timer Mode Register (F1h: Read/Write)

## Counter/Timer 1 Register

The Counter/Timer 1 Register, T1 is shown in Figure 23.

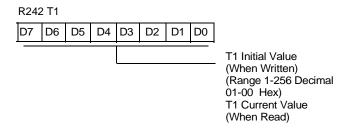


Figure 23. Counter Timer 1 Register (F2h: Read/Write)

## Prescaler 1 Register

The Prescaler 1 Register, PRE1, controls clocking functions and is shown in Figure 24.

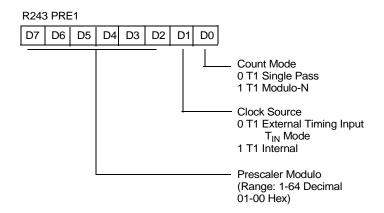


Figure 24. Prescaler 1 Register (F3h: Write Only)

## Counter/Timer 0 Register

The Counter/Timer 0 Register, T0 is shown in Figure 25.

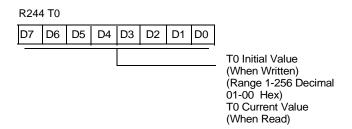


Figure 25. Counter/Timer 0 Register (F4h: Read/Write)

## Prescaler 0 Register

The Prescaler 0 Register PRE0 controls clocking functions and is shown in Figure 26.

30

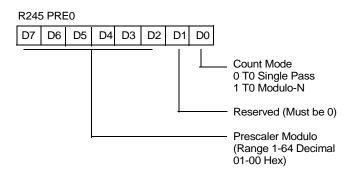


Figure 26. Prescaler 0 Register (F5h: Write Only)

## Port 2 Mode Register

The Port 2 Mode Register, P2M, controls Port 2 I/O functions and is shown in Figure 27.

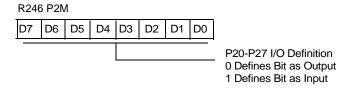


Figure 27. Port 2 Mode Register (F6h: Write Only)

## Port 3 Mode Register

The Port 3 Mode Register P3M controls Port 3 I/O functions and is shown in Figure 28.

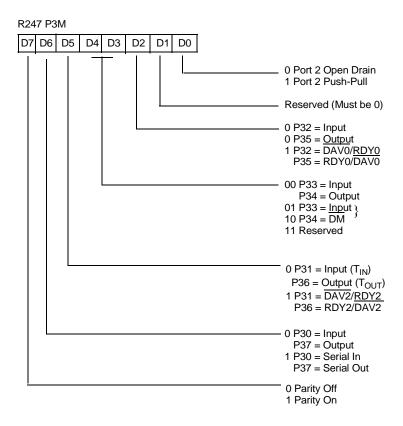


Figure 28. Port 3 Mode Register (F7h: Write Only)

#### Ports 0 and 1 Mode Register

The Ports 0 and 1 Mode Register, P01M, controls port and timing functions for Ports 0 and 1 and is shown in Figure 29.

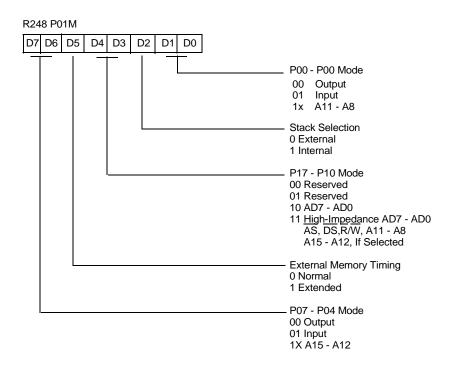


Figure 29. Port 0 and 1 Mode Register (F8h: Write Only)

**Interrupt Priority Register.** The Interrupt Priority Register, IPR, prioritizes interrupt functions and is shown in Figure 30.

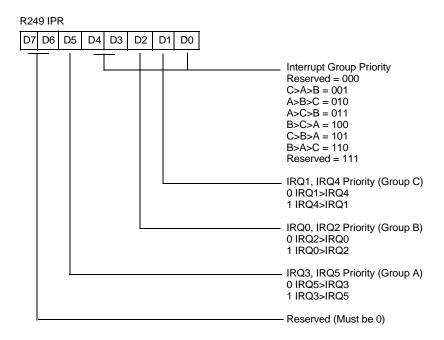


Figure 30. Interrupt Priority Register (F9h: Write Only)

#### **Interrupt Request Register**

The Interrupt Request Register, IRQ, controls interrupt functions and is shown in Figure 31.

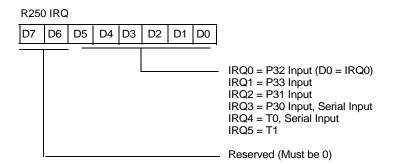


Figure 31. Interrupt Request Register (FAh: Read/Write)

#### **Interrupt Mask Register**

The Interrupt Mask Register, IMR, controls interrupt functions and is shown in Figure 32.

ZiLOG

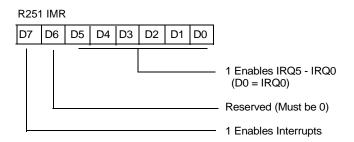


Figure 32. Interrupt Mask Register (FBh: Read/Write)

#### Flags Register

The CPU sets flags in the Flags Register, FLAGS, to allow the user to perform tests based on differing logical states. The FLAGS Register is shown in Figure 33.

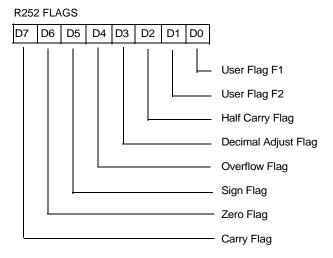


Figure 33. Flags Register (FCh: Read/Write)

#### Register Pointer Register

The Register Pointer Register, RP, controls pointer functions in the working registers and is shown in Figure 34.

ZiLOG

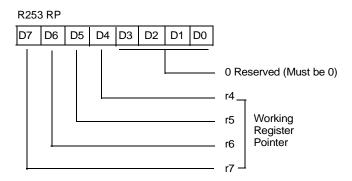


Figure 34. Register Pointer Register (FDh: Read/Write)

### Stack Pointer High Register

The Stack Pointer High Register, SPH, controls pointer functions in the upper byte when the external stack is used and is shown in Figure 35.

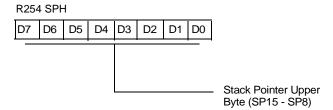


Figure 35. Stack Pointer Register (FEh: Read/Write)

#### **Stack Pointer Low Register**

The Stack Pointer Low Register, SPL, controls pointer functions in the lower byte and is shown in Figure 36.

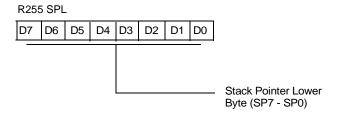


Figure 36. Stack Pointer Register (FFh: Read/Write)

### **Electrical Characteristics**

### **Absolute Maximum Ratings**

Stresses greater than the Absolute Maximum Ratings listed in Table 16 may cause permanent damage to the device. This rating is a stress rating only. Functional operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability.

**Table 16. Absolute Maximum Ratings** 

Symbol	Parameter	Min	Max	Units
$V_{\rm CC}$	Supply Voltage <sup>1</sup>	-0.3	+7.0	V
T <sub>STO</sub>	Storage Temperature	-65	+150	С
T <sub>A</sub>	Operating Ambient Temperature		2	С

#### Notes:

- 1. Voltages on all pins with respect to GND.
- 2. See Ordering Information.

#### **Standard Test Conditions**

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to Ground. Positive current flows into the referenced pin (Figure 37).



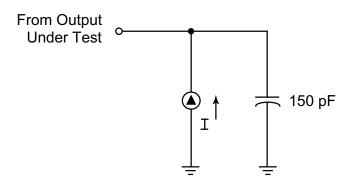


Figure 37. Test Load Diagram

# Capacitance

 $T_A$  = 25°C,  $V_{CC}$  = GND = 0V, f = 1.0 MHz, unmeasured pins returned to GND.

Parameter	Min	Max
Input capacitance	0	12 pF
Output capacitance	0	12 pF
I/O capacitance	0	12 pF

### **DC Electrical Characteristics**

Table 17. DC Electrical Characteristics at Standard and External Temperatures

		$T_A = 0$ °C to +70°C		$T_{A} = -40^{\circ}$	$T_A = -40$ °C to $+105$ °C			
Sym	Parameter	Min	Max	Min	Max	Typical <sup>2</sup> @25°C	Units	Conditions
	Max Input Voltage		7		7		V	I <sub>IH</sub> <200μA
V <sub>CH</sub>	Clock Input High Voltage	3.8	V <sub>CC</sub>	3.8	$V_{CC}$		V	Driven by External Clock Generator

#### Note:

- 1. All inputs driven to 0V,  $V_{\mbox{\footnotesize{CC}}}$  and outputs floating.
- 2.  $V_{CC} = 5.0V$

Table 17. DC Electrical Characteristics at Standard and External Temperatures (Continued)

		$T_A = 0$ °C	to +70°C	$T_{A} = -40^{\circ}$	C to +105°C	Typical <sup>2</sup>		
Sym	Parameter	Min	Max	Min	Max	@25°C	Units	Conditions
$\overline{v_{\mathrm{CL}}}$	Clock Input Low Voltage	-0.3	0.8	-0.3	0.8		V	Driven by External Clock Generator
$V_{IH}$	Input High Voltage	2.0	$V_{CC}$	2.0	V <sub>CC</sub>		V	
$\overline{v_{IL}}$	Input Low Voltage	-0.3	0.8	-0.3	0.8		V	
V <sub>OH</sub>	Output High Voltage	2.4		2.4			V	$I_{OH} = -2.0 \text{ mA}$
V <sub>OH</sub>	Output High Voltage	V <sub>CC</sub> -100r	nV	V <sub>CC</sub> -100	mV		V	$I_{OH} = -100 \ \mu A$
V <sub>OL</sub>	Output Low Voltage		0.4		0.4		V	$I_{OH} = +2 \text{ mA}$
$V_{RH}$	Reset Input High Voltage	3.8	$V_{CC}$	3.8	$V_{CC}$		V	
$V_{RL}$	Reset Input Low Voltage	-0.3	0.8	-0.3	0.8		V	
$I_{IL}$	Input Leakage	-2	2	-2	2		μΑ	Test at 0V, V <sub>CC</sub>
$I_{OL}$	Output Leakage	-2	2	-2	2		μΑ	Test at 0V, V <sub>CC</sub>
I <sub>IR</sub>	Reset Input Current		-80		-80		μΑ	V <sub>RL</sub> =0V
$I_{CC}$	Supply Current	-	35		35	24	mA	@ 16 MHz( <sup>1</sup> )
I <sub>CC1</sub>	Standby Current		7		7	4.5	mA	HALT Mode V <sub>IN</sub> = 0 V, V <sub>CC</sub> @ 16 MHz
I <sub>CC2</sub>	Standby Current		10		10	1	μΑ	STOP Mode $V_{IN} = 0 V, V_{CC}$ (1)
I <sub>ALL</sub>	Autolatch Low Current	-10	10	-14	14		μΑ	

- 1. All inputs driven to 0V,  $V_{CC}$  and outputs floating. 2.  $V_{CC}$  = 5.0V

#### **AC Electrical Characteristics**

Figure 38 illustrates the timing characteristics of the Z86C91MCU with respect to external input/output sources. See Table 18 for descriptions of the numbered timing parameters in the figure.

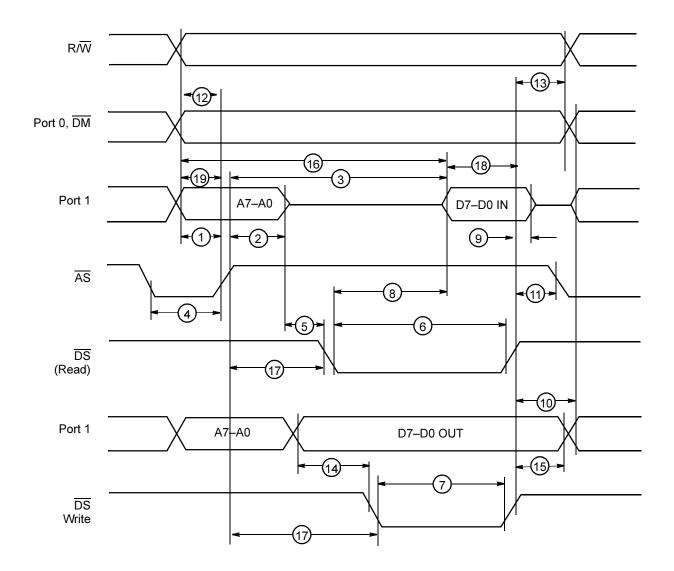


Figure 38. External I/O or Memory READ and WRITE Timing

Table 18. External I/O or Memory READ/WRITE Timing—Standard/Extended **Temperature** 

			$T_A = -0^{\circ}$ @ 16 M	°C to 70°C Hz	$T_A = -4$ 105°C @	0°C to 0 16 MHz		
No	Symbol	Parameter	Min	Max	Min	Max	Units	Notes
1	$T_DA(AS)$	Address Valid to AS Rise Delay	25		25		ns	2,3
2	$T_DAS(A)$	AS Rise to Address Float Delay	35		35		ns	2,3
3	T <sub>D</sub> AS(DR)	AS Rise to Read Data Req'd Valid		180		180	ns	1,2,3
4	$T_{W}AS$	AS Low Width	40		40		ns	2,3
5	T <sub>D</sub> AS(DS)	Address Float to DS Fall	0		0		ns	
6	T <sub>W</sub> DSR	DS (Read) Low Width	135		135		ns	1,2,3
7	$T_{W}DSW$	DS (WRITE) Low Width	80		80		ns	1,2,3
8	$T_DDSR(DR)$	DS Fall to Read Data Req'd Valid		75		75	ns	1,2,3
9	T <sub>H</sub> DR(DS)	Read Data to DS Rise Hold Time	0		0		ns	2,3
10	$T_DDS(A)$	DS Rise to Address Active Delay	50		50		ns	2,3
11	$T_DDS(AS)$	DS Rise to AS Fall Delay	35		35		ns	2,3
12	$T_DR/W(AS)$	R/W Valid to AS Rise Delay	25		25		ns	2,3
13	T <sub>D</sub> DS(R/W)	DS Rise to R/W Not Valid	35		35		ns	2,3
14	$T_DDW(DSW)$	WRITE Data Valid to $\overline{\rm DS}$ Fall (WRITE) Delay	25		25		ns	2,3
15	$T_DDS(DW)$	DS Rise to WRITE Data Not Valid Delay	35		35		ns	2,3
16	$T_DA(DR)$	Address Valid to Read Data Req'd Valid		230		230	ns	1,2,3
17	T <sub>D</sub> AS(DS)	AS Rise to DS Fall Delay	45		45		ns	2,3
18	T <sub>D</sub> DI(DS)	Data Input Setup to DS Rise	60		60		ns	1,2,3
19	T <sub>D</sub> DM(AS)	DM Valid to AS Rise Delay	30		30		ns	2,3

#### Notes:

- 1. When using extended memory timing add 2 TpC.
- Timing numbers provided are for minimum T<sub>P</sub>C.
   See Clock Cycle Dependent Characteristics table

**Table 19. Clock Dependent Formulas** 

Number	Symbol	Equation
1	T <sub>D</sub> A(AS)	0.40 TpC + 0.32
2	$T_DAS(A)$	0.59 TpC - 3.25
3	$T_DAS(DR)$	2.38 TpC + 6.14
4	$T_WAS$	0.66 TpC -1.65
6	$T_{W}DSR$	2.33TpC - 10.56
7	$T_WDSW$	1.27 TpC + 1.67
8	$T_DDSR(DR)$	1.97 TpC - 42.5
10	$T_DDS(A)$	0.8 TpC
11	$T_DDS(AS)$	0.59 TpC - 3.14
12	$T_D R \overline{W}(AS)$	0.4 TpC
13	$T_DDS(R\overline{W})$	0.8 TpC - 15
14	$T_DDW(DSW)$	0.4 TpC
15	$T_DDS(DW)$	0.88 TpC - 19
16	$T_DA(DR)$	4 TpC - 20
17	T <sub>D</sub> AS(DS)	0.91 TpC - 10.7
18	T <sub>S</sub> DI(DS)	0.8 TpC - 10
19	T <sub>D</sub> DM(AS)	0.9 TpC - 26.3

#### **Additional Timing**

Figure 39 illustrates the timing characteristics of the Z86C91 MCU with respect to system clock functions. See Table 20 for descriptions of the numbered timing parameters in the figure.

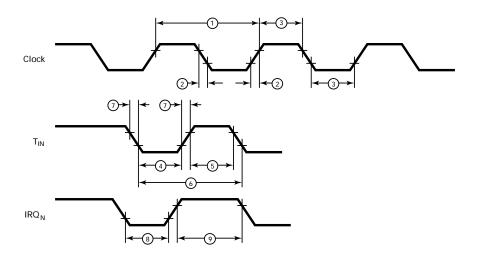


Figure 39. Additional Timing

**Table 20. Additional Timing (Standard and Extended Temperature)** 

			$T_A = 0^{\circ}C \text{ to } +70^{\circ}C T_A = -4 0^{\circ}C \text{ to } +105^{\circ}C$					
			10	6 MHz		16 MHz		
No	Sym	Parameter	Min	Max	Min	Max	Units	Notes
1	T <sub>P</sub> C	Input Clock Period	62.5	1000	62.5	1000	ns	1
2	$T_RC,T_FC$	Clock Input Rise & Fall Times		10		10	ns	1
3	T <sub>W</sub> C	Input Clock Width	25		25		ns	1
4	$T_WT_{IN}L$	Timer Input Low Width	75		75		ns	2
5	$T_W T_{IN} H$	Timer Input High Width	3T <sub>P</sub> C		3T <sub>P</sub> C			2

#### Notes:

- 1. Clock timing references use 3.8V for a logic one and 0.8V for a logic 0.
- 2. Timing references use 2.0V for a logic 1 and 0.8V for a logic 0.
- 3. Interrupt references request via Port 3.
- 4. The interrupt request via Port 3 (P31–P33).
- 5. The interrupt request via Port 3 (P30).

Table 20. Additional Timing (Standard and Extended Temperature) (Continued)

			$T_A = 0^{\circ}C \text{ to } +70^{\circ}C T_A = -4 0^{\circ}C \text{ to } +105^{\circ}C$					
			16	MHz		16 MHz		
No	Sym	Parameter	Min	Max	Min	Max	Units	Notes
6	$T_PT_{IN}$	Timer Input Period	8T <sub>P</sub> C		8T <sub>P</sub> C			2
7	$T_RT_{IN}, T_FT_{IN}$	Timer Input Rise & Fall Timer	100		100		ns	2
8A	T <sub>W</sub> IL	Interrupt Request Low Time	70		70		ns	2,4
8B	T <sub>W</sub> IL	Interrupt Request Low Time	3T <sub>P</sub> C		3T <sub>P</sub> C			2,5
9	T <sub>W</sub> IH	Interrupt Request Input High Time	$3T_{P}C$		3T <sub>P</sub> C			2,3

#### Notes:

- 1. Clock timing references use 3.8V for a logic one and 0.8V for a logic 0.
- 2. Timing references use 2.0V for a logic 1 and 0.8V for a logic 0.
- 3. Interrupt references request via Port 3.
- 4. The interrupt request via Port 3 (P31–P33).
- 5. The interrupt request via Port 3 (P30).

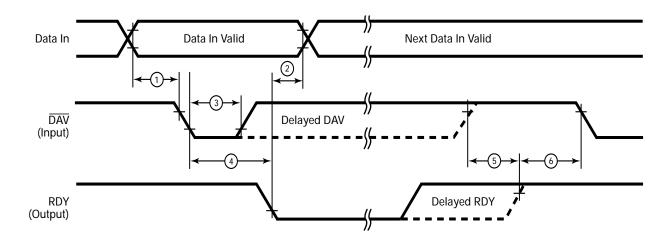


Figure 40. Input Handshake Timing



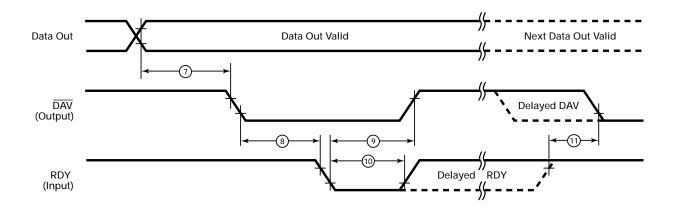


Figure 41. Output Handshake Timing

Table 21. Handshake Timing (Standard and Extended Temperatures)

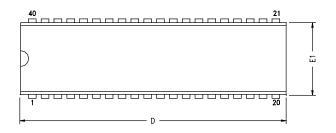
			$T_A = 0^\circ$	C to +70°	$C  T_A = -40$	0°C to +105°C	Data
No	Symbol	Parameter	Min	Max	Min	Max	Direction
1	T <sub>S</sub> DI(DAV)	Data In Setup Time	0		0		Input
2	T <sub>H</sub> DI(RDY)	Data In Hold Time	145		145		Input
3	$T_{W}DAV$	Data Available Width	110		110		Input
4	T <sub>D</sub> DAVI(RDY)	DAV Fall to RDY Fall Delay		115		115	Input
5	T <sub>D</sub> DAVId(RDY)	DAV Out to DAV Fall Delay		115		115	Input
6	RDY0 <sub>D</sub> (DAV)	RDY Rise to DAV Fall Delay	0		0		Input
7	T <sub>D</sub> D0(DAV)	Data Out to DAV Fall Delay		ТрС		ТрС	Output
8	T <sub>D</sub> DAV0(RDY)	DAV Fall to RDY Fall Delay	0		0		Output
9	T <sub>D</sub> RDY0(DAV)	RDY Fall to DAV Rise Delay		115		115	Output
10	$T_{W}RDY$	RDY Width	110		110		Output
11	$T_DRDY0_D(DAV)$	RDY Rise to DAV Fall Delay		115		115	Output

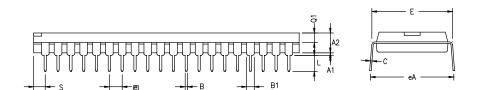
>

**Note:** All timing references use 2.0V for a logic 1 and 0.8V for a logic 0.

# **Packaging**

Figure 42 illustrates the 40-pin DIP package for the microcontroller devices.



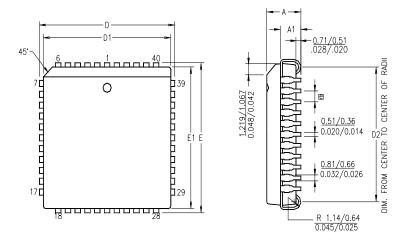


SYMBOL	MILLIN	1ETER	INC	:H
STWIDOL	MIN	MAX	MIN	MAX
A1	0.51	1.02	.020	.040
A2	3.18	3.94	.125	.155
В	0.38	0.53	.015	.021
B1	1.02	1.52	.040	.060
С	0.23	0.38	.009	.015
D	52.07	52.58	2.050	2.070
E	15.24	15.75	.600	.620
E1	13.59	14.22	.535	.560
e	2.54	TYP	.100	TYP
eA	15.49	16.76	.610	.660
L	3.05	3.81	.120	.150
Q1	1.40	1.91	.055	.075
S	1.52	2.29	.060	.090

CONTROLLING DIMENSIONS : INCH

Figure 42. 40-Pin DIP Package Diagram

PS018501-1002 Packaging



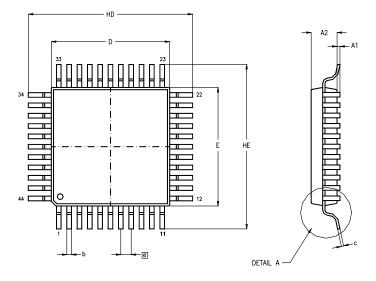
SYMBOL	MILLIN	METER	IN	СН	
JIMBOL	MIN	MAX	MIN	MAX	
A	4.27	4.57	0.168	0.180	
A1	2.41	2.92	0.095	0.115	
D/E	17.40	17.65	0.685	0.695	
D1/E1	16.51	16.66	0.650	0.656	
D2	15.24	16.00	0.600	0.630	
е	1.27 BSC		0.050 BSC		

NOTES:

- 1. CONTROLLING DIMENSION: INCH
  2. LEADS ARE COPLANAR WITHIN 0.004".
  3. DIMENSION: MM/INCH

Figure 43. 44-Pin PLCC Package Diagram

PS018501-1002 Packaging



SYMBOL	MILLIN	METER	IN	СН
STMIDOL	MIN	MAX	MIN	MAX
A1	0.05	0.25	.002	.010
A2	2.00	2.25	.078	.089
Ь	0.25	0.45	.010	.018
С	0.13	0.20	.005	.008
HD	13.70	14.15	.539	.557
D	9.90	10.10	.390	.398
Ħ	13.70	14.15	.539	.557
E	9.90	10.10	.390	.398
е	0.80	BSC	.0315 BSC	
١	0.60	1.20	.024	.047

0-10

DETAIL A

Figure 44. 44-Pin PQFP Package Diagram

NOTES:
1. CONTROLLING DIMENSIONS : MILLIMETER
2. LEAD COPLANARITY : MAX .10 .004"

PS018501-1002 Packaging

# **Ordering Information**

**Table 22. Ordering Information** 

Pin Count	Package	Order Number
40	DIP	Z86C9116PSC
40	DIP	Z86C9116PEC
44	PLCC	Z86C9116VSC
44	PLCC	Z86C9116VEC
44	QFP	Z86C9116FEC
44	QFP	Z86C9116FSC

# **Part Number Description**

ZiLOG part numbers consist of a number of components. For example, part number Z86C9116PSC is a 16-MHz 40-pin DIP that operates in the -0°C to +70°C temperature range, with Plastic Standard Flow. The Z86C9116PSC part number corresponds to the code segments indicated in the following table.

Z	ZiLOG Prefix
86	Z8 Product
С	OTP Product
91	Product Number
16	Speed (MHz)
P	Package
S	Temperature
С	Environmental Flow

For fast results, contact your local ZiLOG sales office for assistance in ordering the part required.

ZiLOG, Inc. 532 Race Street San Jose, CA 95126-3432 Telephone (408) 558-8500 FAX 408 558-8300

Internet: www.ZiLOG.com

# **Document Information**

# **Document Number Description**

The Document Control Number that appears in the footer of each page of this document contains unique identifying attributes, as indicated in the following table:

PS	Product Specification
0185	Unique Document Number
01	Revision Number
0802	Month and Year Published

## **Customer Feedback Form**

# **Z86C91 Product Specification**

If you experience any problems while operating this product, or if you note any inaccuracies while reading this Product Specification, please copy and complete this form, then mail or fax it to ZiLOG (see Return Information, below). We also welcome your suggestions!

#### **Customer Information**

Name	Country
Company	Phone
Address	Fax
City/State/Zip	E-Mail

### **Product Information**

Serial # or Board Fab #/Rev. #		
Software Version		
Document Number		
Host Computer Description/Type		

#### **Return Information**

**ZiLOG** System Test/Customer Support 532 Race Street San Jose, CA 95126-3432 Fax: (408) 558-8536

Email: <u>zservice@zilog.com</u>

# **Problem Description or Suggestion**

Provide a complete description of the problem or your suggestion. If you are reporting a specific problem, include all steps leading up to the occurrence of the problem. Attach additional pages as necessary.		



Компания «Океан Электроники» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

#### Наши преимущества:

- Поставка оригинальных импортных электронных компонентов напрямую с производств Америки, Европы и Азии, а так же с крупнейших складов мира;
- Широкая линейка поставок активных и пассивных импортных электронных компонентов (более 30 млн. наименований);
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Помощь Конструкторского Отдела и консультации квалифицированных инженеров;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Поставка электронных компонентов под контролем ВП;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- При необходимости вся продукция военного и аэрокосмического назначения проходит испытания и сертификацию в лаборатории (по согласованию с заказчиком);
- Поставка специализированных компонентов военного и аэрокосмического уровня качества (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Actel, Aeroflex, Peregrine, VPT, Syfer, Eurofarad, Texas Instruments, MS Kennedy, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits, General Dynamics и др.);

Компания «Океан Электроники» является официальным дистрибьютором и эксклюзивным представителем в России одного из крупнейших производителей разъемов военного и аэрокосмического назначения «JONHON», а так же официальным дистрибьютором и эксклюзивным представителем в России производителя высокотехнологичных и надежных решений для передачи СВЧ сигналов «FORSTAR».



**«JONHON»** (основан в 1970 г.)

Разъемы специального, военного и аэрокосмического назначения:

(Применяются в военной, авиационной, аэрокосмической, морской, железнодорожной, горно- и нефтедобывающей отраслях промышленности)

«**FORSTAR**» (основан в 1998 г.)

ВЧ соединители, коаксиальные кабели, кабельные сборки и микроволновые компоненты:

(Применяются в телекоммуникациях гражданского и специального назначения, в средствах связи, РЛС, а так же военной, авиационной и аэрокосмической отраслях промышленности).



Телефон: 8 (812) 309-75-97 (многоканальный)

Факс: 8 (812) 320-03-32

Электронная почта: ocean@oceanchips.ru

Web: http://oceanchips.ru/

Адрес: 198099, г. Санкт-Петербург, ул. Калинина, д. 2, корп. 4, лит. А