

# 1:8 Clock Fanout Buffer

## Features

- Low-voltage operation  $V_{DD} = 3.3V$
- 1:8 fanout
- Single-input-configurable for LVDS, LVPECL, or LVTTL
- 8 pair of LVPECL outputs
- Drives a 50-ohm load
- Low input capacitance
- Low output skew
- Low propagation delay Typical ( $t_{pd} < 4\text{ ns}$ )
- Industrial versions available
- Package available include: TSSOP
- Does not exceed Bellcore 802.3 standards
- Operation at  $\Rightarrow 350\text{ MHz} - 700\text{ Mbps}$

## Description

This Cypress series of network circuits are produced using advanced 0.35-micron CMOS technology, achieving the industry's fastest logic.

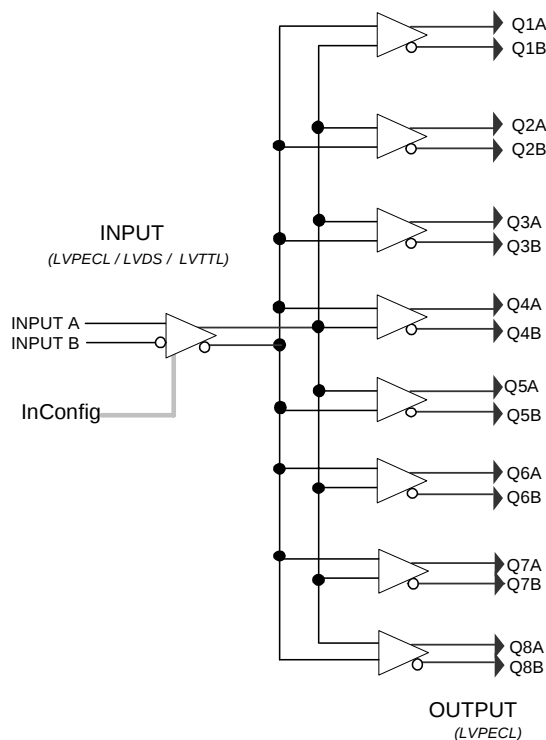
The Cypress CY2DP818 fanout buffer features a single LVDS or a single-ended LVTTL-compatible input and eight LVPECL output pairs.

Designed for data-communications clock-management applications, the large fanout from a single input reduces loading on the input clock.

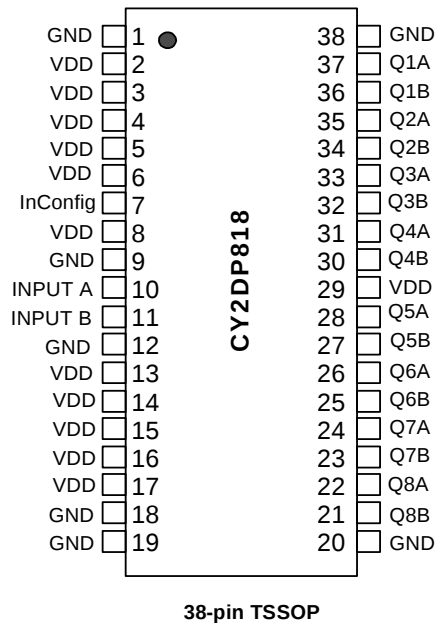
The CY2DP818 is ideal for both level translations from single-ended to LVPECL and/or for the distribution of LVPECL-based clock signals.

The Cypress CY2DP818 has configurable input functions. The input is user configurable via the Inconfig pin for single ended or differential input.

## Block Diagram



## Pin Configuration



## Pin Description

| Pin Number                                                    | Pin Name                                                                     | Pin Standard Interface                                        | Description                                                                                                                                            |
|---------------------------------------------------------------|------------------------------------------------------------------------------|---------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1, 9,12,18,19,20,38                                           | GND                                                                          | POWER                                                         | Ground                                                                                                                                                 |
| 2,3,4,5,6,8, 13,14,15,16,17,29                                | VDD                                                                          | POWER                                                         | Power Supply                                                                                                                                           |
| 10,11                                                         | Input A, Input B                                                             | Default: LVPECL/LDVS<br>Optional: LVTTTL/LVCMOS<br>single pin | Differential input pair or single line.<br>LVPECL/LVDS default. See InConfig,<br>below.                                                                |
| 37, 36,35,34,<br>33,32,31, 30,<br>28,27,26,25,<br>24,23,22,21 | Q1(A,B), Q2(A,B)<br>Q3(A,B), Q4(A,B)<br>Q5(A,B), Q6(A,B)<br>Q7(A,B), Q8(A,B) | LVPECL                                                        | Differential Outputs                                                                                                                                   |
| 7                                                             | InConfig                                                                     | LVTTTL/LVCMOS                                                 | Converts inputs from the default<br>LVPECL/LVDS (logic = 0)<br>To LVTTTL/LVCMOS (logic = 1)<br>See Figure 4 and Figure 5 for additional<br>Information |

## Maximum Ratings<sup>[1]</sup>

Storage Temperature: ..... -65°C to + 150°C  
Ambient Temperature: ..... -40°C to +85°C  
Supply Voltage to Ground Potential  
(Inputs and V<sub>CC</sub> only) ..... -0.3V to 4.6V

Supply Voltage to Ground Potential  
(Outputs only) ..... -0.3V to V<sub>DD</sub> + 0.3V  
DC Input Voltage ..... -0.3V to V<sub>DD</sub> + 0.3V  
DC Output Voltage ..... -0.3V to V<sub>DD</sub> + 0.9V  
Power Dissipation ..... 0.75W

**Table 1. Power Supply Characteristics**

| Parameter | Description                                 | Test Conditions                                                                                                               | Min. | Typ. | Max. | Unit   |
|-----------|---------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------|------|------|------|--------|
| ICCD      | Dynamic Power Supply Current                | V <sub>DD</sub> = Max.<br>Input toggling 50% Duty Cycle,<br>Outputs Open                                                      |      | 1.5  | 2.0  | mA/MHz |
| IC        | Total Power Supply Current                  | V <sub>DD</sub> = Max.<br>Input toggling 50% Duty Cycle,<br>Outputs 50 ohms<br>f <sub>L</sub> =100 MHz                        |      |      | 350  | mA     |
| IC Core   | Core current when output loads are disabled | V <sub>DD</sub> = Max.<br>Input toggling 50% Duty Cycle, Outputs<br>Disabled, not connected to VTT<br>f <sub>L</sub> =100 MHz |      |      | 50   | mA     |

**Table 2. Input Receiver Configuration for Differential or LVTTTL/LVCMOS**

| INCONFIG<br>Pin 7<br>Binary Value | Input Receiver Family | Input Receiver Type                                            |
|-----------------------------------|-----------------------|----------------------------------------------------------------|
| 1                                 | LVTTTL in LVCMOS      | Single-ended, non-inverting, inverting, void of bias resistors |
| 0                                 | LVDS                  | Low-voltage differential signaling                             |
|                                   | LVPECL                | Low-voltage pseudo (positive) emitter coupled logic            |

### Notes:

- Stresses greater than those listed under absolute maximum ratings may cause permanent damage to the device. This is intended to be a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**Table 3. Function Control of the TTL Input Logic used to Accept or Invert the Input Signal**

| LVTTTL/LVCMOS Input Logic |                    |             |                                |
|---------------------------|--------------------|-------------|--------------------------------|
| Input Condition           |                    | Input Logic | Output Logic Q Pins, Q1A or Q1 |
| Ground                    | Input B (–) Pin 11 |             |                                |
|                           | Input A (+) Pin 10 | Input       | True                           |
| VCC                       | Input B (–) Pin 11 |             |                                |
|                           | Input A (+) Pin 10 | Input       | Invert                         |
| Ground                    | Input A (+) Pin 10 |             |                                |
|                           | Input B (–) Pin 11 | Input       | Invert                         |
| VCC                       | Input A (+) Pin 10 |             |                                |
|                           | Input B (–) Pin 11 | Input       | True                           |

**Table 4. DC Electrical Characteristics: 3.3V–LVDS Input**

| Parameter | Description                                                          | Conditions                                           |                   | Min.         | Typ.                 | Max.     | Unit          |
|-----------|----------------------------------------------------------------------|------------------------------------------------------|-------------------|--------------|----------------------|----------|---------------|
| $V_{ID}$  | Magnitude of Differential Input Voltage                              |                                                      |                   | 100          |                      | 600      | mV            |
| $V_{IC}$  | Common-mode of Differential Input Voltage $ V_{ID} $ (min. and max.) |                                                      |                   | $ V_{ID} /2$ | $2.4 - ( V_{ID} /2)$ |          | V             |
| $V_{IH}$  | Input High Voltage                                                   | Guaranteed Logic High Level                          |                   | 2            |                      |          | V             |
| $V_{IL}$  | Input Low Voltage                                                    | Guaranteed Logic Low Level                           |                   |              |                      | 0.8      | V             |
| $I_{IH}$  | Input High Current                                                   | $V_{DD} = \text{Max.}$                               | $V_{IN} = V_{DD}$ |              | $\pm 10$             | $\pm 20$ | $\mu\text{A}$ |
| $I_{IL}$  | Input Low Current                                                    | $V_{DD} = \text{Max.}$                               | $V_{IN} = V_{SS}$ |              | $\pm 10$             | $\pm 20$ | $\mu\text{A}$ |
| $I_I$     | Input High Current                                                   | $V_{DD} = \text{Max.}, V_{IN} = V_{DD}(\text{Max.})$ |                   |              |                      | $\pm 20$ | $\mu\text{A}$ |

**Table 5. DC Electrical Characteristics: 3.3V–LVPECL Input**

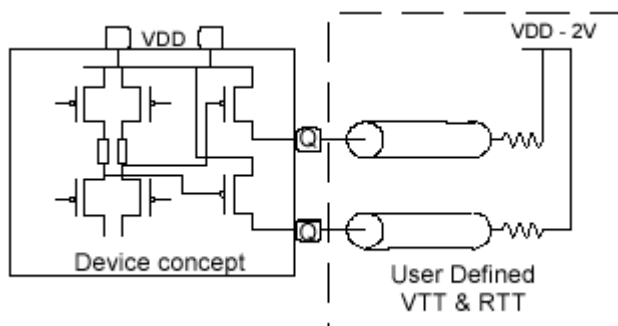
| Parameter | Description                    | Conditions                                           |                   | Min. | Typ.     | Max.     | Unit          |
|-----------|--------------------------------|------------------------------------------------------|-------------------|------|----------|----------|---------------|
| $V_{ID}$  | Differential Input Voltage p-p | Guaranteed Logic High Level                          |                   | 400  |          | 2600     | mV            |
| $V_{IH}$  | Input High Voltage             | Guaranteed Logic High Level                          |                   | 2.15 |          | 2.4      | V             |
| $V_{IL}$  | Input Low Voltage              | Guaranteed Logic Low Level                           |                   | 1.5  |          | 1.8      | V             |
| $I_{IH}$  | Input High Current             | $V_{DD} = \text{Max.}$                               | $V_{IN} = V_{DD}$ |      | $\pm 10$ | $\pm 20$ | $\mu\text{A}$ |
| $I_{IL}$  | Input Low Current              | $V_{DD} = \text{Max.}$                               | $V_{IN} = V_{SS}$ |      | $\pm 10$ | $\pm 20$ | $\mu\text{A}$ |
| $I_I$     | Input High Current             | $V_{DD} = \text{Max.}, V_{IN} = V_{DD}(\text{Max.})$ |                   |      |          | $\pm 20$ | $\mu\text{A}$ |
| $V_{CM}$  | Common-mode Voltage            |                                                      |                   |      |          | 225      | mV            |

**Table 6. DC Electrical Characteristics: 3.3V–LVTTTL/LVCMOS Input**

| Parameter | Description         | Conditions                                          |                        | Min. | Typ. | Max. | Units         |
|-----------|---------------------|-----------------------------------------------------|------------------------|------|------|------|---------------|
| $V_{IH}$  | Input High Voltage  | Guaranteed Logic High Level                         |                        | 2    |      |      | V             |
| $V_{IL}$  | Input Low Voltage   | Guaranteed Logic Low Level                          |                        |      |      | 0.8  | V             |
| $I_{IH}$  | Input High Current  | $V_{DD} = \text{Max}$                               | $V_{IN} = 2.7\text{V}$ |      |      | 1    | $\mu\text{A}$ |
| $I_{IL}$  | Input Low Current   | $V_{DD} = \text{Max}$                               | $V_{IN} = 0.5\text{V}$ |      |      | –1   | $\mu\text{A}$ |
| $I_I$     | Input High Current  | $V_{DD} = \text{Max.}, V_{IN} = V_{DD}(\text{Max})$ |                        |      |      | 20   | $\mu\text{A}$ |
| $V_{IK}$  | Clamp Diode Voltage | $V_{DD} = \text{Min.}, I_{IN} = -18\text{mA}$       |                        |      | –0.7 | –1.2 | V             |
| $V_H$     | Input Hysteresis    |                                                     |                        |      | 80   |      | mV            |

**Table 7. DC Electrical Characteristics: 3.3V–LVPECL Output**

| Parameter | Description                            | Conditions                                                                              | Min. | Typ. | Max. | Unit |
|-----------|----------------------------------------|-----------------------------------------------------------------------------------------|------|------|------|------|
| $V_{OD}$  | Driver Differential Output voltage p-p | $V_{DD} = \text{Min.}, V_{IN} = V_{IH} \text{ or } V_{IL}$<br>$R_L = 50 \text{ ohm}$    | 1000 |      | 3600 | mV   |
| $V_{OC}$  | Driver common-mode p-p                 | $V_{DD} = \text{Min.}, V_{IN} = V_{IH} \text{ or } V_{IL}$<br>$R_L = 50 \text{ ohm}$    |      |      | 300  | mV   |
| Rise Time | Differential 20% to 80%                | $CL = 10 \text{ pF}$ $R_L$ and $CL$ to GND<br>$R_L = 50 \text{ ohm}$                    | 300  |      | 1200 | ps   |
| Fall Time |                                        |                                                                                         |      |      |      |      |
| $V_{OH}$  | Output High Voltage                    | $V_{DD} = \text{Min.}, V_{IN} = V_{IH} \text{ or } V_{IL}$<br>$I_{OH} = -12 \text{ mA}$ | 2.1  |      | 3.0  | V    |
| $V_{OL}$  | Output Low Voltage                     | $V_{DD} = \text{Min.}, V_{IN} = V_{IH} \text{ or } V_{IL}$<br>User defined by VTT RTT.  | 0.8  |      | 1.3  | V    |
| $I_{OS}$  | Short Circuit Current                  | $V_{DD} = \text{Max.}, V_{OUT} = \text{GND}$                                            | -125 |      | -150 | mA   |



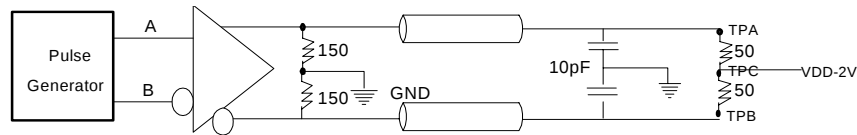
### Driver Design

**Table 8. AC Switching Characteristics @ 3.3 V** ( $V_{DD} = 3.3\text{V} \pm 5\%$ , Temperature =  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$ )

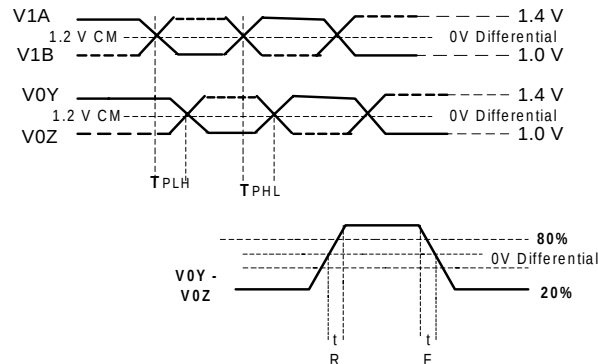
| Parameter   | Description                                                                                                                                                       | Conditions                | Min. | Typ. | Max. | Unit |
|-------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------|------|------|------|------|
| $t_{PLH}$   | Propagation Delay – Low to High                                                                                                                                   | $V_{OD} = 100 \text{ mV}$ | 3    | 4    | 5    | ns   |
| $t_{PHL}$   | Propagation Delay – High to Low                                                                                                                                   |                           | 3    | 4    | 5    | ns   |
| $T_{PE}$    | Enable (EN) to functional operation                                                                                                                               |                           |      |      | 6    | ns   |
| $T_{PD}$    | Functional operation to Disable                                                                                                                                   |                           |      |      | 5    | ns   |
| $t_{SK(0)}$ | Output Skew: Skew between outputs of the same package (in phase)                                                                                                  |                           |      |      | 0.2  | ns   |
| $t_{SK(p)}$ | Pulse Skew: Skew between opposite transitions of the same output ( $t_{PHL} - t_{PLH}$ )                                                                          |                           |      | 0.2  |      | ns   |
| $t_{SK(t)}$ | Package Skew: Skew between outputs of different packages at the same power supply voltage, temperature and package type. Same input signal level and output load. | $V_{ID} = 100 \text{ mV}$ |      |      | 1    | ns   |

**Table 9. High-frequency Parametrics**

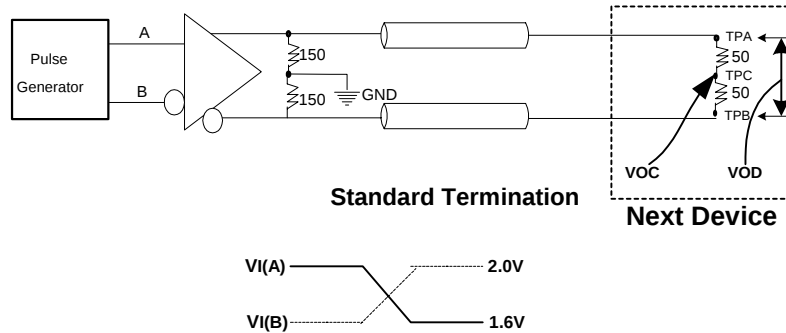
| Parameter | Description                                 | Conditions                                  | Min. | Typ. | Max. | Unit |
|-----------|---------------------------------------------|---------------------------------------------|------|------|------|------|
| $F_{max}$ | Maximum frequency<br>$V_{DD} = 3.3\text{V}$ | 45%–55% duty cycle<br>Standard load circuit |      |      | 350  | MHz  |



### Standard Termination



**Figure 1. Differential Receiver to Driver Propagation Delay and Driver Transition Time**<sup>[2,3,4,5]</sup>



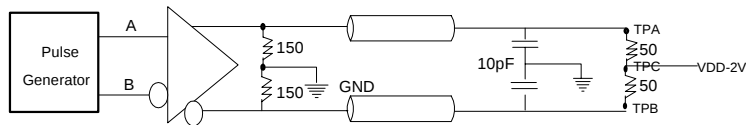
### Standard Termination

### Next Device

**Figure 2. Test Circuit and Voltage Definitions for the Driver Common-Mode Output Voltage**<sup>[2,3,4,5]</sup>

#### Notes:

- All input pulses are supplied by a frequency generator with the following characteristics:  $t_R$  and  $t_F \leq 1$  ns; pulse rate = 50 Mpps; pulse width =  $10 \pm 0.2$  ns.
- $R_L = 50 \text{ ohm} \pm 1\%$ ;  $Z_{line} = 50 \text{ ohm}$  6".
- CL includes instrumentation and fixture capacitance within 6 mm of the UT.
- TPA and B are used for prop delay and Rise/Fall measurements. TPC is used for VOC measurements only and is otherwise connected to  $V_{DD} - 2$ .



Standard Termination

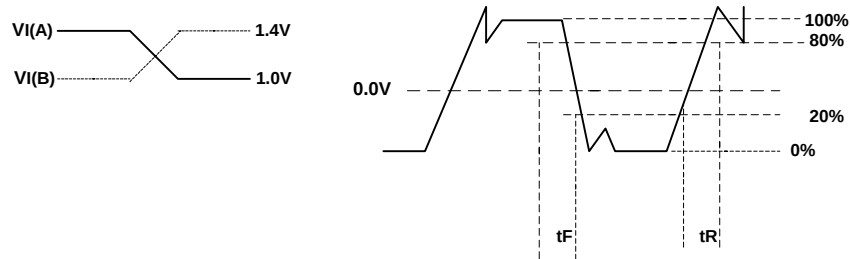


Figure 3. Test Circuit and Voltage Definitions for the Differential Output Signal<sup>[2,3,4,5]</sup>

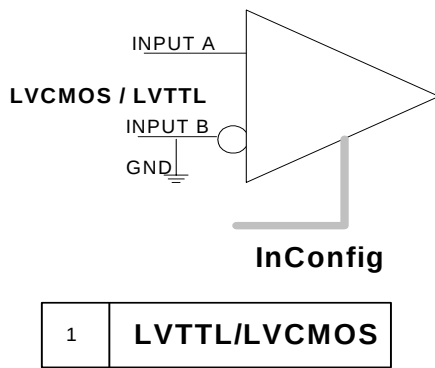


Figure 4. <sup>[6]</sup>

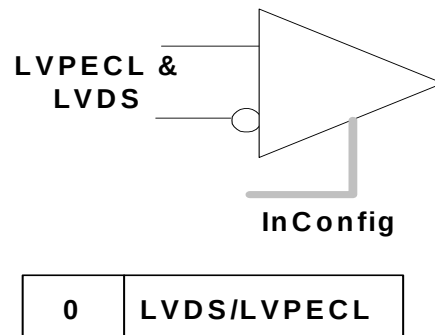


Figure 5. <sup>[7]</sup>

Notes:

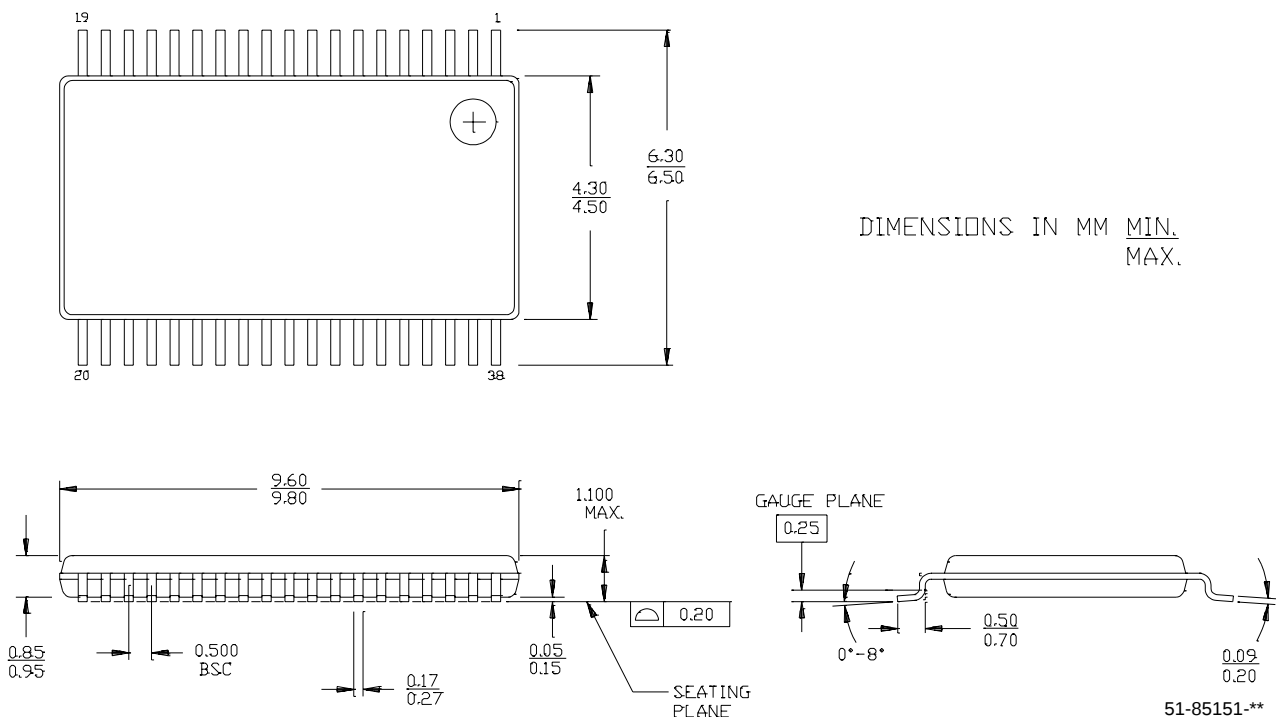
6. See Table 3.
7. LVPECL or LVDS differential input value.

## Ordering Information

| Part Number | Package Type               | Product Flow             |
|-------------|----------------------------|--------------------------|
| CY2DP818ZI  | 38-pin TSSOP               | Industrial, -40° to 85°C |
| CY2DP818ZIT | 38-pin TSSOP–Tape and Reel | Industrial, -40° to 85°C |
| CY2DP818ZC  | 38-pin TSSOP               | Commercial, 0°C to 70°C  |
| CY2DP818ZCT | 38-pin TSSOP–Tape and Reel | Commercial, 0°C to 70°C  |

## Package Drawing and Dimensions

### 38-lead TSSOP (4.40 mm Body) Z38



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| <b>Document Title: CY2DP818 1:8 Clock Fanout Buffer</b><br><b>Document Number: 38-07061</b> |                |                   |                        |                                        |
|---------------------------------------------------------------------------------------------|----------------|-------------------|------------------------|----------------------------------------|
| <b>REV.</b>                                                                                 | <b>ECN NO.</b> | <b>Issue Date</b> | <b>Orig. of Change</b> | <b>Description of Change</b>           |
| **                                                                                          | 107086         | 06/07/01          | IKA                    | New Data Sheet                         |
| *A                                                                                          | 115913         | 07/11/02          | CTK                    | IC, VCM, VOC, Rise/Fall Time Fmax (20) |

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