EMC1422

1°C Temperature Sensor with Hardware Thermal Shutdown

PRODUCT FEATURES

Datasheet

General Description

The EMC1422 is a high accuracy, low cost, System Management Bus (SMBus) temperature sensor. Advanced features such as Resistance Error Correction (REC), Beta Compensation (to support CPU diodes requiring the BJT/transistor model including 45nm, 65nm and 90nm processors) and automatic diode type detection combine to provide a robust solution for complex environmental monitoring applications.

Additionally, the EMC1422 provides a hardware programmable system shutdown feature that is programmed at part power-up via two pull-up resistor values and that cannot be masked or corrupted through the SMBus.

Each device provides ±1° accuracy for external diode temperatures and ±2°C accuracy for the internal diode temperature. The EMC1422 monitors two temperature channels (one external and one internal).

Resistance Error Correction automatically eliminates the temperature error caused by series resistance allowing greater flexibility in routing thermal diodes. Beta Compensation eliminates temperature errors caused by low, variable beta transistors common in today's fine geometry processors. The automatic beta detection feature monitors the external diode/transistor and determines the optimum sensor settings for accurate temperature measurements regardless of processor technology. This frees the user from providing unique sensor configurations for each temperature monitoring application. These advanced features plus ±1°C measurement accuracy provide a low-cost, highly flexible and accurate solution for critical temperature monitoring applications.

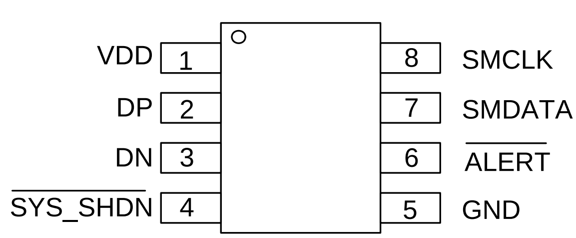
Applications

- Notebook Computers
- Desktop Computers
- Industrial
- Embedded applications

Features

- Hardware Thermal Shutdown
  - triggers dedicated $\overline{\text{SYS\_SHDN}}$ pin
  - hardware configured range 77°C to 112°C in 1°C steps
  - cannot be disabled or modified by software
- Support for diodes requiring the BJT/transistor model
- Designed to support 45nm processors
- Support for 90nm and 65nm CPU diodes
- Pin compatible with ADM1032, MAX6649, and LM99
- Automatically determines external diode type and optimal settings
- Resistance Error Correction
- External Temperature Monitors
  - ±1°C Accuracy (60°C < T_{DIODE} < 100°C)
  - 0.125°C Resolution
  - Supports up to 2.2nF diode filter capacitor
- Internal Temperature Monitor
  - ±2°C accuracy
- 3.3V Supply Voltage
- Programmable temperature limits for $\overline{\text{ALERT}}$
- Small 8-pin MSOP Lead-free RoHS Compliant Package

EMC1422 Pin Description



ORDER NUMBER:

EMC1422-1-ACZL-TR FOR 8 PIN, MSOP LEAD-FREE ROHS COMPLIANT PACKAGE

Note: See Table 1.1, "Part Selection" for SMBus addressing options.

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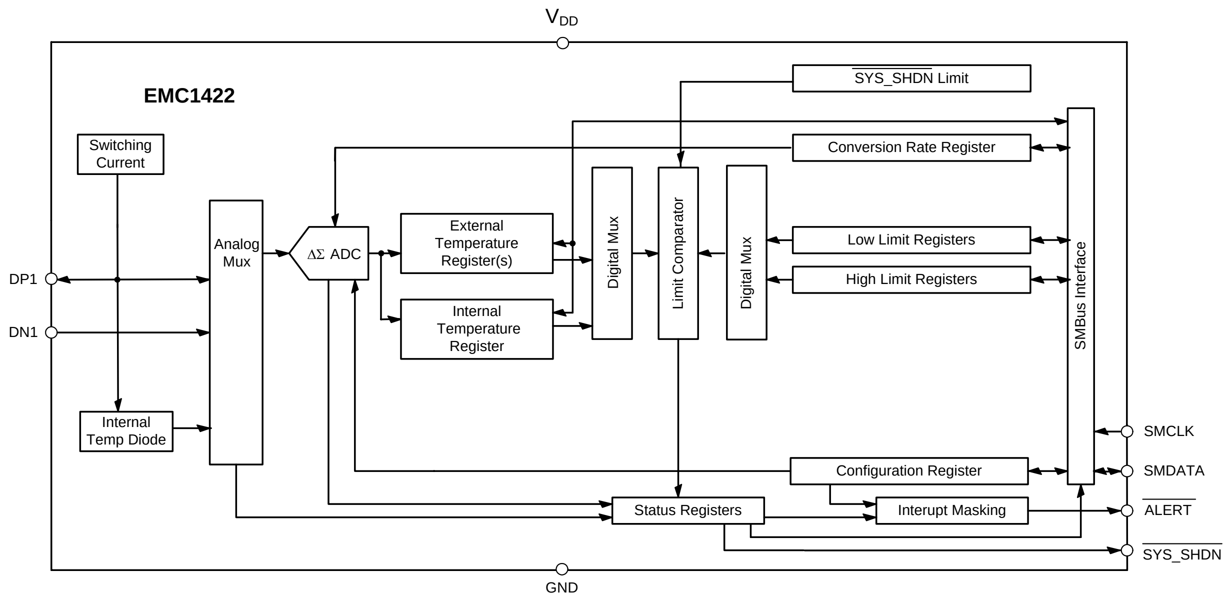

1.1 Part Selection

The EMC1422 device configuration is highlighted below.

Table 1.1 Part Selection

PART NUMBER	SMBUS ADDRESS	FUNCTIONALITY				PRODUCT ID
		EXTERNAL DIODES	DIODE 1 DEFAULT CONFIGURATION	DIODE 2 DEFAULT CONFIGURATION	OTHER	
EMC1422 - 1	100_1100b	1	Detect Diode w/ REC enabled	N/A	Software programmable and maskable High Limit Software programmable and maskable SYS_SHDN Limit Hardware set SYS_SHDN Limit on External Diode 1	22h

Chapter 2 Pin Description

Table 2.1 EMC1422 Preliminary Pin Description

PIN NUMBER	NAME	FUNCTION	TYPE
1	VDD	Power supply	Power
2	DP	External diode positive (anode) connection	AIO
3	DN	External diode negative (cathode) connection	AIO
4	$\overline{\text{SYS\_SHDN}}$	Active low System Shutdown output signal - requires pull-up resistor which selects the Hardware Thermal Shutdown Limit	OD
5	GND	Ground	Power
6	$\overline{\text{ALERT}}$	Active low digital $\overline{\text{ALERT}}$ output signal - requires pull-up resistor,	OD
7	SMDATA	SMBus Data input/output	DIOD
8	SMCLK	SMBus Clock input	DI

The pin types are described below:

Power - these pins are used to supply either VDD or GND to the device.

AIO - Analog Input / Output.

DI - Digital Input.

OD - Open Drain Digital Output.

DIOD - Digital Input / Open Drain Output.

Chapter 3 Electrical Specifications

3.1 Absolute Maximum Ratings

Table 3.1 Absolute Maximum Ratings

DESCRIPTION	RATING	UNIT
Supply Voltage (V_{DD})	-0.3 to 4.0	V
Voltage on SMDATA and SMCLK pins	-0.3 to 5.5	V
Voltage on any other pin to Ground	-0.3 to V_{DD} +0.3	V
Operating Temperature Range	-40 to +125	°C
Storage Temperature Range	-55 to +150	°C
Lead Temperature Range	Refer to JEDEC Spec. J-STD-020	
Package Thermal Characteristics for MSOP-8		
Thermal Resistance (θ_{j-a})	140.8	°C/W
ESD Rating, All pins HBM	2000	V

Note: Stresses at or above those listed could cause permanent damage to the device. This is a stress rating only and functional operation of the device at any other condition above those indicated in the operation sections of this specification is not implied. When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes on their outputs when the AC power is switched on or off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists, it is suggested that a clamp circuit be used.

3.2 Electrical Specifications

Table 3.2 Electrical Specifications

V_{DD} = 3.0V to 3.6V, T_A = -40°C to 125°C, all typical values at T_A = 27°C unless otherwise noted.						
CHARACTERISTIC	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNITS**	**CONDITIONS**
DC Power						
Supply Voltage	V_{DD}	3.0	3.3	3.6	V	
Supply Current	I_{DD}		430	850	uA	1 conversion / sec, dynamic averaging disabled
			930	1200	uA	4 conversions / sec, dynamic averaging enabled
			1120		uA	$\geq$ 16 conversions / sec, dynamic averaging enabled

Table 3.2 Electrical Specifications (continued)

CHARACTERISTIC	SYMBOL	MIN	TYP	MAX	UNITS	CONDITIONS
V_{DD} = 3.0V to 3.6V, T_A = -40°C to 125°C, all typical values at T_A = 27°C unless otherwise noted.						
Internal Temperature Monitor						
Temperature Accuracy			±0.25	±1	°C	0°C < T_A < 100°C
				±2	°C	-40°C < T_A < 125°C
Temperature Resolution			0.125		°C	
External Temperature Monitor						
Temperature Accuracy			±0.25	±1	°C	+20°C < T_{DIODE} < +110°C 0°C < T_A < 100°C
			±0.5	±2	°C	-40°C < T_{DIODE} < 127°C
Temperature Resolution			0.125		°C	
Conversion Time all Channels	t_{CONV}		190		ms	EMC1422, default settings
Capacitive Filter	C_{FILTER}		2.2	2.5	nF	Connected across external diode
$\overline{\text{ALERT}}$ and $\overline{\text{SYS\_SHDN}}$ pins						
Output Low Voltage	V_{OL}	0.4			V	I_{SINK} = 8mA
Power up time				15	ms	Temp selection read Note 3.1

Note 3.1 During the power up time, SMBus communication is permitted, however the $\overline{\text{SYS\_SHDN}}$ and $\overline{\text{ALERT}}$ pins must not be pulled low.

3.3 SMBus Electrical Characteristics

Table 3.3 SMBus Electrical Specifications

V_{DD} = 3.0V to 3.6V, T_A = -40°C to 125°C, all typical values are at T_A = 27°C unless otherwise noted.						
CHARACTERISTIC	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNITS**	**CONDITIONS**
SMBus Interface						
Input High Voltage	V_{IH}	2.0		V_{DD}	V	5V Tolerant
Input Low Voltage	V_{IL}	-0.3		0.8	V	5V Tolerant
Input High/Low Current	I_{IH} / I_{IL}			±5	uA	Powered or unpowered TA < 85°C
Hysteresis			420		mV	
Input Capacitance	C_{IN}		5		pF	
Output Low Sink Current	I_{OL}	8.2		15	mA	SMDATA = 0.4V
SMBus Timing						
Clock Frequency	f_{SMB}	10		400	kHz	
Spike Suppression	t_{SP}			50	ns	
Bus free time Start to Stop	t_{BUF}	1.3			us	
Hold Time: Start	$t_{HD:STA}$	0.6			us	
Setup Time: Start	$t_{SU:STA}$	0.6			us	
Setup Time: Stop	$t_{SU:STP}$	0.6			us	
Data Hold Time	$t_{HD:DAT}$	0.3			us	
Data Setup Time	$t_{SU:DAT}$	100			ns	
Clock Low Period	t_{LOW}	1.3			us	
Clock High Period	t_{HIGH}	0.6			us	
Clock/Data Fall time	t_{FALL}			300	ns	Min = 20+0.1C_{LOAD} ns
Clock/Data Rise time	t_{RISE}			300	ns	Min = 20+0.1C_{LOAD} ns
Capacitive Load	C_{LOAD}			400	pF	per bus line

Chapter 4 System Management Bus Interface Protocol

4.1 System Management Bus Interface Protocol

The EMC1422 communicates with a host controller, such as an SMSC SIO, through the SMBus. The SMBus is a two-wire serial communication protocol between a computer host and its peripheral devices. A detailed timing diagram is shown in Figure 4.1

For the first 15ms after power-up the device may not respond to SMBus communications.

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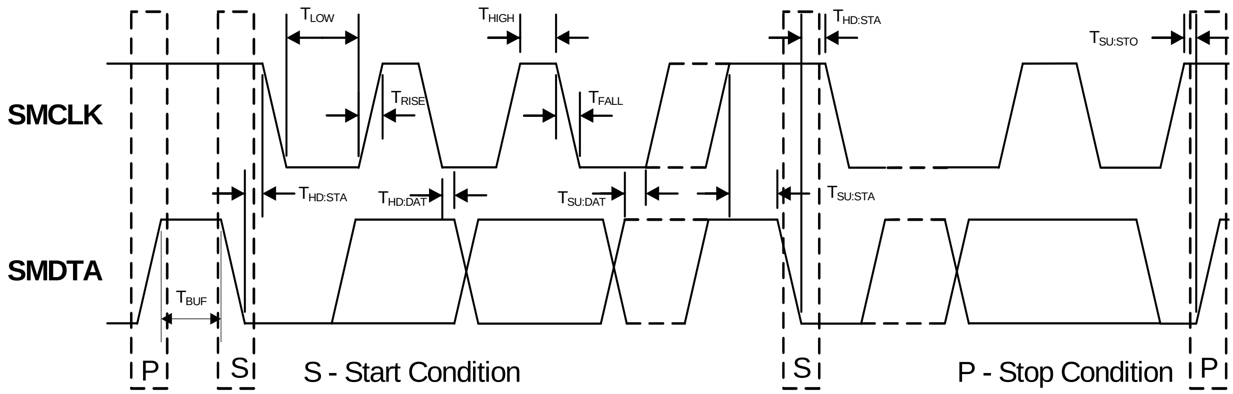


Figure 4.1 SMBus Timing Diagram

The EMC1422 is SMBus 2.0 compatible and support Send Byte, Read Byte, Write Byte, Receive Byte, and the Alert Response Address as valid protocols as shown below.

All of the below protocols use the convention in Table 4.1.

Table 4.1 Protocol Format

DATA SENT TO DEVICE	DATA SENT TO THE HOST
# of bits sent	# of bits sent

Attempting to communicate with the EMC1422 SMBus interface with an invalid slave address or invalid protocol will result in no response from the device and will not affect its register contents. Stretching of the SMCLK signal is supported, provided other devices on the SMBus control the timing.

4.2 Write Byte

The Write Byte is used to write one byte of data to the registers as shown below Table 4.2:

Table 4.2 Write Byte Protocol

START	SLAVE ADDRESS	WR	ACK	REGISTER ADDRESS	ACK	REGISTER DATA	ACK	STOP
1	7	1	1	8	1	8	1	1

4.3 Read Byte

The Read Byte protocol is used to read one byte of data from the registers as shown in Table 4.3.

Table 4.3 Read Byte Protocol

START	SLAVE ADDRESS	WR	ACK	REGISTER ADDRESS	ACK	START	SLAVE ADDRESS	RD	ACK	REGISTER DATA	NACK	STOP
1	7	1	1	8	1	1	7	1	1	8	1	1

4.4 Send Byte

The Send Byte protocol is used to set the internal address register pointer to the correct address location. No data is transferred during the Send Byte protocol as shown in Table 4.4.

Table 4.4 Send Byte Protocol

START	SLAVE ADDRESS	WR	ACK	REGISTER ADDRESS	ACK	STOP
1	7	1	1	8	1	1

4.5 Receive Byte

The Receive Byte protocol is used to read data from a register when the internal register address pointer is known to be at the right location (e.g. set via Send Byte). This is used for consecutive reads of the same register as shown in Table 4.5.

Table 4.5 Receive Byte Protocol

START	SLAVE ADDRESS	RD	ACK	REGISTER DATA	NACK	STOP
1	7	1	1	8	1	1

4.6 Alert Response Address

The $\overline{\text{ALERT}}$ output can be used as a processor interrupt or as an SMBus Alert.

When it detects that the $\overline{\text{ALERT}}$ pin is asserted, the host will send the Alert Response Address (ARA) to the general address of 000_1100b. All devices with active interrupts will respond with their client address as shown in Table 4.6.

Table 4.6 Alert Response Address Protocol

START	ALERT RESPONSE ADDRESS	RD	ACK	DEVICE ADDRESS	NACK	STOP
1	7	1	1	8	1	1

The EMC1422 will respond to the ARA in the following way:

1. Send Slave Address and verify that full slave address was sent (i.e. the SMBus communication from the device was not prematurely stopped due to a bus contention event).
2. Set the MASK bit to clear the $\overline{\text{ALERT}}$ pin.

APPLICATION NOTE: The ARA does not clear the Status Register and if the MASK bit is cleared prior to the Status Register being cleared, the $\overline{\text{ALERT}}$ pin will be reasserted.

4.7 SMBus Address

The EMC1422-1 responds to hard-wired SMBus slave address as shown in Table 1.1.

Note: Other addresses are available. Contact SMSC for more information.

4.8 SMBus Timeout

The EMC1422 supports SMBus Timeout. If the clock line is held low for longer than 30ms, the device will reset its SMBus protocol. This function can be disabled by clearing the TIMEOUT bit in the Consecutive Alert Register (see Section 6.13).

Chapter 5 Product Description

The EMC1422 is an SMBus temperature sensor with Hardware Thermal Shutdown. The EMC1422 monitors one internal diode and one externally connected temperature diode.

Thermal management is performed in cooperation with a host device. This consists of the host reading the temperature data of both the external and internal temperature diodes of the EMC1422 and using that data to control the speed of one or more fans.

The EMC1422 has two levels of monitoring. The first provides a maskable ALERT signal to the host when measured temperatures meet or exceed user programmable limits. This allows the EMC1422 to be used as an independent thermal watchdog to warn the host of temperature hot spots without direct control by the host.

The second level of monitoring asserts the SYS_SHDN pin when the External Diode temperature exceeds a hardware specified threshold temperature. Additionally, the internal diodecan be configured to assert the SYS_SHDN pin when the measured temperature exceeds user programmable limits.

Since the EMC1422 automatically corrects for temperature errors due to series resistance in temperature diode lines, there is greater flexibility in where external diodes are positioned and better measurement accuracy than previously available with non-resistance error correcting devices. The automatic beta detection feature means that there is no need to program the device according to which type of diode is present. This also includes CPU diodes that require the transistor or BJT model for monitoring their temperature. Therefore, the EMC1422 can power up ready to operate for any system configuration.

Figure 5.1 shows a system level block diagram of the EMC1422.

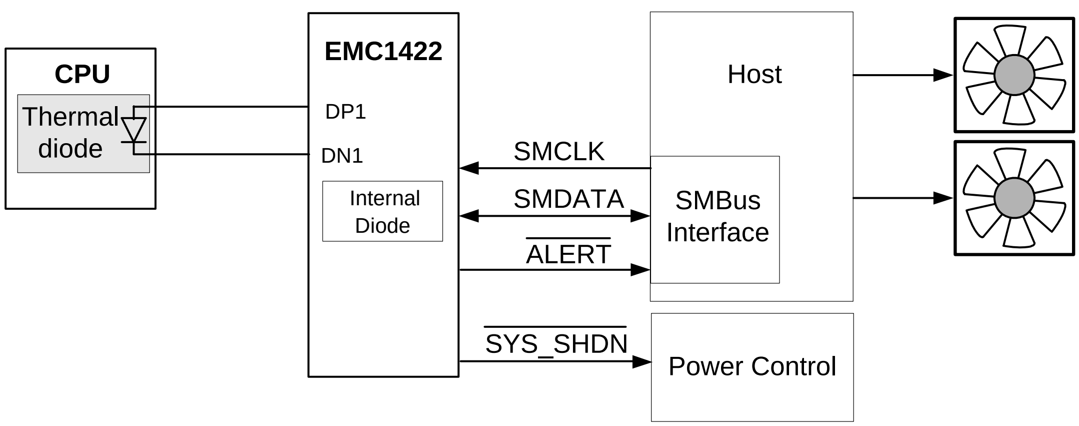


Figure 5.1 System Diagram for EMC1422

5.0.1 Conversion Rates

The EMC1422 may be configured for different conversion rates based on the system requirements. The conversion rate is configured as described in Section 6.5. The default conversion rate is 4 conversions per second. Other available conversion rates are shown in Table 6.6.

5.0.2 Dynamic Averaging

Dynamic averaging causes the EMC1422 to measure the external diode channels for an extended time based on the selected conversion rate. This functionality can be disabled for increased power savings at the lower conversion rates (see Section 6.4). When dynamic averaging is enabled, the device will automatically adjust the sampling and measurement time for the external diode channels. This allows the device to average 2x or 16x longer than the normal 11 bit operation (nominally 21ms per channel) while still maintaining the selected conversion rate. The benefits of dynamic averaging are improved noise rejection due to the longer integration time as well as less random variation of the temperature measurement.

When enabled, the dynamic averaging will affect the average supply current based on the chosen conversion rate as shown in Table 5.1 for the EMC1422.

Table 5.1 Supply Current vs. Conversion Rate for EMC1422

CONVERSION RATE	AVERAGE SUPPLY CURRENT		AVERAGING FACTOR (BASED ON 11-BIT OPERATION)	
	ENABLED (DEFAULT)	DISABLED	ENABLED (DEFAULT)	DISABLED
1 / sec	365uA	130uA	16x	1x
2 / sec	625uA	165uA	16x	1x
4 / sec (default)	660uA	225uA	8x	1x
8 / sec	725uA	350uA	4x	1x
16 / sec	730uA	485uA	2x	1x
32 / sec	745uA	745uA	1x	1x
64 / sec	775uA	775uA	0.5x	0.5x

5.1 SYS_SHDN Output

The SYS_SHDN output is asserted independently of the ALERT output and cannot be masked. If the External Diode temperature exceeds the Hardware Thermal Shutdown Limit for the programmed number of consecutive measurements, then the SYS_SHDN pin is asserted.

The Hardware Thermal Shutdown Limit is defined at power-up via the pull-up resistors on the SYS_SHDN and ALERT pins as shown in Table 5.2. This limit cannot be modified or masked via software.

In addition to External Diode channel triggering the SYS_SHDN pin when the measured temperature exceeds to the Hardware Thermal Shutdown Limit, each of the measurement channels can be configured to assert the SYS_SHDN pin when they exceed the corresponding THERM Limit.

When the SYS_SHDN pin is asserted, it will not release until the External Diode temperature drops below the Hardware Thermal Shutdown Limit minus 10°C and all other measured temperatures drop below the THERM Limit minus the THERM Hysteresis value (when linked to SYS_SHDN).

Figure 5.2 shows a block diagram of the interaction between the input channels and the SYS_SHDN pin.

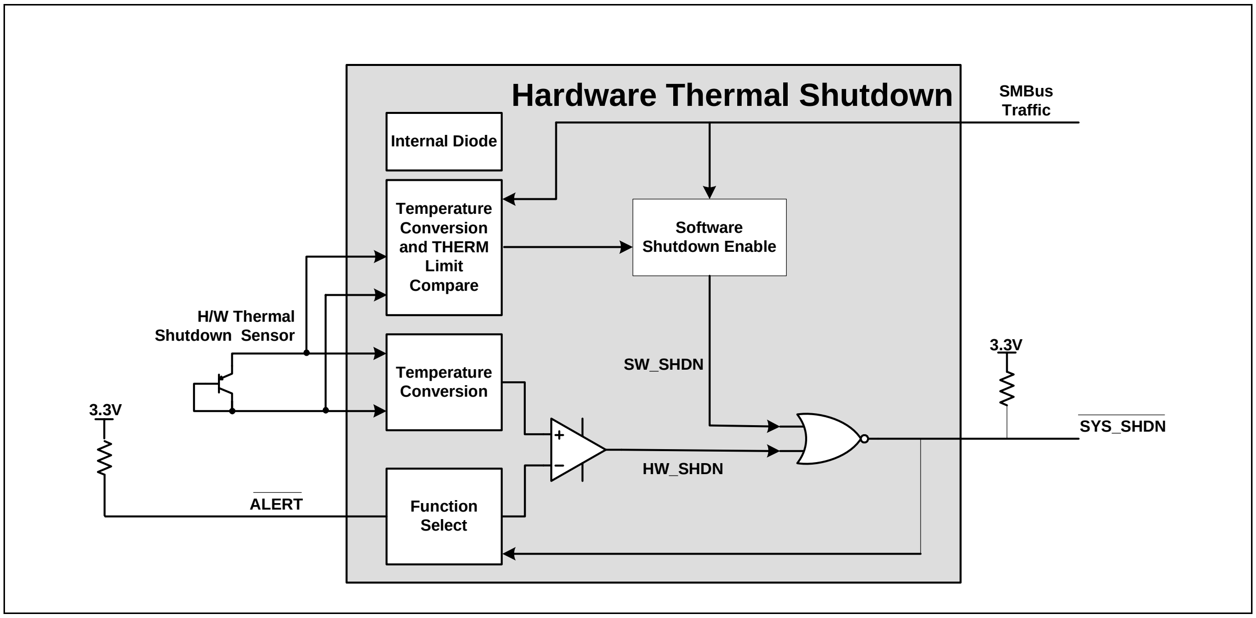


Figure 5.2 Block Diagram of Hardware Thermal Shutdown

5.2 Hardware Thermal Shutdown Limit

The Hardware Thermal Shutdown Limit temperature is determined by pull-up resistors on the SYS_SHDN and ALERT pins shown in Table 5.2.

Table 5.2 SYS_SHDN Threshold Temperature

SYS_SHD PULL-UP / ALERT PULL-UP	4.7K OHM ±10%	6.8K OHM ±10%	10K OHM ±10%	15K OHM ±10%	22K OHM ±10%	33K OHM ±10%
4.7K OHM ±10%	77°C	83°C	89°C	95°C	101°C	107°C
6.8K OHM ±10%	78°C	84°C	90°C	96°C	102°C	108°C
10K OHM ±10%	79°C	85°C	91°C	97°C	103°C	109°C
15K OHM ±10%	80°C	86°C	92°C	98°C	104°C	110°C
22K OHM ±10%	81°C	87°C	93°C	99°C	105°C	111°C
33K OHM ±10%	82°C	88°C	94°C	100°C	106°C	112°C

5.3 ALERT Output

The ALERT pin is an open drain output and requires a pull-up resistor to V_{DD} and has two modes of operation: interrupt mode and comparator Mode. The mode of the ALERT output is selected via the ALERT / COMP bit in the Configuration Register (see Section 6.4).

5.3.1 ALERT Pin Interrupt Mode

When configured to operate in interrupt mode, the ALERT pin asserts low when an out of limit measurement (≥ high limit or < low limit) is detected on any diode or when a diode fault is detected. The ALERT pin will remain asserted as long as an out-of-limit condition remains. Once the out-of-limit condition has been removed, the ALERT pin will remain asserted until the appropriate status bits are cleared.

The ALERT pin can be masked by setting the MASK bit. Once the ALERT pin has been masked, it will be de-asserted and remain de-asserted until the MASK bit is cleared by the user. Any interrupt conditions that occur while the ALERT pin is masked will update the Status Register normally.

The ALERT pin is used as an interrupt signal or as an Smbus Alert signal that allows an SMBus slave to communicate an error condition to the master. One or more ALERT outputs can be hard-wired together.

5.3.2 ALERT Pin Comparator Mode

When the ALERT pin is configured to operate in comparator mode it will be asserted if any of the measured temperatures exceeds the respective high limit. The ALERT pin will remain asserted until all temperatures drop below the corresponding high limit minus the THERM Hysteresis value.

When the ALERT pin is asserted in comparator mode, the corresponding high limit status bits will be set. Reading these bits will not clear them until the ALERT pin is deasserted. Once the ALERT pin is deasserted, the status bits will be automatically cleared.

The MASK bit will not block the ALERT pin in this mode, however the individual channel masks (see Section 6.12) will prevent the respective channel from asserting the ALERT pin.

5.4 ALERT and SYS_SHDN Pin Considerations

Because of the decode method used to determine the Hardware Thermal Shutdown Limit, it is important that the pull-up resistance on both the ALERT and SYS_SHDN pins be within the tolerances shown in Table 5.2. Additionally, the pull-up resistor on the ALERT and SYS_SHDN pins must be connected to the same 3.3V supply that drives the VDD pin.

For 15ms after power up, the ALERT and SYS_SHDN pins must not be pulled low or the Hardware Thermal Shutdown Limit will not be decoded properly. If the system requirements do not permit these conditions, then the ALERT and SYS_SHDN pins must be isolated from their respective busses during this time.

One method of isolating this pin is shown in Figure 5.3.

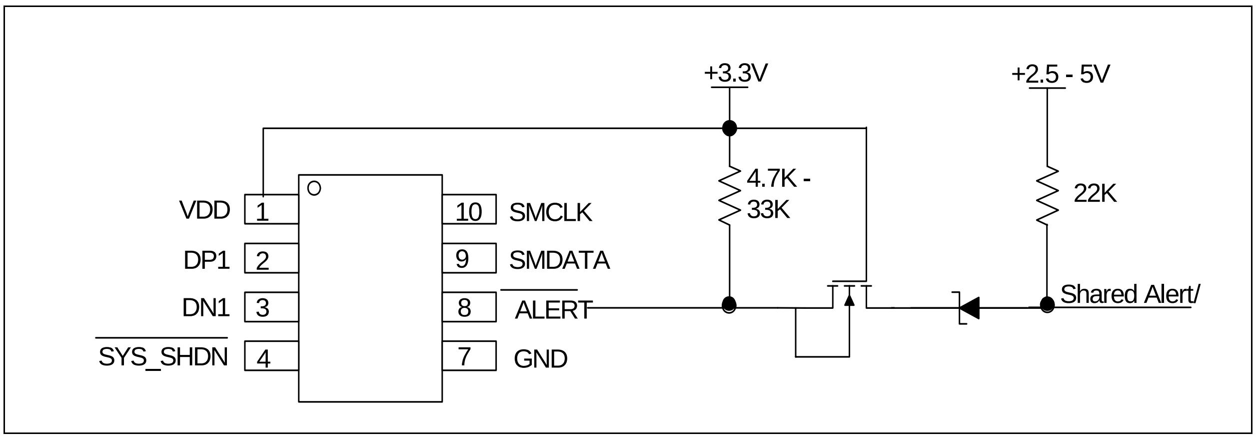


Figure 5.3 Isolating ALERT and SYS_SHDN Pins

5.5 Beta Compensation

The EMC1422 is configured to monitor the temperature of basic diodes (e.g. 2N3904), or CPU thermal diodes. It automatically detects the type of external diode (CPU diode or diode connected transistor) and determines the optimal setting to reduce temperature errors introduced by beta variation.Compensating for this error is also known as implementing the transistor or BJT model for temperature measurement.

For discrete transistors configured with the collector and base shorted together, the beta is generally sufficiently high such that the percent change in beta variation is very small. For example, a 10% variation in beta for two forced emitter currents with a transistor whose ideal beta is 50 would contribute approximately 0.25°C error at 100°C. However for substrate transistors where the base-emitter junction is used for temperature measurement and the collector is tied to the substrate, the proportional beta variation will cause large error. For example, a 10% variation in beta for two forced emitter currents with a transistor whose ideal beta is 0.5 would contribute approximately 8.25°C error at 100°C.

5.6 Resistance Error Correction (REC)

Parasitic resistance in series with the external diodes will limit the accuracy obtainable from temperature measurement devices. The voltage developed across this resistance by the switching diode currents cause the temperature measurement to read higher than the true temperature. Contributors to series resistance are PCB trace resistance, on die (i.e. on the processor) metal resistance, bulk resistance in the base and emitter of the temperature transistor. Typically, the error caused by series resistance is +0.7°C per ohm. The EMC1422 automatically corrects up to 100 ohms of series resistance.

APPLICATION NOTE: When monitoring a substrate transistor or CPU diode and beta compensation is enabled, the Ideality Factor should not be adjusted. Beta Compensation automatically corrects for most ideality errors.

5.7 Diode Faults

The EMC1422 detects an open on the DP and DN pins, and a short across the DP and DN pins. For each temperature measurement made, the device checks for a diode fault on the external diode channel(s). When a diode fault is detected, the ALERT pin asserts (unless masked, see Section 5.8) and the temperature data reads 00h in the MSB and LSB registers (note: the low limit will not be checked). A diode fault is defined as one of the following: an open between DP and DN, a short from V_{DD} to DP, or a short from V_{DD} to DN.

If a short occurs across DP and DN or a short occurs from DP to GND, the low limit status bit is set and the ALERT pin asserts (unless masked). This condition is indistinguishable from a temperature measurement of 0.000degC (-64°C in extended range) resulting in temperature data of 00h in the MSB and LSB registers.

If a short from DN to GND occurs (with a diode connected), temperature measurements will continue as normal with no alerts.

5.8 Consecutive Alerts

The EMC1422 contains multiple consecutive alert counters. One set of counters applies to the $\overline{\text{ALERT}}$ pin and the second set of counters applies to the $\overline{\text{SYS\_SHDN}}$ pin. Each temperature measurement channel has a separate consecutive alert counter for each of the $\overline{\text{ALERT}}$ and $\overline{\text{SYS\_SHDN}}$ pins. All counters are user programmable and determine the number of consecutive measurements that a temperature channel(s) must be out-of-limit or reporting a diode fault before the corresponding pin is asserted.

See Section 6.13 for more details on the consecutive alert function.

5.9 Digital Filter

To reduce the effect of noise and temperature spikes on the reported temperature, the External Diode channel uses a programmable digital filter. This filter can be configured as Level 1, Level 2, or Disabled. The typical filter performance is shown in Figure 5.4 and Figure 5.5.

Figure 5.4 Temperature Filter Step Response

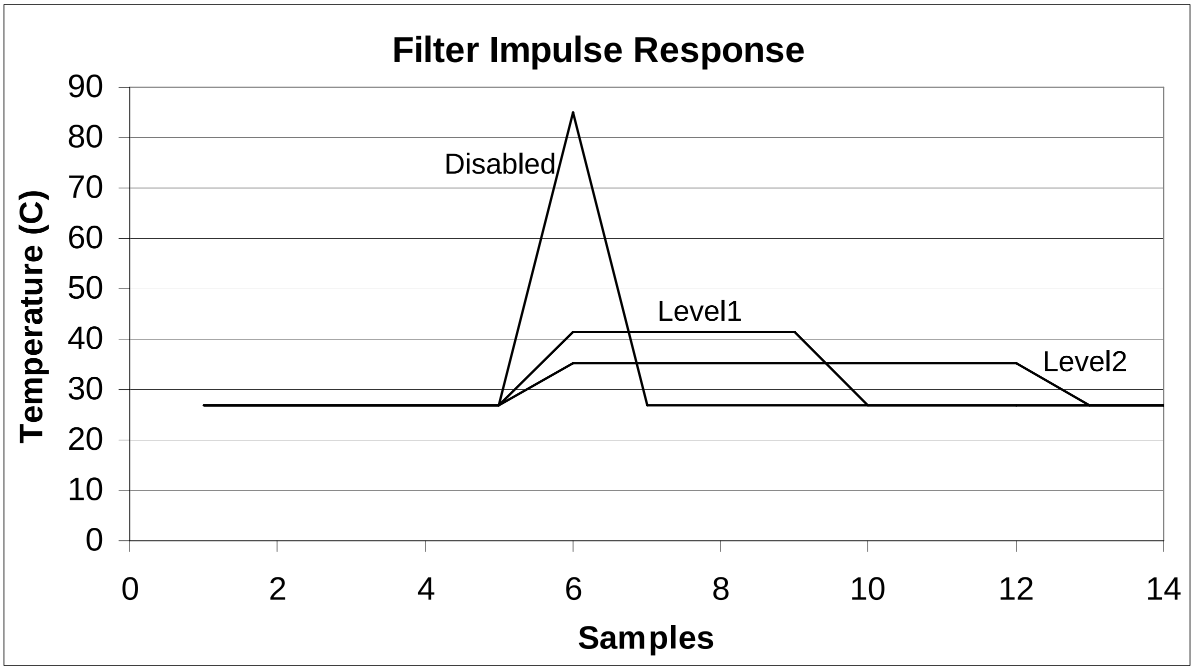


Figure 5.5 Temperature Filter Impulse Response

5.10 Temperature Monitors

In general, thermal diode temperature measurements are based on the change in forward bias voltage of a diode when operated at two different currents. This ΔV_{BE} is proportional to absolute temperature as shown in the following equation:

$$\Delta V_{BE} = \frac{\eta kT}{q} \ln\left(\frac{I_{HIGH}}{I_{LOW}}\right) \qquad [1]$$

where:

k = Boltzmann's constant

T = absolute temperature in Kelvin

q = electron charge

η = diode ideality factor

Figure 5.6 shows a block diagram of the temperature measurement circuit. The negative terminal for the remote temperature diode, DN, is internally biased with a forward diode voltage referenced to ground.

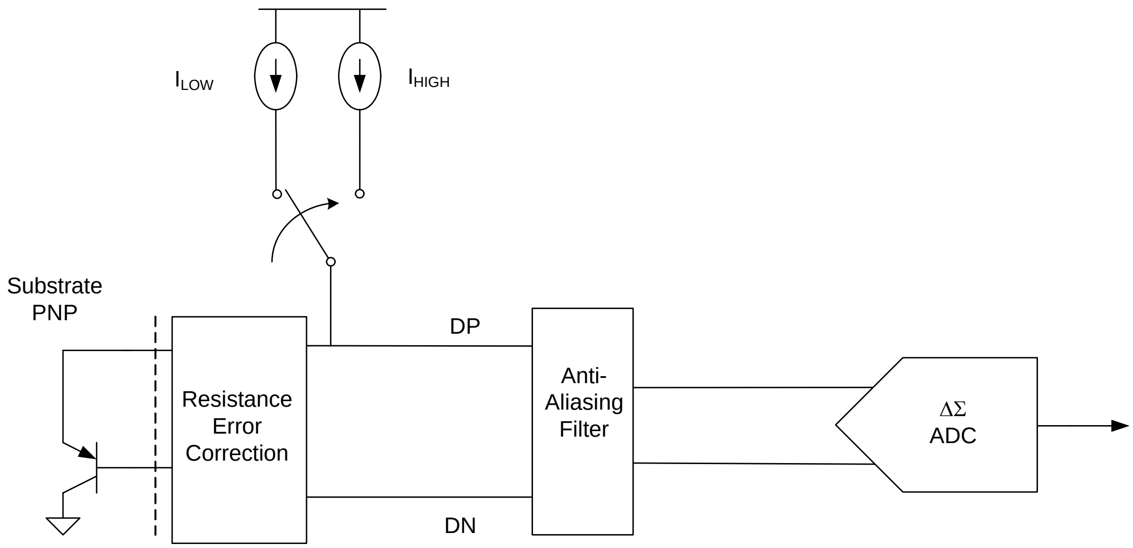


Figure 5.6 Block Diagram of Temperature Monitoring Circuit

5.11 Temperature Measurement Results and Data

The temperature measurement results are stored in the internal and external temperature registers. These are then compared with the values stored in the high and low limit registers. Both external and internal temperature measurements are stored in 11-bit format with the eight (8) most significant bits stored in a high byte register and the three (3) least significant bits stored in the three (3) MSB positions of the low byte register. All other bits of the low byte register are set to zero.

The EMC1422 has two selectable temperature ranges. The default range is from 0°C to +127°C and the temperature is represented as binary number able to report a temperature from 0°C to +127.875°C in 0.125°C steps.

The extended range is an extended temperature range from -64°C to +191°C. The data format is a binary number offset by 64°C. The extended range is used to measure temperature diodes with a large known offset (such as AMD processor diodes) where the diode temperature plus the offset would be equivalent to a temperature higher than +127°C.

Table 5.3 shows the default and extended range formats.

Table 5.3 EMC1422 Temperature Data Format

TEMPERATURE (°C)	DEFAULT RANGE 0°C TO 127°C	EXTENDED RANGE RANGE -64°C TO 191°C
Diode Fault	000 0000 0000	000 0000 0000
-64	000 0000 0000	000 0000 0000 Note 5.2
-1	000 0000 0000	001 1111 1111
0	000 0000 0000 Note 5.1	010 0000 0000
0.125	000 0000 0001	010 0000 0001
1	000 0000 1000	010 0000 1000

Table 5.3 EMC1422 Temperature Data Format (continued)

TEMPERATURE (°C)	DEFAULT RANGE 0°C TO 127°C	EXTENDED RANGE RANGE -64°C TO 191°C
64	010 0000 0000	100 0000 0000
65	010 0000 1000	100 0000 1000
127	011 1111 1000	101 1111 1000
127.875	011 1111 1111	101 1111 1111
128	011 1111 1111 Note 5.3	110 0000 0000
190	011 1111 1111	111 1111 0000
191	011 1111 1111	111 1111 1000
>= 191.875	011 1111 1111	111 1111 1111 Note 5.4

Note 5.1 In default mode, all temperatures < 0°C will be reported as 0°C.

Note 5.2 In the extended range, all temperatures < -64°C will be reported as -64°C.

Note 5.3 For the default range, all temperatures > +127.875°C will be reported as +127.875°C.

Note 5.4 For the extended range, all temperatures > +191.875°C will be reported as +191.875°C.

5.12 External Diode Connections

The EMC1422 is hard-wired to measure a specific kind of thermal diode and none of the measurement options can be changed by software. Figure 5.7 shows the different diode configurations.

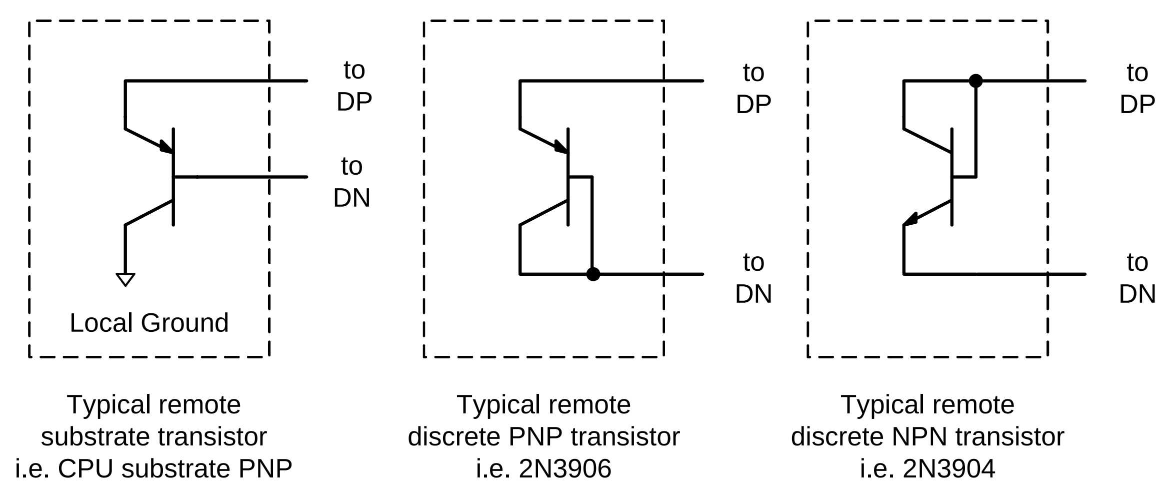


Figure 5.7 Diode Configurations

Chapter 6 Register Description

The registers shown in Table 6.1 are accessible through the SMBus. An entry of '-' indicates that the bit is not used and will always read '0'.

Table 6.1 Register Set in Hexadecimal Order

REGISTER ADDRESS	R/W	REGISTER NAME	FUNCTION	DEFAULT VALUE	PAGE
00h	R	Internal Diode Data High Byte	Stores the integer data for the Internal Diode	00h	Page 26
01h	R	External Diode Data High Byte	Stores the integer data for the External Diode	00h	
02h	R	Status	Stores the status bits for the Internal Diode and External Diodes	00h	Page 26
03h	R/W	Configuration	Controls the general operation of the device (mirrored at address 09h)	00h	Page 27
04h	R/W	Conversion Rate	Controls the conversion rate for updating temperature data (mirrored at address 0Ah)	06h (4/sec)	Page 28
05h	R/W	Internal Diode High Limit	Stores the 8-bit high limit for the Internal Diode (mirrored at address 0Bh)	55h (85°C)	Page 28
06h	R/W	Internal Diode Low Limit	Stores the 8-bit low limit for the Internal Diode (mirrored at address 0Ch)	00h (0°C)	
07h	R/W	External Diode High Limit High Byte	Stores the integer portion of the high limit for the External Diode (mirrored at register 0Dh)	55h (85°C)	
08h	R/W	External Diode Low Limit High Byte	Stores the integer portion of the low limit for the External Diode (mirrored at register 0Eh)	00h (0°C)	
09h	R/W	Configuration	Controls the general operation of the device (mirrored at address 03h)	00h	Page 27
0Ah	R/W	Conversion Rate	Controls the conversion rate for updating temperature data (mirrored at address 04h)	06h (4/sec)	Page 28

Table 6.1 Register Set in Hexadecimal Order (continued)

REGISTER ADDRESS	R/W	REGISTER NAME	FUNCTION	DEFAULT VALUE	PAGE
0Bh	R/W	Internal Diode High Limit	Stores the 8-bit high limit for the Internal Diode (mirrored at address 05h)	55h (85°C)	Page 28
0Ch	R/W	Internal Diode Low Limit	Stores the 8-bit low limit for the Internal Diode (mirrored at address 06h)	00h (0°C)	
0Dh	R/W	External Diode High Limit High Byte	Stores the integer portion of the high limit for the External Diode (mirrored at register 07h)	55h (85°C)	
0Eh	R/W	External Diode Low Limit High Byte	Stores the integer portion of the low limit for the External Diode (mirrored at register 08h)	00h (0°C)	
10h	R	External Diode Data Low Byte	Stores the fractional data for the External Diode	00h	Page 26
11h	R/W	Scratchpad	Scratchpad register for software compatibility	00h	Page 29
12h	R/W	Scratchpad	Scratchpad register for software compatibility	00h	Page 29
13h	R/W	External Diode High Limit Low Byte	Stores the fractional portion of the high limit for the External Diode	00h	Page 28
14h	R/W	External Diode Low Limit Low Byte	Stores the fractional portion of the low limit for the External Diode	00h	
19h	R/W	External Diode THERM Limit	Stores the 8-bit critical temperature limit for the External Diode	55h (85°C)	Page 29
1Dh	R/W	SYS_SHDN Configuration	Controls which software channels, if any, are linked to the SYS_SHDN pin	00h	Page 30
1Eh	R	Hardware Thermal Shutdown Limit	When read, returns the selected Hardware Thermal Shutdown Limit	N/A	Page 31
1Fh	R/W	Channel Mask Register	Controls the masking of individual channels	00h	Page 31
20h	R/W	Internal Diode THERM Limit	Stores the 8-bit critical temperature limit for the Internal Diode	55h (85°C)	Page 29
21h	R/W	THERM Hysteresis	Stores the 8-bit hysteresis value that applies to all THERM limits	0Ah (10°C)	
22h	R/W	Consecutive ALERT	Controls the number of out-of-limit conditions that must occur before an interrupt is asserted	70h	Page 31
29h	R	Internal Diode Data Low Byte	Stores the fractional data for the Internal Diode	00h	Page 26
35h	R-C	High Limit Status	Status bits for the High Limits	00h	Page 33
36h	R-C	Low Limit Status	Status bits for the Low Limits	00h	Page 33
37h	R	THERM Limit Status	Status bits for the THERM Limits	00h	Page 34

Table 6.1 Register Set in Hexadecimal Order (continued)

REGISTER ADDRESS	R/W	REGISTER NAME	FUNCTION	DEFAULT VALUE	PAGE
40h	R/W	Filter Control	Controls the digital filter setting for the External Diode channel	00h	Page 34
FDh	R	Product ID	Stores a fixed value that identifies each product	Table 6.21	Page 35
FEh	R	SMSC ID	Stores a fixed value that represents SMSC	5Dh	Page 35
FFh	R	Revision	Stores a fixed value that represents the revision number	01h	Page 35

6.1 Data Read Interlock

When any temperature channel high byte register is read, the corresponding low byte is copied into an internal 'shadow' register. The user is free to read the low byte at any time and be guaranteed that it will correspond to the previously read high byte. Regardless if the low byte is read or not, reading from the same high byte register again will automatically refresh this stored low byte data.

6.2 Temperature Data Registers

Table 6.2 Temperature Data Registers

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
00h	R	Internal Diode High Byte	128	64	32	16	8	4	2	1	00h
29h	R	Internal Diode Low Byte	0.5	0.25	0.125	-	-	-	-	-	00h
01h	R	External Diode High Byte	128	64	32	16	8	4	2	1	00h
10h	R	External Diode Low Byte	0.5	0.25	0.125	-	-	-	-	-	00h

As shown in Table 6.2, all temperatures are stored as an 11-bit value with the high byte representing the integer value and the low byte representing the fractional value left justified to occupy the MSBits.

6.3 Status Register

Table 6.3 Status Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
02h	R	Status	BUSY	-	-	HIGH	LOW	FAULT	THERM	HWSD	00h

The Status Register reports general error conditions. To identify specific channels, refer to Section 6.9, Section 6.14, Section 6.15, and Section 6.16. The individual Status Register bits are cleared when the appropriate High Limit, Low Limit, or THERM Limit register has been read or cleared.

Bit 7 - BUSY - This bit indicates that the ADC is currently converting. This bit does not cause either the ALERT or THERM pin to be asserted.

Bit 4 - HIGH - This bit is set when any of the temperature channels exceeds its programmed high limit. See the High Limit Status Register for specific channel information (Section 6.14). When set, this bit will assert the ALERT pin.

Bit 3 - LOW - This bit is set when any of the temperature channels drops below its programmed low limit. See the Low Limit Status Register for specific channel information (Section 6.15). When set, this bit will assert the ALERT pin.

Bit 2 - FAULT - This bit is asserted when a diode fault is detected on any of the external diode channels. See the External Diode Fault Register for specific channel information (Section 6.9). When set, this bit will assert the ALERT pin.

Bit 1 - THERM - This bit is set when the any of the temperature channels exceeds its programmed THERM limit. See the THERM Limit Status Register for specific channel information (Section 6.16).

Bit 0 - HWSD - This bit is set when the External Diode Temperature exceeds the Hardware Thermal Shutdown Limit set by the pull-up resistors on the ALERT and SYS_SHDN pins. When set, this bit will assert the SYS_SHDN pin.

6.4 Configuration Register

Table 6.4 Configuration Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
03h	R/W	Configuration	MASK_ALL	-	ALERT/COMP	-	-	RANGE	DAVG_DIS	-	00h
09h											

The Configuration Register controls the basic operation of the device. This register is fully accessible at either address.

Bit 7 - MASK_ALL - Masks the ALERT pin from asserting.

- ‘0’ (default) - The ALERT pin is not masked. If any of the appropriate status bits are set the ALERT pin will be asserted.
- ‘1’ - The ALERT pin is masked. It will not be asserted for any interrupt condition unless it is configured as a THERM pin. The Status Registers will be updated normally.

Bit 5 - ALERT/COMP - Controls the operation of the ALERT pin.

- ‘0’ (default) - The ALERT pin acts as described in Section 5.3.
- ‘1’ - The ALERT pin acts in comparator mode as described in Section 5.3.2. In this mode the MASK_ALL bit is ignored.

Bit 2 - RANGE - Configures the measurement range and data format of the temperature channels.

- ‘0’ (default) - The temperature measurement range is 0°C to +127.875°C and the data format is binary.
- ‘1’ -The temperature measurement range is -64°C to +191.875°C and the data format is offset binary (see Table 5.3).

Bit 1 - DAVG_DIS - Disables the dynamic averaging feature on all temperature channels.

- ‘0’ (default) - The dynamic averaging feature is enabled. All temperature channels will be converted with an averaging factor that is based on the conversion rate as shown in Table 5.1.
- ‘1’ - The dynamic averaging feature is disabled. All temperature channels will be converted with a maximum averaging factor of 1x (equivalent to 11-bit conversion). For higher conversion rates, this averaging factor will be reduced as shown in Table 5.1.

6.5 Conversion Rate Register

Table 6.5 Conversion Rate Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
04h	R/W	Conversion Rate	-	-	-	-	CONV[3:0]				06h (4/sec)
0Ah											

The Conversion Rate Register controls how often the temperature measurement channels are updated and compared against the limits. This register is fully accessible at either address.

Bits 3-0 - CONV[3:0] - Determines the conversion rate as shown in Table 6.6.

Table 6.6 Conversion Rate

CONV[3:0]					CONVERSIONS / SECOND
HEX	3	2	1	0	
0h	0	0	0	0	1
1h	0	0	0	1	1
2h	0	0	1	0	1
3h	0	0	1	1	1
4h	0	1	0	0	1
5h	0	1	0	1	2
6h	0	1	1	0	4 (default)
7h	0	1	1	1	8
8h	1	0	0	0	16
9h	1	0	0	1	32
Ah	1	0	1	0	64
Bh - Fh	All others				1

6.6 Limit Registers

Table 6.7 Temperature Limit Registers

ADDR.	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
05h	R/W	Internal Diode High Limit	128	64	32	16	8	4	2	1	55h (85°C)
0Bh											
06h	R/W	Internal Diode Low Limit	128	64	32	16	8	4	2	1	00h (0°C)
0Ch											

Table 6.7 Temperature Limit Registers (continued)

ADDR.	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
07h 0Dh	R/W	External Diode High Limit High Byte	128	64	32	16	8	4	2	1	55h (85°C)
13h	R/W	External Diode High Limit Low Byte	0.5	0.25	0.125	-	-	-	-	-	00h
08h 0Eh	R/W	External Diode Low Limit High Byte	128	64	32	16	8	4	2	1	00h (0°C)
14h	R/W	External Diode Low Limit Low Byte	0.5	0.25	0.125	-	-	-	-	-	00h

The device contains both high and low limits for all temperature channels. If the measured temperature exceeds the high limit, then the corresponding status bit is set and the ALERT pin is asserted. Likewise, if the measured temperature is less than or equal to the low limit, the corresponding status bit is set and the ALERT pin is asserted.

The data format for the limits must match the selected data format for the temperature so that if the extended temperature range is used, the limits must be programmed in the extended data format.

The limit registers with multiple addresses are fully accessible at either address.

6.7 Scratchpad Registers

Table 6.8 Scratchpad Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
11h	R/W	Scratchpad	7	6	5	4	3	2	1	0	00h
12h	R/W	Scratchpad	7	6	5	4	3	2	1	0	00h

The Scratchpad Registers are Read Write registers that are used for place holders to be software compatible with legacy programs. Reading from the registers will return what is written to them.

6.8 Therm Limit Registers

Table 6.9 Therm Limit Registers

ADDR.	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
19h	R/W	External Diode THERM Limit	128	64	32	16	8	4	2	1	55h (85°C)
20h	R/W	Internal Diode THERM Limit	128	64	32	16	8	4	2	1	55h (85°C)

Table 6.9 Therm Limit Registers (continued)

ADDR.	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
21h	R/W	THERM Hysteresis	128	64	32	16	8	4	2	1	0Ah (10°C)

6.9 External Diode Fault Register

Table 6.10 External Diode Fault Register

ADDR.	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
1Bh	R-C	External Diode Fault	-	-	-	-	-	-	FLT	-	00h

The External Diode Fault Register indicates which of the external diodes caused the FAULT bit in the Status Register to be set. This register is cleared when it is read.

Bit 1 - FLT - This bit is set if the External Diode channel reported a diode fault.

6.10 Software Thermal Shutdown Configuration Register

Table 6.11 Software Thermal Shutdown Configuration Register

ADDR.	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
1Dh	R/W	Software Thermal Shutdown Configuration	-	-	-	-	-	-	EXTSYS	INTSYS	00h

The Software Thermal Shutdown Configuration Register controls whether any of the software channels will assert the SYS_SHDN pin. If a channel is enabled, the temperature is compared against the corresponding THERM Limit. If the measured temperature exceeds the THERM Limit, then the SYS_SHDN pin is asserted. This functionality is in addition to the Hardware Shutdown circuitry.

Bit 1 - EXTSYS - configures the External Diode channel to assert the SYS_SHDN pin based on the THERM Limit.

- ‘0’ (default) - the External Diode channel is not linked to the SYS_SHDN pin. If the temperature exceeds the THERM Limit, the ETHERM status bit is set but the SYS_SHDN pin is not asserted.
- ‘1’ - the External Diode channel is linked to the SYS_SHDN pin. If the temperature exceeds the THERM Limit, the ETHERM status bit is set and the SYS_SHDN pin is asserted. It will remain asserted until the temperature drops below the THERM Limit minus the THERM Hysteresis.

Bit 0 - INTSYS - configures the Internal Diode channel to assert the SYS_SHDN pin based on it’s respective THERM Limit.

- ‘0’ (default) - the Internal Diode channel is not linked to the SYS_SHDN pin. If the temperature exceeds it’s THERM Limit, the ITHERM status bit is set but the SYS_SHDN pin is not asserted.
- ‘1’ - the Internal Diode channel is linked to the SYS_SHDN pin. If the temperature exceeds it’s THERM Limit, the ITHERM status bit is set and the SYS_SHDN pin is asserted. It will remain asserted until the temperature drops below it’s THERM Limit minus the THERM Hysteresis.

6.11 Hardware Thermal Shutdown Limit Register

Table 6.12 Hardware Thermal Shutdown Limit Register

ADDR.	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
1Eh	R	Hardware Thermal Shutdown Limit	128	64	32	16	8	4	2	1	N/A

This read only register returns the Hardware Thermal Shutdown Limit selected by the value of the pull-up resistors on the ALERT and SYS_SHDN pins. The data represents the hardware set temperature in °C using the active temperature setting set by the RANGE bit in the Configuration Register. See Table 5.3 for the data format.

When the External Diode Temperature exceeds this limit, the SYS_SHDN pin is asserted and will remain asserted until the External Diode Temperature drops below this limit minus 10°C.

6.12 Channel Mask Register

Table 6.13 Channel Mask Register

ADDR.	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
1Fh	R/W	Channel Mask	-	-	-	-	-	-	E MASK	INT MASK	00h

The Channel Mask Register controls individual channel masking. When a channel is masked, the ALERT pin will not be asserted when the masked channel reads a diode fault or out of limit error. The channel mask does not mask the SYS_SHDN pin.

Bit 1 - EMASK - Masks the ALERT pin from asserting when the External Diode channel is out of limit or reports a diode fault.

- ‘0’ (default) - The External Diode channel will cause the ALERT pin to be asserted if it is out of limit or reports a diode fault.
- ‘1’ - The External Diode channel will not cause the ALERT pin to be asserted if it is out of limit or reports a diode fault.

Bit 0 - INTMASK - Masks the ALERT pin from asserting when the Internal Diode temperature is out of limit.

- ‘0’ (default) - The Internal Diode channel will cause the ALERT pin to be asserted if it is out of limit.
- ‘1’ - The Internal Diode channel will not cause the ALERT pin to be asserted if it is out of limit.

6.13 Consecutive ALERT Register

Table 6.14 Consecutive ALERT Register

ADDR.	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
22h	R/W	Consecutive ALERT	TIME OUT	CTHRM[2:0]			CALRT[2:0]			-	70h

The Consecutive ALERT Register determines how many times an out-of-limit error or diode fault must be detected in consecutive measurements before the ALERT or SYS_SHDN pin is asserted. Additionally, the Consecutive ALERT Register controls the SMBus Timeout functionality.

An out-of-limit condition (i.e. HIGH, LOW, or FAULT) occurring on the same temperature channel in consecutive measurements will increment the consecutive alert counter. The counters will also be reset if no out-of-limit condition or diode fault condition occurs in a consecutive reading.

When the ALERT pin is configured as an interrupt, when the consecutive alert counter reaches its programmed value, the following will occur: the STATUS bit(s) for that channel and the last error condition(s) (i.e. EHIGH) will be set to '1', the ALERT pin will be asserted, the consecutive alert counter will be cleared, and measurements will continue.

When the ALERT pin is configured as a comparator, the consecutive alert counter will ignore diode fault and low limit errors and only increment if the measured temperature exceeds the High Limit. Additionally, once the consecutive alert counter reaches the programmed limit, the ALERT pin will be asserted, but the counter will not be reset. It will remain set until the temperature drops below the High Limit minus the THERM Hysteresis value.

For example, if the CALRT[2:0] bits are set for 4 consecutive alerts, the high limits are set at 70°C, and none of the channels are masked, then the ALERT pin will be asserted after the following four measurements:

1. Internal Diode reads 71°C and the external diode reads 69°C. Consecutive alert counter for INT is incremented to 1.
2. Both the Internal Diode and the External Diode read 71°C. Consecutive alert counter for INT is incremented to 2and for EXT is set to 1.
3. The External Diode reads 71°C and the Internal Diode reads 69°C. Consecutive alert counter for INT is cleared and EXT is incremented to 2.
4. The Internal Diode reads 71°C and the external diode reads 71°C. Consecutive alert counter for INT is set to 1 and EXT is incremented to 3.
5. The Internal Diode reads 71°C and the external diode reads 71°C. Consecutive alert counter for INT is incremented to 2 and EXT is incremented to 4. The appropriate status bits are set for EXT and the ALERT pin is asserted. EXT counter is reset to 0 and all other counters hold the last value until the next temperature measurement.

Bit 7 - TIMEOUT - Determines whether the SMBus Timeout function is enabled.

- '0' (default) - The SMBus Timeout feature is disabled. The SMCLK line can be held low indefinitely without the device resetting its SMBus protocol.
- '1' - The SMBus Timeout feature is enabled. If the SMCLK line is held low for more than 30ms, then the device will reset the SMBus protocol.

Bits 6-4 CTHRM[2:0] - Determines the number of consecutive measurements that must exceed the corresponding THERM Limit and Hardware Thermal Shutdown Limit before the SYS_SHDN pin is asserted. All temperature channels use this value to set the respective counters. The consecutive THERM counter is incremented whenever any of the measurements exceed the corresponding THERM Limit or if the External Diode measurement exceeds the Hardware Thermal Shutdown Limit.

If the temperature drops below the THERM limit or Hardware Thermal Shutdown Limit, then the counter is reset. If the programmed number of consecutive measurements exceed the THERM Limit or Hardware Thermal Shutdown Limit, and the appropriate channel is linked to the SYS_SHDN pin, then the SYS_SHDN pin will be asserted low.

Once the SYS_SHDN pin is asserted, the consecutive THERM counter will not reset until the corresponding temperature drops below the appropriate limit minus the corresponding hysteresis.

The bits are decoded as shown in Table 6.15. The default setting is 4 consecutive out of limit conversions.

Bits 3-1 - CALRT[2:0] - Determine the number of consecutive measurements that must have an out of limit condition or diode fault before the ALERT pin is asserted. All temperature channels use this value to set the respective counters. The bits are decoded as shown in Table 6.15. The default setting is 1 consecutive out of limit conversion.

Table 6.15 Consecutive Alert / THERM Settings

2	1	0	NUMBER OF CONSECUTIVE OUT OF LIMIT MEASUREMENTS
0	0	0	1 (default for CALRT[2:0])
0	0	1	2
0	1	1	3
1	1	1	4 (default for CTHRM[2:0])

APPLICATION NOTE: When measuring a 65nm Intel CPUs, the Ideality Setting should be the default 12h. When measuring 45nm Intel CPUs, the Ideality Setting should be 15h.

6.14 High Limit Status Register

Table 6.16 High Limit Status Register

ADDR.	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
35h	R-C	High Limit Status	-	-	-	-	-	-	EHIGH	IHIGH	00h

The High Limit Status Register contains the status bits that are set when a temperature channel high limit is exceeded. If any of these bits are set, then the HIGH status bit in the Status Register is set. Reading from the High Limit Status Register will clear all bits if. Reading from the register will also clear the HIGH status bit in the Status Register.

The $\overline{\text{ALERT}}$ pin will be set if the programmed number of consecutive alert counts have been met and any of these status bits are set.

The status bits will remain set until read unless the $\overline{\text{ALERT}}$ pin is configured as a comparator output (see Section 5.3.2).

Bit 1 - EHIGH - This bit is set when the External Diode channel exceeds its programmed high limit.

Bit 0 - IHIGH - This bit is set when the Internal Diode channel exceeds its programmed high limit.

6.15 Low Limit Status Register

Table 6.17 Low Limit Status Register

ADDR.	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
36h	R-C	Low Limit Status	-	-	-	-	-	-	ELOW	ILOW	00h

The Low Limit Status Register contains the status bits that are set when a temperature channel drops below the low limit. If any of these bits are set, then the LOW status bit in the Status Register is set. Reading from the Low Limit Status Register will clear all bits. Reading from the register will also clear the LOW status bit in the Status Register.

The $\overline{\text{ALERT}}$ pin will be set if the programmed number of consecutive alert counts have been met and any of these status bits are set.

The status bits will remain set until read unless the $\overline{\text{ALERT}}$ pin is configured as a comparator output (see Section 5.3.2).

Bit 1 - ELOW - This bit is set when the External Diode channel drops below its programmed low limit.

Bit 0 - ILOW - This bit is set when the Internal Diode channel drops below its programmed low limit.

6.16 THERM Limit Status Register

Table 6.18 THERM Limit Status Register

ADDR.	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
37h	R-C	THERM Limit Status	-	-	-	-	-	-	E THERM	ITHERM	00h

The THERM Limit Status Register contains the status bits that are set when a temperature channel THERM Limit is exceeded. If any of these bits are set, then the THERM status bit in the Status Register is set. Reading from the THERM Limit Status Register will not clear the status bits. Once the temperature drops below the THERM Limit minus the THERM Hysteresis, the corresponding status bits will be automatically cleared. The THERM bit in the Status Register will be cleared when all individual channel THERM bits are cleared.

Bit 1 - ETHERM - This bit is set when the External Diode channel exceeds it's programmed THERM limit.

Bit 0- ITHERM - This bit is set when the Internal Diode channel exceeds it's programmed THERM limit.

6.17 Filter Control Register

Table 6.19 Filter Configuration Register

ADDR.	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
40h	R/W	Filter Control	-	-	-	-	-	-	FILTER[1:0]		00h

The Filter Configuration Register controls the digital filter on the External Diode channel.

Bits 1-0 - FILTER[1:0] - Control the level of digital filtering that is applied to the External Diode temperature measurements as shown in Table 6.20. See Figure 5.4and Figure 5.5 for examples on the filter behavior.

Table 6.20 Filter Settings

FILTER[1:0]		AVERAGING
1	0	
0	0	Disabled (default)
0	1	Level 1
1	0	Level 1
1	1	Level 2

6.18 Product ID Register

Table 6.21 Product ID Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
FDh	R	Product ID	0	0	1	0	0	0	1	0	22h EMC1422

The Product ID Register holds a unique value that identifies the device.

6.19 SMSC ID Register (FEh)

Table 6.22 Manufacturer ID Register

ADDR.	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
FEh	R	SMSC ID	0	1	0	1	1	1	0	1	5Dh

The Manufacturer ID register contains an 8 bit word that identifies the SMSC as the manufacturer of the EMC1422.

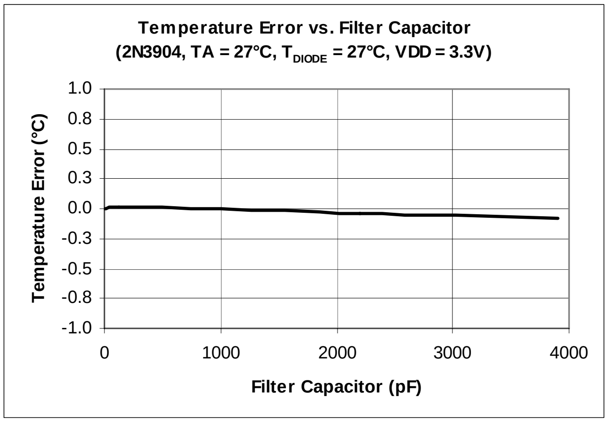
6.20 Revision Register (FFh)

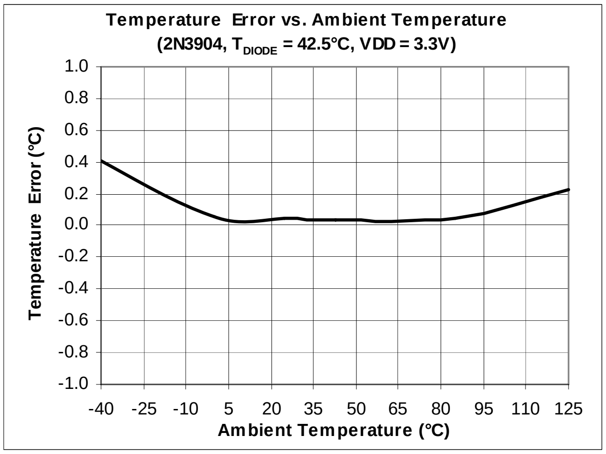
Table 6.23 Revision Register

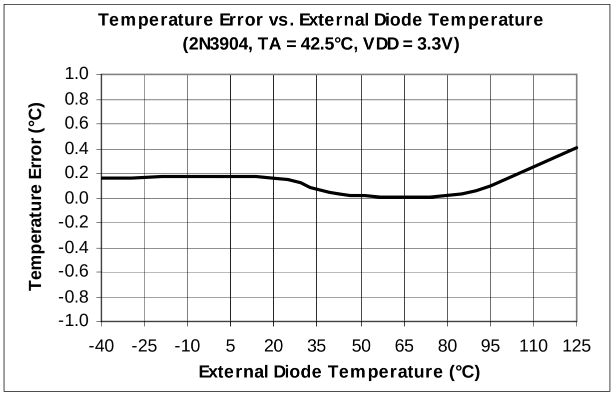
ADDR.	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
FFh	R	Revision	0	0	0	0	0	0	0	1	01h

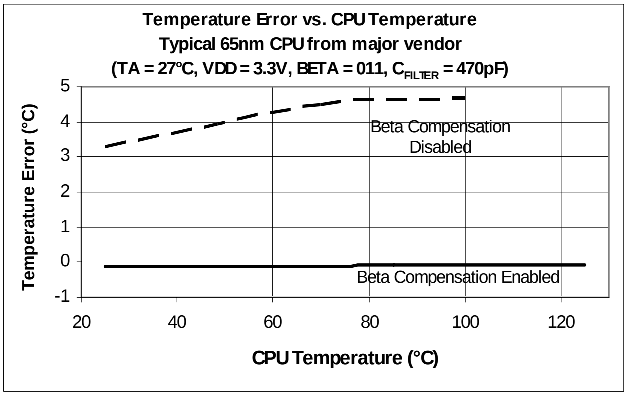
The Revision register contains an 8 bit word that identifies the die revision.

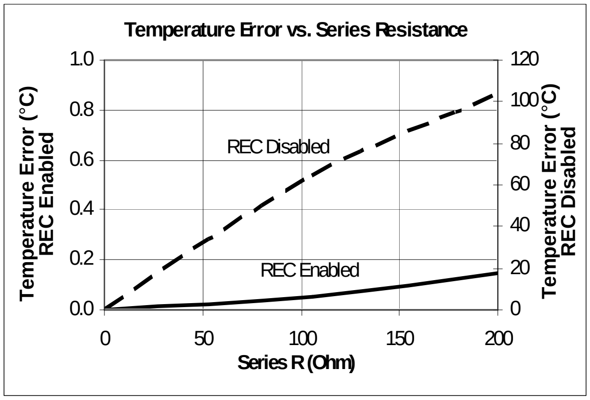
Chapter 7 Typical Operating Curves

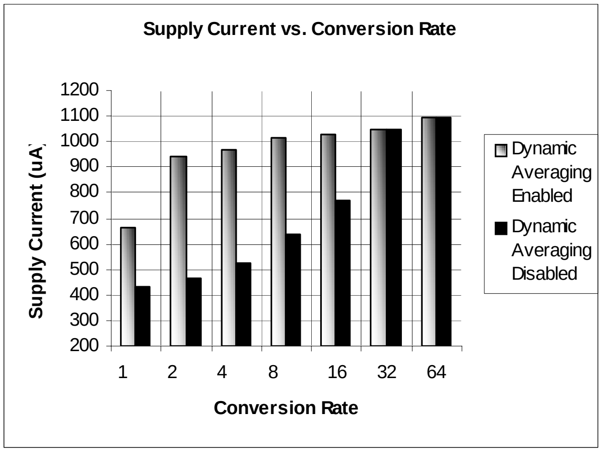






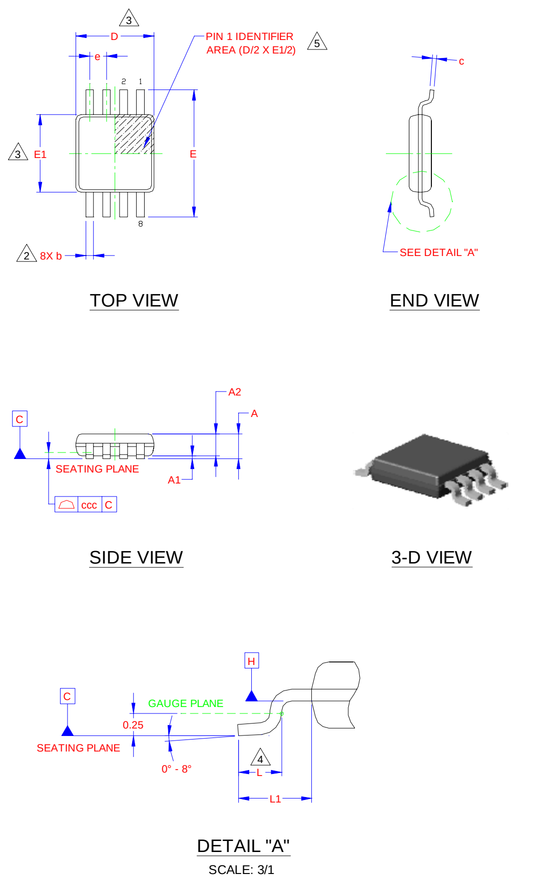



Temperature Error vs. Series Resistance
Temperature Error (°C)
REC Enabled
Temperature Error (°C)
REC Disabled
1.0
0.8
0.6
0.4
0.2
0.0
120
100
80
60
40
20
0
REC Disabled
REC Enabled
0
50
100
150
200
Series R (Ohm)


Supply Current vs. Conversion Rate
Supply Current (uA)
1200
1100
1000
900
800
700
600
500
400
300
200
1
2
4
8
16
32
64
Conversion Rate
Dynamic Averaging Enabled
Dynamic Averaging Disabled

Chapter 8 Package Information

REVISION	DESCRIPTION	DATE	RELEASED BY
-	SEE SPEC FRONT PAGE FOR REVISION HISTORY	-	-



COMMON DIMENSIONS					
SYMBOL	MIN	NOM	MAX	NOTE	REMARK
A	0.80	–	1.10	–	OVERALL PKG HEIGHT
A1	0.05	–	0.15	–	STANDOFF
A2	0.75	0.85	0.95	–	BODY THICKNESS
D	2.80	3.00	3.20	3	"X" BODY SIZE
E	4.65	4.90	5.15	–	LEAD SPAN
E1	2.80	3.00	3.20	3	"Y" BODY SIZE
L	0.40	–	0.80	4	LEAD FOOT LENGTH
L1	0.95 REF			–	LEAD LENGTH
b	0.22	–	0.38	2	LEAD WIDTH
c	0.08	–	0.23	–	LEAD FOOT THICKNESS
e	0.65 BSC			–	LEAD PITCH
ccc	–	–	0.10	–	COPLANARITY

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETER.
2. TOLERANCE ON THE TRUE POSITION OF THE LEADS IS ± 0.065mm MAXIMUM.
3. PACKAGE BODY DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD PROTRUSIONS OR FLASH. MAXIMUM MOLD PROTRUSIONS OR FLASH IS 0.15 mm (0.006 INCHES) PER END AND SIDE. DIMENSIONS "D" AND "E1" ARE DETERMINED AT DATUM PLANE "H".
4. DIMENSION FOR FOOT LENGTH "L" IS MEASURED AT THE GAUGE PLANE 0.25mm ABOVE THE SEATING PLANE.
5. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN MILLIMETERS AND TOLERANCES ARE:
DECIMAL X.X ±0.1, X.XX ±0.05, X.XXX ±0.025; ANGULAR ±1°
DIM AND TOL PER ASME Y14.5M - 1994
MATERIAL: -
FINISH: -
PRINT WITH "SCALE TO FIT" DO NOT SCALE DRAWING

THIRD ANGLE PROJECTION

	NAME	DATE
DRAWN	S.K.ILIEV	7/05/04
CHECKED	S.K.ILIEV	7/05/04
APPROVED	S.K.ILIEV	7/07/04

80 ARKAY DRIVE
HAUPPAUGE, NY 11788
USA

SMSC™ SUCCESS BY DESIGN

TITLE: PACKAGE OUTLINE
8 PIN TSSOP, 3x3 MM BODY, 0.65 MM PITCH
DWG NUMBER: MO-8-TSSOP-3x3 REV: D
SCALE: 1:1 STD COMPLIANCE: JEDEC: MO-187 / D SHEET: 1 OF 1

Figure 8.1 8 Pin MSOP / TSSOP Package

OCEAN CHIPS
Океан Электроники
Поставка электронных компонентов

Компания «Океан Электроники» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

Наши преимущества:

- Поставка оригинальных импортных электронных компонентов напрямую с производств Америки, Европы и Азии, а так же с крупнейших складов мира;
- Широкая линейка поставок активных и пассивных импортных электронных компонентов (более 30 млн. наименований);
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Помощь Конструкторского Отдела и консультации квалифицированных инженеров;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Поставка электронных компонентов под контролем ВП;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- При необходимости вся продукция военного и аэрокосмического назначения проходит испытания и сертификацию в лаборатории (по согласованию с заказчиком);
- Поставка специализированных компонентов военного и аэрокосмического уровня качества (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Actel, Aeroflex, Peregrine, VPT, Syfer, Eurofarad, Texas Instruments, MS Kennedy, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits, General Dynamics и др.);

Компания «Океан Электроники» является официальным дистрибьютором и эксклюзивным представителем в России одного из крупнейших производителей разъемов военного и аэрокосмического назначения **«JONHON»**, а так же официальным дистрибьютором и эксклюзивным представителем в России производителя высокотехнологичных и надежных решений для передачи СВЧ сигналов **«FORSTAR»**.

AVIC JONHON

«JONHON» (основан в 1970 г.)

Разъемы специального, военного и аэрокосмического назначения:

(Применяются в военной, авиационной, аэрокосмической, морской, железнодорожной, горно- и нефтедобывающей отраслях промышленности)

«FORSTAR» (основан в 1998 г.)

ВЧ соединители, коаксиальные кабели, кабельные сборки и микроволновые компоненты:

(Применяются в телекоммуникациях гражданского и специального назначения, в средствах связи, РЛС, а так же военной, авиационной и аэрокосмической отраслях промышленности).

FORSTAR®

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Электронная почта: ocean@oceanchips.ru
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Адрес: 198099, г. Санкт-Петербург, ул. Калинина, д. 2, корп. 4, лит. А