

4V Drive Nch + Pch MOSFET

SH8M14

● Structure

Silicon N-channel MOSFET/

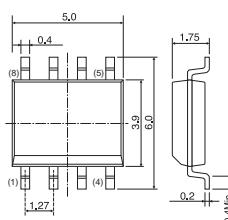
Silicon P-channel MOSFET

● Features

- 1) Low on-resistance.
- 2) High power package(SOP8).
- 3) Low voltage drive(4V drive).

● Dimensions (Unit : mm)

SOP8



● Application

Switching

● Packaging specifications

Type	Package	Taping
	Code	TB
SH8M14	Basic ordering unit (pieces)	2500
		○

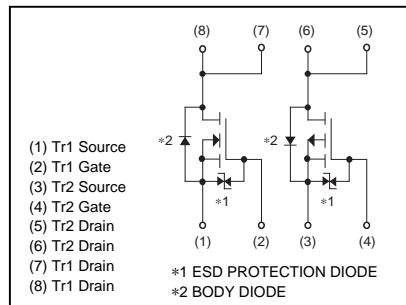
● Absolute maximum ratings (Ta = 25°C)

Parameter	Symbol	Limits		Unit
		Tr1 : N-ch	Tr2 : P-ch	
Drain-source voltage	V _{DSS}	30	-30	V
Gate-source voltage	V _{GSS}	±20	±20	V
Drain current	Continuous I _D	±9	±7	A
	Pulsed I _{DP}	±36	±28	A
Source current (Body Diode)	Continuous I _s	1.6	-1.6	A
	Pulsed I _{sp}	36	-28	A
Power dissipation	P _D	2.0		W / TOTAL
		1.4		W / ELEMENT
Channel temperature	T _{ch}	150		°C
Range of storage temperature	T _{stg}	-55 to +150		°C

*1 Pw≤10μs, Duty cycle≤1%

*2 Mounted on a ceramic board.

● Inner circuit



● Electrical characteristics (Ta = 25°C)

<Tr1(Nch)>

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	I _{GSS}	-	-	±10	µA	V _{GS} =±20V, V _{DS} =0V
Drain-source breakdown voltage	V _{(BR)DSS}	30	-	-	V	I _D =1mA, V _{GS} =0V
Zero gate voltage drain current	I _{DSS}	-	-	1	µA	V _{DS} =30V, V _{GS} =0V
Gate threshold voltage	V _{GS(th)}	1.0	-	2.5	V	V _{DS} =10V, I _D =1mA
Static drain-source on-state resistance	R _{DS(on)} *		-	15	21	I _D =9A, V _{GS} =10V
			-	18	25	I _D =9A, V _{GS} =4.5V
				20	28	I _D =9A, V _{GS} =4V
Forward transfer admittance	Y _{fs} *	5.0	-	-	S	V _{DS} =10V, I _D =9A
Input capacitance	C _{iss}	-	630	-	pF	V _{DS} =10V
Output capacitance	C _{oss}	-	230	-	pF	V _{GS} =0V
Reverse transfer capacitance	C _{rss}	-	110	-	pF	f=1MHz
Turn-on delay time	t _{d(on)} *	-	10	-	ns	I _D =4.5A, V _{DD} =15V
Rise time	t _r *	-	33	-	ns	V _{GS} =10V
Turn-off delay time	t _{d(off)} *	-	42	-	ns	R _L =3.3Ω
Fall time	t _f *	-	10	-	ns	R _G =10Ω
Total gate charge	Q _g *	-	8.5	-	nC	I _D =9A, V _{DD} =15V
Gate-source charge	Q _{gs} *	-	2.3	-	nC	V _{GS} =5V
Gate-drain charge	Q _{gd} *	-	4.0	-	nC	

*Pulsed

● Body diode characteristics (Source-Drain) (Ta = 25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Forward Voltage	V _{SD} *	-	-	1.2	V	I _s =9A, V _{GS} =0V

*Pulsed

● Electrical characteristics (Ta = 25°C)

<Tr2(Pch)>

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	I _{GSS}	-	-	±10	µA	V _{GS} =±20V, V _{DS} =0V
Drain-source breakdown voltage	V _{(BR)DSS}	-30	-	-	V	I _D =-1mA, V _{GS} =0V
Zero gate voltage drain current	I _{DSS}		-	-1	µA	V _{DS} =-30V, V _{GS} =0V
Gate threshold voltage	V _{GS(th)}	-1.0	-	-2.5	V	V _{DS} =-10V, I _D =-1mA
		-	21.5	29.0		I _D =-7A, V _{GS} =-10V
Static drain-source on-state resistance	R _{DS(on)*}	-	29.0	39.0	mΩ	I _D =-3.5A, V _{GS} =-4.5V
		-	31.0	40.8		I _D =-3.5A, V _{GS} =-4.0V
Forward transfer admittance	Y _{fs} *	6.0	-	-	S	V _{DS} =-10V, I _D =-7A
Input capacitance	C _{iss}	-	1200	-	pF	V _{DS} =-10V
Output capacitance	C _{oss}	-	170	-	pF	V _{GS} =0V
Reverse transfer capacitance	C _{rss}	-	170	-	pF	f=1MHz
Turn-on delay time	t _{d(on)*}	-	12	-	ns	I _D =-3.5A, V _{DD} =-15V
Rise time	t _r *	-	40	-	ns	V _{GS} =-10V
Turn-off delay time	t _{d(off)*}	-	80	-	ns	R _L =4.27Ω
Fall time	t _f *	-	65	-	ns	R _G =10Ω
Total gate charge	Q _g *	-	18	-	nC	I _D =-7A, V _{DD} =-15V
Gate-source charge	Q _{gs} *	-	3.5	-	nC	V _{GS} =-5V
Gate-drain charge	Q _{gd} *	-	6.5	-	nC	

*Pulsed

● Body diode characteristics (Source-Drain) (Ta = 25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Forward Voltage	V _{SD} *	-	-	-1.2	V	I _s =-7A, V _{GS} =0V

*Pulsed

●Electrical characteristic curves ($T_a=25^\circ\text{C}$)

⟨Tr.1(Nch)⟩

Fig.1 Typical Output Characteristics (I)

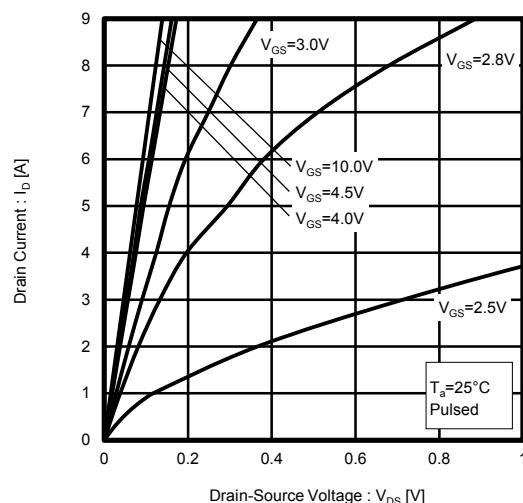


Fig.3 Static Drain-Source On-State Resistance vs. Drain Current

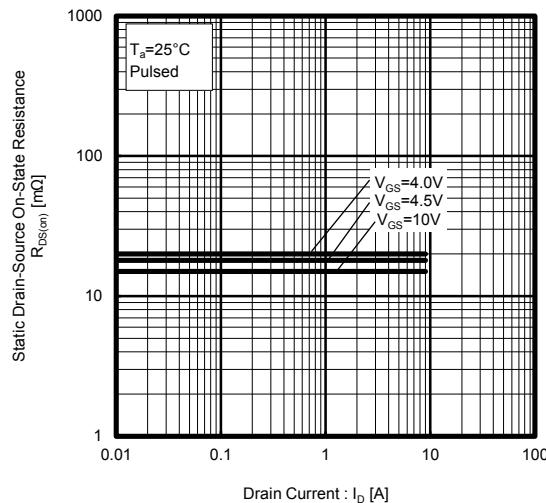


Fig.5 Static Drain-Source On-State Resistance vs. Drain Current

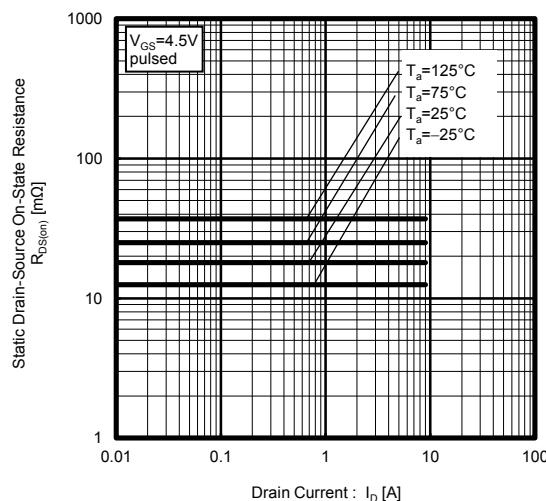


Fig.2 Typical Output Characteristics (II)

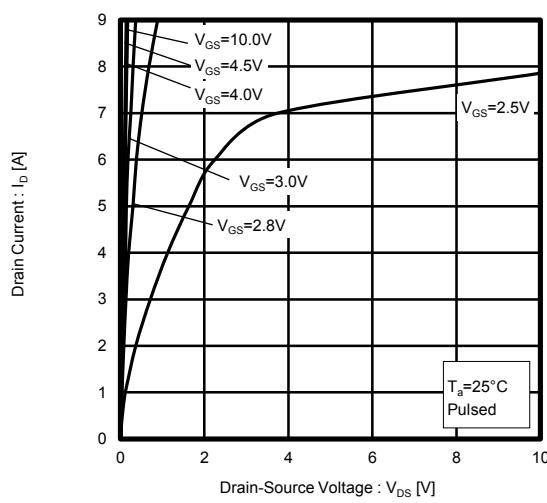


Fig.4 Static Drain-Source On-State Resistance vs. Drain Current

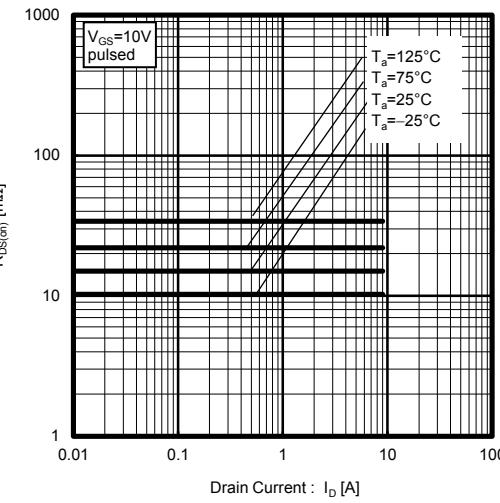
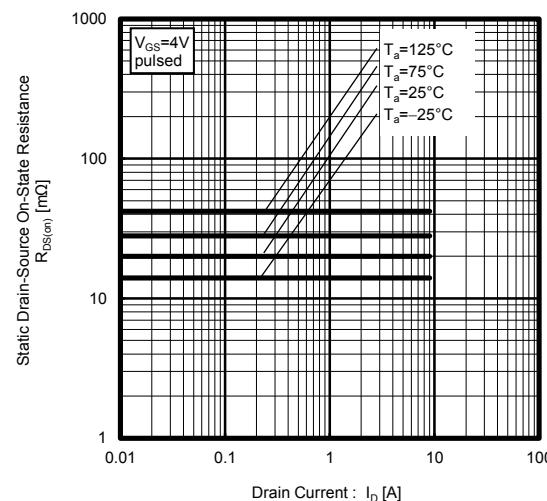


Fig.6 Static Drain-Source On-State Resistance vs. Drain Current



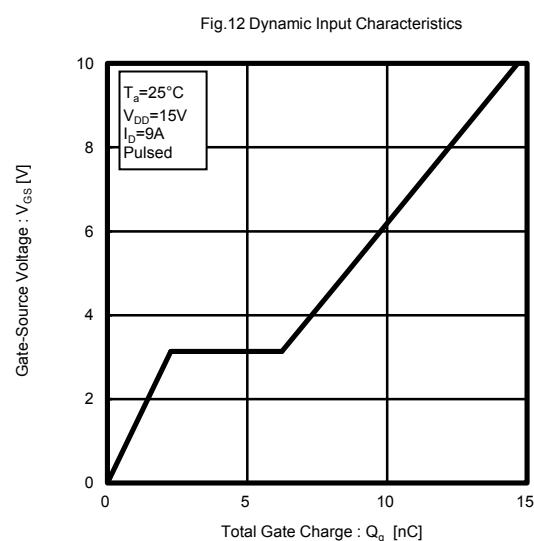
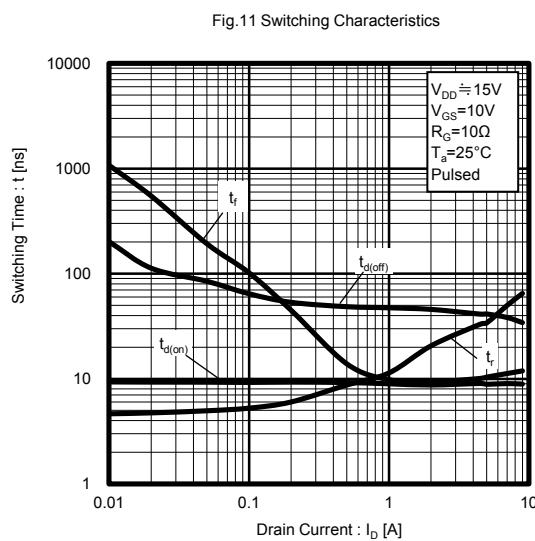
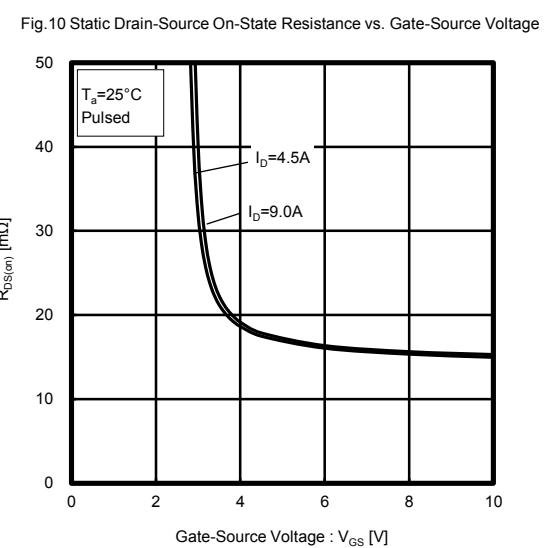
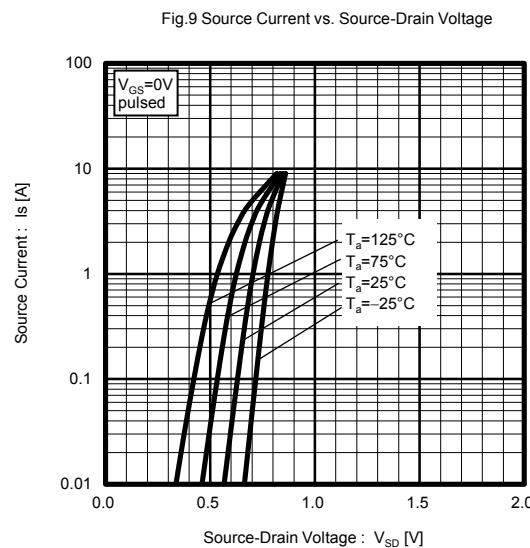
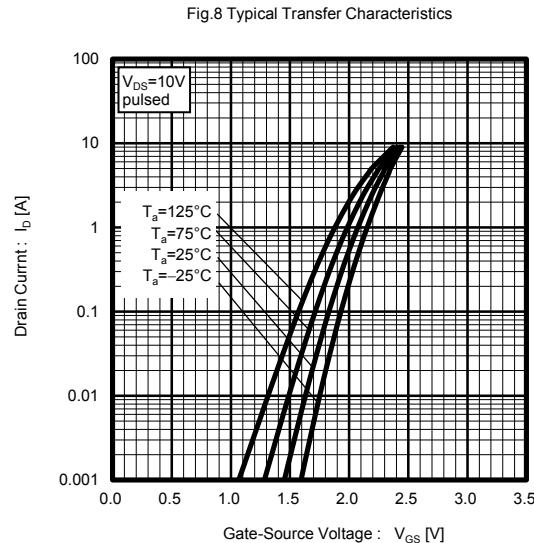
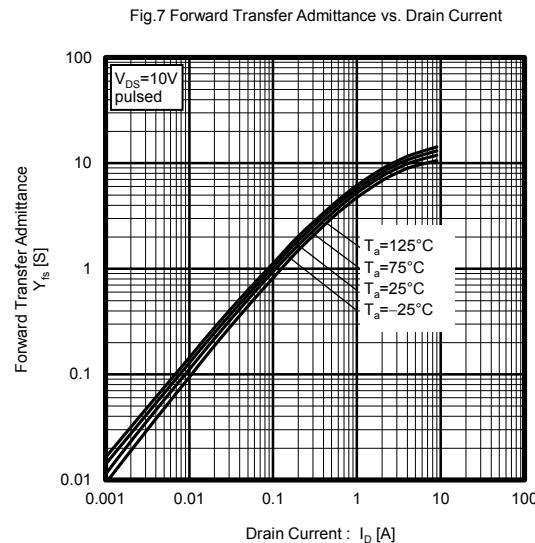


Fig.13 Typical Capacitance vs. Drain-Source Voltage

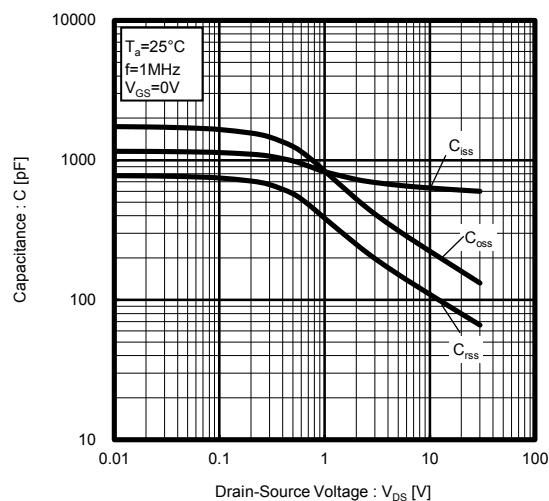


Fig.14 Maximum Safe Operating Area

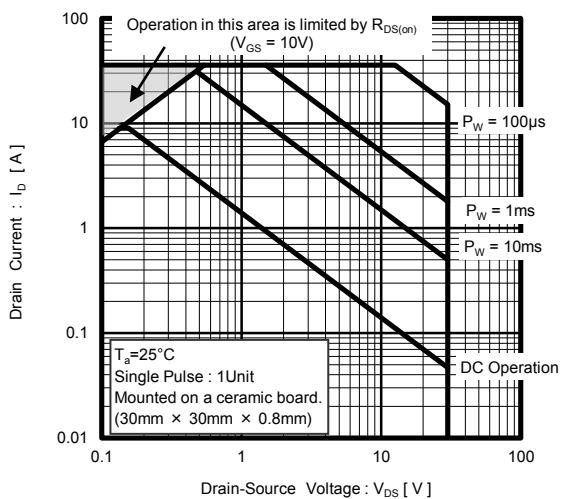
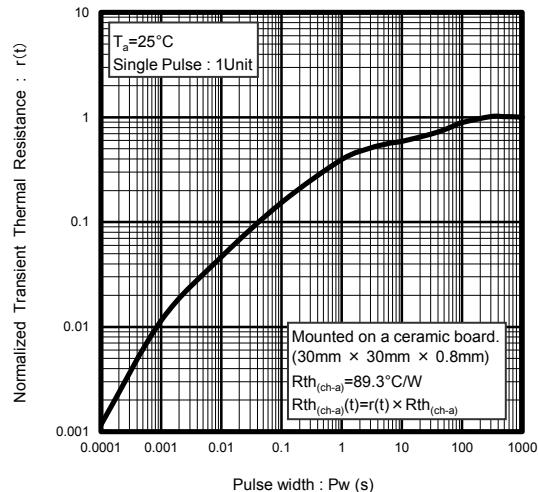


Fig.15 Normalized Transient Thermal Resistance v.s. Pulse Width



〈Tr.2(Pch)〉

Fig.1 Typical Output Characteristics(I)

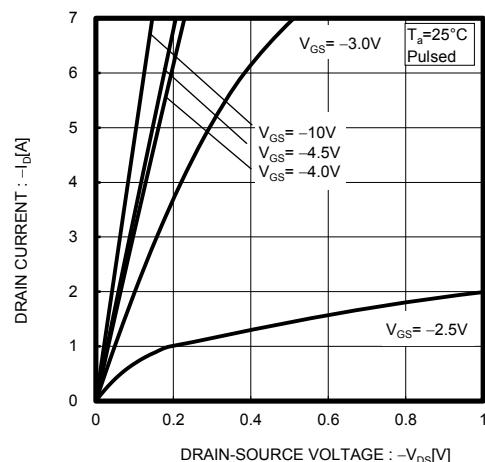


Fig.2 Typical Output Characteristics(II)

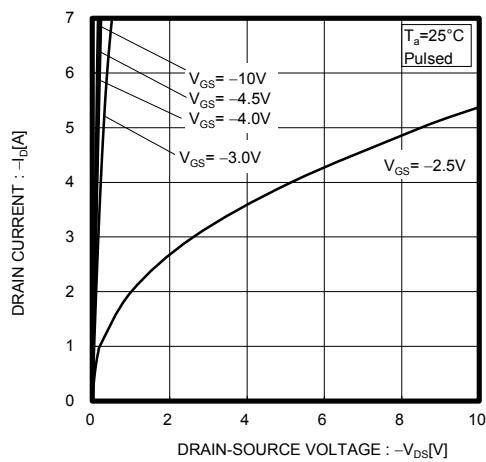


Fig.3 Typical Transfer Characteristics

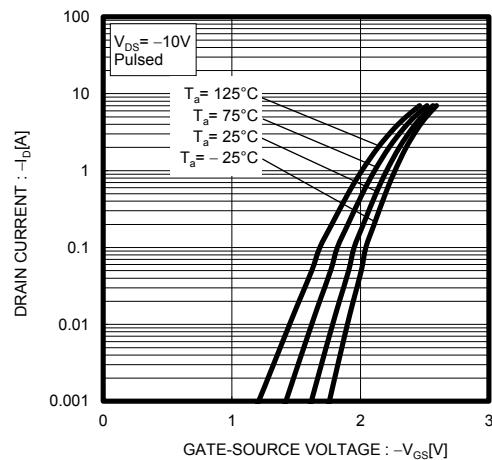


Fig.5 Static Drain-Source On-State Resistance vs. Drain Current(I)

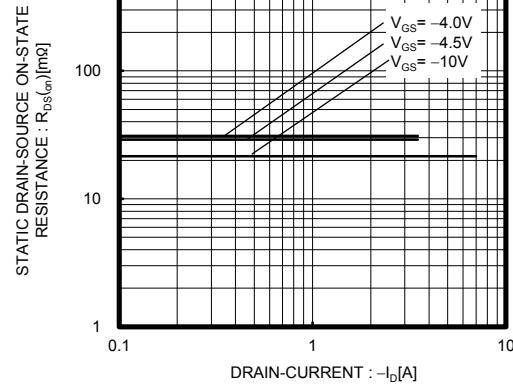


Fig.6 Static Drain-Source On-State Resistance vs. Drain Current(III)

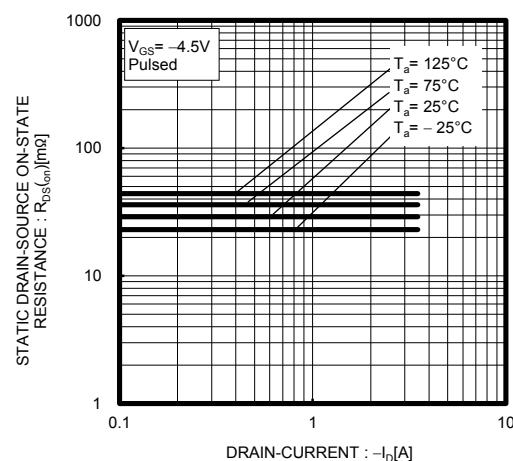
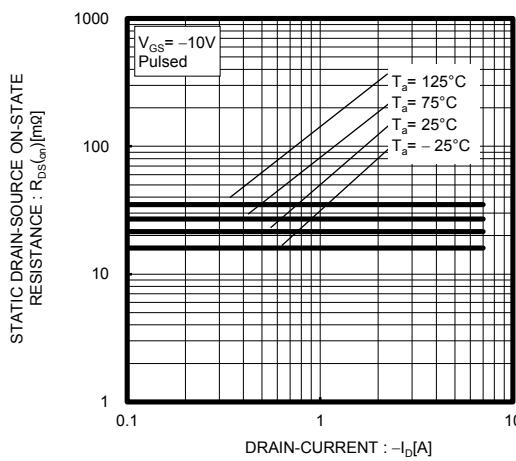


Fig.7 Static Drain-Source On-State
Resistance vs. Drain Current(IV)

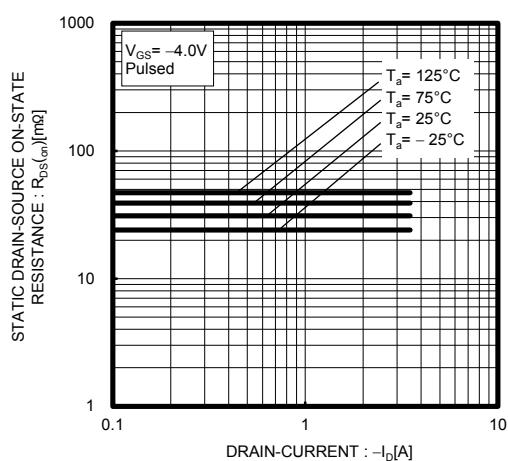


Fig.8 Forward Transfer Admittance
vs. Drain Current

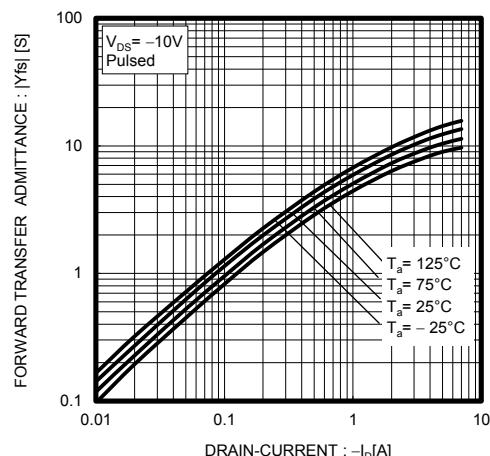


Fig.9 Reverse Drain Current
vs. Source-Drain Voltage

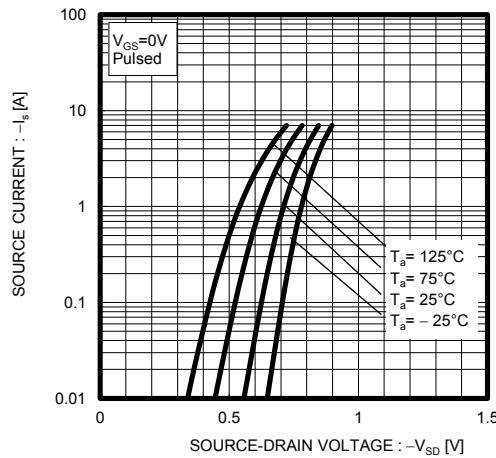


Fig.10 Static Drain-Source On-State
Resistance vs. Gate Source Voltage

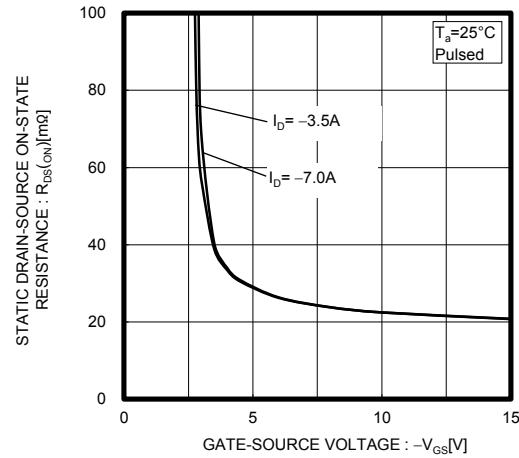


Fig.11 Switching Characteristics

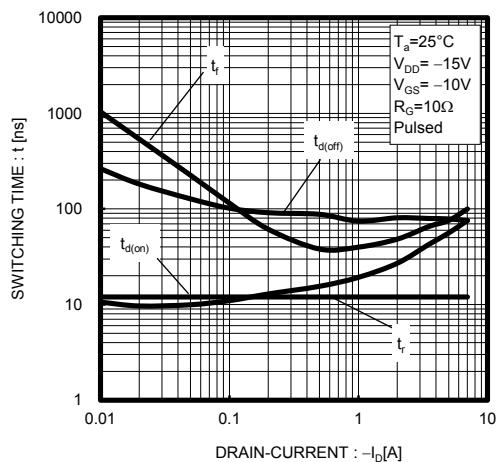


Fig.12 Dynamic Input Characteristics

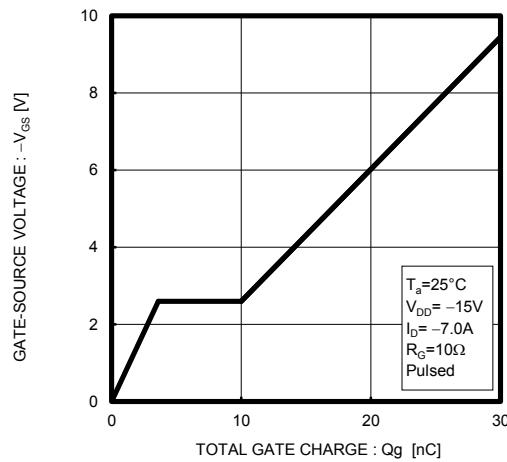


Fig.13 Typical Capacitance
vs. Drain-Source Voltage

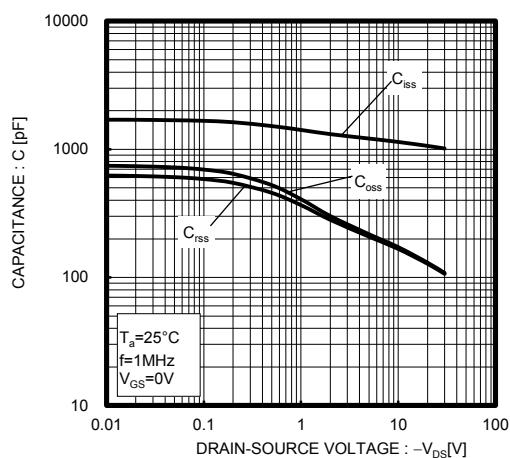


Fig.14 Maximum Safe Operating Area

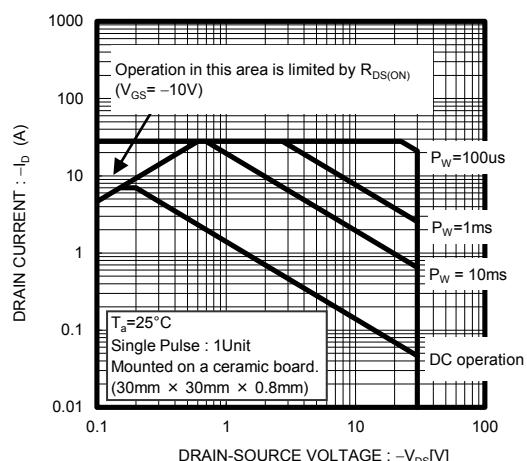
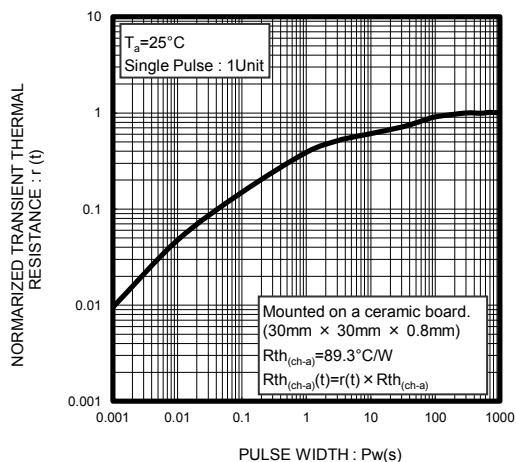


Fig.15 Normalized Transient Thermal Resistance vs. Pulse Width



● Measurement circuits

<Tr1(Nch)>

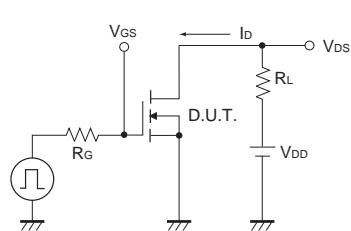


Fig.1-1 Switching Time Measurement Circuit

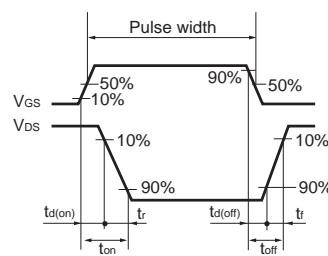


Fig.1-2 Switching Waveforms

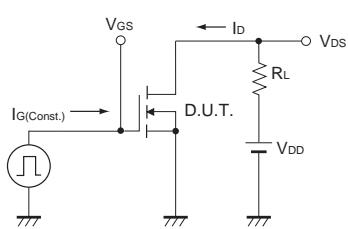


Fig.2-1 Gate Charge Measurement Circuit

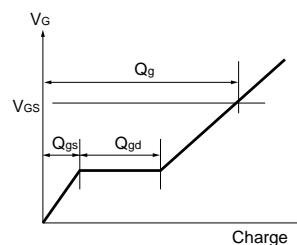


Fig.2-2 Gate Charge Waveform

<Tr2(Pch)>

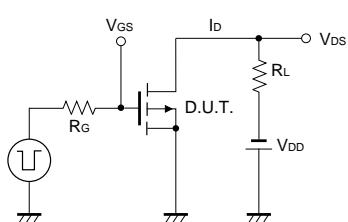


Fig.3-1 Switching Time Measurement Circuit

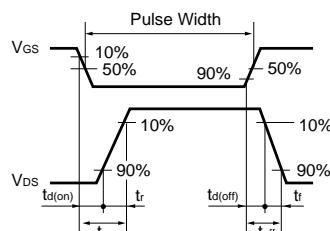


Fig.3-2 Switching Waveforms

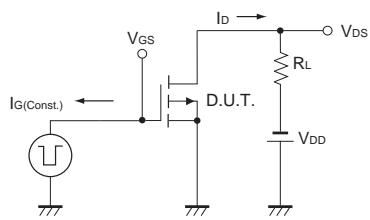


Fig.4-1 Gate Charge Measurement Circuit

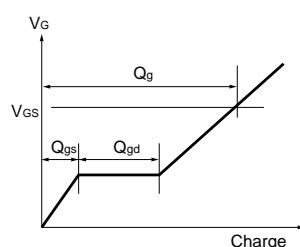


Fig.4-2 Gate Charge Waveform

● Notice

This product might cause chip aging and breakdown under the large electrified environment. Please consider to design ESD protection circuit.

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