

CBTD3306

Dual bus switch with level shifting

Rev. 9 — 15 November 2018

Product data sheet

1. General description

The CBTD3306 dual FET bus switch features independent line switches. Each switch is disabled when the associated output enable ($\overline{\text{OE}}$) input is HIGH.

The CBTD3306 is characterized for operation from $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$.

2. Features and benefits

- Designed to be used in 5 V to 3.3 V level shifting applications with internal diode
- $5\text{ }\Omega$ switch connection between two ports
- TTL-compatible input levels
- Multiple package options
- Latch-up protection exceeds 100 mA per JESD78B
- ESD protection:
 - HBM JESD22-A114F exceeds 2000 V
 - CDM JESD22-C101E exceeds 1000 V

3. Ordering information

Table 1. Ordering information

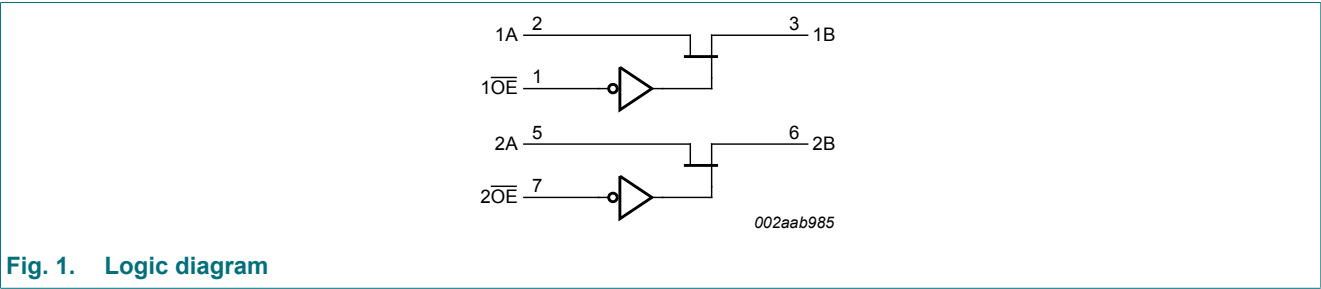
Type number	Package		
	Name	Description	Version
CBTD3306PW	TSSOP8	plastic thin shrink small outline package; 8 leads; body width 4.4 mm	SOT530-1
CBTD3306GT	XSON8	plastic extremely thin small outline package; no leads; 8 terminals; body 1 x 1.95 x 0.5 mm	SOT833-1
CBTD3306GM	XQFN8	plastic, extremely thin quad flat package; no leads; 8 terminals; body 1.6 x 1.6 x 0.5 mm	SOT902-2

4. Marking

Table 2. Marking codes

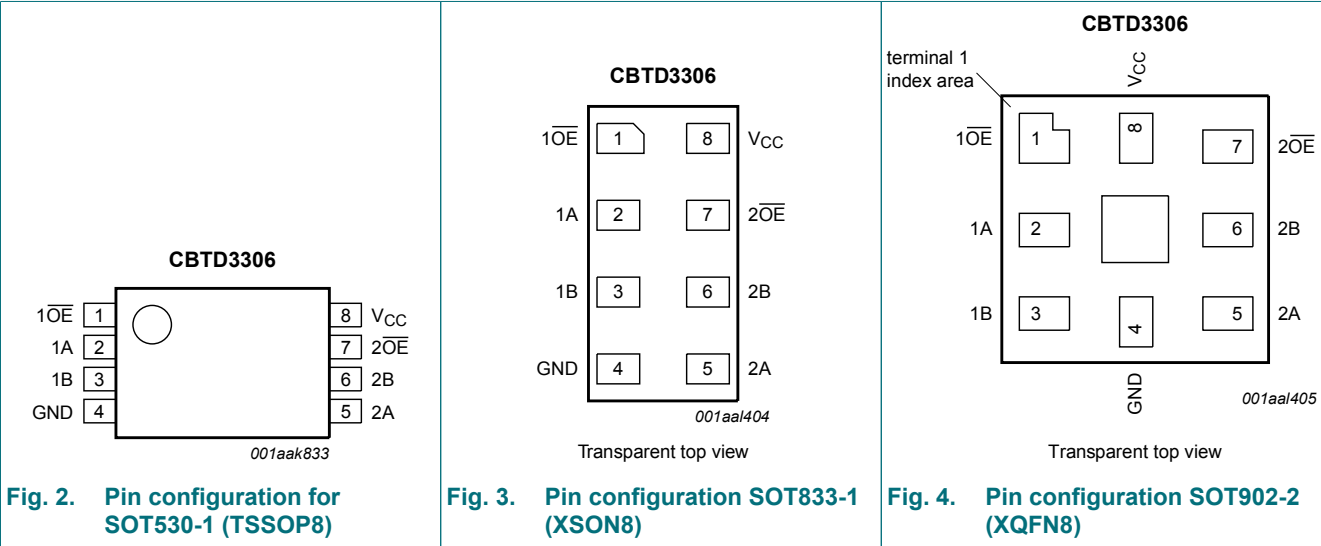
Type number	Marking code
CBTD3306PW	D306
CBTD3306GT	W06
CBTD3306GM	W06

5. Functional diagram



6. Pinning information

6.1. Pinning



6.2. Pin description

Table 3. Pin description

Symbol	Pin	Description
1OE, 2OE	1, 7	output enable input
1A, 2A	2, 5	data input/output (A port)
1B, 2B	3, 6	data input/output (B port)
GND	4	ground (0 V)
VCC	8	positive supply voltage

7. Functional description

Table 4. Function selection

H = HIGH voltage level; L = LOW voltage level; Z = high-impedance OFF-state.

Input	Input/output
nOE	nA, nB
L	nA = nB
H	Z

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). [1]

T_{amb} = -40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+7.0	V
V _I	input voltage	[2]	-0.5	+7.0	V
I _{SW}	switch current		-	128	mA
I _{IK}	input clamping current	V _{I/O} = 0 V	-50	-	mA
T _{stg}	storage temperature		-65	+150	°C

[1] Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under Section 9. is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

[2] The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

9. Recommended operating conditions

Table 6. Operating conditions

All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{CC}	supply voltage		4.5	-	5.5	V
V _{IH}	HIGH-level input voltage		2.0	-	-	V
V _{IL}	LOW-level input voltage		-	-	0.8	V
T _{amb}	ambient temperature	operating in free air	-40	-	+85	°C

10. Static characteristics

Table 7. Static characteristics

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	T _{amb} = -40 °C to +85 °C			Unit
			Min	Typ [1]	Max	
V _{IK}	input clamping voltage	V _{CC} = 4.5 V; I _I = -18 mA	-	-	-1.2	V
I _I	input leakage current	V _{CC} = 5.5 V; V _I = GND or 5.5 V	-	-	±1	µA
I _{CC}	supply current	V _{CC} = 5.5 V; I _{SW} = 0 mA; V _I = V _{CC} or GND	-	-	1.5	mA
V _{pass}	pass voltage	see Fig. 5 to Fig. 9	-	-	-	V
ΔI _{CC}	additional supply current	per input pin; V _{CC} = 5.5 V; one input at 3.4 V, other inputs at V _{CC} or GND [2]	-	-	2.5	mA
C _I	input capacitance	control pin; V _I = 3 V or 0 V	-	3.2	-	pF
C _{io(off)}	off-state input/output capacitance	port off; V _I = 3 V or 0 V; n $\overline{\text{OE}}$ = V _{CC}	-	6.5	-	pF
R _{ON}	ON resistance	V _{CC} = 4.5 V; V _I = 0 V; I _I = 64 mA [3]	-	3.6	5	Ω
		V _{CC} = 4.5 V; V _I = 0 V; I _I = 30 mA [3]	-	3.6	5	Ω
		V _{CC} = 4.5 V; V _I = 2.4 V; I _I = 15 mA [3]	-	17	35	Ω

[1] All typical values are at V_{CC} = 5 V, T_{amb} = 25 °C.

[2] This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

[3] Measured by the voltage drop between the nA and the nB terminals at the indicated current through the switch. ON resistance is determined by the lowest voltage of the two (nA or nB) terminals.

10.1. Typical pass voltage graphs

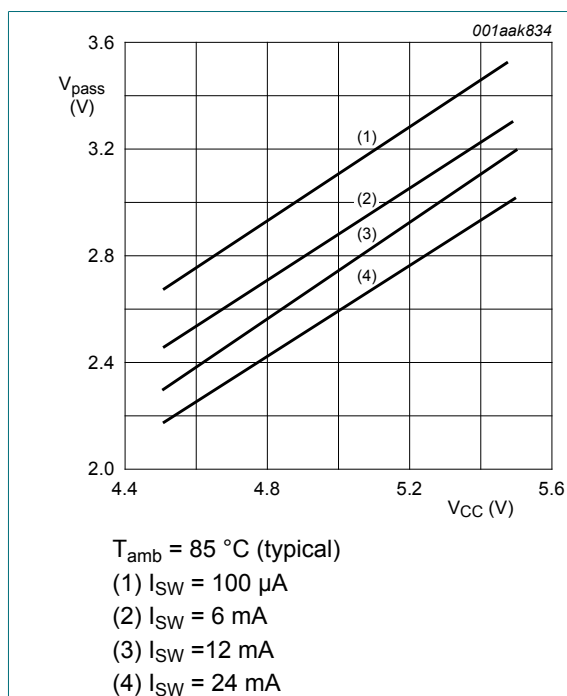


Fig. 5. Pass voltage versus supply voltage

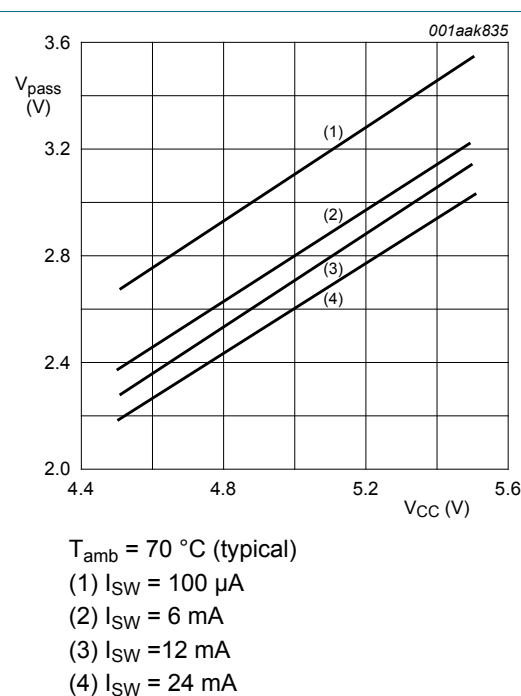
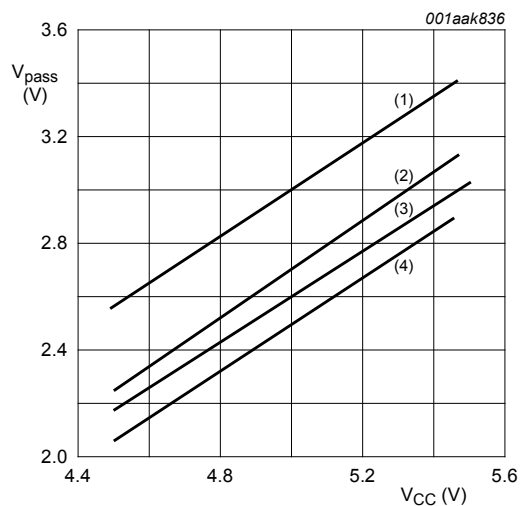


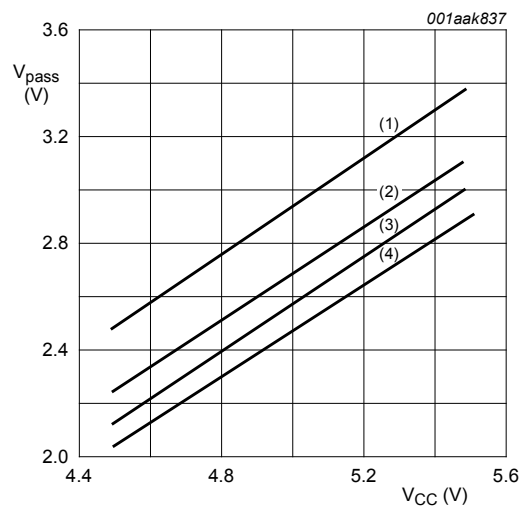
Fig. 6. Pass voltage versus supply voltage



$T_{amb} = 25\text{ °C}$ (typical)

- (1) $I_{SW} = 100\text{ }\mu\text{A}$
- (2) $I_{SW} = 6\text{ mA}$
- (3) $I_{SW} = 12\text{ mA}$
- (4) $I_{SW} = 24\text{ mA}$

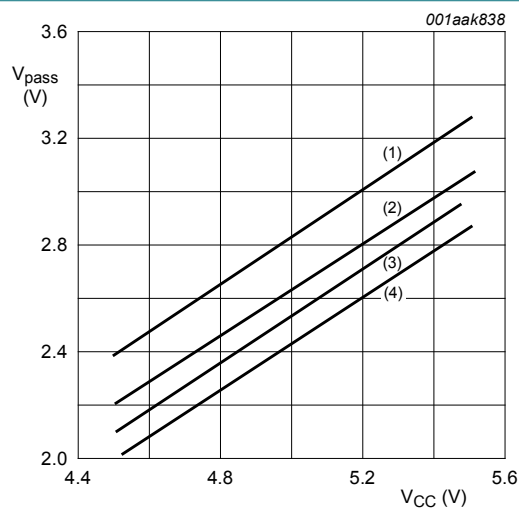
Fig. 7. Pass voltage versus supply voltage



$T_{amb} = 0\text{ °C}$ (typical)

- (1) $I_{SW} = 100\text{ }\mu\text{A}$
- (2) $I_{SW} = 6\text{ mA}$
- (3) $I_{SW} = 12\text{ mA}$
- (4) $I_{SW} = 24\text{ mA}$

Fig. 8. Pass voltage versus supply voltage



$T_{amb} = -40\text{ °C}$ (typical)

- (1) $I_{SW} = 100\text{ }\mu\text{A}$
- (2) $I_{SW} = 6\text{ mA}$
- (3) $I_{SW} = 12\text{ mA}$
- (4) $I_{SW} = 24\text{ mA}$

Fig. 9. Pass voltage versus supply voltage

11. Dynamic characteristics

Table 8. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V). For test circuit see Fig. 12.

Symbol	Parameter	Conditions	T _{amb} = -40 °C to +85 °C			Unit
			Min	Typ	Max	
t _{pd}	propagation delay	nA, nB to nB, nA; see Fig. 10 [1][2] V _{CC} = 5.0 V ± 0.5 V	-	-	0.25	ns
t _{en}	enable time	n $\overline{\text{OE}}$ to nA or nB; see Fig. 11 [2] V _{CC} = 5.0 V ± 0.5 V	1.0	-	5.4	ns
t _{dis}	disable time	n $\overline{\text{OE}}$ to nA or nB; see Fig. 11 [2] V _{CC} = 5.0 V ± 0.5 V	1.0	-	4.9	ns

- [1] The propagation delay is the calculated RC time constant of the typical ON resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
- [2] t_{pd} is the same as t_{PLH} and t_{PHL}; t_{en} is the same as t_{PZL} and t_{PZH}; t_{dis} is the same as t_{PLZ} and t_{PHZ}.

11.1. Waveforms and test circuit

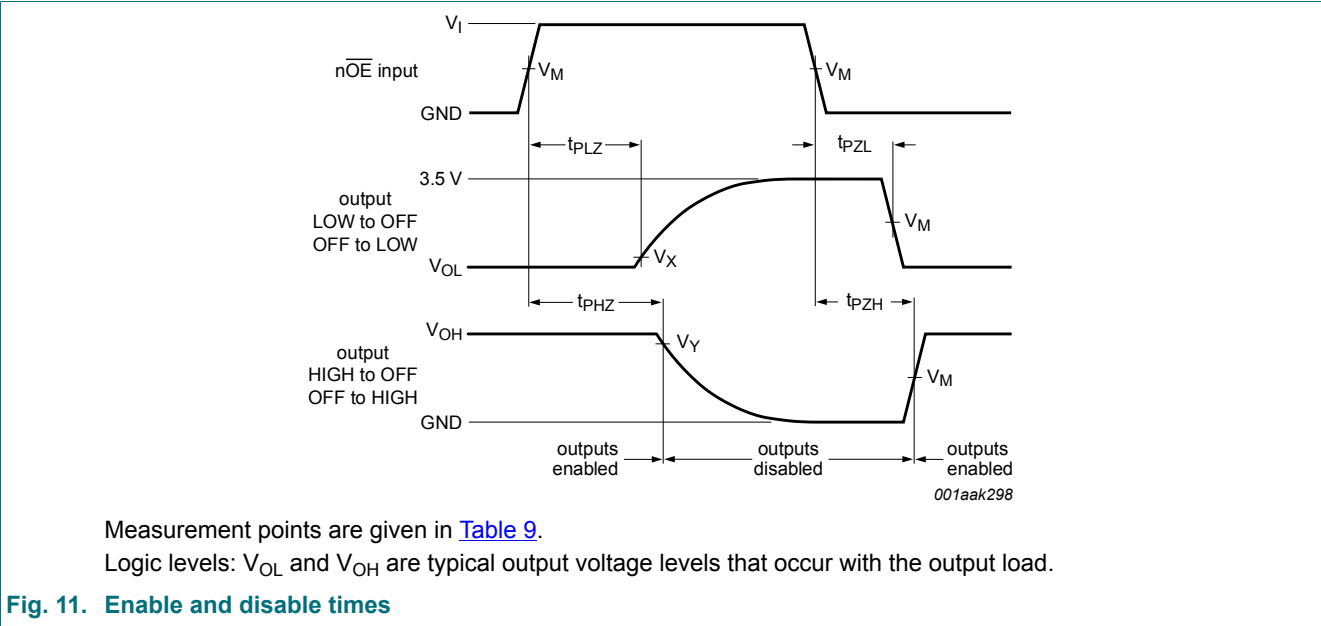
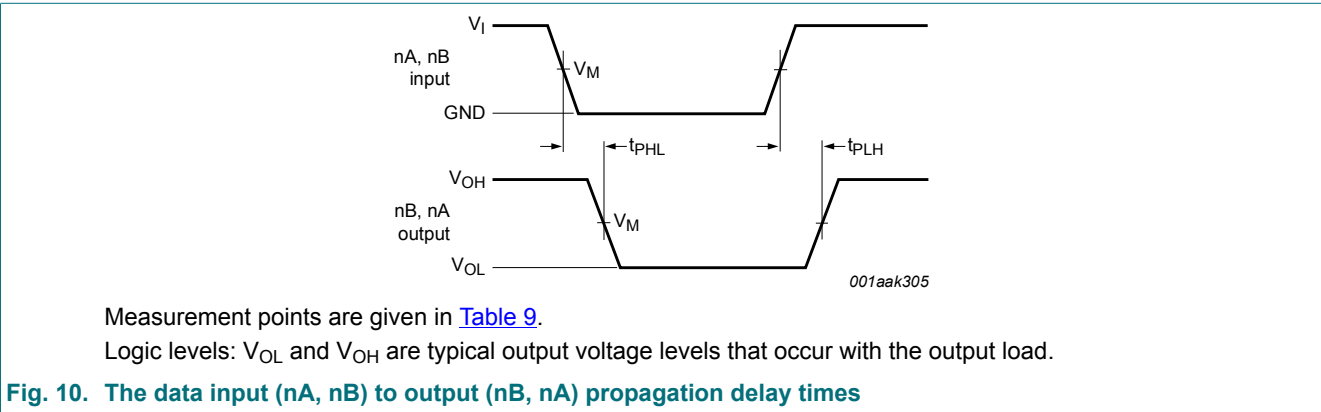
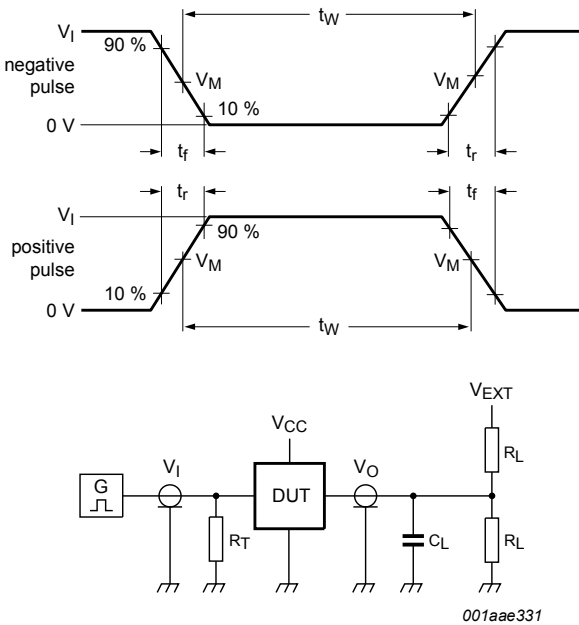


Table 9. Measurement points

Supply voltage	Input		Output		
V _{CC}	V _I	V _M	V _M	V _X	V _Y
V _{CC} = 5.0 V ± 0.5 V	GND to 3.0 V	1.5 V	1.5 V	V _{OL} + 0.3 V	V _{OH} - 0.3 V



Test data is given in [Table 10](#).

All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz; Z_o = 50 Ω.

The outputs are measured one at a time with one transition per measurement.

Definitions for test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

V_{EXT} = External voltage for measuring switching times.

Fig. 12. Test circuit for measuring switching times

Table 10. Test data

Supply voltage	Input		Load		V _{EXT}		
	V _I	t _r , t _f	C _L	R _L	t _{PLH} , t _{PHL}	t _{PLZ} , t _{PZL}	t _{PHZ} , t _{PZH}
V _{CC} = 5.0 V ± 0.5 V	GND to 3.0 V	≤ 2.5 ns	50 pF	500 Ω	open	7.0 V	open

12. Package outline

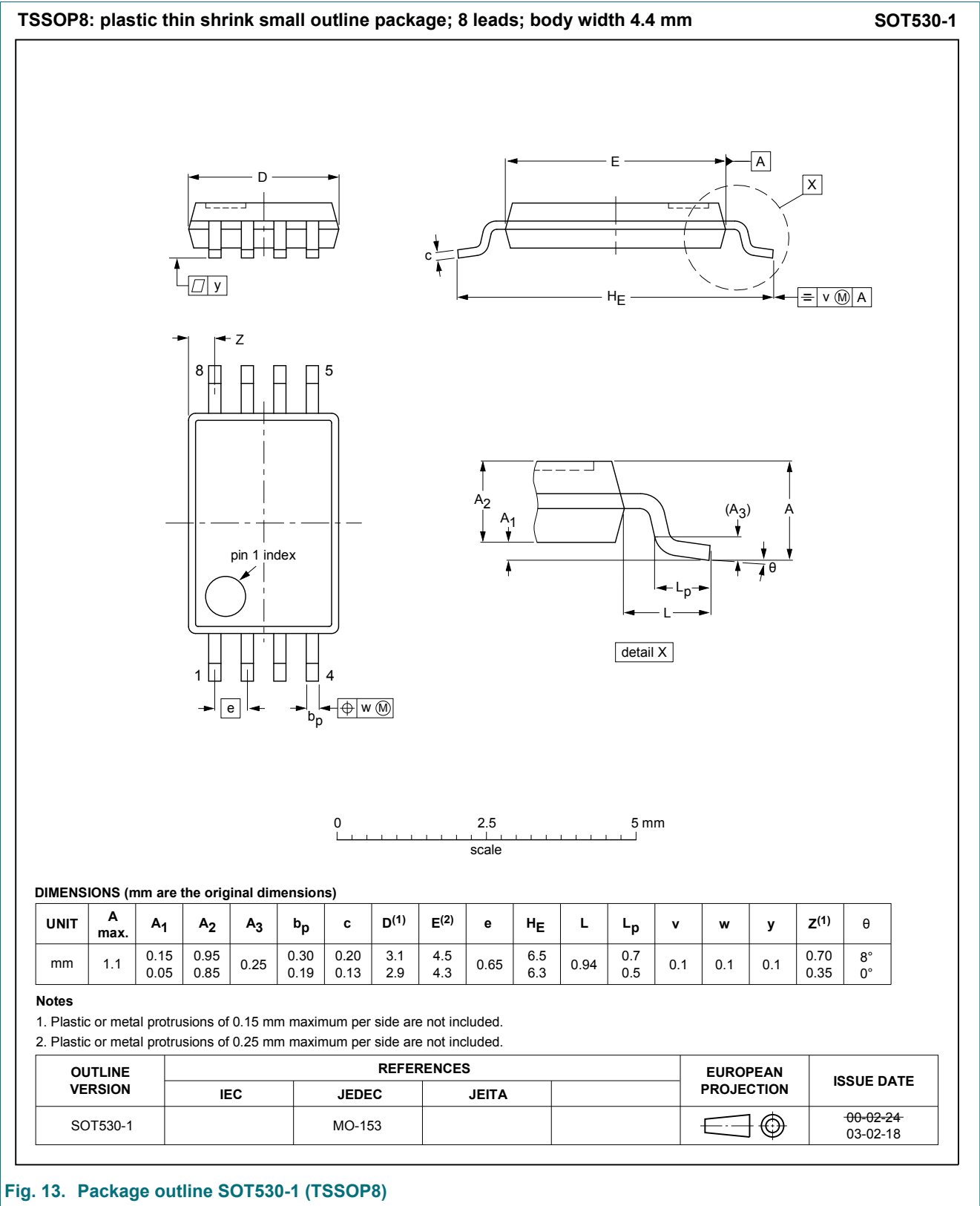
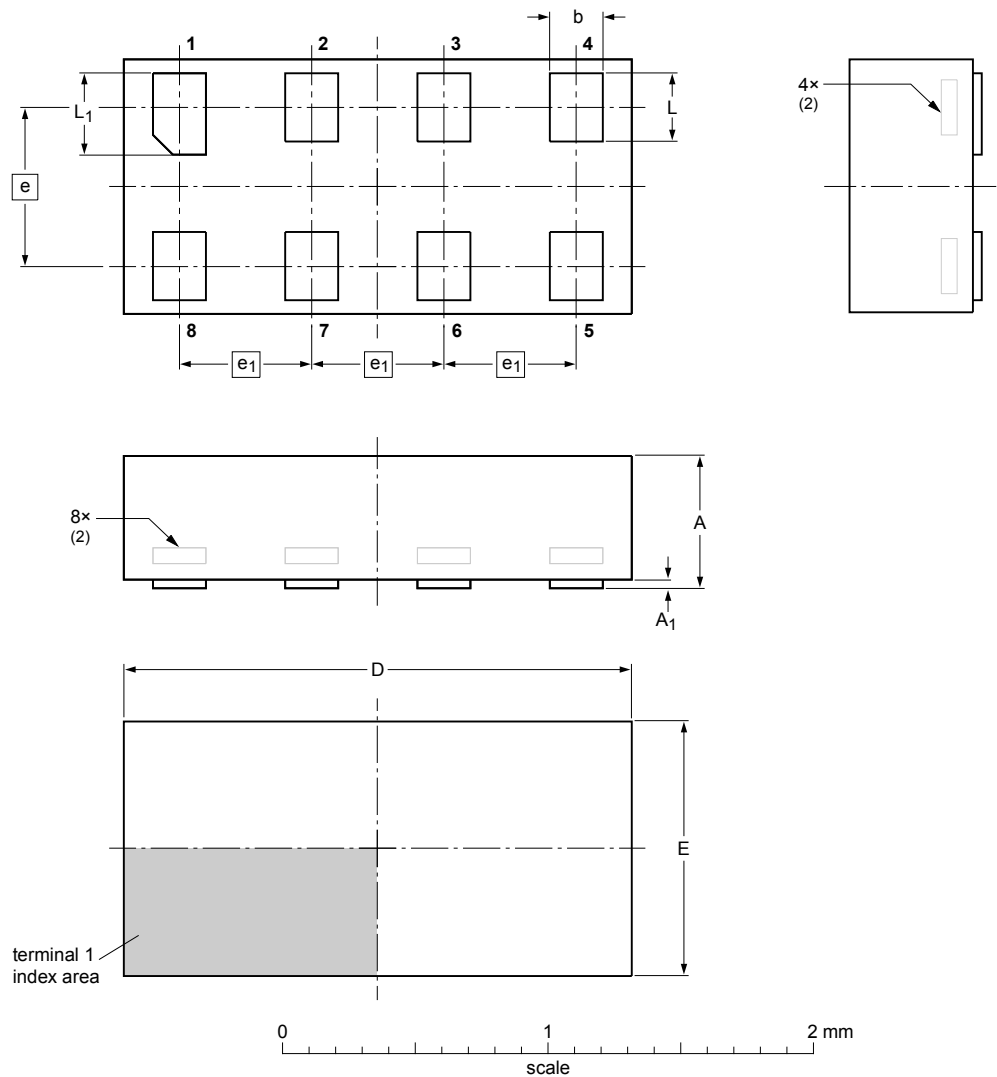


Fig. 13. Package outline SOT530-1 (TSSOP8)

XSON8: plastic extremely thin small outline package; no leads; 8 terminals; body 1 x 1.95 x 0.5 mm

SOT833-1



DIMENSIONS (mm are the original dimensions)

UNIT	A ⁽¹⁾ max	A ₁ max	b	D	E	e	e ₁	L	L ₁
mm	0.5	0.04	0.25 0.17	2.0 1.9	1.05 0.95	0.6	0.5	0.35 0.27	0.40 0.32

Notes

1. Including plating thickness.
2. Can be visible in some manufacturing processes.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT833-1	---	MO-252	---			-07-11-14- 07-12-07

Fig. 14. Package outline SOT833-1 (XSON8)

XQFN8: plastic, extremely thin quad flat package; no leads;
8 terminals; body 1.6 x 1.6 x 0.5 mm

SOT902-2

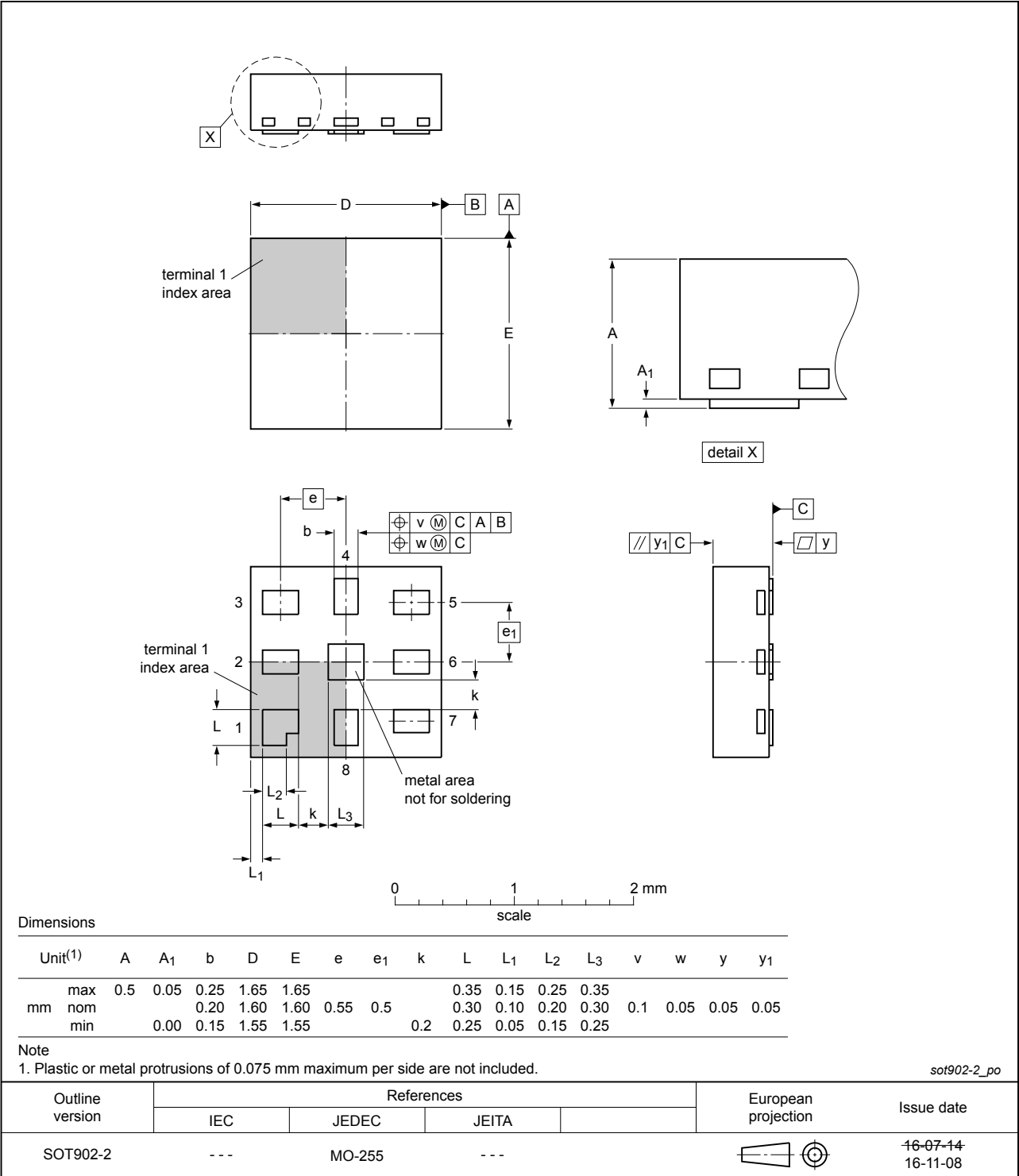


Fig. 15. Package outline SOT902-2 (XQFN8)

13. Abbreviations

Table 11. Abbreviations

Acronym	Description
CDM	Charged Device Model
ESD	ElectroStatic Discharge
FET	Field Effect Transistor
HBM	Human Body Model
PRR	Pulse Rate Repetition
TTL	Transistor-Transistor Logic

14. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
CBTD3306 v.9	20181115	Product data sheet	-	CBTD3306 v.8
Modifications:	- The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. - Legal texts have been adapted to the new company name where appropriate. - Type number CBTD3306D (SOT96-1/SO8) removed.			
CBTD3306 v.8	20120501	Product data sheet	-	CBTD3306 v.7
Modifications:	For type number CBTD3306GM the SOT code has changed to SOT902-2.			
CBTD3306 v.7	20120103	Product data sheet	-	CBTD3306 v.6
Modifications:	Marking code for type number CBTD3306D changed.			
CBTD3306 v.6	20111121	Product data sheet	-	CBTD3306 v.5
Modifications:	Legal pages updated.			
CBTD3306 v.5	20110428	Product data sheet	-	CBTD3306 v.4
CBTD3306 v.4	20100325	Product data sheet	-	CBTD3306 v.3
CBTD3306 v.3	20100223	Product data sheet	-	CBTD3306 v.2
CBTD3306 v.2	20091015	Product data sheet	-	CBTD3306 v.1
CBTD3306 v.1	20011108	Product data	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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Date of release: 15 November 2018

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