Micropower RRIO Operational Amplifier

ADA4092-4

FEATURES

- Single-supply operation: 3 V to 30 V
- Wide input voltage range
- Rail-to-rail output swing
- Low supply current: 200 µA/amplifier
- Wide bandwidth: 1.4 MHz
- High phase margin: 69°
- Slew rate: 0.4 V/µs
- Low offset voltage: 1.50 mV maximum
- No phase reversal
- Overvoltage protection (OVP)
  - 25 V above/below supply rails at ±5 V
  - 12 V above/below supply rails at ±15 V

PIN CONFIGURATION

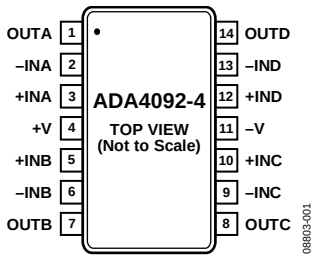

Figure 1. 14-Lead TSSOP (RU-14)

APPLICATIONS

- Industrial process control
- Battery-powered instrumentation
- Power supply control and protection
- Telecommunications
- Remote sensors
- Low voltage strain gage amplifiers
- DAC output amplifiers

GENERAL DESCRIPTION

The ADA4092-4 quad is a micropower, single-supply, 1.4 MHz bandwidth amplifier featuring rail-to-rail inputs and outputs. It is guaranteed to operate from a +3 V to +30 V single supply as well as from ±1.5 V to ±15 V dual supplies.

The ADA4092-4 features a unique input stage that allows the input voltage to exceed either supply safely without any phase reversal or latch-up; this is called overvoltage protection (OVP).

Applications for these amplifiers include portable telecommunications equipment, power supply control and protection, and interface for transducers with wide output ranges. Sensors requiring a rail-to-rail input amplifier include Hall effect, piezoelectric, and resistive transducers.

The ability to swing rail-to-rail at both the input and output enables designers, for example, to build multistage filters in single-supply systems and to maintain high signal-to-noise ratios (SNR).

The ADA4092-4 is specified over the extended industrial temperature range of −40°C to +125°C. The ADA4092-4 is part of the growing selection of 30 V, low power op amps from Analog Devices, Inc., see Table 1.

The ADA4092-4 is available in the 14–lead TSSOP surface-mount package.

Table 1. Low Power, 30 V Operational Amplifiers

Family	Rail-to-Rail I/O	RRIO Precision	PJFET	Low Noise
Single				OP1177
Dual		ADA4091-2	AD8682	OP2177
Quad	ADA4092-4	ADA4091-4	AD8684	OP4177

Rev. B

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REVISION HISTORY

6/11—Rev. A to Rev. B

Changes to Single-Supply Operating Range 1

5/10—Rev. 0 to Rev. A

Changes to Data Sheet Title, General Description, and Table 1 1

4/10—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

V_{SY} = ±1.5 V, V_{CM} = 0 V, T_A = 25°C, unless otherwise noted.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}		−1.5	+0.2	+1.5	mV
		−40°C ≤ T_A ≤ +125°C	−2.5		+2.5	mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			3		µV/°C
Input Bias Current	I_B		−60	−45		nA
		−40°C ≤ T_A ≤ +85°C	−60		+60	nA
		−40°C ≤ T_A ≤ +125°C	−275		+275	nA
Input Offset Current	I_{OS}		−4	+1	+4	nA
		−40°C ≤ T_A ≤ +85°C	−5		+5	nA
		−40°C ≤ T_A ≤ +125°C	−75		+75	nA
Input Voltage Range	IVR		−1.5		+1.5	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = −1.5 V to +1.5 V	70	85		dB
		−40°C ≤ T_A ≤ +125°C	68			dB
Large Signal Voltage Gain	A_{VO}	R_L = 100 kΩ, V_O = −1.2 V to +1.2 V	106	113		dB
		−40°C ≤ T_A ≤ +125°C	101			dB
		R_L = 10 kΩ, V_O = −1.2 V to +1.2 V	92	94		dB
		−40°C ≤ T_A ≤ +125°C	85			dB
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 100 kΩ to GND	1.485	1.495		V
		−40°C ≤ T_A ≤ +125°C	1.480			V
		R_L = 10 kΩ to GND	1.470	1.480		V
		−40°C to +125°C	1.455			V
Output Voltage Low	V_{OL}	R_L = 100 kΩ to GND		−1.497	−1.490	V
		−40°C ≤ T_A ≤ +125°C			−1.480	V
		R_L = 10 kΩ to GND		−1.495	−1.485	V
		−40°C ≤ T_A ≤ +125°C			−1.475	V
Short-Circuit Limit	I_{SC}	Source/sink		±30		mA
Closed-Loop Impedance	Z_{OUT}	f = 1 MHz, A_V = +1		130		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_{SY} = 2.7 V to 36 V	98	112		dB
		−40°C ≤ T_A ≤ +125°C	90			dB
Supply Current per Amplifier	I_{SY}	I_O = 0 mA		165	200	µA
		−40°C ≤ T_A ≤ +125°C			300	µA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 100 kΩ, C_L = 30 pF		0.4		V/µs
Settling Time	t_S	To 0.01%		25		µs
Gain Bandwidth Product	GBP			1.2		MHz
Phase Margin	Φ_M			66		Degrees
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		0.8		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		30		nV/√Hz

V_{SY} = ±5.0 V, V_{CM} = 0 V, T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}		−1.5	+0.2	+1.5	mV
		−40°C ≤ T_A ≤ +125°C	−2.5		+2.5	mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			3		µV/°C
Input Bias Current	I_B		−60	−53		nA
		−40°C ≤ T_A ≤ +85°C	−80		+80	nA
		−40°C ≤ T_A ≤ +125°C	−350		+350	nA
Input Offset Current	I_{OS}		−4	+1	+4	nA
		−40°C ≤ T_A ≤ +85°C	−7		+7	nA
		−40°C ≤ T_A ≤ +125°C	−100		+100	nA
Input Voltage Range	IVR		−5		+5	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = −5.0 V to +5.0 V	82	95		dB
		−40°C ≤ T_A ≤ +125°C	78			dB
Large Signal Voltage Gain	A_{VO}	R_L = 100 kΩ, V_O = ±4.7 V	113	117		dB
		−40°C ≤ T_A ≤ +125°C	106			dB
		R_L = 10 kΩ, V_O = ±4.7 V	98	100		dB
		−40°C ≤ T_A ≤ +125°C	90			dB
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 100 kΩ to GND	4.980	4.990		V
		−40°C ≤ T_A ≤ +125°C	4.975			V
		R_L = 10 kΩ to GND	4.945	4.960		V
		−40°C ≤ T_A ≤ +125°C	4.900			V
Output Voltage Low	V_{OL}	R_L = 100 kΩ to GND		−4.997	−4.990	V
		−40°C ≤ T_A ≤ +125°C			−4.980	V
		R_L = 10 kΩ to GND		−4.990	−4.980	V
		−40°C ≤ T_A ≤ +125°C			−4.975	V
Short-Circuit Limit	I_{SC}	Source/sink		±20		mA
Closed-Loop Impedance	Z_{OUT}	f = 1 MHz, A_V = +1		90		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_{SY} = 2.7 V to 36 V	98	112		dB
		−40°C ≤ T_A ≤ +125°C	90			dB
Supply Current per Amplifier	I_{SY}	I_O = 0 mA		180	225	µA
		−40°C ≤ T_A ≤ +125°C			300	µA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 100 kΩ, C_L = 30 pF		0.4		V/µs
Settling Time	t_S	To 0.01%		25		µs
Gain Bandwidth Product	GBP			1.3		MHz
Phase Margin	Φ_M			67		Degrees
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		0.8		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		30		nV/√Hz

V_{SY} = ±15.0 V, V_{CM} = 0 V, V_O = 0 V, T_A = 25°C, unless otherwise noted.

Table 4.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}		−1.5	+0.2	+1.5	mV
		−40°C ≤ T_A ≤ +125°C	−2.5		+2.5	mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			3		µV/°C
Input Bias Current	I_B		−60	−50		nA
		−40°C ≤ T_A ≤ +85°C	−80		+80	nA
		−40°C ≤ T_A ≤ +125°C	−500		+500	nA
Input Offset Current	I_{OS}		−4	+1	+4	nA
		−40°C ≤ T_A ≤ +85°C	−10		+10	nA
		−40°C ≤ T_A ≤ +125°C	−140		+140	nA
Input Voltage Range	IVR		−15		+15	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = −15.0 V to +15.0 V	90	103		dB
		−40°C ≤ T_A ≤ +125°C	87			dB
Large Signal Voltage Gain	A_{VO}	R_L = 100 kΩ, V_O = ±14.7 V	116	118		dB
		−40°C ≤ T_A ≤ +125°C	108			dB
		R_L = 10 kΩ, V_O = ±14.7 V	102	104		dB
		−40°C ≤ T_A ≤ +125°C	93			dB
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 100 kΩ to GND	14.970	14.980		V
		−40°C ≤ T_A ≤ +125°C	14.950			V
		R_L = 10 kΩ to GND	14.900	14.915		V
		−40°C ≤ T_A ≤ +125°C	14.800			V
Output Voltage Low	V_{OL}	R_L = 100 kΩ to GND		−14.985	−14.980	V
		−40°C ≤ T_A ≤ +125°C			−14.965	V
		R_L = 10 kΩ to GND		−14.970	−14.950	V
		−40°C ≤ T_A ≤ +125°C			−14.940	V
Short-Circuit Limit	I_{SC}	Source/sink		±20		mA
Closed-Loop Impedance	Z_{OUT}	f = 1 MHz, A_V = +1		68		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_{SY} = 2.7 V to 36 V	98	112		dB
		−40°C ≤ T_A ≤ +125°C	90			dB
Supply Current per Amplifier	I_{SY}	I_O = 0 mA		200	250	µA
		−40°C ≤ T_A ≤ +125°C			350	µA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 100 kΩ, C_L = 30 pF		0.4		V/µs
Settling Time	t_S	To 0.01%		25		µs
Gain Bandwidth Product	GBP			1.4		MHz
Phase Margin	Φ_M			69		Degrees
Channel Separation	CS	f = 1 kHz		100		dB
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		0.8		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		30		nV/√Hz

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
Supply Voltage	36 V
Input Voltage	Refer to the Input Overvoltage Protection section
Differential Input Voltage	$\pm V_{SY}$
Input Current	±5 mA
Output Short-Circuit Duration to GND	Indefinite
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +125°C
Junction Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the device soldered on a 4-layer JEDEC standard printed circuit board (PCB) with zero airflow.

Table 6. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
14-Lead TSSOP (RU-14)	112	35	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

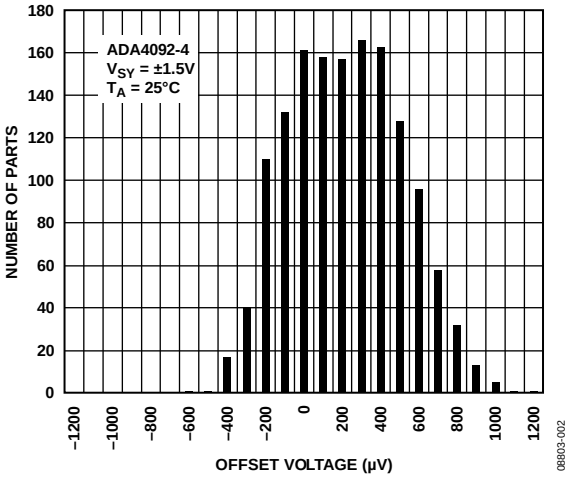


Figure 2. Input Offset Voltage Distribution, 3 V

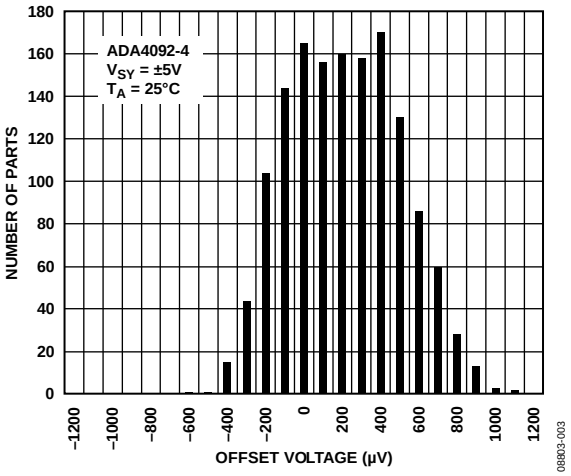


Figure 3. Input Offset Voltage Distribution, 10 V

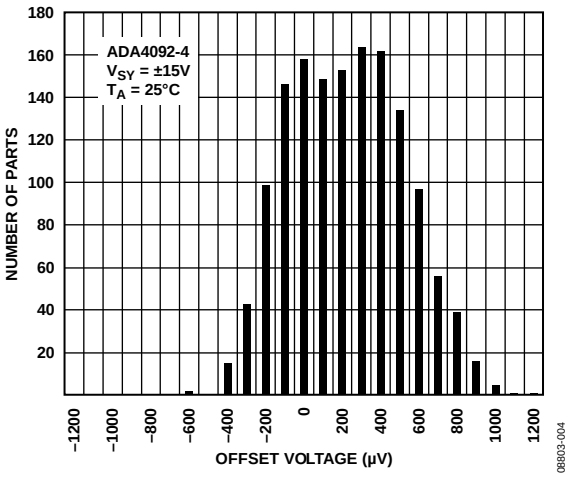


Figure 4. Input Offset Voltage Distribution, 30 V

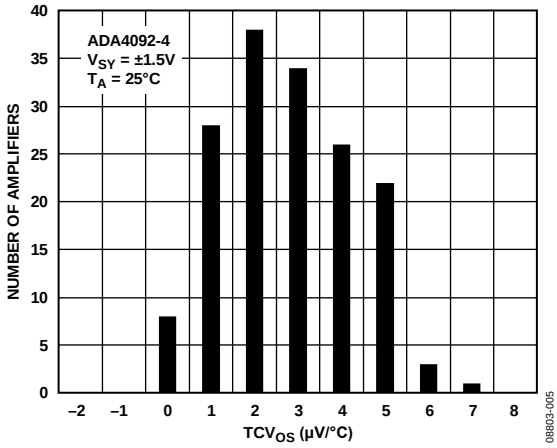


Figure 5. TCV_{OS} Distribution, 3 V

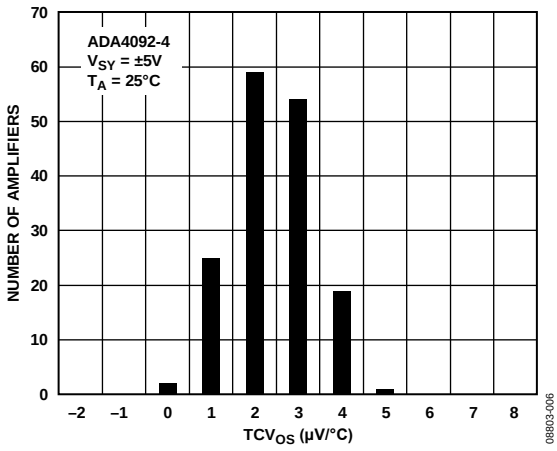


Figure 6. TCV_{OS} Distribution, 10 V

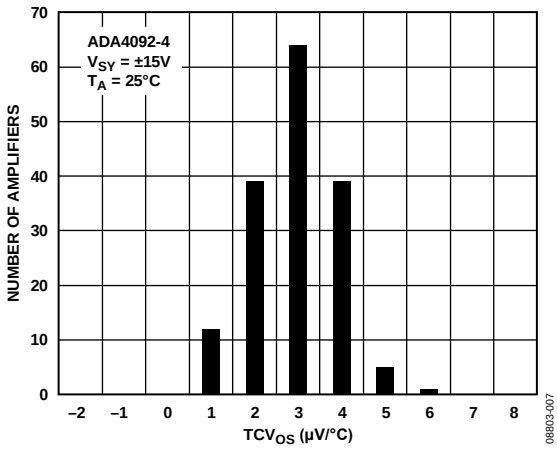


Figure 7. TCV_{OS} Distribution, 30 V

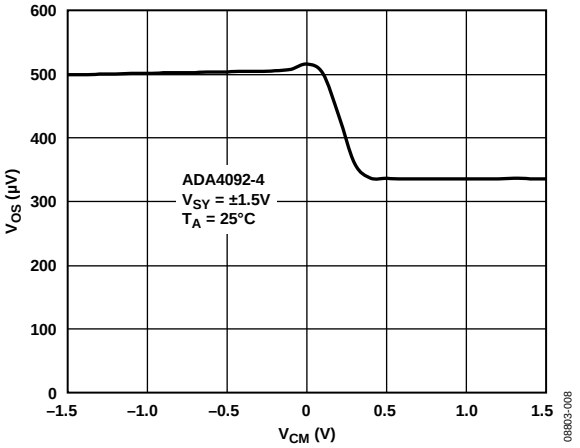


Figure 8. Input Offset Voltage vs. Common-Mode Voltage, 3 V

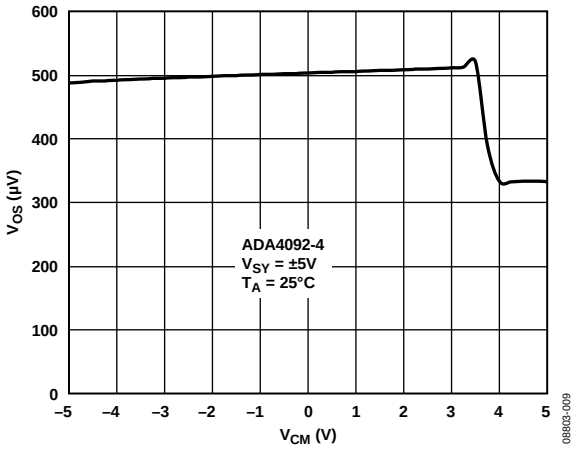


Figure 9. Input Offset Voltage vs. Common-Mode Voltage, 10 V

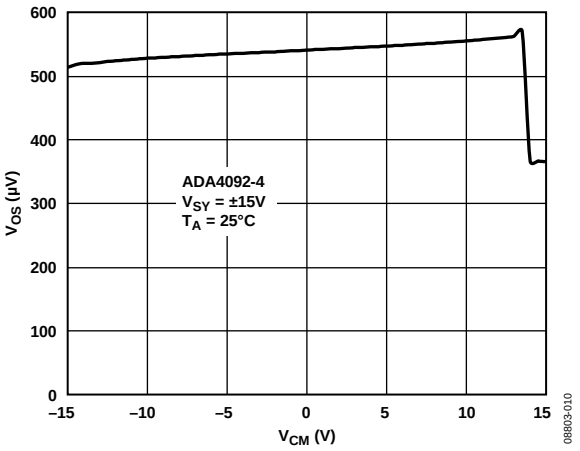


Figure 10. Input Offset Voltage vs. Common-Mode Voltage, 30 V

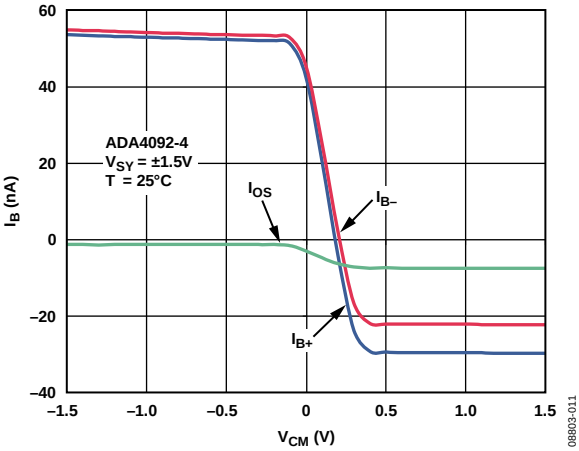


Figure 11. Input Bias Current vs. Common-Mode Voltage, 3 V

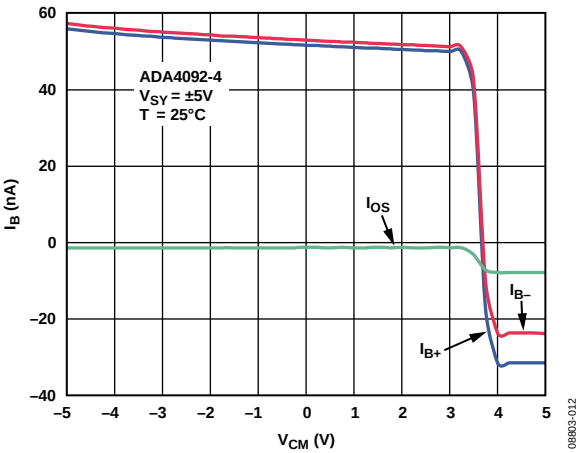


Figure 12. Input Bias Current vs. Common-Mode Voltage, 10 V

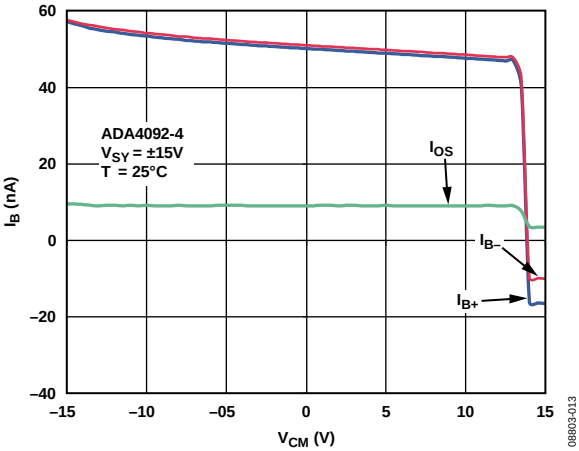


Figure 13. Input Bias Current vs. Common-Mode Voltage, 30 V

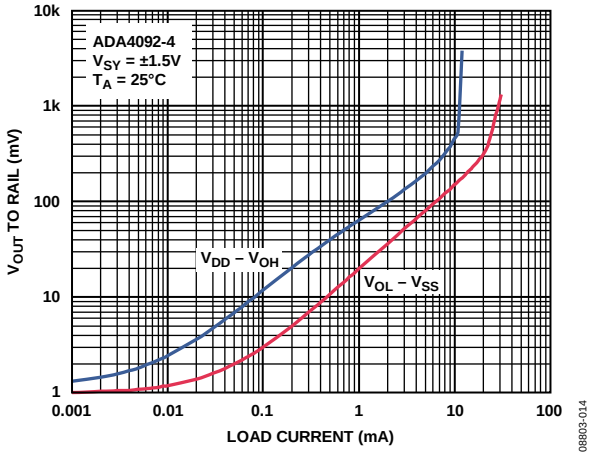


Figure 14. Dropout Voltage vs. Load Current, 3 V

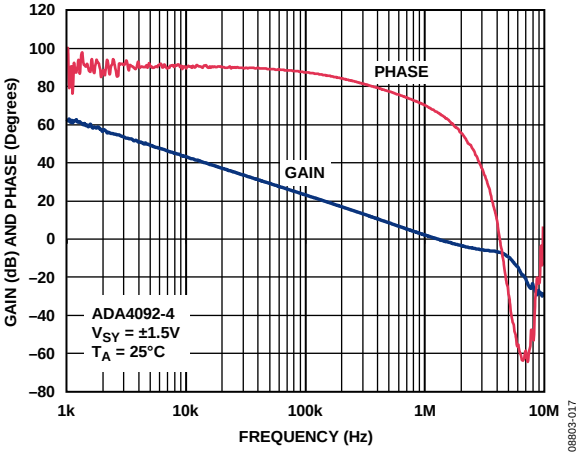


Figure 17. Open-Loop Gain and Phase vs. Frequency, 3 V

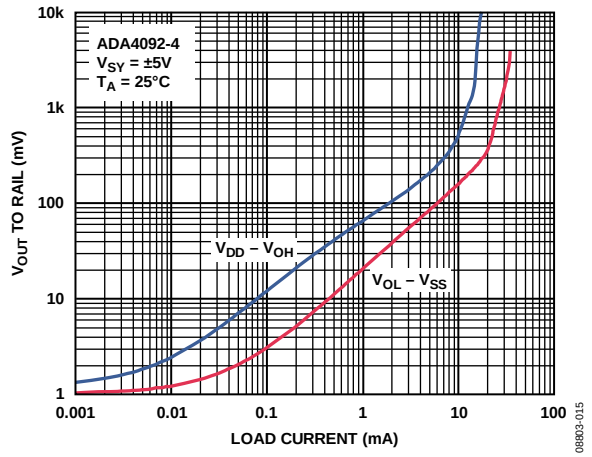


Figure 15. Dropout Voltage vs. Load Current, 10 V

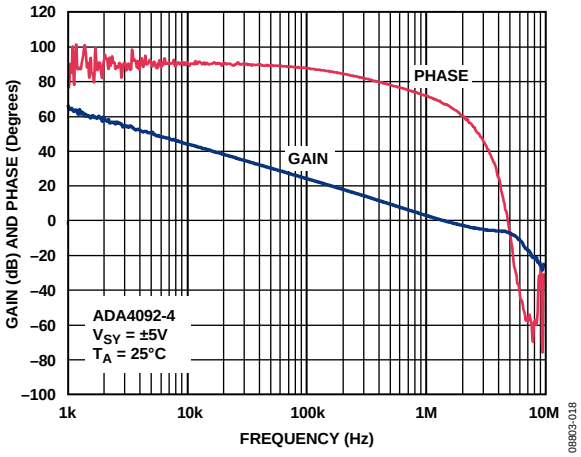


Figure 18. Open-Loop Gain and Phase vs. Frequency, 10 V

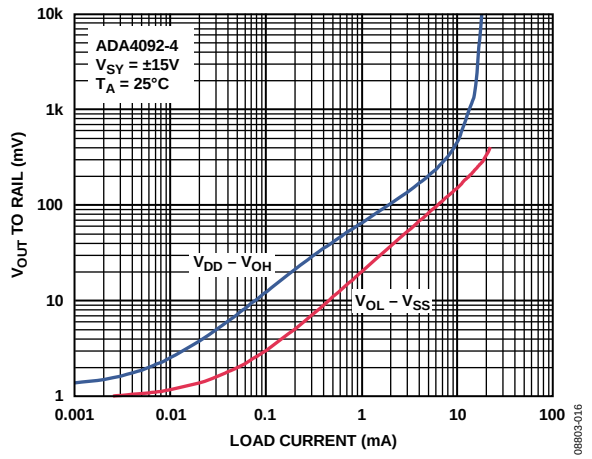


Figure 16. Dropout Voltage vs. Load Current, 30 V

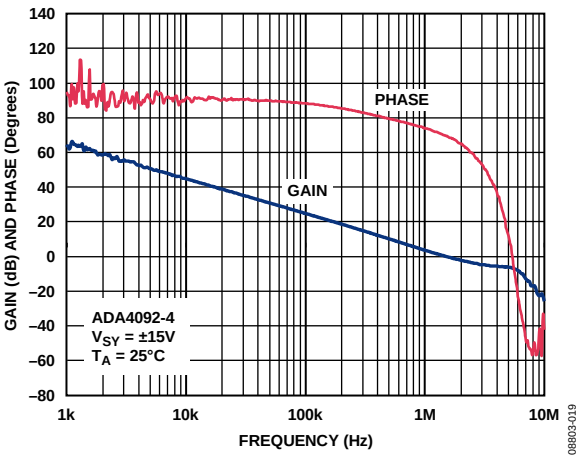


Figure 19. Open-Loop Gain and Phase vs. Frequency, 30 V

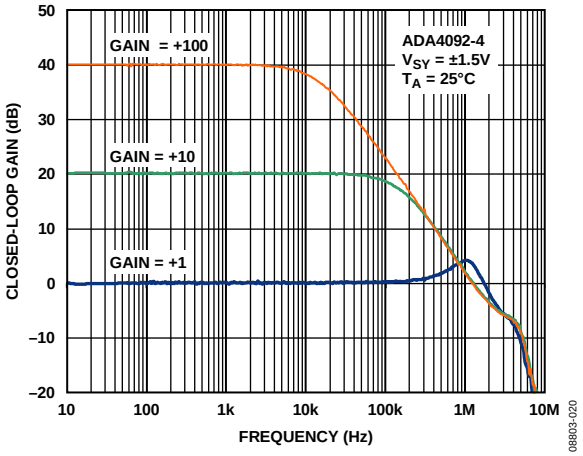


Figure 20. Closed-Loop Gain vs. Frequency, 3 V

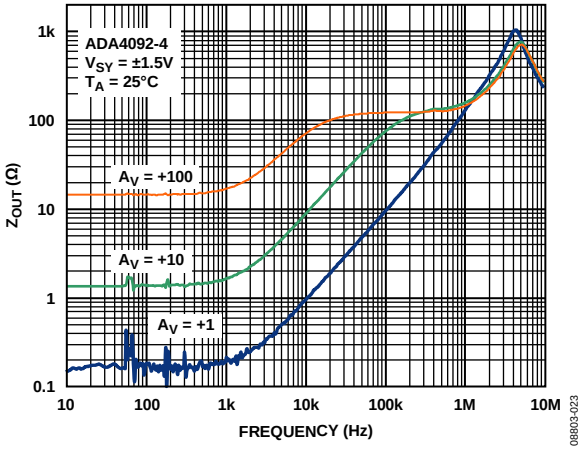


Figure 23. Closed-Loop Output Impedance vs. Frequency, 3 V

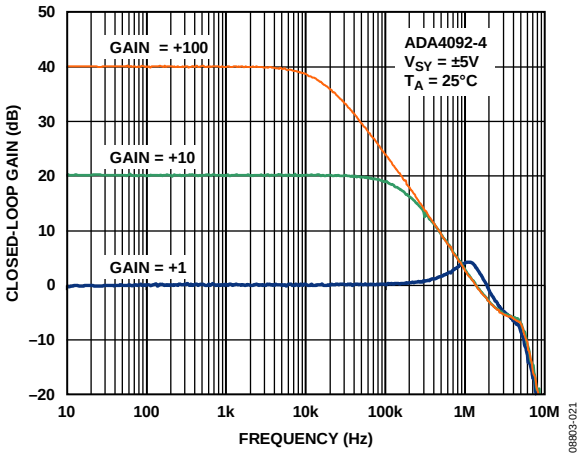


Figure 21. Closed-Loop Gain vs. Frequency, 10 V

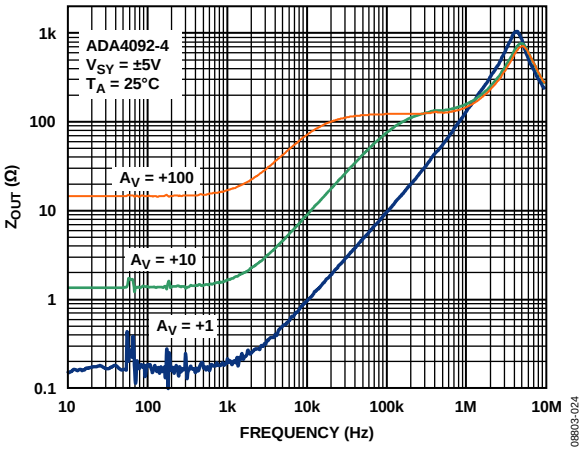


Figure 24. Closed-Loop Output Impedance vs. Frequency, 10 V

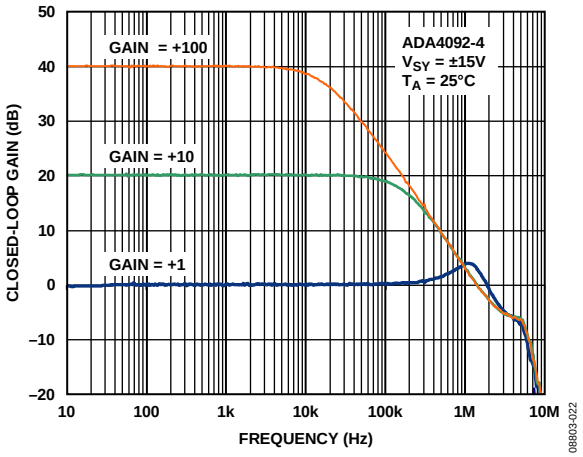


Figure 22. Closed-Loop Gain vs. Frequency, 30 V

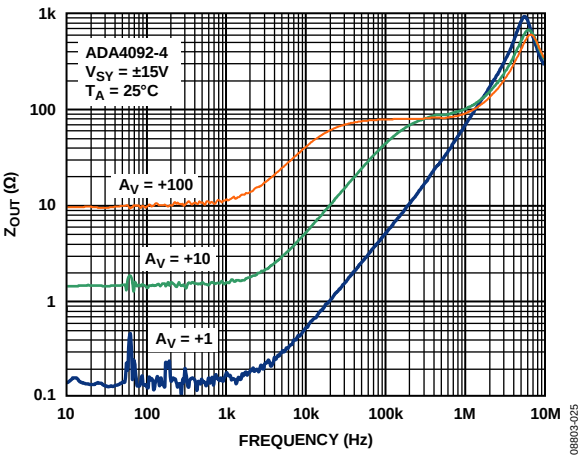


Figure 25. Output Impedance vs. Frequency, 30 V

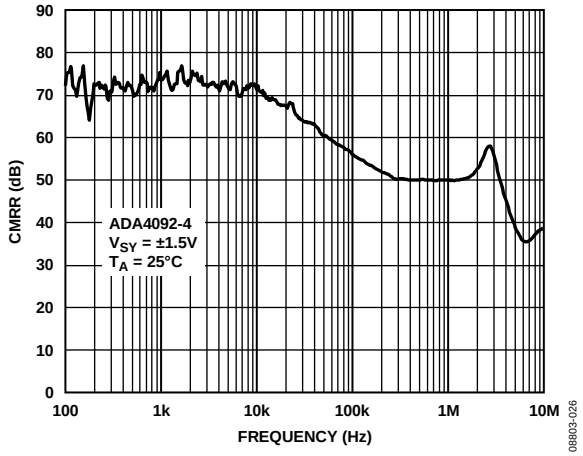


Figure 26. CMRR vs. Frequency, 3 V

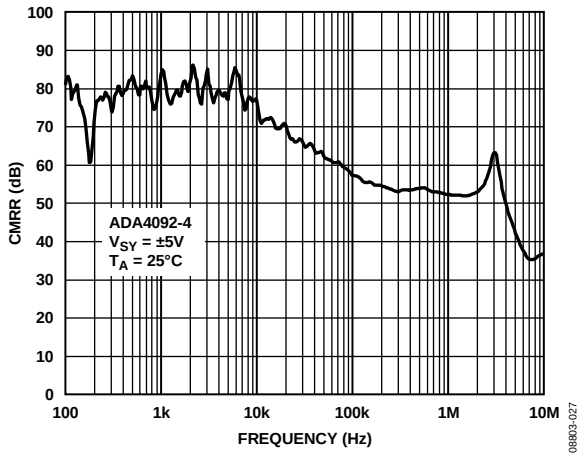


Figure 27. CMRR vs. Frequency, 10 V

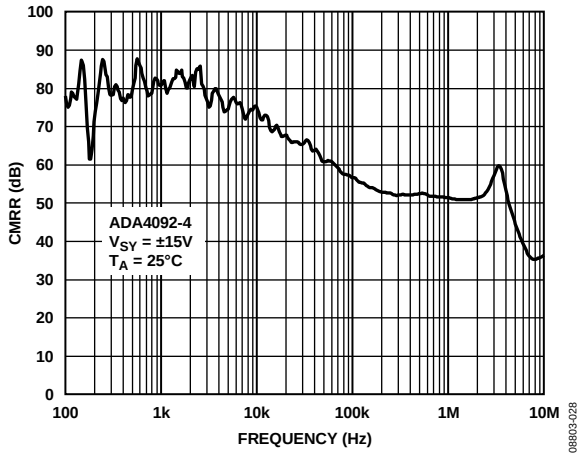


Figure 28. CMRR vs. Frequency, 30 V

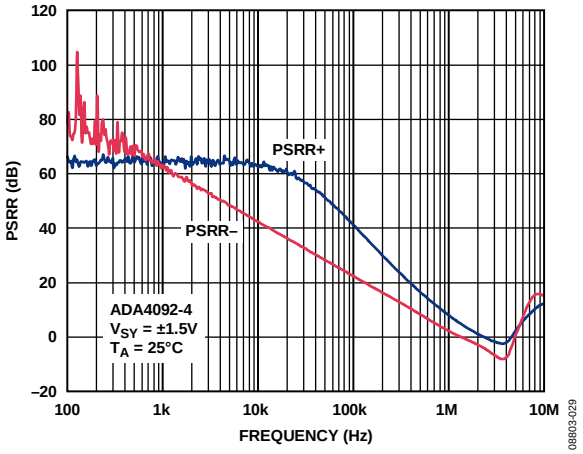


Figure 29. PSRR vs. Frequency, 3 V

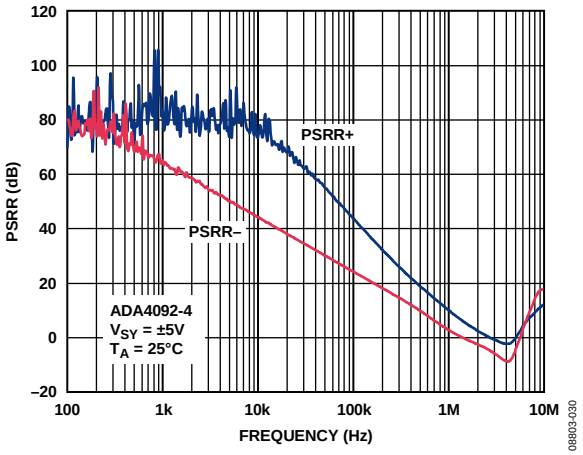


Figure 30. PSRR vs. Frequency, 10 V

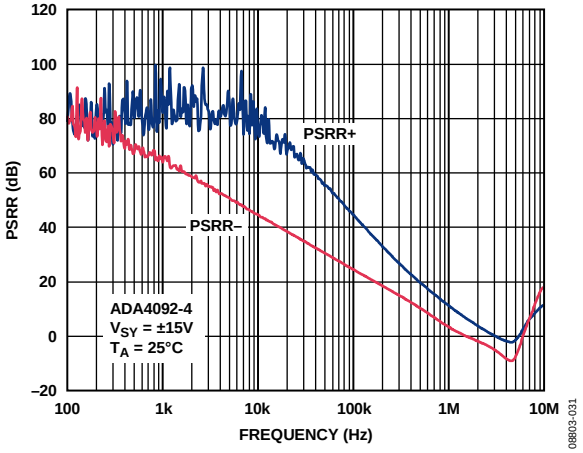


Figure 31. PSRR vs. Frequency, 30 V

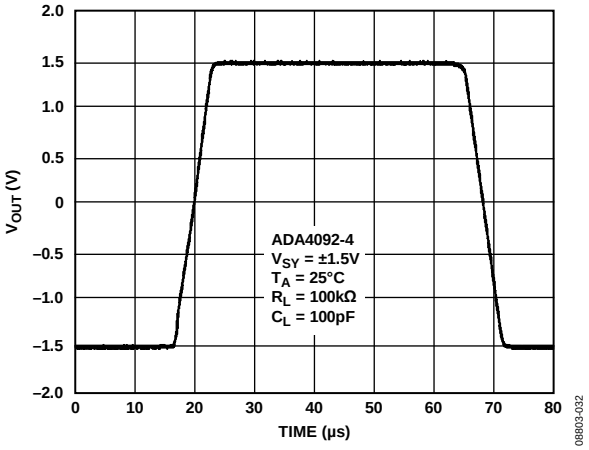


Figure 32. Large Signal Transient Response, 3 V

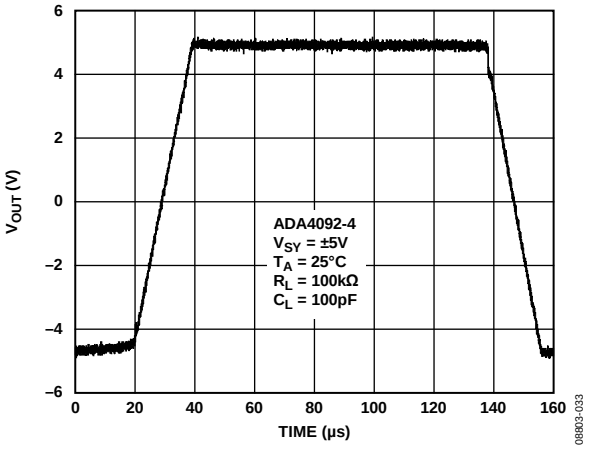


Figure 33. Large Signal Transient Response, 10 V

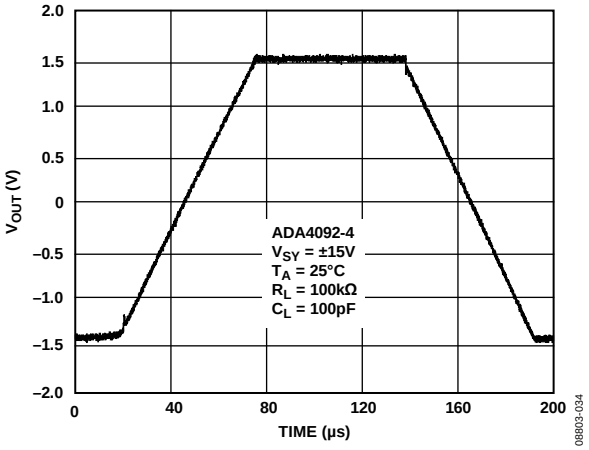


Figure 34. Large Signal Transient Response, 30 V

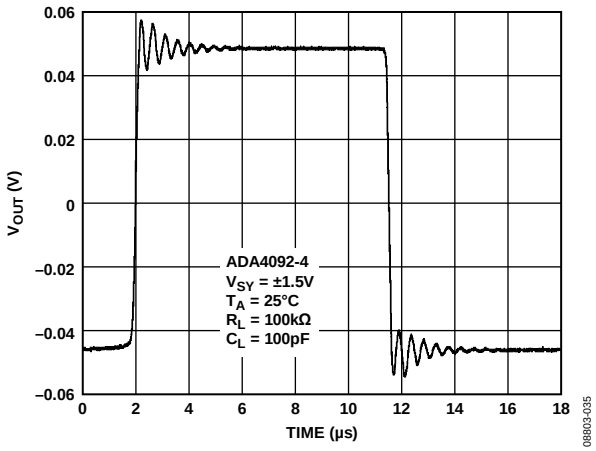


Figure 35. Small Signal Transient Response, 3 V

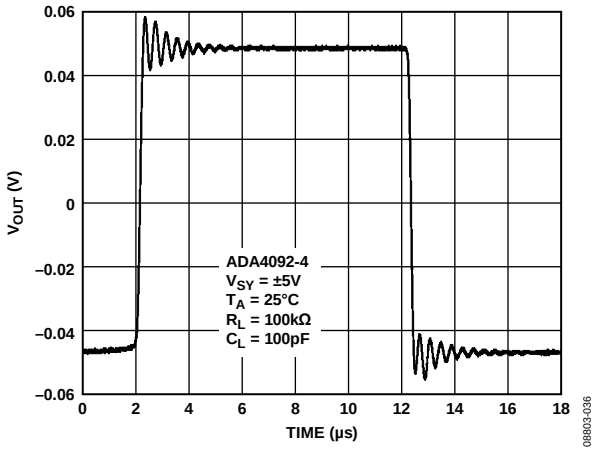


Figure 36. Small Signal Transient Response, 10 V

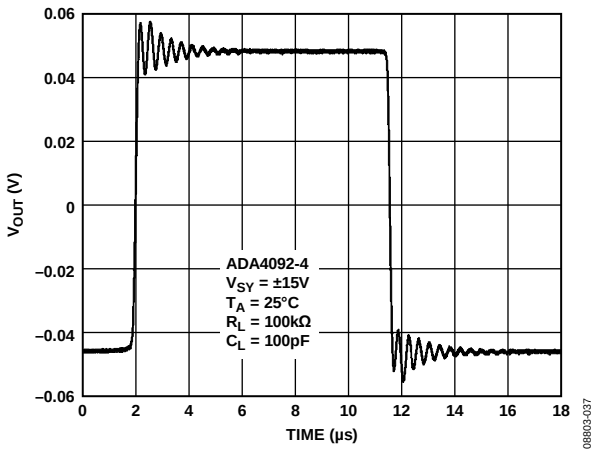


Figure 37. Small Signal Transient Response, 30 V

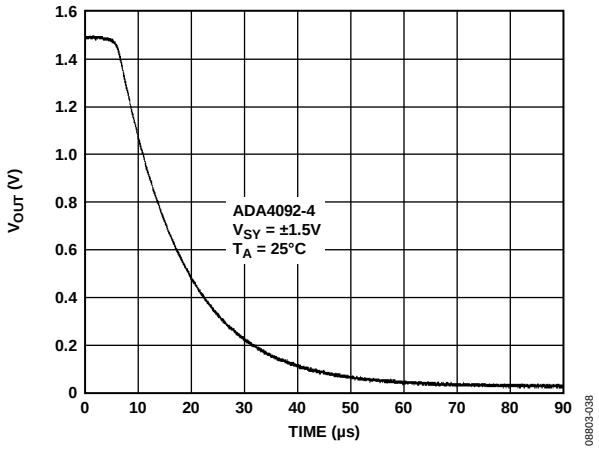


Figure 38. Positive Overload Recovery, 3 V

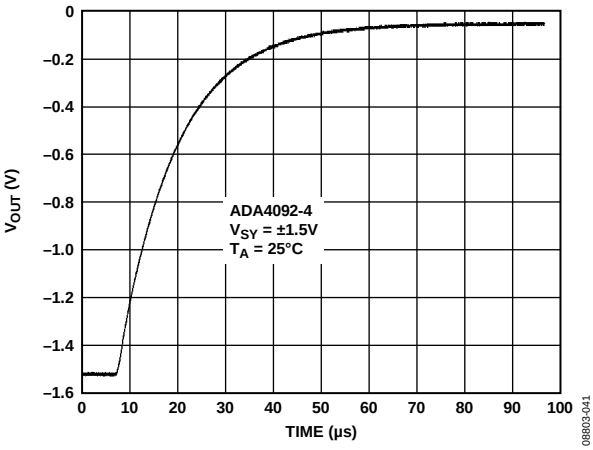


Figure 41. Negative Overload Recovery, 3 V

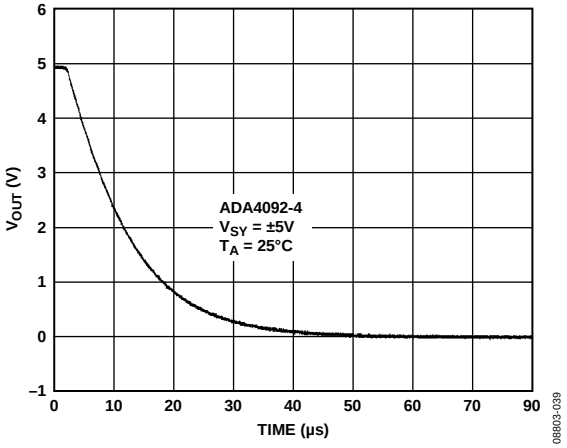


Figure 39. Positive Overload Recovery, 10 V

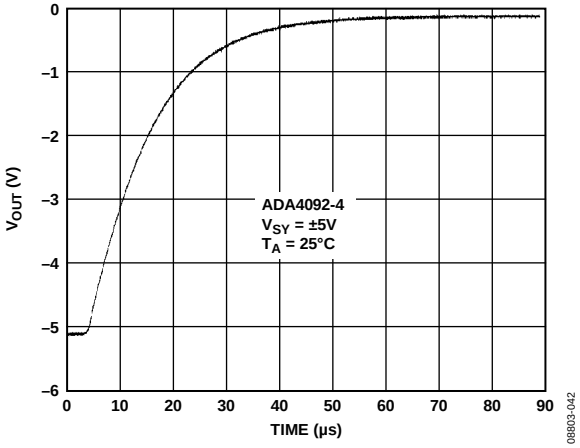


Figure 42. Negative Overload Recovery, 10 V

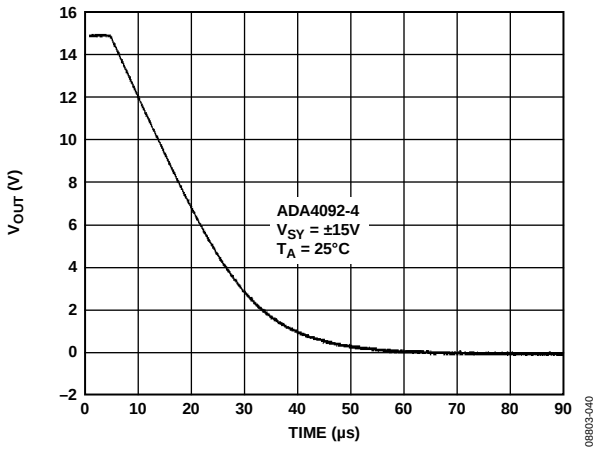


Figure 40. Positive Overload Recovery, 30 V

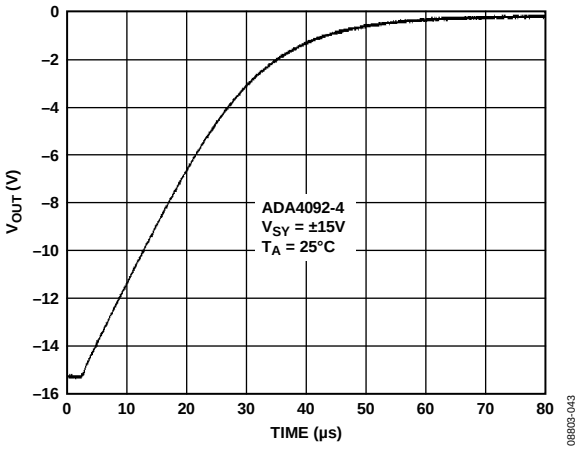


Figure 43. Negative Overload Recovery, 30 V

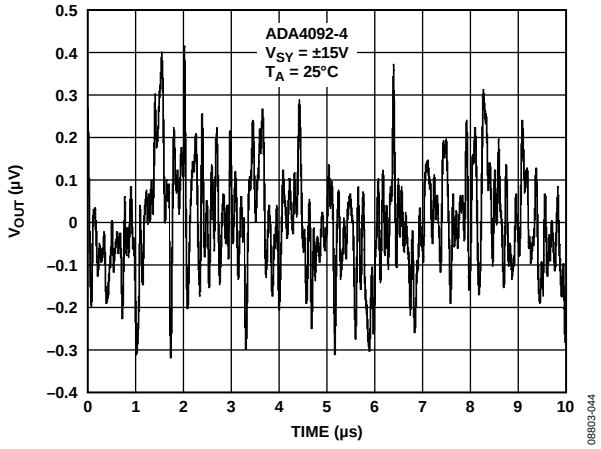


Figure 44. Peak-to-Peak Voltage Noise

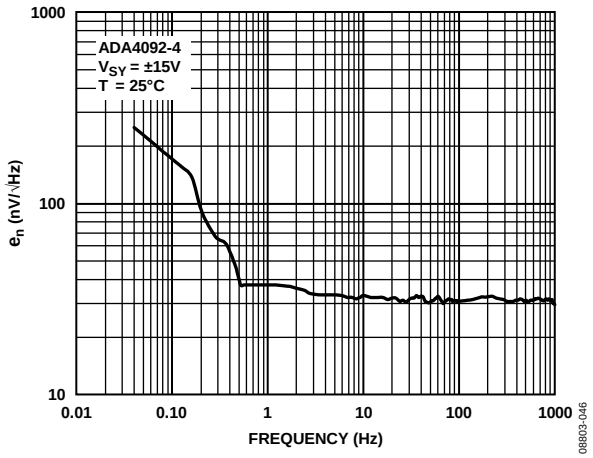


Figure 46. Voltage Noise Density

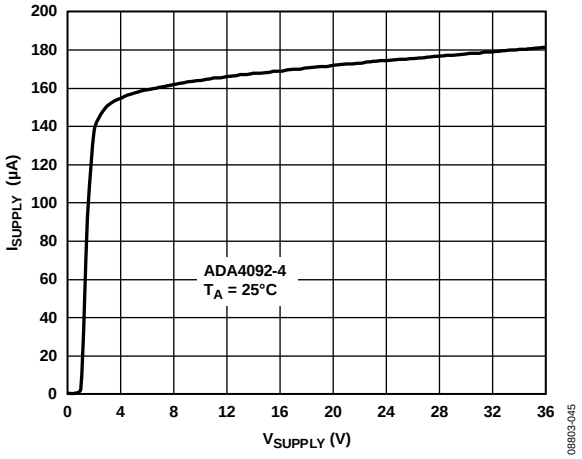


Figure 45. Supply Current vs. Supply Voltage

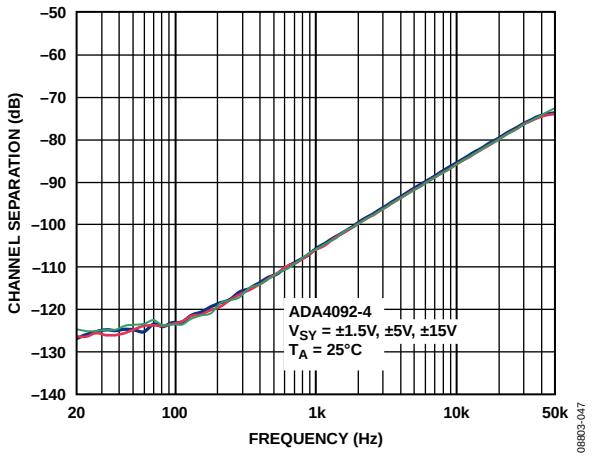


Figure 47. Channel Separation vs. Frequency

THEORY OF OPERATION

The ADA4092-4 is a single-supply, micropower amplifier featuring rail-to-rail inputs and outputs. To achieve wide input and output ranges, these amplifiers employ unique input and output stages.

INPUT STAGE

In Figure 48, the input stage comprises two differential pairs, a PNP pair (PNP input stage) and an NPN pair (NPN input stage). These input stages do not work in parallel. Instead, only one stage is on for any given input common-mode signal level. The PNP stage (Transistor Q1 and Transistor Q2) is required to ensure that the amplifier remains in the linear region when the input voltage approaches and reaches the negative rail. Alternatively, the NPN stage (Transistor Q5 and Transistor Q6) is needed for input voltages up to, and including, the positive rail.

For the majority of the input common-mode range, the PNP stage is active, as shown in Figure 8 through Figure 13. Notice that the V_{OS} shifts and that the bias current switches direction at approximately 1.5 V below the positive rail. At voltages below this level, the bias current flows out of the ADA4092-4 input, from the PNP input stage. However, above this voltage, the bias current enters the device due to the NPN stage. The actual mechanism within the amplifier for switching between the input stages comprises Q3, Q4, and Q7. As the input common-mode voltage increases, the emitters of Q1 and Q2 follow that voltage plus a diode drop. Eventually, the emitters of Q1 and Q2 are high enough to turn on Q3, which diverts the tail current away from the PNP input stage, turning it off. The tail current of the PNP pair is diverted to the Q4/Q7 current mirror to activate the NPN input stage, as shown in Figure 48.

A common practice in bipolar amplifiers to protect the input transistors from large differential voltages is to include series resistors and differential diodes. See Figure 49 for the full input protection circuitry. These diodes turn on whenever the differential voltage exceeds approximately 0.6 V. In this condition, current flows between the input pins, limited only by the two 5 kΩ resistors. Evaluate each application carefully to make sure that the increase in current does not affect performance.

OUTPUT STAGE

The output stage in the ADA4092-4 device uses a PNP and an NPN transistor, as do most output stages. However, Q32 and Q33, the output transistors, connect with their collectors to an output pin to achieve the rail-to-rail output swing.

As the output voltage approaches either the positive or the negative rail, these transistors begin to saturate. Thus, the final limit on output voltage is the saturation voltage of these transistors, which is about 50 mV. The output stage has inherent gain arising from the transistor output impedance, as well as any external load impedance; consequently, the open-loop gain of the op amp is dependent on the load resistance and decreases when the output voltage is close to either rail.

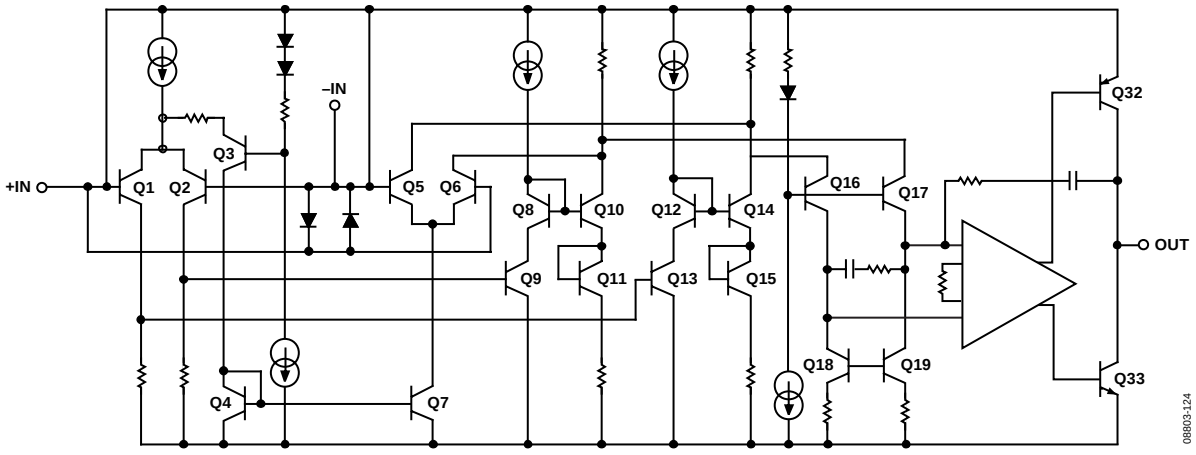


Figure 48. Simplified Schematic Without Input Protection (See Figure 49)

INPUT OVERVOLTAGE PROTECTION

The ADA4092-4 has two different ESD circuits for enhanced protection, as shown in Figure 49.

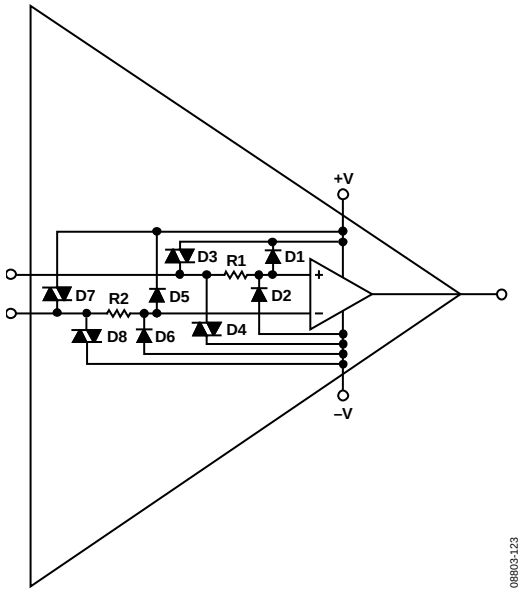


Figure 49. Complete Input Protection Network

One circuit is a series resistor of 5 kΩ to the internal inputs and diodes (D1 and D2 or D5 and D6) from the internal inputs to the supply rails. The other protection circuit is a circuit with two DIACs (D3 and D4 or D7 and D8) to the supply rails. A DIAC can be considered a bidirectional Zener diode with a transfer characteristic, as shown in Figure 50.

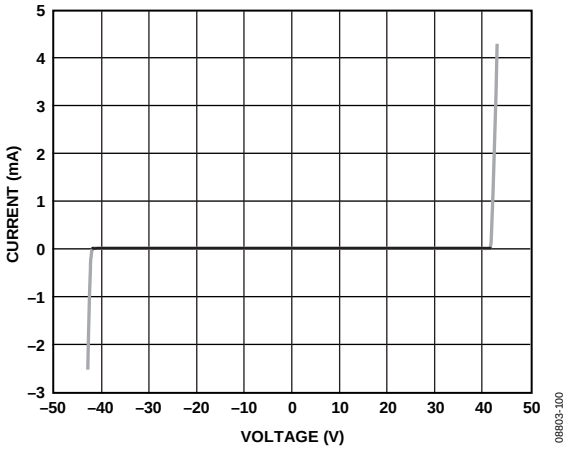


Figure 50. DIAC Transfer Characteristic

For a worst-case design analysis, consider two cases. The ADA4092-4 has a normal ESD structure from the internal op amp inputs to the supply rails. In addition, it has 42 V DIACs from the external inputs to the rails, as shown in Figure 48.

Therefore, consider two conditions to determine which case is the limiting factor.

1. Consider, for example, that when operating on ±15 V, the inputs can go +42 V above the negative supply rail. With the −V pin equal to −15 V, +42 V above this supply (the negative supply) is +27 V.
2. There is a restriction on the input current of 5 mA through a 5 kΩ resistor to the ESD structure to the positive rail. In the first condition, +27 V through the 5 kΩ resistor to +15 V gives a current of 2.4 mA. Thus, the DIAC is the limiting factor. If the ADA4092-4 supply voltages are changed to ±5 V, then −5 V + 42 V = +37 V. However, +5 V + (5 kΩ × 5 mA) = 30 V. Thus, the normal resistor diode structure is the limitation when running on lower supply voltages.

Additional resistance can be added externally in series with each input to protect against higher peak voltages; however, the additional thermal noise of the resistors must be considered.

The flatband voltage noise of the ADA4092-4 is approximately 25 nV/√Hz, and a 5 kΩ resistor has a noise of 9 nV/√Hz. Adding an additional 5 kΩ resistor increases the total noise by less than 15% root sum square (rss). Therefore, maintain resistor values below this value (5 kΩ) when overall noise performance is critical.

Note that this represents input protection under abnormal conditions only. The correct amplifier operation input voltage range (IVR) is specified in Table 2, Table 3, and Table 4.

COMPARATOR OPERATION

Although op amps are quite different from comparators, occasionally an unused section of a dual or a quad op amp can be pressed into service as a comparator; however, this is not recommended. For rail-to-rail output op amps, the output stage is generally a ratioed current mirror with bipolar or MOSFET transistors. With the part operating open loop, the second stage increases the current drive to the ratioed mirror to close the loop, but it cannot, which results in an increase in supply current. With three of the op amps operating normally and the fourth one in comparator mode, the supply current increases by about 200 μA (see Figure 51).

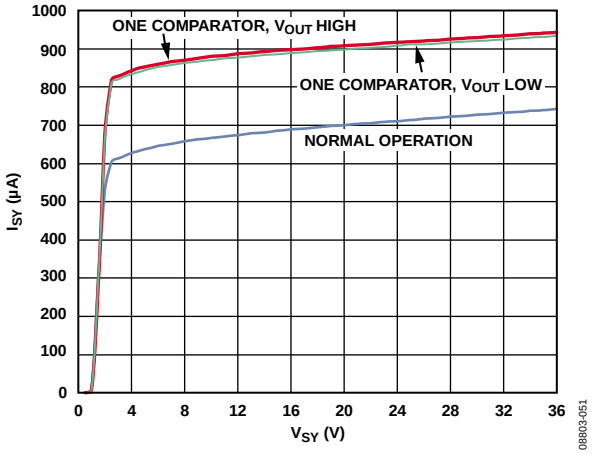
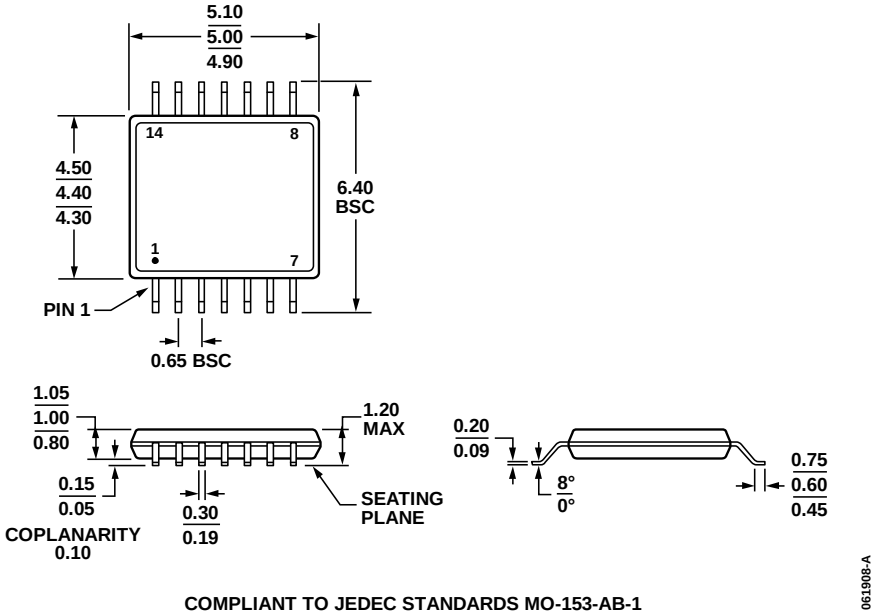


Figure 51. Comparator Supply Current

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-153-AB-1

Figure 52. 14-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-14)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADA4092-4ARUZ	−40°C to +125°C	14-Lead Thin Shrink Small Outline Package [TSSOP]	RU-14
ADA4092-4ARUZ-RL	−40°C to +125°C	14-Lead Thin Shrink Small Outline Package [TSSOP]	RU-14

[1] Z = RoHS Compliant Part.

NOTES

NOTES

NOTES

D08803-0-6/11(B)

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