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January 2014

NC7SZ125 TinyLogic[®] UHS Buffer with Three-State Output

Features

- Ultra-High Speed: t_{PD} 2.6 ns (Typical) into 50 pF at 5 V V_{CC}
- High Output Drive: ±24 mA at 3 V V_{CC}
- Broad V_{CC} Operating Range: 1.65 V to 5.5 V
- Matches Performance of LCX Operated at 3.3 V V_{CC}
- Power Down High-Impedance Inputs/Outputs
- Over-Voltage Tolerance Inputs Facilitate 5 V to 3 V Translation
- Proprietary Noise/EMI Reduction Circuitry
- Ultra-Small MicroPak™ Packages
- Space-Saving SOT23 and SC70 Packages

Description

The NC7SZ125 is a single buffer with three-state output from Fairchild's Ultra-High Speed (UHS) of TinyLogic $^{\otimes}$. The device is fabricated with advanced CMOS technology to achieve ultra high speed with high output drive while maintaining low static power dissipation over a very broad $V_{\rm CC}$ operating range. The device is specified to operate over the 1.65 V to 5.5 V range. The inputs and output are high impedance above ground when $V_{\rm CC}$ is 0 V. Inputs tolerate voltages up to 6 V independent of $V_{\rm CC}$ operating voltage. The output tolerates voltages above $V_{\rm CC}$ when in the 3-STATE condition.

Ordering Information

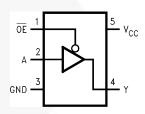
Part Number	t Number Top Mark Package		Packing Method
NC7SZ125M5X	7Z25	5-Lead SOT23, JEDEC MO-178 1.6 mm	3000 Units on Tape & Reel
NC7SZ125P5X	Z25	5-Lead SC70, EIAJ SC-88a, 1.25 mm Wide	3000 Units on Tape & Reel
NC7SZ125L6X	DD	6-Lead MicroPak™, 1.00 mm Wide	5000 Units on Tape & Reel
NC7SZ125FHX	DD	6-Lead, MicroPak2, 1x1 mm Body, .35mm Pitch	5000 Units on Tape & Reel

Connection Diagrams



Figure 1. Logic Symbol

Pin Configurations





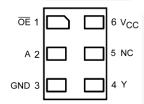


Figure 3. MicroPak™ (Top Through View)

Pin Definitions

Pin # SC70 / SOT23	Pin # MicroPak	Name	Description
1	1	OE	Input
2	2	A	Input
3	3	GND	Ground
4	4	Υ	Output
5	6	V _{CC}	Supply Voltage
\(\frac{1}{2}\)	5	NC	No Connect

Function Table

In	puts	Output
/OE	In A	Out Y
L	L	r r
L	Н	Н
Н	X	Z

H = HIGH Logic Level

L = LOW Logic Level

X = HIGH or LOW Logic Level

Z = HIGH Impedance State

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter			Min.	Max.	Unit	
V _{CC}	Supply Voltage			-0.5	6.0	V	
V _{IN}	DC Input Voltage			-0.5	6.0	V	
V _{OUT}	DC Output Voltage			-0.5	6.0	V	
	DC Input Diada Current	V _{IN} < -0.5	5 V		-50	mA	
I _{IK}	DC Input Diode Current	$V_{IN} > 6.0$	V		+20	IIIA	
	DC Output Diada Current	V _{OUT} < -0	.5 V		-50	mA	
I _{OK}	DC Output Diode Current	V _{OUT} > 6	V _{OUT} > 6 V, V _{CC} =GND		+20	IIIA	
I _{OUT}	DC Output Current	DC Output Current		(±50	mA	
I _{CC} or I _{GND}	DC V _{CC} or Ground Current				±50	mA	
T _{STG}	Storage Temperature Range			-65	+150	°C	
T_J	Junction Temperature Under Bia	IS			+150	°C	
T_L	Junction Lead Temperature (Sol	dering, 10 Second	s)		+260	°C	
- /-		SOT-23			200		
Б	Device Discipation at 19590	SC70-5	SC70-5		150	\/	
P_D	Power Dissipation at +85°C	MicroPak	c-6		130	mW	
		MicroPak	MicroPak2-6		120		
ESD	Human Body Model, JESD22-A1	114			4000	V	
ESD	Charged Device Model, JESD22	-C101			2000	V	

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Conditions	Min.	Max.	Unit	
\/	Supply Voltage Operating		1.65	5.50	V	
V _{CC}	Supply Voltage Data Retention		1.50	5.50	7 v	
V _{IN}	Input Voltage		0	5.5	V	
M	Output Voltage	Active State	0	V _{CC}	V	
V _{OUT}	Output Voltage	Three-State	0	5.5	V	
T _A	Operating Temperature		-40	+85	°C	
		V _{CC} at 1.8 V, 2.5 V ±0.2 V	0	20	K 1	
t_r , t_f	Input Rise and Fall Times	V _{CC} at 3.3 V ±0.3 V	0	10	ns/V	
		V _{CC} at 5.0 V ±0.5 V	0	5		
		SOT-23		300		
0	The arrest Designation	SC70-5		425	°C/W	
θ_{JA}	Thermal Resistance	MicroPak-6		500		
		MicroPak2-6		560		

Note:

1. Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

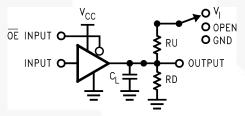
Comple at	Danamatan	. , .	O a maliti a ma	T,	$T_A=+25$ °C			T _A =-40 to +85°C	
Symbol	mbol Parameter	V _{cc} Conditions		Min.	Тур.	Max.	Min.	Max.	Units
.,	HIGH Level	1.65 to 1.95		0.75V _{CC}			0.75V _{CC}		.,
V_{IH}	Input Voltage	2.30 to 5.50		0.70V _{CC}			0.70V _{CC}		V
.,	LOW Level Input	1.65 to 1.95				0.25V _{CC}		0.25V _{CC}	.,
V_{IL}	Voltage	2.30 to 5.50				0.30V _{CC}		0.30V _{CC}	V
		1.65		1.55	1.65		1.55		
		1.80		1.70	1.80		1.70		
		2.30	V _{IN} =V _{IH} , I _{OH} =-100 μA	2.20	2.30		2.20		V
		3.00		2.90	3.00		2.90		
1/	HIGH Level	4.50		4.40	4.50		4.40		
V_{OH}	Output Voltage	1.65	I _{OH} =-4 mA	1.29	1.52		1.29		
		2.30	I _{OH} =-8 mA	1.90	2.15	Á	1.90		
		3.00	I _{OH} =-16 mA	2.40	2.80		2.40		
		3.00	I _{OH} =-24 mA	2.30	2.68	leg-	2.30		
		4.50	I _{OH} =-32 mA	3.80	4.20		3.80		
	1.65			0.00	0.10		0.00		
		1.80			0.00	0.10		0.10	
		2.30	$V_{IN}=V_{IL}$, $I_{OL}=100 \mu A$		0.00	0.10	¥!	0.10	
	1/	3.00			0.00	0.10		0.10	
	LOW Level	4.50			0.00	0.10		0.10	.,
V_{OL}	Output Voltage	1.65	I _{OL} =4 mA		0.80	0.24		0.24	V
		2.30	I _{OL} =8 mA		0.10	0.30		0.30	
		3.00	I _{OL} =16 mA		0.15	0.40		0.40	
		3.00	I _{OL} =24 mA		0.22	0.55		0.55	
		4.50	I _{OL} =32 mA		0.22	0.55		0.55	
I _{IN}	Input Leakage Current	0 to 5.5	0 ≥ V _{IN} ≥ 5.5 V			±1		±10	μΑ
l _{oz}	3-STATE Output Leakage	0 to 5.5	$V_{IN}=V_{IH} \text{ or } V_{IL}$ $0 \ge V_O \ge 5.5 \text{ V}$			±1	A	±10	μA
I _{OFF}	Power Off Leakage Current	0	V _{IN} or V _{OUT} =5.5 V			1		10	μA
I _{cc}	Quiescent Supply Current	1.65 to 5.50	V _{IN} =5.5 V, GND			2		20	μA

AC Electrical Characteristics

Compleal	Danamatan	Parameter V Condit		T _A =+25°C		T _A =-40 to +85°C		Units	Ciaura	
Symbol Parameter		V _{cc}	Conditions	Min.	Тур.	Max.	Min.	Max.	Units	Figure
		1.65		2.0	6.4	13.2	2.0	13.8		
		1.80	C _L =15 pF,	2.0	5.3	11.0	2.0	11.5		
		2.50 ±0.20	$R_D=1 M\Omega$	8.0	3.4	7.5	0.8	8.0		
t _{PLH} ,t _{PHL}	Propagation Delay	3.30 ±0.30	S ₁ =OPEN	0.5	2.5	5.2	0.5	5.5	ns	Figure 4
*FLN, *FNL	. ropaganon zonaj	5.00 ±0.50		0.5	2.1	4.5	0.5	4.8		Figure 6
		3.30 ±0.30	C _L =50 pF,	1.5	3.2	5.7	1.5	6.0		
		5.00 ±0.50	$R_D=500 \Omega$ $S_1=OPEN$	0.8	2.6	5.0	0.8	5.3		
		1.65	$\begin{array}{c} \text{C}_\text{L} \! = \! 50 \text{ pF}, \\ \text{R}_\text{D} \! = \! 500 \ \Omega \\ \text{RU} \! = \! 500 \ \Omega \\ \text{S}_1 \! = \! \text{GND for } t_{\text{PZH}} \\ \text{S}_1 \! = \! V_{\text{IN}} \text{for } t_{\text{PZL}} \\ V_{\text{IN}} \! = \! 2 \text{-} V_{\text{CC}} \end{array}$	2.0	8.4	15.0	2.0	15.6	ns	
		1.80		2.0	7.0	12.5	2.0	13.0		
$t_{PZL,}t_{PZH}$	Output Enable Time	2.50 ±0.20		1.5	4.6	8.5	1.5	9.0		
		3.30 ±0.30		1.5	3.5	6.2	1.5	6.5		
		5.00 ±0.50		0.8	2.8	5.5	0.8	5.8		Figure 4
		1.65	C _L =50 pF,	2.0	6.5	13.2	2.0	14.5	115	Figure 6
		1.80	R _D =500 Ω	2.0	5.4	11.0	2.0	12.0		
$t_{PLZ,}t_{PHZ}$	Output Disable Time	2.50 ±0.20	RU=500 Ω S ₁ =GND for t _{PHZ}	1.5	3.5	8.0	1.5	8.5		
		3.30 ±0.30	$S_1 = V_{IN}$ for t_{PLZ}	1.0	2.8	5.7	1.0	6.0		
			V _{IN} =2•V _{CC}	0.5	2.1	4.7	0.5	5.0		
C _{IN}	Input Capacitance	0.00			4				pF	
C_OUT	Output Capacitance	0.00			8					
<u></u>	Power Dissipation	3.30			17				, F	
C _{PD}	Capacitance ⁽²⁾	5.00			24				pF	Figure 5

Note:

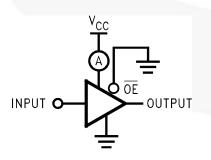
2. C_{PD} is defined as the value of the internal equivalent capacitance which is derived from dynamic operating current consumption (I_{CCD}) at no output lading and operating at 50% duty cycle. C_{PD} is related to I_{CCD} dynamic operating current by the expression: I_{CCD}=(C_{PD})(V_{CC})(f_{IN})+(I_{CC}static).



Note:

3. C_L includes load and stray capacitance. Input PRR=1.0 MHz, t_W =500 ns.

Figure 4. AC Test Circuit



Note:

 Input=AC Waveform; t_r=t_f=1.8 ns; PRR=10 MHz; Duty Cycle=50%.

Figure 5. I_{CCD} Test Circuit

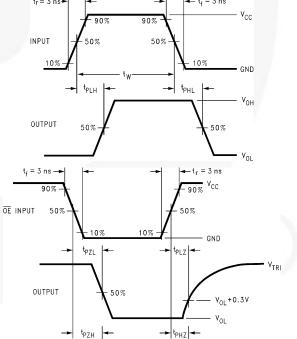


Figure 6. AC Waveforms

OUTPUT

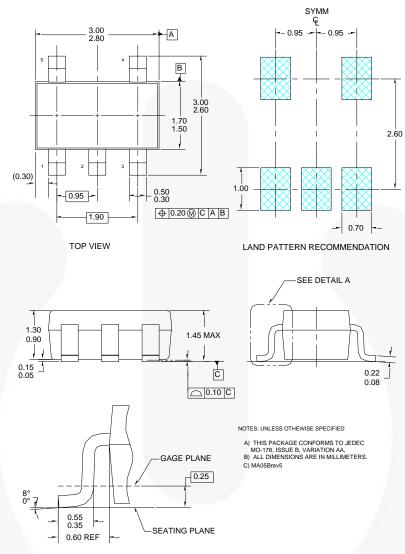


Figure 7. 5-Lead SOT23, JEDEC MO-178 1.6 mm

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Tape and Reel Specifications

Please visit Fairchild Semiconductor's online packaging area for the most recent tape and reel specifications: http://www.fairchildsemi.com/packaging/SOT23-5L_tr.pdf.

Package Designator Tape Section		Cavity Number	Cavity Status	Cover Type Status
	Leader (Start End)	125 (Typical)	Empty	Sealed
M5X	Carrier	3000	Filled	Sealed
	Trailer (Hub End)	75 (Typical)	Empty	Sealed

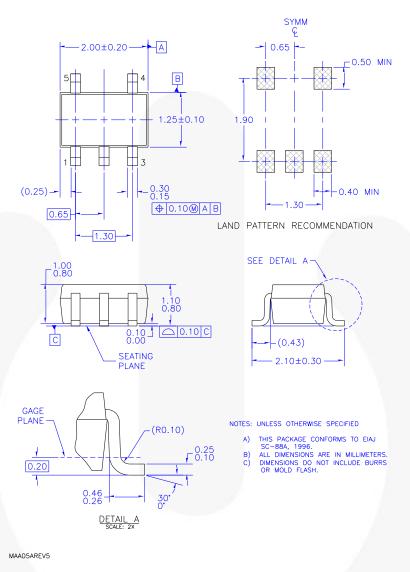


Figure 8. 5-Lead, SC70, EIAJ SC-88a, 1.25 mm Wide

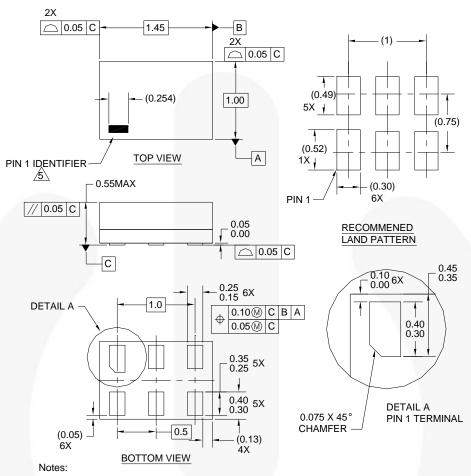
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Package Designator	Tape Section	Cavity Number	Cavity Status	Cover Type Status
	Leader (Start End)		Empty	Sealed
P5X	Carrier	3000	Filled	Sealed
	Trailer (Hub End)	75 (Typical)	Empty	Sealed



- 1. CONFORMS TO JEDEC STANDARD M0-252 VARIATION UAAD
- 2. DIMENSIONS ARE IN MILLIMETERS
- 3. DRAWING CONFORMS TO ASME Y14.5M-1994
- 4. FILENAME AND REVISION: MAC06AREV4
- 5. PIN ONE IDENTIFIER IS 2X LENGTH OF ANY

OTHER LINE IN THE MARK CODE LAYOUT.

Figure 9. 6-Lead, MicroPak™, 1.0 mm Wide

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Package Designator	Tape Section	Cavity Number	Cavity Status	Cover Type Status	
	Leader (Start End)		Empty	Sealed	
L6X	Carrier	5000	Filled	Sealed	
	Trailer (Hub End)	75 (Typical)	Empty	Sealed	

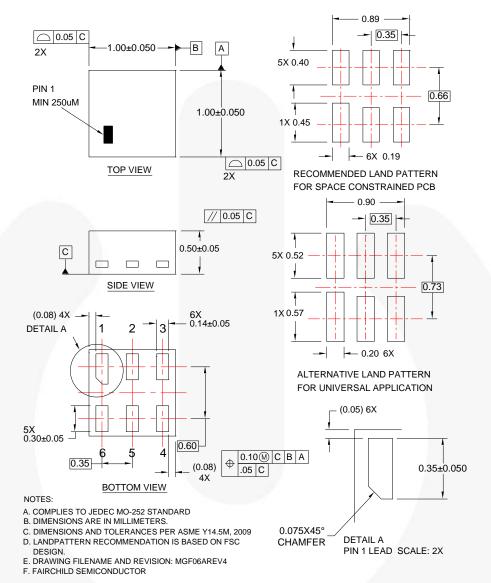


Figure 10. 6-Lead, MicroPak2, 1x1 mm Body, .35 mm Pitch

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Tape and Reel Specifications

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Package Designator Tape Sect		Cavity Number	Cavity Status	Cover Type Status
	Leader (Start End)	125 (Typical)	Empty	Sealed
FHX	Carrier	5000	Filled	Sealed
	Trailer (Hub End)	75 (Typical)	Empty	Sealed





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