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FDB9406_F085

N-Channel PowerTrench® MOSFET

40 V, 110 A, 1.8 mΩ

June 2014

Features

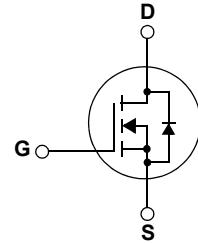
- Typ $R_{DS(on)} = 1.31\text{m}\Omega$ at $V_{GS} = 10\text{V}$, $I_D = 80\text{A}$
- Typ $Q_{g(\text{tot})} = 107\text{nC}$ at $V_{GS} = 10\text{V}$, $I_D = 80\text{A}$
- UIS Capability
- RoHS Compliant
- Qualified to AEC Q101

Applications

- Automotive Engine Control
- Powertrain Management
- Solenoid and Motor Drivers
- Electronic Steering
- Integrated Starter/Alternator
- Distributed Power Architectures and VRM
- Primary Switch for 12V Systems



TO-263
FDB SERIES



For current package drawing, please refer to the Fairchild website at www.fairchildsemi.com/packaging

MOSFET Maximum Ratings $T_J = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Ratings	Units
V_{DSS}	Drain to Source Voltage	40	V
V_{GS}	Gate to Source Voltage	± 20	V
I_D	Drain Current - Continuous ($V_{GS}=10$) (<i>Note 1</i>)	110	A
	Pulsed Drain Current	See Figure4	
E_{AS}	Single Pulse Avalanche Energy	(<i>Note 2</i>)	mJ
P_D	Power Dissipation	176	W
	Derate above 25°C	1.18	$\text{W}/^\circ\text{C}$
T_J , T_{STG}	Operating and Storage Temperature	-55 to + 175	$^\circ\text{C}$
$R_{\theta JC}$	Thermal Resistance, Junction to Case	0.85	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Maximum Thermal Resistance, Junction to Ambient	(<i>Note 3</i>)	$^\circ\text{C}/\text{W}$

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDB9406	FDB9406_F085	D2-PAK(TO-263)	330mm	24mm	800 units

Notes:

- 1: Current is limited by bondwire configuration.
- 2: Starting $T_J = 25^\circ\text{C}$, $L = 0.045\text{mH}$, $I_{AS} = 88\text{A}$, $V_{DD} = 40\text{V}$ during inductor charging and $V_{DD} = 0\text{V}$ during time in avalanche.
- 3: $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design. The maximum rating presented here is based on mounting on a 1 in² pad of 2oz copper.

Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
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Off Characteristics

B_{VDSS}	Drain-to-Source Breakdown Voltage	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}$	40	-	-	V
I_{DSS}	Drain-to-Source Leakage Current	$V_{DS} = 40\text{V}, T_J = 25^\circ\text{C}$	-	-	1	μA
		$V_{GS} = 0\text{V}, T_J = 175^\circ\text{C}$ (Note 4)	-	-	1	mA
I_{GSS}	Gate-to-Source Leakage Current	$V_{GS} = \pm 20\text{V}$	-	-	± 100	nA

On Characteristics

$V_{GS(\text{th})}$	Gate-to-Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$	2.0	2.83	4.0	V
$R_{DS(\text{on})}$	Drain-to-Source On Resistance	$I_D = 80\text{A}, T_J = 25^\circ\text{C}$	-	1.31	1.8	$\text{m}\Omega$
		$V_{GS} = 10\text{V}, T_J = 175^\circ\text{C}$ (Note 4)	-	2.2	2.8	$\text{m}\Omega$

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 25\text{V}, V_{GS} = 0\text{V}, f = 1\text{MHz}$	-	7710	-	pF
C_{oss}	Output Capacitance		-	2015	-	pF
C_{rss}	Reverse Transfer Capacitance		-	140	-	pF
R_g	Gate Resistance	$f = 1\text{MHz}$	-	2.7	-	Ω
$Q_{g(\text{ToT})}$	Total Gate Charge at 10V	$V_{GS} = 0 \text{ to } 10\text{V}$	-	107	138	nC
$Q_{g(\text{th})}$	Threshold Gate Charge	$V_{GS} = 0 \text{ to } 2\text{V}$	-	14	19	nC
Q_{gs}	Gate-to-Source Gate Charge	$I_D = 80\text{A}$	-	33	-	nC
Q_{gd}	Gate-to-Drain "Miller" Charge		-	18	-	nC

Switching Characteristics

t_{on}	Turn-On Time	$V_{DD} = 20\text{V}, I_D = 80\text{A}, V_{GS} = 10\text{V}, R_{\text{GEN}} = 6\Omega$	-	-	160	ns
$t_{d(on)}$	Turn-On Delay		-	32	-	ns
t_r	Rise Time		-	81	-	ns
$t_{d(off)}$	Turn-Off Delay		-	50	-	ns
t_f	Fall Time		-	23	-	ns
t_{off}	Turn-Off Time		-	-	93	ns

Drain-Source Diode Characteristics

V_{SD}	Source-to-Drain Diode Voltage	$I_{SD} = 80\text{A}, V_{GS} = 0\text{V}$	-	-	1.25	V
t_{rr}	Reverse-Recovery Time	$I_F = 80\text{A}, dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	85	110	ns
		$V_{DD} = 32\text{V}$	-	122	160	nC

Note:

4: The maximum value is specified by design at $T_J = 175^\circ\text{C}$. Product is not tested to this condition in production.

Typical Characteristics

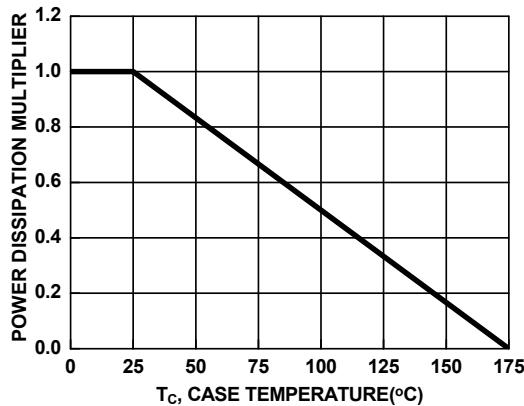


Figure 1. Normalized Power Dissipation vs. Case Temperature

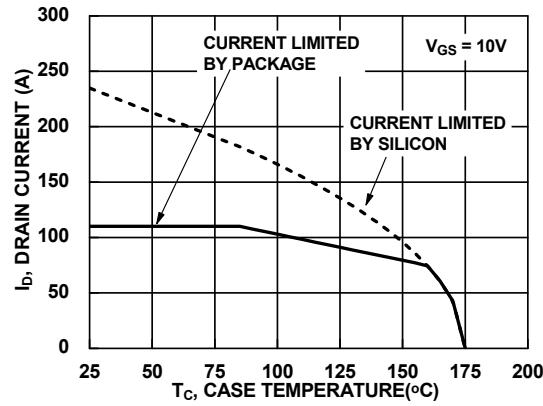


Figure 2. Maximum Continuous Drain Current vs. Case Temperature

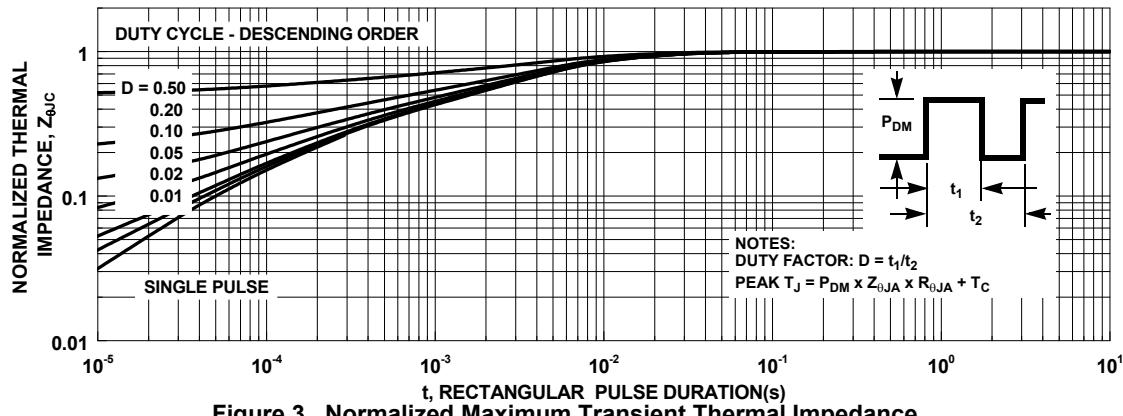


Figure 3. Normalized Maximum Transient Thermal Impedance

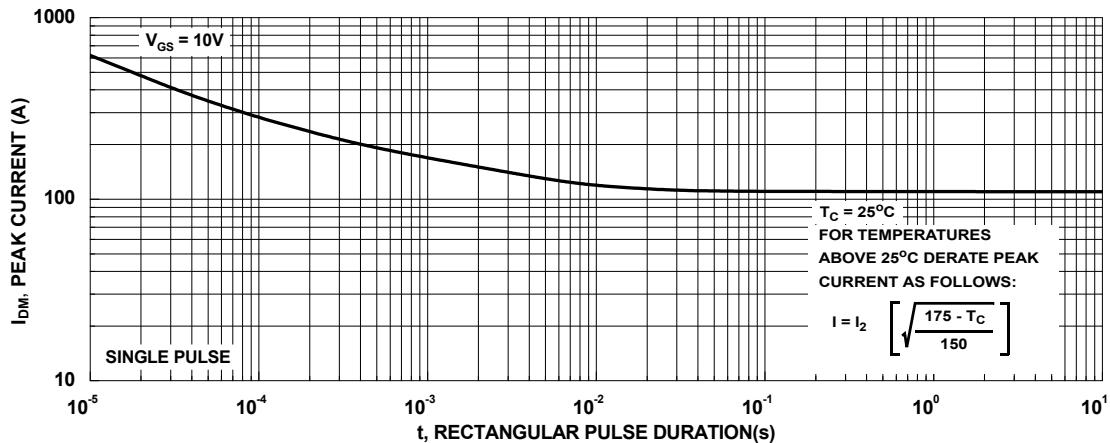


Figure 4. Peak Current Capability

Typical Characteristics

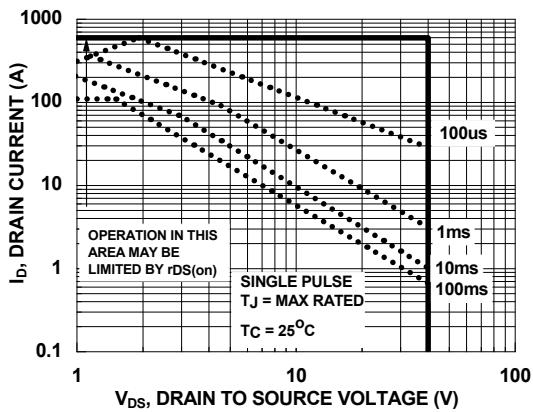
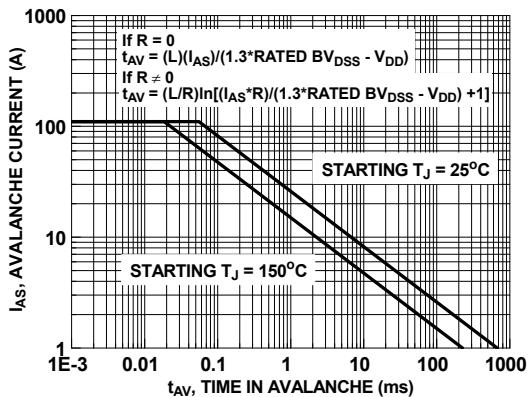


Figure 5. Forward Bias Safe Operating Area



NOTE: Refer to Fairchild Application Notes AN7514 and AN7515

Figure 6. Unclamped Inductive Switching Capability

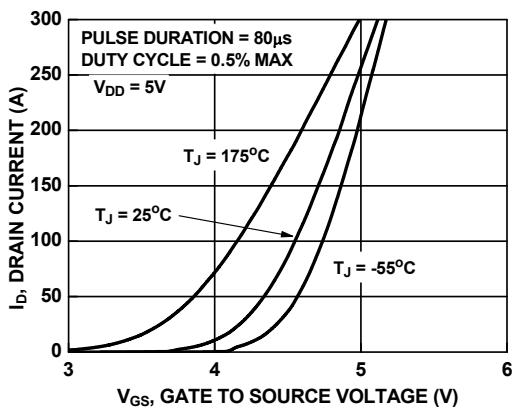


Figure 7. Transfer Characteristics

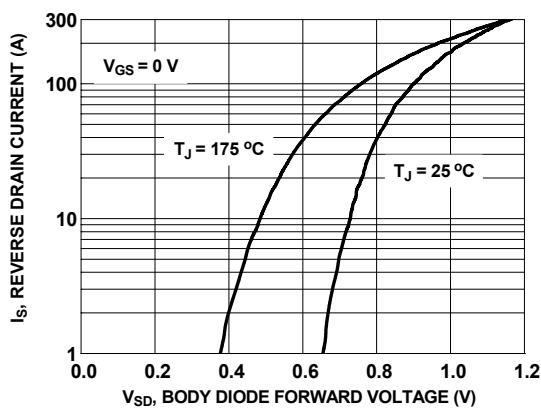


Figure 8. Forward Diode Characteristics

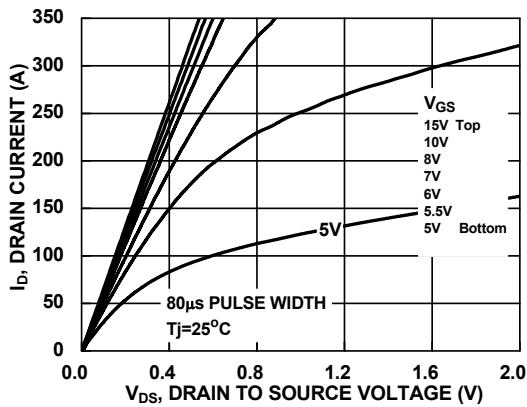


Figure 9. Saturation Characteristics

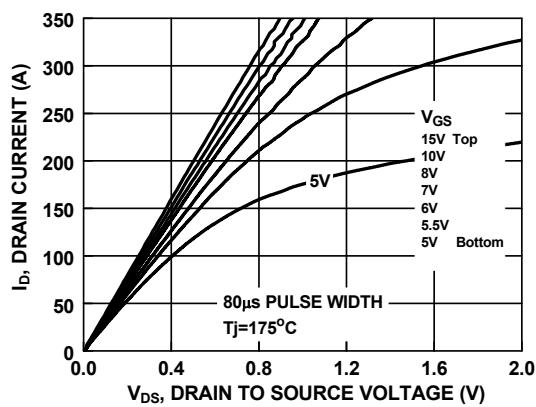


Figure 10. Saturation Characteristics

Typical Characteristics

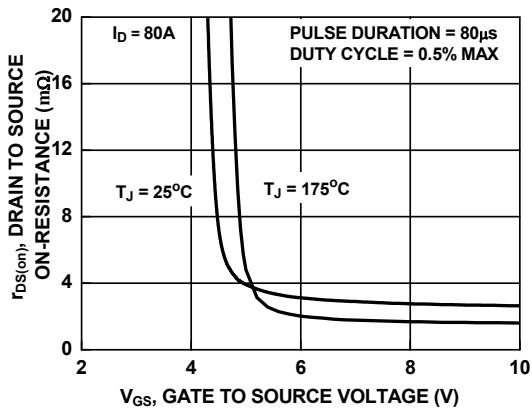


Figure 11. $R_{DS(on)}$ vs. Gate Voltage

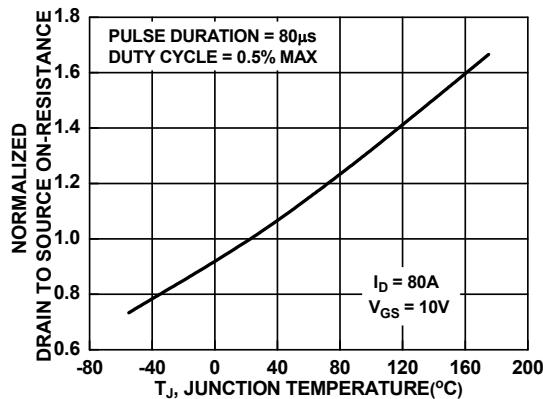


Figure 12. Normalized $R_{DS(on)}$ vs. Junction Temperature

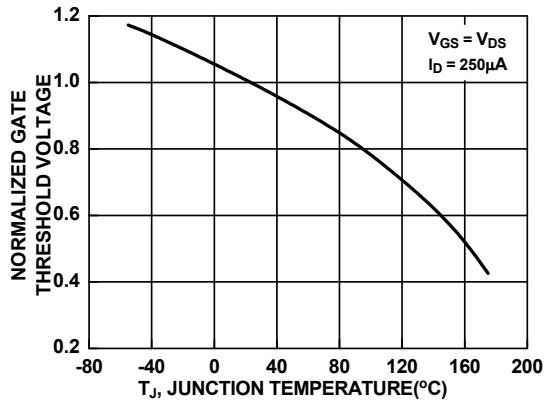


Figure 13. Normalized Gate Threshold Voltage vs. Temperature

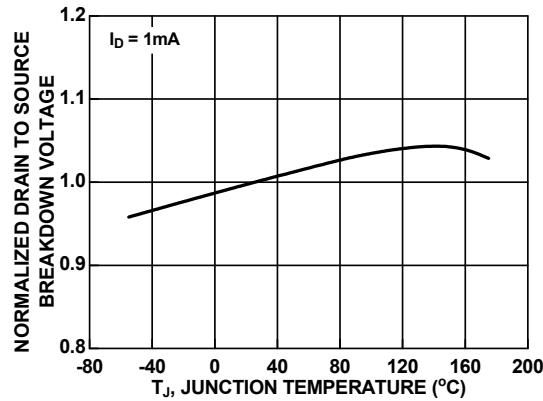


Figure 14. Normalized Drain to Source Breakdown Voltage vs. Junction Temperature

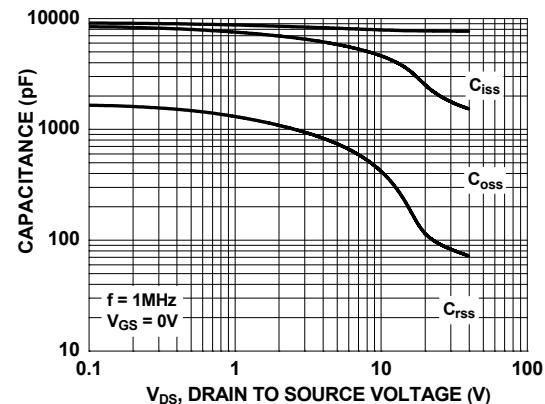


Figure 15. Capacitance vs. Drain to Source Voltage

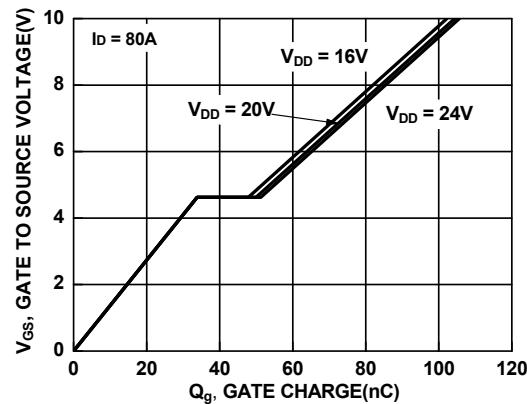


Figure 16. Gate Charge vs. Gate to Source Voltage



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