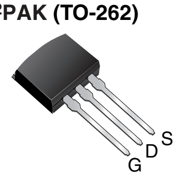
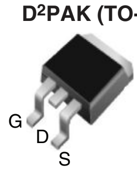
Power MOSFET

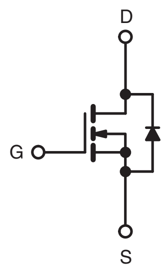
PRODUCT SUMMARY		
V_{DS} (V)	400	
$R_{DS(on)}$ (Max.) (Ω)	V_{GS} = 10 V	1.0
Q_g (Max.) (nC)	22	
Q_{gs} (nC)	5.8	
Q_{gd} (nC)	9.3	
Configuration	Single	

I²PAK (TO-262)



D²PAK (TO-263)





N-Channel MOSFET

FEATURES

- **Halogen-free According to IEC 61249-2-21 Definition**
- Low Gate Charge Q_g Results in Simple Drive Requirement
- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness
- Fully Characterized Capacitance and Avalanche Voltage and Current
- Effective C_{oss} Specified
- Compliant to RoHS Directive 2002/95/EC

RoHS* COMPLIANT

HALOGEN FREE Available

APPLICATIONS

- Switch Mode Power Supply (SMPS)
- Uninterruptible Power Supply
- High Sspeed Power Switching

TYPICAL SMPS TOPOLOGIES

- Single Transistor Flyback Xfmr. Reset
- Single Transistor Forward Xfmr. Reset (Both US Line Input Only)

ORDERING INFORMATION				
Package	D²PAK (TO-263)	D²PAK (TO-263)	D²PAK (TO-263)	I²PAK (TO-262)
Lead (Pb)-free and Halogen-free	SiHF730AS-GE3	SiHF730ASTRL-GE3[a]	SiHF730ASTRR-GE3[a]	SiHF730AL-GE3
Lead (Pb)-free	IRF730ASPbF	IRF730ASTRLPbF[a]	IRF730ASTRRPbF[a]	IRF730ALPbF
	SiHF730AS-E3	SiHF730ASTL-E3[a]	SiHF730ASTR-E3[a]	SiHF730AL-E3

Note

a. See device orientation.

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)

PARAMETER			SYMBOL	LIMIT	UNIT
Drain-Source Voltage			V_{DS}	400	V
Gate-Source Voltage			V_{GS}	± 30	
Continuous Drain Current	V_{GS} at 10 V	T_C = 25 °C	I_D	5.5	A
		T_C = 100 °C		3.5	
Pulsed Drain Current[a, e]			I_{DM}	22	
Linear Derating Factor				0.6	W/°C
Single Pulse Avalanche Energy[b, e]			E_{AS}	290	mJ
Avalanche Current[a]			I_{AR}	5.5	A
Repetiitive Avalanche Energy[a]			E_{AR}	7.4	mJ
Maximum Power Dissipation	T_C = 25 °C		P_D	74	W
Peak Diode Recovery dV/dt[c, e]			dV/dt	4.6	V/ns
Operating Junction and Storage Temperature Range			T_J, T_{stg}	- 55 to + 150	°C
Soldering Recommendations (Peak Temperature)	for 10 s			300[d]	

Notes

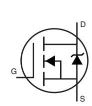
a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
b. Starting T_J = 25 °C, L = 19 mH, R_g = 25 Ω, I_{AS} = 5.5 A (see fig. 12).
c. $I_{SD} \leq$ 5.5 A, dI/dt ≤ 90 A/μs, $V_{DD} \leq V_{DS}$, $T_J \leq$ 150 °C.
d. 1.6 mm from case.
e. Uses IRF730A, SiHF730A data and test conditions.

* Pb containing terminations are not RoHS compliant, exemptions may apply

THERMAL RESISTANCE RATINGS				
PARAMETER	**SYMBOL**	**TYP.**	**MAX.**	**UNIT**
Maximum Junction-to-Ambient (PCB Mounted, steady-state)[a]	R_{thJA}	-	40	°C/W
Maximum Junction-to-Case (Drain)	R_{thJC}	-	1.7	

Note

a. When mounted on 1" square PCB (FR-4 or G-10 material).

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Static						
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0, I_D = 250 μA	400	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to 25 °C, I_D = 1 mA[d]	-	0.5	-	V/°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = 250 μA	2.0	-	4.5	V
Gate-Source Leakage	I_{GSS}	V_{GS} = ± 30 V	-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 400 V, V_{GS} = 0 V	-	-	25	μA
		V_{DS} = 320 V, V_{GS} = 0 V, T_J = 125 °C	-	-	250	
Drain-Source On-State Resistance	$R_{DS(on)}$	V_{GS} = 10 V; I_D = 3.3 A[b]	-	-	1.0	Ω
Forward Transconductance	g_{fs}	V_{DS} = 50 V, I_D = 3.3 A[d]	3.1	-	-	S
Dynamic						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1.0 MHz, see fig. 5[d]	-	600	-	pF
Output Capacitance	C_{oss}		-	103	-	
Reverse Transfer Capacitance	C_{rss}		-	4.0	-	
Output Capacitance	C_{oss}	V_{GS} = 0 V; V_{DS} = 1.0 V, f = 1.0 MHz	-	890	-	
		V_{GS} = 0 V; V_{DS} = 320 V, f = 1.0 MHz	-	30	-	
Effective Output Capacitance	C_{oss} eff.	V_{GS} = 0 V; V_{DS} = 0 V to 320 V[c, d]	-	45	-	
Total Gate Charge	Q_g	V_{GS} = 10 V; I_D = 3.5 A, V_{DS} = 320 V, see fig. 6 and 13[b, d]	-	-	22	nC
Gate-Source Charge	Q_{gs}		-	-	5.8	
Gate-Drain Charge	Q_{gd}		-	-	9.3	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 200 V, I_D = 3.5 A, R_g = 12 Ω, R_D = 57 Ω, see fig. 10[b, d]	-	10	-	ns
Rise Time	t_r		-	22	-	
Turn-Off Delay Time	$t_{d(off)}$		-	20	-	
Fall Time	t_f		-	16	-	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	5.5	A
Pulsed Diode Forward Current[a]	I_{SM}		-	-	22	
Body Diode Voltage	V_{SD}	T_J = 25 °C, I_S = 5.5 A, V_{GS} = 0 V[b]	-	-	1.6	V
Body Diode Reverse Recovery Time	t_{rr}	T_J = 25 °C, I_F = 3.5 A, dI/dt = 100 A/μs[b, d]	-	370	550	ns
Body Diode Reverse Recovery Charge	Q_{rr}		-	1.6	2.4	μC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)				

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
b. Pulse width ≤ 300 μs; duty cycle ≤ 2 %.
c. C_{oss} eff. is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DS}.
d. Uses IRF730A, SiHF730A data and test conditions.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

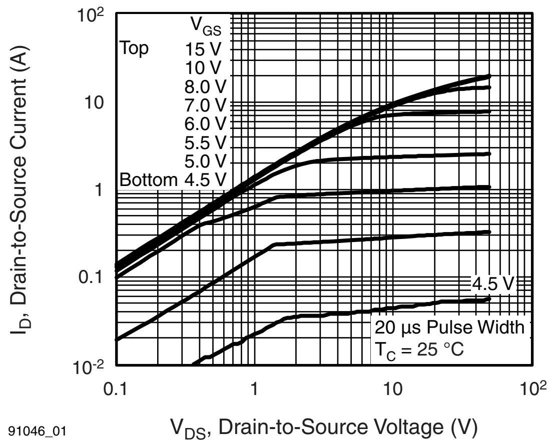


Fig. 1 - Typical Output Characteristics

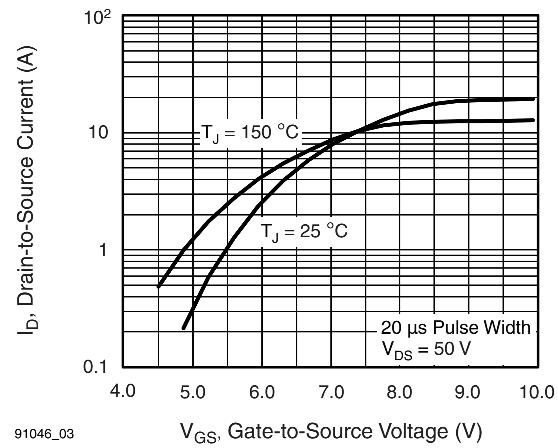


Fig. 3 - Typical Transfer Characteristics

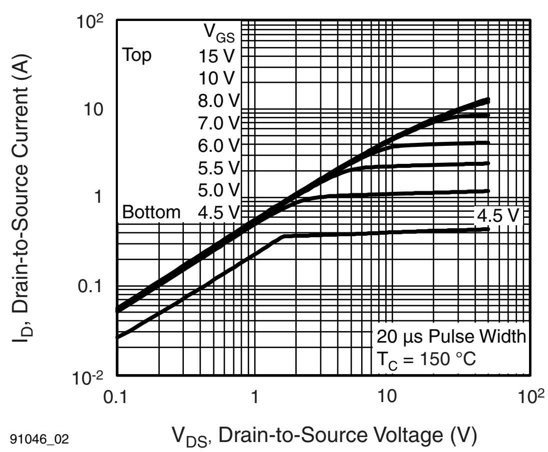


Fig. 2 - Typical Output Characteristics

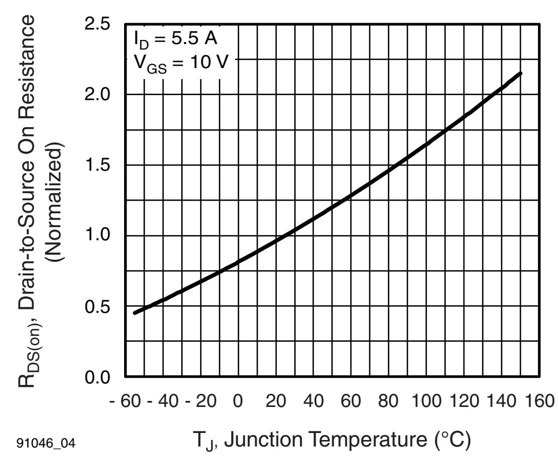


Fig. 4 - Normalized On-Resistance vs. Temperature

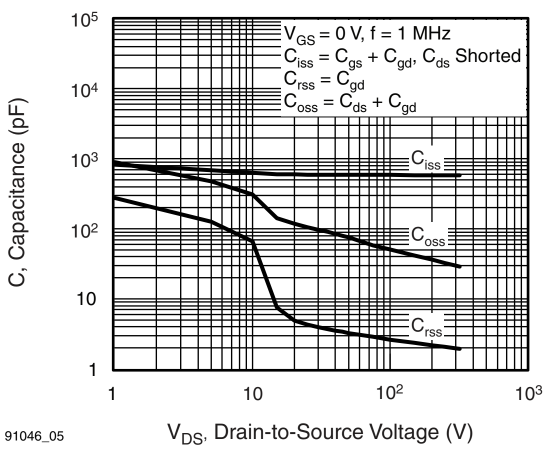


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

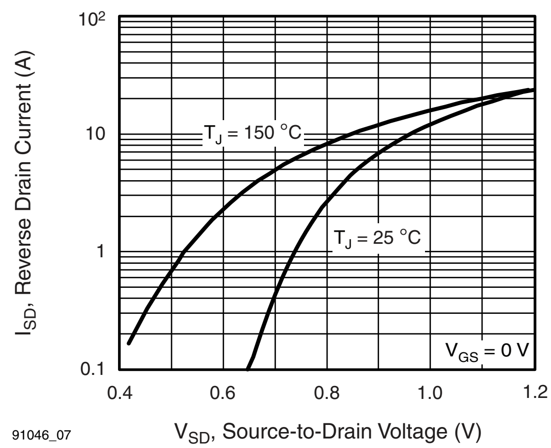


Fig. 7 - Typical Source-Drain Diode Forward Voltage

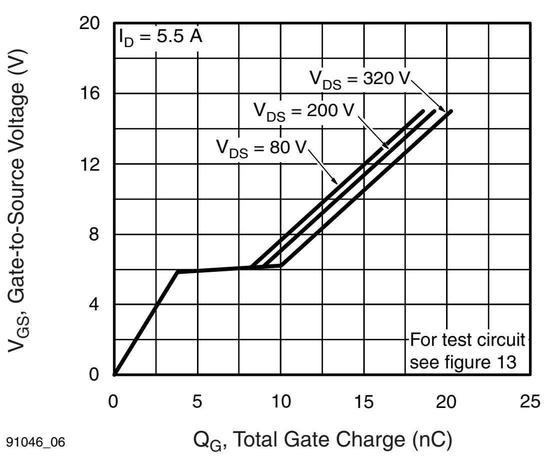


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

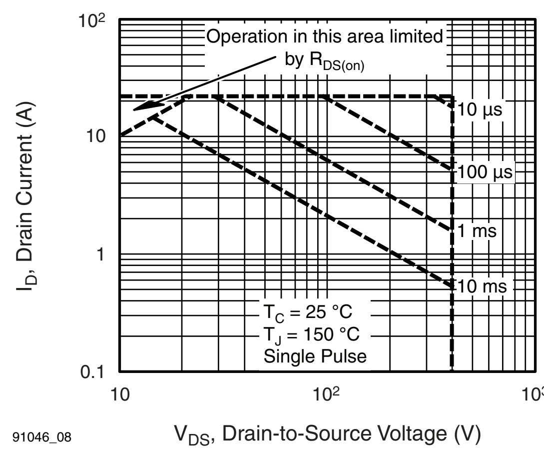


Fig. 8 - Maximum Safe Operating Area

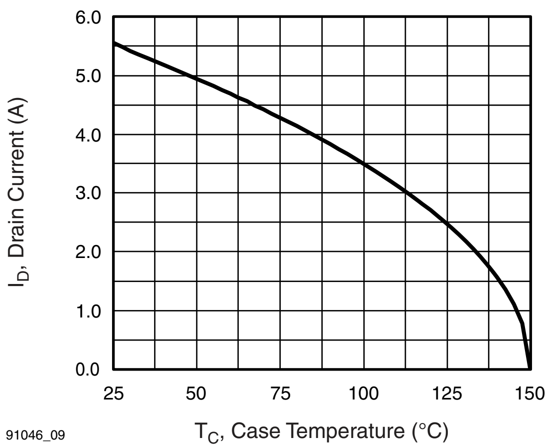


Fig. 9 - Maximum Drain Current vs. Case Temperature

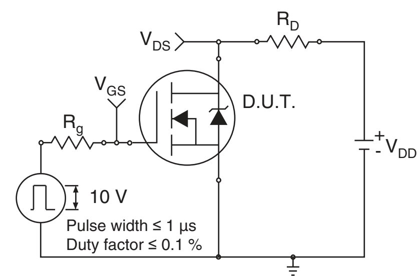


Fig. 10a - Switching Time Test Circuit

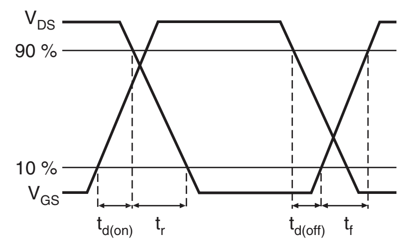


Fig. 10b - Switching Time Waveforms

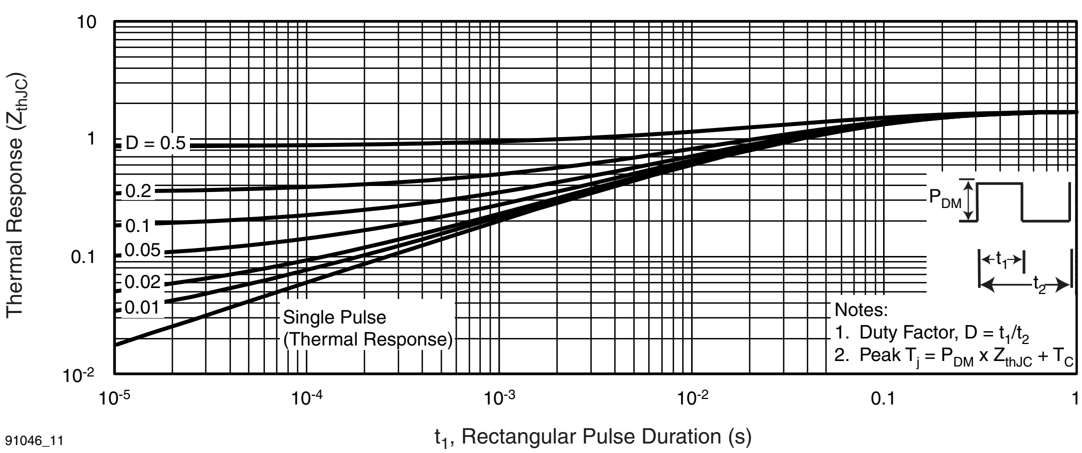


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

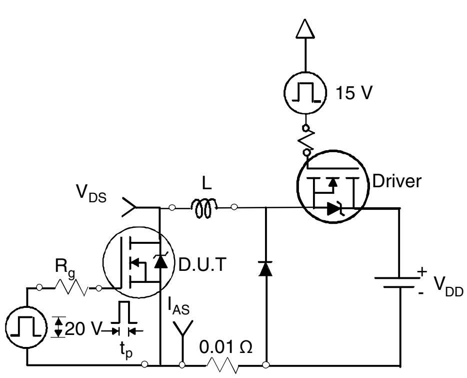


Fig. 12a - Unclamped Inductive Test Circuit

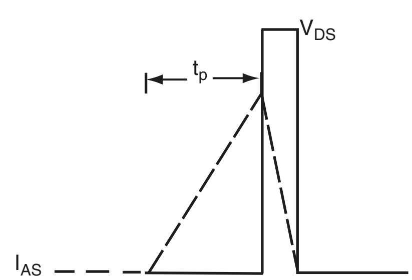


Fig. 12b - Unclamped Inductive Waveforms

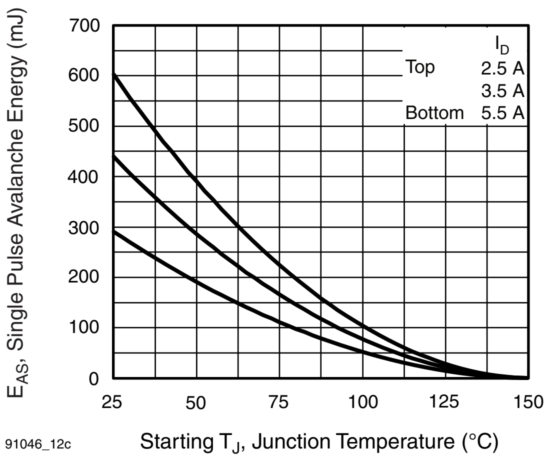


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

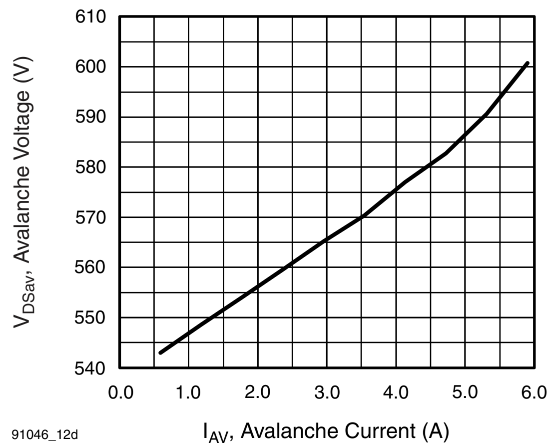


Fig. 12d - Typical Drain-to-Source Voltage vs. Avalanche Current

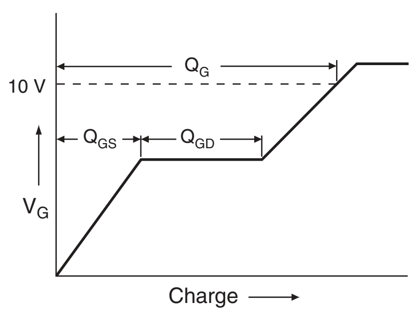


Fig. 13a - Maximum Avalanche Energy vs. Drain Current

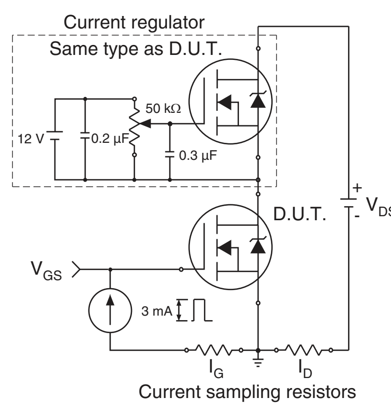
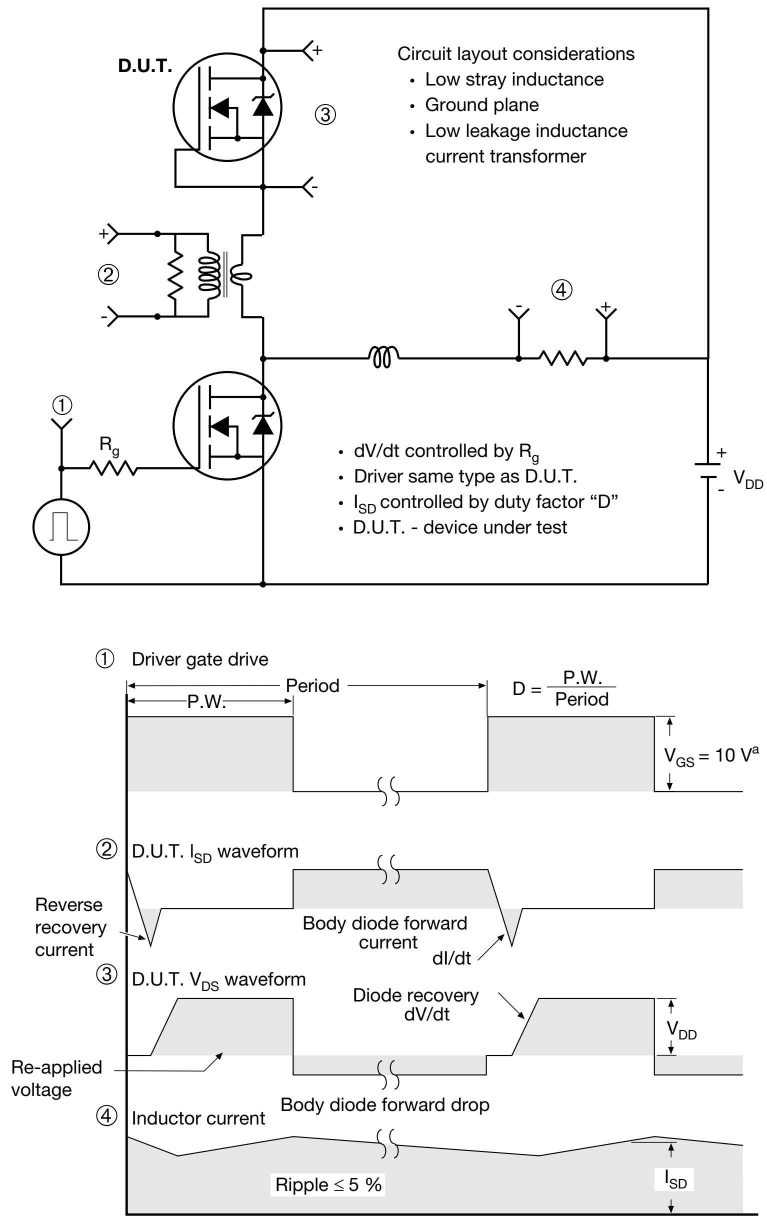


Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit



Note

a. V_{GS} = 5 V for logic level devices

Fig. 14 - For N-Channel

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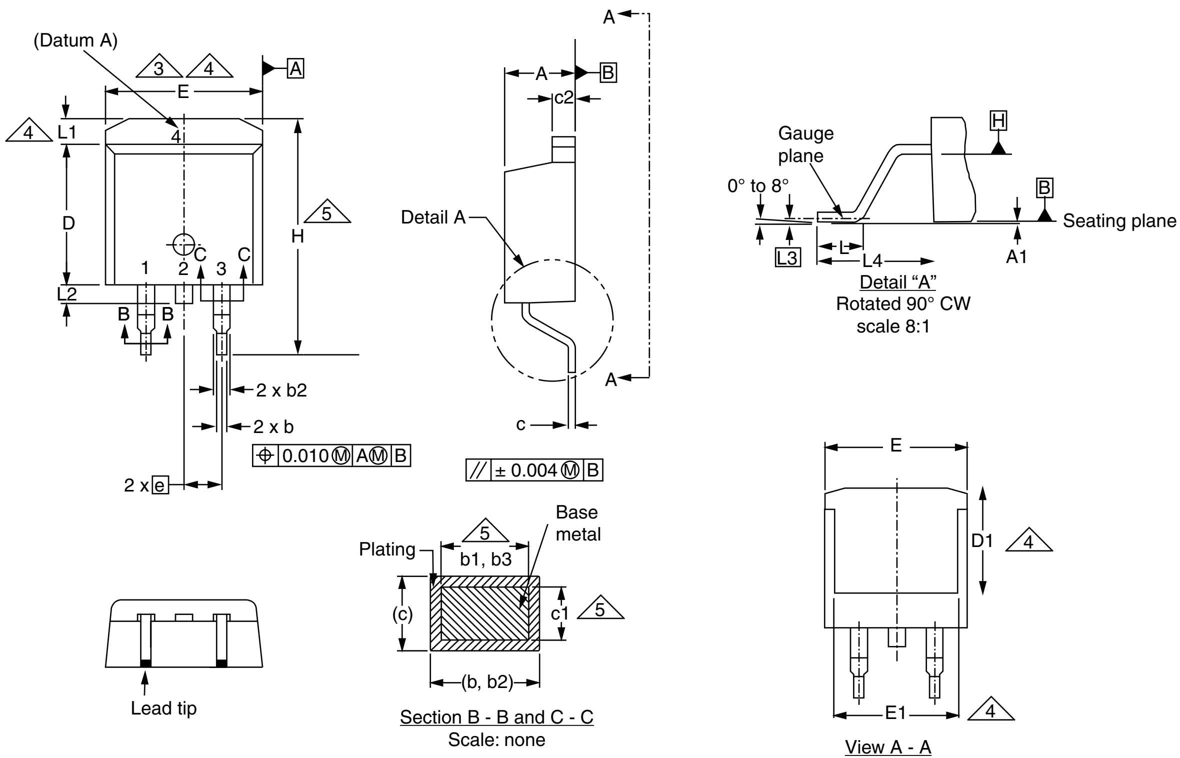
TO-263AB (HIGH VOLTAGE)



	MILLIMETERS		INCHES	
DIM.	MIN.	MAX.	MIN.	MAX.
A	4.06	4.83	0.160	0.190
A1	0.00	0.25	0.000	0.010
b	0.51	0.99	0.020	0.039
b1	0.51	0.89	0.020	0.035
b2	1.14	1.78	0.045	0.070
b3	1.14	1.73	0.045	0.068
c	0.38	0.74	0.015	0.029
c1	0.38	0.58	0.015	0.023
c2	1.14	1.65	0.045	0.065
D	8.38	9.65	0.330	0.380

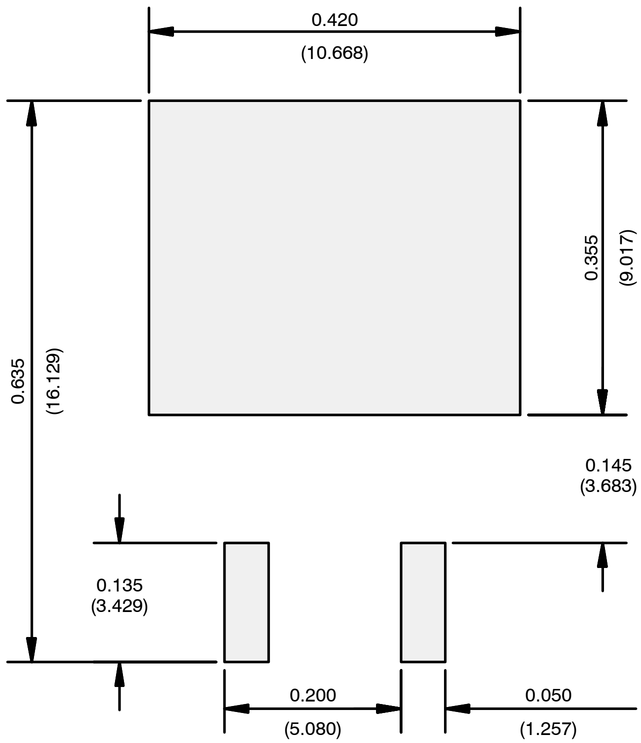
	MILLIMETERS		INCHES	
DIM.	MIN.	MAX.	MIN.	MAX.
D1	6.86	-	0.270	-
E	9.65	10.67	0.380	0.420
E1	6.22	-	0.245	-
e	2.54 BSC		0.100 BSC	
H	14.61	15.88	0.575	0.625
L	1.78	2.79	0.070	0.110
L1	-	1.65	-	0.066
L2	-	1.78	-	0.070
L3	0.25 BSC		0.010 BSC	
L4	4.78	5.28	0.188	0.208

ECN: S-82110-Rev. A, 15-Sep-08
DWG: 5970

Notes

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimensions are shown in millimeters (inches).
3. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outmost extremes of the plastic body at datum A.
4. Thermal PAD contour optional within dimension E, L1, D1 and E1.
5. Dimension b1 and c1 apply to base metal only.
6. Datum A and B to be determined at datum plane H.
7. Outline conforms to JEDEC outline to TO-263AB.

RECOMMENDED MINIMUM PADS FOR D^2PAK: 3-Lead



Recommended Minimum Pads
Dimensions in Inches/(mm)

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- Экспресс доставка в любую точку России;
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- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
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«FORSTAR» (основан в 1998 г.)

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