

## Li-ION/POLYMER 2/3-CELL PROTECTOR Second protection IC

NO.EA-282-120409

### OUTLINES

R5435x Series are CMOS-based high voltage tolerant over-charge protection ICs for Li-ion/Li-polymer secondary battery. The R5435x can detect overcharge of 2-cell to 3-cell Li-ion/ Li-polymer batteries. The R5435x is consists of 3 voltage detectors, a voltage reference unit, an oscillator, a counter, a delay circuit, a logic circuit.

When the over-charge is detected, after the IC internally fixed delay time, the output of C<sub>OUT</sub> becomes "H".

After detecting over-charge, when the cell voltage becomes lower than the over-charge released voltage, the over-charge state is released.

If all the cells voltages become equal or less than the shutdown detector threshold, all the circuits are halted and shut down, as a result, the consumption current of IC itself (Shutdown current) is extremely reduced.

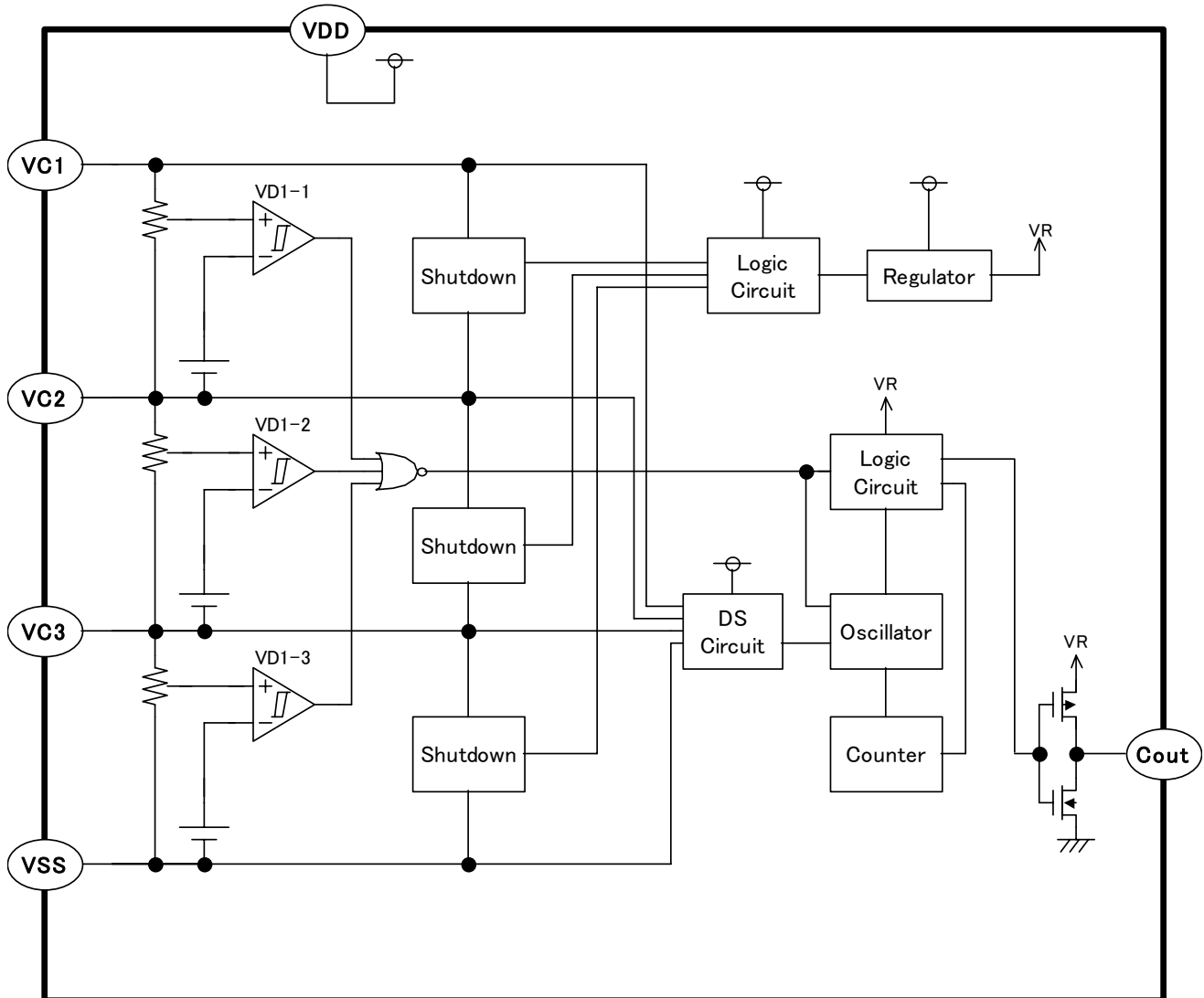
By connect short 2 cells other than monitored cell, over-charge and released delay time can be shortened.

The output type is CMOS.

### FEATURES

- Manufactured with High Voltage Tolerant Process ..... Absolute Maximum Rating 30V
- Low supply current ..... Cell voltage 3.9V, for 3-cell Typ. 3.0μA
- High accuracy detector threshold ..... Over-charge detector (Ta=25°C) ±20mV  
(Ta=0 to 60°C) ±25mV
- Variety of detector threshold
  - Over-charge detector threshold 4.1V-4.55V step of 0.005V (V<sub>DET1n</sub>) (n=1, 2, 3)
  - Over-charge released voltage V<sub>DET1n</sub>-0V to V<sub>DET1n</sub>-0.4V step of 0.05V (V<sub>REL1n</sub>) (n=1, 2, 3)  
MIN.3.95V
- Setting of Output delay time..... Over-charge detector Output Delay options 2, 4, 6s(Built-in delay)
- Shutdown Function .....When all the cell voltages become equal or less than shutdown detector threshold, the IC will be into shutdown mode and the consumption current of IC itself becomes extremely small. Even if one of the cells becomes equal or more than shutdown released voltage, the shutdown mode is released.
- Shutdown detector threshold .....Typ. 3.5V±0.4V
- Shutdown Release Hysteresis ..... none
- Shutdown current .....Max. 0.1μA
- 2/3 cell protection enabler .....By external wiring, 2 or 3-cell protection can be selected.
- Over-charge released condition.....Released by voltage type
- C<sub>OUT</sub> output .....C<sub>OUT</sub>: 4.7V regulator power supply CMOS output. Active "H"
- Delay Time Shortening Function.....As a result of specified setting, the delay times are shortened, over-charge detector time is shortened from 2sec to 1/50, 4sec and 6sec to 1/80.  
 ex. V<sub>C2</sub>=V<sub>C3</sub>=V<sub>SS</sub>, the delay time for cell 1 is shortened. V<sub>C1</sub>=V<sub>C2</sub>, V<sub>C3</sub>=V<sub>SS</sub>, the delay time for cell 2 is shortened.  
 V<sub>C1</sub>=V<sub>C2</sub>=V<sub>C3</sub>, the delay time for cell 3 is shortened.
- Small package..... TSOT-23-6, DFN(PLP)1616-6B

### BLOCK DIAGRAM



## SELECTION GUIDE

In the R5435Xxxxx Series, input threshold of over-charge and output delay time can be designated according to the application.

Part Number is designated as follows:

(ex.)

R5435N 301AA ←Part Number  
 ↑ ↑ ↑↑  
 a b cd

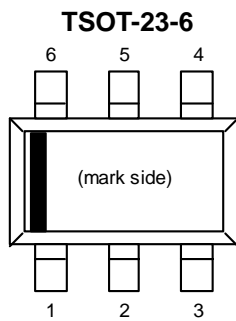
Code	Contents
a	Package Type N: TSOT-23-6, K: PLP1616-6B
b	Serial Number for the R5435 Series designating input threshold for over-charge detector
c	Designation of Output delay option
d	Designation of version symbols.

### • Code List

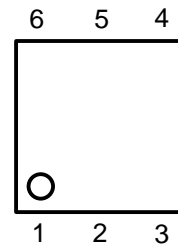
Code	$V_{DET1n}(V)^{*1}$	$V_{REL1n}(V)^{*1}$	$tV_{DET1}(s)$	$tV_{DTR1}(ms)$
R5435x301AA	4.450	4.150	2	16
R5435x302BA	4.350	3.950	4	16
R5435x303AA	4.350	4.050	2	16
R5435x303CA	4.350	4.050	6	6
R5435x304AA	4.400	4.100	2	16
R5435x305AA	4.300	4.000	2	16
R5435x306BA	4.450	3.950	4	16

\*1: n=1, 2, 3

## PIN CONFIGURATIONS



**DFN(PLP)1616-6B**



## PIN DESCRIPTION

### TSOT-23-6

Pin No.	Symbol	Description
1	$V_{DD}$	$V_{DD}$ Pin
2	$V_{C1}$	Positive terminal pin for Cell-1
3	$V_{C2}$	Positive terminal pin for Cell-2
4	$V_{C3}$	Positive terminal Pin for Cell-3
5	$V_{SS}$	$V_{SS}$ pin. Ground pin for the IC
6	$C_{OUT}$	Output pin of over-charge detection

### DFN(PLP)1616-6B

Pin No.	Symbol	Description
1	$V_{C2}$	Positive terminal pin for Cell-2
2	$V_{C1}$	Positive terminal pin for Cell-1
3	$V_{DD}$	$V_{DD}$ Pin
4	$C_{OUT}$	Output pin of over-charge detection
5	$V_{SS}$	$V_{SS}$ pin. Ground pin for the IC
6	$V_{C3}$	Positive terminal Pin for Cell-3

\*The tab voltage level of the backside of the package is the substrate level ( $V_{SS}$ ).

Connect the tab to the  $V_{SS}$  pin (Recommended) or leave the tab open.

## ABSOLUTE MAXIMUM RATINGS

Ta=25°C, V<sub>SS</sub>=0V

Symbol	Item	Ratings	Unit
V <sub>DD</sub>	Supply voltage	-0.3 to 30	V
V <sub>C1</sub>	Input voltage Positive input pin voltage for Cell-1	V <sub>C2</sub> -0.3 to V <sub>C2</sub> +6.5	V
V <sub>C2</sub>	Positive input pin voltage for Cell-2	V <sub>C3</sub> -0.3 to V <sub>C3</sub> +6.5	
V <sub>C3</sub>	Positive input pin voltage for Cell-3	-0.3 to 6.5	
V <sub>COU</sub>	Output voltage C <sub>OUT</sub> pin voltage	-0.3 to V <sub>OH1</sub> +0.3	V
P <sub>D</sub>	Power dissipation	460 (TSOT-23-6) 640 (PLP1616-6B)	mW
Ta	Operating temperature range	-40 to 85	°C
Tstg	Storage temperature range	-55 to 125	°C

## ELECTRICAL CHARACTERISTICS

## ● R5435x301AA

Unless otherwise specified, Ta=25°C

Symbol	Item	Conditions	Min.	Typ.	Max.	Unit
V <sub>DD1</sub>	Operating input voltage	Voltage defined as V <sub>DD</sub> -V <sub>SS</sub>	3.3		15	V
V <sub>DET1N</sub>	CELLn Over-charge threshold (n=1,2,3)	Detect rising edge of supply voltage (25°C)	4.430	4.450	4.470	V
		Detect rising edge of supply voltage (0 to 60°C) <sup>*Note1</sup>	4.425		4.475	
V <sub>REL1N</sub>	CELLn Over-charge released voltage (n=1,2,3)	Detect falling edge of supply voltage	4.100	4.150	4.200	V
t <sub>VDET1</sub>	Output delay of over-charge	V <sub>CELLn</sub> =3.9V, V <sub>CELL1</sub> =3.9V to 4.7V (n=2,3) <sup>*Note2</sup>	1.6	2.0	2.4	s
t <sub>VREL1</sub>	Output delay of release from over-charge	V <sub>CELLn</sub> =3.9V, V <sub>CELL1</sub> =4.7V to 3.9V (n=2,3)	12.8	16	19.2	ms
V <sub>SHT</sub>	Shutdown detector threshold	Detect falling edge	3.1	3.5	3.9	V
t <sub>VDR1</sub>	Output delay of over-charge timer reset	V <sub>CELLn</sub> =V <sub>DET1n</sub> +0.050V to V <sub>REL1n</sub> -0.100V to V <sub>DET1n</sub> +0.050V to V <sub>REL1n</sub> -0.100V	8	16	24	ms
V <sub>OH1</sub>	C <sub>OUT</sub> Pch ON voltage1	I <sub>OH</sub> =0μA, V <sub>CELLn</sub> =4.7V (n=1,2,3)	4.0	4.7	5.4	V
V <sub>OH2</sub>	C <sub>OUT</sub> Pch ON voltage2	I <sub>OH</sub> =-50μA, V <sub>CELLn</sub> =4.7V (n=1,2,3)	V <sub>OH1</sub> -0.5	V <sub>OH1</sub> -0.1		V
V <sub>OL</sub>	C <sub>OUT</sub> Nch ON voltage	I <sub>OL</sub> =50μA, V <sub>CELLn</sub> =3.9V (n=1,2,3)		0.1	0.5	V
I <sub>SHT</sub>	Shutdown Current	V <sub>CELLn</sub> =3.1V (n=1,2,3)			0.1	μA
I <sub>SS</sub>	Supply current	V <sub>CELLn</sub> =3.9V (n=1,2,3)		3.0	5.5	μA

\*Note1: This specification is guaranteed by design, not mass production tested.

\*Note2: V<sub>CELLn</sub> means Cell-n's voltage. n=1, 2, 3

## ● R5435x302BA

Unless otherwise specified, Ta=25°C

Symbol	Item	Conditions	Min.	Typ.	Max.	Unit
V <sub>DD1</sub>	Operating input voltage	Voltage defined as V <sub>DD</sub> -V <sub>SS</sub>	3.3		15	V
V <sub>DET1N</sub>	CELLn Over-charge threshold (n=1,2,3)	Detect rising edge of supply voltage (25°C)	4.330	4.350	4.370	V
		Detect rising edge of supply voltage (0 to 60°C) <sup>*Note1</sup>	4.325		4.375	
V <sub>REL1N</sub>	CELLn Over-charge released voltage (n=1,2,3)	Detect falling edge of supply voltage	3.900	3.950	4.000	V
t <sub>VDET1</sub>	Output delay of over-charge	V <sub>CELLn</sub> =3.9V, V <sub>CELL1</sub> =3.9V to 4.7V (n=2,3) <sup>*Note2</sup>	3.2	4.0	4.8	s
t <sub>VREL1</sub>	Output delay of release from over-charge	V <sub>CELLn</sub> =3.9V, V <sub>CELL1</sub> =4.7V to 3.9V (n=2,3)	12.8	16	19.2	ms
V <sub>SHT</sub>	Shutdown detector threshold	Detect falling edge	3.1	3.5	3.9	V
t <sub>VDR1</sub>	Output delay of over-charge timer reset	V <sub>CELLn</sub> =V <sub>DET1n</sub> +0.050V to V <sub>REL1n</sub> -0.100V to V <sub>DET1n</sub> +0.050V to V <sub>REL1n</sub> -0.100V	8	16	24	ms
V <sub>OH1</sub>	C <sub>OUT</sub> Pch ON voltage1	I <sub>OH</sub> =0μA, V <sub>CELLn</sub> =4.7V (n=1,2,3)	4.0	4.7	5.4	V
V <sub>OH2</sub>	C <sub>OUT</sub> Pch ON voltage2	I <sub>OH</sub> =-50μA, V <sub>CELLn</sub> =4.7V (n=1,2,3)	V <sub>OH1</sub> -0.5	V <sub>OH1</sub> -0.1		V
V <sub>OL</sub>	C <sub>OUT</sub> Nch ON voltage	I <sub>OL</sub> =50μA, V <sub>CELLn</sub> =3.9V (n=1,2,3)		0.1	0.5	V
I <sub>SHT</sub>	Shutdown Current	V <sub>CELLn</sub> =3.1V (n=1,2,3)			0.1	μA
I <sub>SS</sub>	Supply current	V <sub>CELLn</sub> =3.9V (n=1,2,3)		3.0	5.5	μA

\*Note1: This specification is guaranteed by design, not mass production tested.

\*Note2: V<sub>CELLn</sub> means Cell-n's voltage. n=1, 2, 3

## ● R5435x303AA

Unless otherwise specified, Ta=25°C

Symbol	Item	Conditions	Min.	Typ.	Max.	Unit
V <sub>DD1</sub>	Operating input voltage	Voltage defined as V <sub>DD</sub> -V <sub>SS</sub>	3.3		15	V
V <sub>DET1n</sub>	CELLn Over-charge threshold (n=1,2,3)	Detect rising edge of supply voltage (25°C)	4.330	4.350	4.370	V
		Detect rising edge of supply voltage (0 to 60°C) <sup>*Note1</sup>	4.325		4.375	
V <sub>REL1n</sub>	CELLn Over-charge released voltage (n=1,2,3)	Detect falling edge of supply voltage	4.000	4.050	4.100	V
t <sub>VDET1</sub>	Output delay of over-charge	V <sub>CELLn</sub> =3.9V, V <sub>CELL1</sub> =3.9V to 4.7V (n=2,3) <sup>*Note2</sup>	1.6	2.0	2.4	s
t <sub>VREL1</sub>	Output delay of release from over-charge	V <sub>CELLn</sub> =3.9V, V <sub>CELL1</sub> =4.7V to 3.9V (n=2,3)	12.8	16	19.2	ms
V <sub>SHT</sub>	Shutdown detector threshold	Detect falling edge	3.1	3.5	3.9	V
t <sub>VDTR1</sub>	Output delay of over-charge timer reset	V <sub>CELLn</sub> =V <sub>DET1n</sub> +0.050V to V <sub>REL1n</sub> -0.100V to V <sub>DET1n</sub> +0.050V to V <sub>REL1n</sub> -0.100V	8	16	24	ms
V <sub>OH1</sub>	C <sub>OUT</sub> Pch ON voltage1	I <sub>OH</sub> =0μA, V <sub>CELLn</sub> =4.7V (n=1,2,3)	4.0	4.7	5.4	V
V <sub>OH2</sub>	C <sub>OUT</sub> Pch ON voltage2	I <sub>OH</sub> =-50μA, V <sub>CELLn</sub> =4.7V (n=1,2,3)	V <sub>OH1</sub> -0.5	V <sub>OH1</sub> -0.1		V
V <sub>OL</sub>	C <sub>OUT</sub> Nch ON voltage	I <sub>OL</sub> =50μA, V <sub>CELLn</sub> =3.9V (n=1,2,3)		0.1	0.5	V
I <sub>SHT</sub>	Shutdown Current	V <sub>CELLn</sub> =3.1V (n=1,2,3)			0.1	μA
I <sub>SS</sub>	Supply current	V <sub>CELLn</sub> =3.9V (n=1,2,3)		3.0	5.5	μA

\*Note1: This specification is guaranteed by design, not mass production tested.

\*Note2: V<sub>CELLn</sub> means Cell-n's voltage. n=1, 2, 3

## ● R5435x303CA

Unless otherwise specified, Ta=25°C

Symbol	Item	Conditions	Min.	Typ.	Max.	Unit
V <sub>DD1</sub>	Operating input voltage	Voltage defined as V <sub>DD</sub> -V <sub>SS</sub>	3.3		15	V
V <sub>DET1n</sub>	CELLn Over-charge threshold (n=1,2,3)	Detect rising edge of supply voltage (25°C)	4.330	4.350	4.370	V
		Detect rising edge of supply voltage (0 to 60°C) <sup>*Note1</sup>	4.325		4.375	
V <sub>REL1n</sub>	CELLn Over-charge released voltage (n=1,2,3)	Detect falling edge of supply voltage	4.000	4.050	4.100	V
t <sub>VDET1</sub>	Output delay of over-charge	V <sub>CELLn</sub> =3.9V, V <sub>CELL1</sub> =3.9V to 4.7V (n=2,3) <sup>*Note2</sup>	4.8	6.0	7.2	s
t <sub>VREL1</sub>	Output delay of release from over-charge	V <sub>CELLn</sub> =3.9V, V <sub>CELL1</sub> =4.7V to 3.9V (n=2,3)	12.8	16	19.2	ms
V <sub>SHT</sub>	Shutdown detector threshold	Detect falling edge	3.1	3.5	3.9	V
t <sub>VDTR1</sub>	Output delay of over-charge timer reset	V <sub>CELLn</sub> =V <sub>DET1n</sub> +0.050V to V <sub>REL1n</sub> -0.100V to V <sub>DET1n</sub> +0.050V to V <sub>REL1n</sub> -0.100V	2	6	10	ms
V <sub>OH1</sub>	C <sub>OUT</sub> Pch ON voltage1	I <sub>OH</sub> =0μA, V <sub>CELLn</sub> =4.7V (n=1,2,3)	4.0	4.7	5.4	V
V <sub>OH2</sub>	C <sub>OUT</sub> Pch ON voltage2	I <sub>OH</sub> =-50μA, V <sub>CELLn</sub> =4.7V (n=1,2,3)	V <sub>OH1</sub> -0.5	V <sub>OH1</sub> -0.1		V
V <sub>OL</sub>	C <sub>OUT</sub> Nch ON voltage	I <sub>OL</sub> =50μA, V <sub>CELLn</sub> =3.9V (n=1,2,3)		0.1	0.5	V
I <sub>SHT</sub>	Shutdown Current	V <sub>CELLn</sub> =3.1V (n=1,2,3)			0.1	μA
I <sub>SS</sub>	Supply current	V <sub>CELLn</sub> =3.9V (n=1,2,3)		3.0	5.5	μA

\*Note1: This specification is guaranteed by design, not mass production tested.

\*Note2: V<sub>CELLn</sub> means Cell-n's voltage. n=1, 2, 3

## R5435x

### ● R5435x304AA

Unless otherwise specified, Ta=25°C

Symbol	Item	Conditions	Min.	Typ.	Max.	Unit
V <sub>DD1</sub>	Operating input voltage	Voltage defined as V <sub>DD</sub> -V <sub>SS</sub>	3.3		15	V
V <sub>DET1n</sub>	CELLn Over-charge threshold (n=1,2,3)	Detect rising edge of supply voltage (25°C)	4.380	4.400	4.420	V
		Detect rising edge of supply voltage (0 to 60°C) <sup>*Note1</sup>	4.375		4.425	
V <sub>REL1n</sub>	CELLn Over-charge released voltage (n=1,2,3)	Detect falling edge of supply voltage	4.050	4.100	4.150	V
tV <sub>DET1</sub>	Output delay of over-charge	V <sub>CELLn</sub> =3.9V, V <sub>CELL1</sub> =3.9V to 4.7V (n=2,3) <sup>*Note2</sup>	1.6	2.0	2.4	s
tV <sub>REL1</sub>	Output delay of release from over-charge	V <sub>CELLn</sub> =3.9V, V <sub>CELL1</sub> =4.7V to 3.9V (n=2,3)	12.8	16	19.2	ms
V <sub>SHT</sub>	Shutdown detector threshold	Detect falling edge	3.1	3.5	3.9	V
tV <sub>DTR1</sub>	Output delay of over-charge timer reset	V <sub>CELLn</sub> =V <sub>DET1n</sub> +0.050V to V <sub>REL1n</sub> -0.100V to V <sub>DET1n</sub> +0.050V to V <sub>REL1n</sub> -0.100V	8	16	24	ms
V <sub>OH1</sub>	C <sub>OUT</sub> Pch ON voltage1	I <sub>OH</sub> =0μA, V <sub>CELLn</sub> =4.7V (n=1,2,3)	4.0	4.7	5.4	V
V <sub>OH2</sub>	C <sub>OUT</sub> Pch ON voltage2	I <sub>OH</sub> =-50μA, V <sub>CELLn</sub> =4.7V (n=1,2,3)	V <sub>OH1</sub> -0.5	V <sub>OH1</sub> -0.1		V
V <sub>OL</sub>	C <sub>OUT</sub> Nch ON voltage	I <sub>OL</sub> =50μA, V <sub>CELLn</sub> =3.9V (n=1,2,3)		0.1	0.5	V
I <sub>SHT</sub>	Shutdown Current	V <sub>CELLn</sub> =3.1V (n=1,2,3)			0.1	μA
I <sub>SS</sub>	Supply current	V <sub>CELLn</sub> =3.9V (n=1,2,3)		3.0	5.5	μA

\*Note1: This specification is guaranteed by design, not mass production tested.

\*Note2: V<sub>CELLn</sub> means Cell-n's voltage. n=1, 2, 3

### ● R5435x305AA

Unless otherwise specified, Ta=25°C

Symbol	Item	Conditions	Min.	Typ.	Max.	Unit
V <sub>DD1</sub>	Operating input voltage	Voltage defined as V <sub>DD</sub> -V <sub>SS</sub>	3.3		15	V
V <sub>DET1n</sub>	CELLn Over-charge threshold (n=1,2,3)	Detect rising edge of supply voltage (25°C)	4.280	4.300	4.320	V
		Detect rising edge of supply voltage (0 to 60°C) <sup>*Note1</sup>	4.275		4.325	
V <sub>REL1n</sub>	CELLn Over-charge released voltage (n=1,2,3)	Detect falling edge of supply voltage	3.950	4.000	4.050	V
tV <sub>DET1</sub>	Output delay of over-charge	V <sub>CELLn</sub> =3.9V, V <sub>CELL1</sub> =3.9V to 4.7V (n=2,3) <sup>*Note2</sup>	1.6	2.0	2.4	s
tV <sub>REL1</sub>	Output delay of release from over-charge	V <sub>CELLn</sub> =3.9V, V <sub>CELL1</sub> =4.7V to 3.9V (n=2,3)	12.8	16	19.2	ms
V <sub>SHT</sub>	Shutdown detector threshold	Detect falling edge	3.1	3.5	3.9	V
tV <sub>DTR1</sub>	Output delay of over-charge timer reset	V <sub>CELLn</sub> =V <sub>DET1n</sub> +0.050V to V <sub>REL1n</sub> -0.100V to V <sub>DET1n</sub> +0.050V to V <sub>REL1n</sub> -0.100V	8	16	24	ms
V <sub>OH1</sub>	C <sub>OUT</sub> Pch ON voltage1	I <sub>OH</sub> =0μA, V <sub>CELLn</sub> =4.7V (n=1,2,3)	4.0	4.7	5.4	V
V <sub>OH2</sub>	C <sub>OUT</sub> Pch ON voltage2	I <sub>OH</sub> =-50μA, V <sub>CELLn</sub> =4.7V (n=1,2,3)	V <sub>OH1</sub> -0.5	V <sub>OH1</sub> -0.1		V
V <sub>OL</sub>	C <sub>OUT</sub> Nch ON voltage	I <sub>OL</sub> =50μA, V <sub>CELLn</sub> =3.9V (n=1,2,3)		0.1	0.5	V
I <sub>SHT</sub>	Shutdown Current	V <sub>CELLn</sub> =3.1V (n=1,2,3)			0.1	μA
I <sub>SS</sub>	Supply current	V <sub>CELLn</sub> =3.9V (n=1,2,3)		3.0	5.5	μA

\*Note1: This specification is guaranteed by design, not mass production tested.

\*Note2: V<sub>CELLn</sub> means Cell-n's voltage. n=1, 2, 3



## ● R5435x306BA

Unless otherwise specified, Ta=25°C

Symbol	Item	Conditions	Min.	Typ.	Max.	Unit
V <sub>DD1</sub>	Operating input voltage	Voltage defined as V <sub>DD</sub> -V <sub>SS</sub>	3.3		15	V
V <sub>DET1n</sub>	CELLn Over-charge threshold (n=1,2,3)	Detect rising edge of supply voltage (25°C)	4.430	4.450	4.470	V
		Detect rising edge of supply voltage (0 to 60°C) <sup>*Note1</sup>	4.425		4.475	
V <sub>REL1n</sub>	CELLn Over-charge released voltage (n=1,2,3)	Detect falling edge of supply voltage	3.900	3.950	4.000	V
t <sub>VDET1</sub>	Output delay of over-charge	V <sub>CELLn</sub> =3.9V, V <sub>CELL1</sub> =3.9V to 4.7V (n=2,3) <sup>*Note2</sup>	3.2	4.0	4.8	s
t <sub>VREL1</sub>	Output delay of release from over-charge	V <sub>CELLn</sub> =3.9V, V <sub>CELL1</sub> =4.7V to 3.9V (n=2,3)	12.8	16	19.2	ms
V <sub>SHT</sub>	Shutdown detector threshold	Detect falling edge	3.1	3.5	3.9	V
t <sub>VDTR1</sub>	Output delay of over-charge timer reset	V <sub>CELLn</sub> =V <sub>DET1n</sub> +0.050V to V <sub>REL1n</sub> -0.100V to V <sub>DET1n</sub> +0.050V to V <sub>REL1n</sub> -0.100V	8	16	24	ms
V <sub>OH1</sub>	C <sub>OUT</sub> Pch ON voltage1	I <sub>OH</sub> =0μA, V <sub>CELLn</sub> =4.7V (n=1,2,3)	4.0	4.7	5.4	V
V <sub>OH2</sub>	C <sub>OUT</sub> Pch ON voltage2	I <sub>OH</sub> =-50μA, V <sub>CELLn</sub> =4.7V (n=1,2,3)	V <sub>OH1</sub> -0.5	V <sub>OH1</sub> -0.1		V
V <sub>OL</sub>	C <sub>OUT</sub> Nch ON voltage	I <sub>OL</sub> =50μA, V <sub>CELLn</sub> =3.9V (n=1,2,3)		0.1	0.5	V
I <sub>SHT</sub>	Shutdown Current	V <sub>CELLn</sub> =3.1V (n=1,2,3)			0.1	μA
I <sub>SS</sub>	Supply current	V <sub>CELLn</sub> =3.9V (n=1,2,3)		3.0	5.5	μA

\*Note1: This specification is guaranteed by design, not mass production tested.

\*Note2: V<sub>CELLn</sub> means Cell-n's voltage. n=1, 2, 3

## RECOMMENDED OPERATING CONDITIONS (ELECTRICAL CHARACTERISTICS)

All of electronic equipment should be designed that the mounted semiconductor devices operate within the recommended operating conditions. The semiconductor devices cannot operate normally over the recommended operating conditions, even if when they are used over such conditions by momentary electronic noise or surge. And the semiconductor devices may receive serious damage when they continue to operate over the recommended operating conditions.

## OPERATION

### • VDET1n / Over-Charge Detectors (n=1, 2, 3)

While the cells are charged, the voltage between  $V_{C1}$  pin and  $V_{C2}$  pin (voltage of the Cell-1), the voltage between  $V_{C2}$  pin and  $V_{C3}$  pin (voltage of the Cell-2), and the voltage between  $V_{C3}$  pin and  $V_{SS}$  pin (voltage of the Cell-3) are supervised. If at least one of the cells' voltage becomes equal or more than the over-charge detector threshold, the over-charge is detected, and an external charge control Nch MOSFET turns on with  $C_{OUT}$  pin being at "H" level and by cutting a fuse on the charger path, and charge stops.

To reset the over-charge and make the  $C_{OUT}$  pin level to "L" again after detecting over-charge, in such conditions that a time when all the cells' voltages are down to a level lower than over-charge released voltage.

Internal fixed output delay times for over-charge detection, over-charge detector timer reset, release from over-charge exist. Even if one of voltage of the cells keeps its level more than the over-charge detector threshold, and output delay time passes, over-charge voltage is detected. If all the cell voltages become lower than the over-charge detector threshold within the output delay time of over-charge detector by noise or other reasons, the time period is less than over-charge detector timer reset output delay time, the over-charge delay time is accumulated and maintained, and the accumulated delay time reaches the output delay time of over-charge, the over-charge is detected. After detecting over-charge, even if all the cell voltages become equal or less than the released voltage from over-charge, if at least one of the cells voltage becomes higher than the released voltage from over-charge within the output delay time of the release from over-charge, then over-charge is not released.

The output type of the  $C_{OUT}$  pin is CMOS output between  $V_{SS}$  and the built-in regulator, and "H" level of  $C_{OUT}$  pin is the output voltage of the built-in regulator. (Typ. 4.7V)

### • Shutdown Function

The voltage between  $V_{C1}$  pin and  $V_{C2}$  pin (the voltage of Cell-1), the voltage between  $V_{C2}$  pin and  $V_{C3}$  pin (Cell-2 voltage), and the voltage between  $V_{C3}$  pin and  $V_{SS}$  pin (Cell-3 voltage) are supervised. If all the cells voltages become equal or less than the shutdown detector threshold, all the circuits are halted and shut down, as a result, the consumption current of IC itself (Shutdown current) is extremely reduced. (Max. 0.1 $\mu$ A)

After detecting shutdown, at least one of the cell voltages becomes equal or more than the shutdown detector threshold, the shutdown state is released.

### • DS (Delay Shortening) Function

By connect short 2 cells other than monitored cell, over-charge and released delay time can be shortened.  
Table of the cell of delay time shortened and direct wiring positions

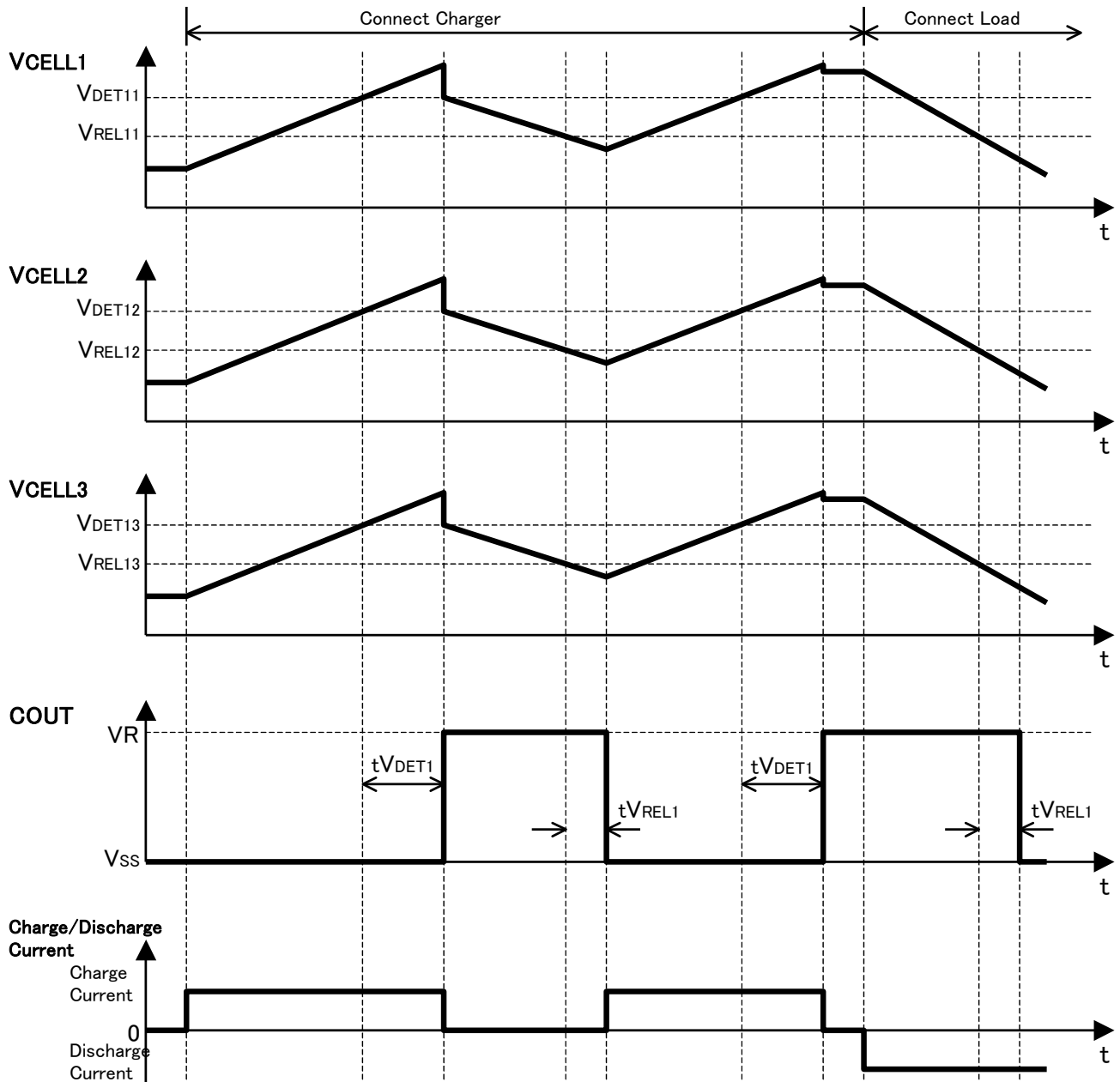
Delay time shortened CELL	Direct wiring positions
CELL1	$V_{C2}$ pin and $V_{C3}$ pin, $V_{C3}$ pin and $V_{SS}$ pin
CELL2	$V_{C1}$ pin and $V_{C2}$ pin, $V_{C3}$ pin and $V_{SS}$ pin
CELL3	$V_{C1}$ pin and $V_{C2}$ pin, $V_{C2}$ pin and $V_{C3}$ pin

### • 2-cell/ 3-cell protection alternative

When the IC should be used as a 2-cell protection IC, connect short  $V_{C3}$  pin and  $V_{SS}$  pin.

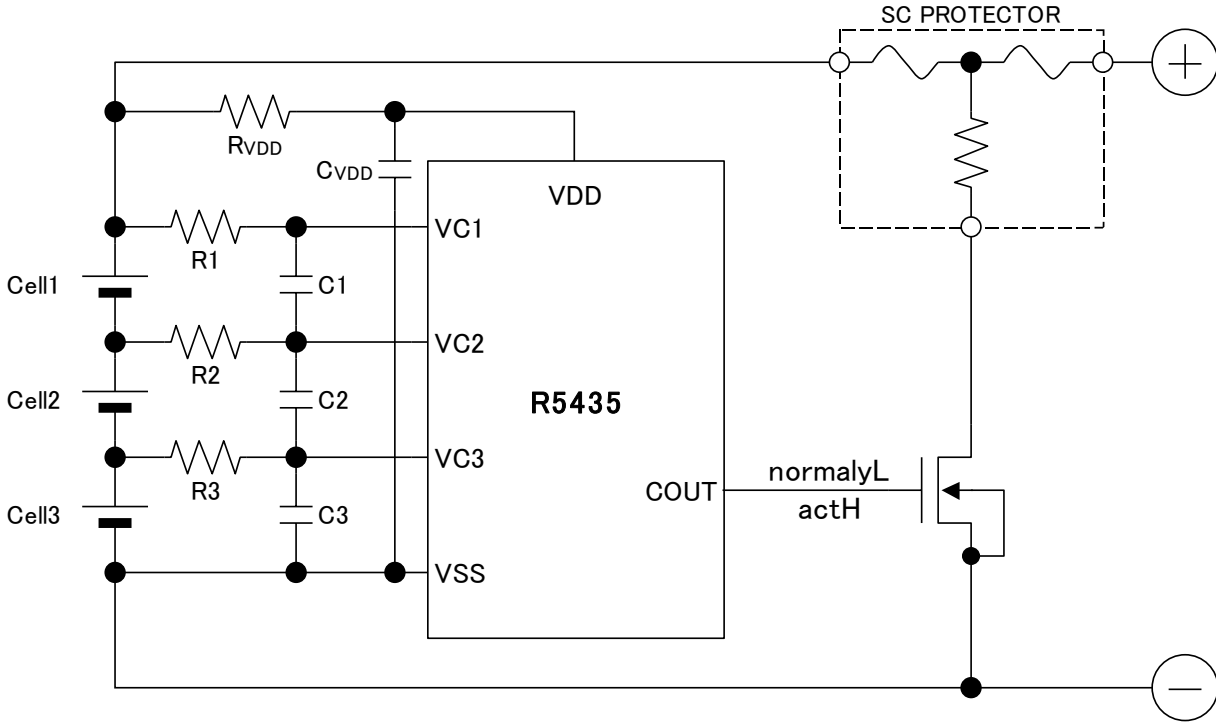
## TIMING CHART

● Over-charge operation

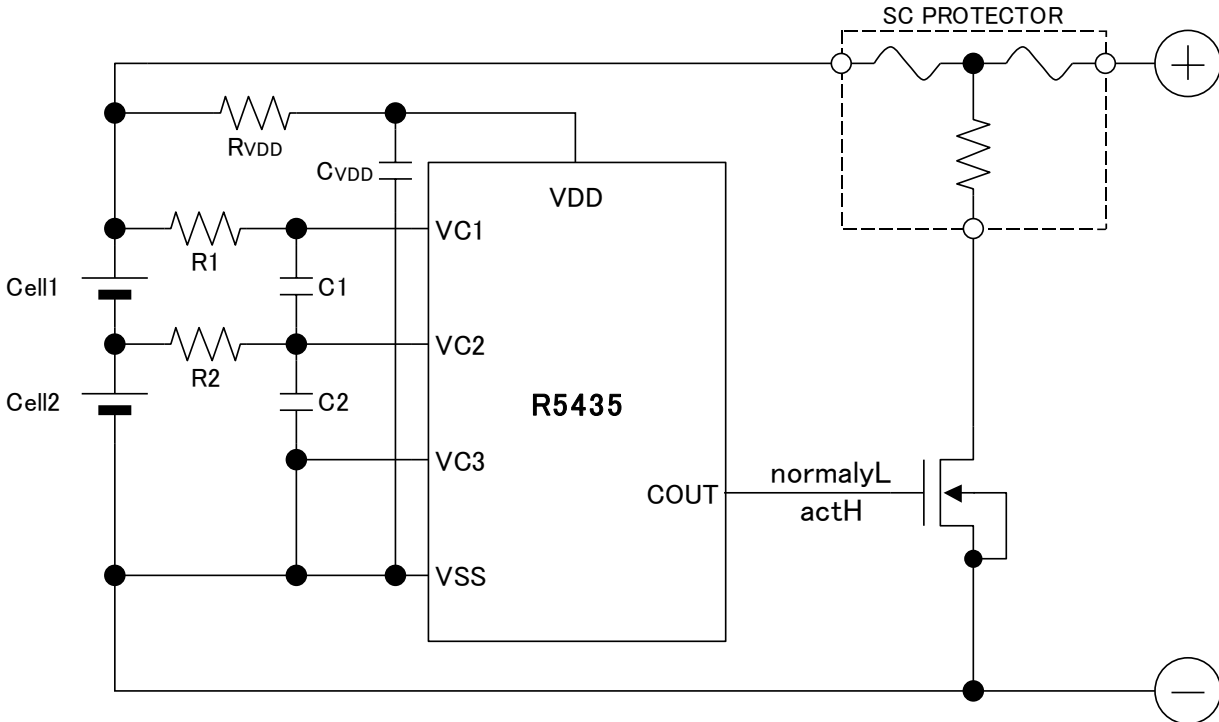


## TYPICAL APPLICATIONS

### (1) Circuit example (3-cell protection)



### (2) Circuit example (2-cell protection)



\*In terms of the order of connecting cells, the positive terminal of the cell 1 should be the last. Otherwise, COUT may output "H" tentatively, and the fuse may be fused.

## ●External parts ratings

Symbol	Typ.	Unit	Range
$R_{VDD}$	100	$\Omega$	100~1000
R1	1000	$\Omega$	330~1000
R2	1000	$\Omega$	330~1000
R3	1000	$\Omega$	330~1000
$C_{VDD}$	0.1	$\mu\text{F}$	0.01~1
C1	0.1	$\mu\text{F}$	0.01~1
C2	0.1	$\mu\text{F}$	0.01~1
C3	0.1	$\mu\text{F}$	0.01~1

## Technical Notes

The voltage fluctuation is stabilized with  $R_{VDD}$  and  $C_{VDD}$ . If a small  $R_{VDD}$  is set, in the case of the large transient may happen to the cell voltage, by the flowing current, the IC may be unstable. If a large  $R_{VDD}$  is set, by the consumption current of the IC itself, the voltage difference between  $V_{DD}$  pin and  $V_{C1}$  pin is generated, and unexpected operation may result. Therefore, the appropriate value range of  $R_{VDD}$  is from 100 $\Omega$  to 1k $\Omega$ . To make a stable operation of the IC, the appropriate value range of  $C_{VDD}$  is from 0.01 $\mu\text{F}$  to 1.0 $\mu\text{F}$ .

The voltage fluctuation is stabilized with R1 to R3 and C1 to C3. If a R1 to R3 is too large, by the conduction current at detection, the detector threshold may shift higher. Therefore, the appropriate value range of R1 to R3 is equal or less than 1k $\Omega$ . To make a stable operation of the IC, the appropriate value range of C1 to C3 is 0.01 $\mu\text{F}$  or more.

The typical application circuit diagrams are just examples. This circuit performance largely depends on the PCB layout and external components. In the actual application, fully evaluation is necessary.

Over-voltage and the over current beyond the absolute maximum rating should not be forced to the protection IC and external components. During the time until the fuse is open after detecting over-charge, a large current may flow through the FET. Select an FET with large enough current capacity in order to endure the large current.

Ricoh cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Ricoh product. If technical notes are not complied with the circuit which is used Ricoh product, Ricoh is not responsible for any damages and any accidents.

To connect the SC protector, connect the SC protector to the cell must be the last.

\*SC protector

Contact: Sony Chemical & Information Device Company Ltd.

Zip code 141-0032

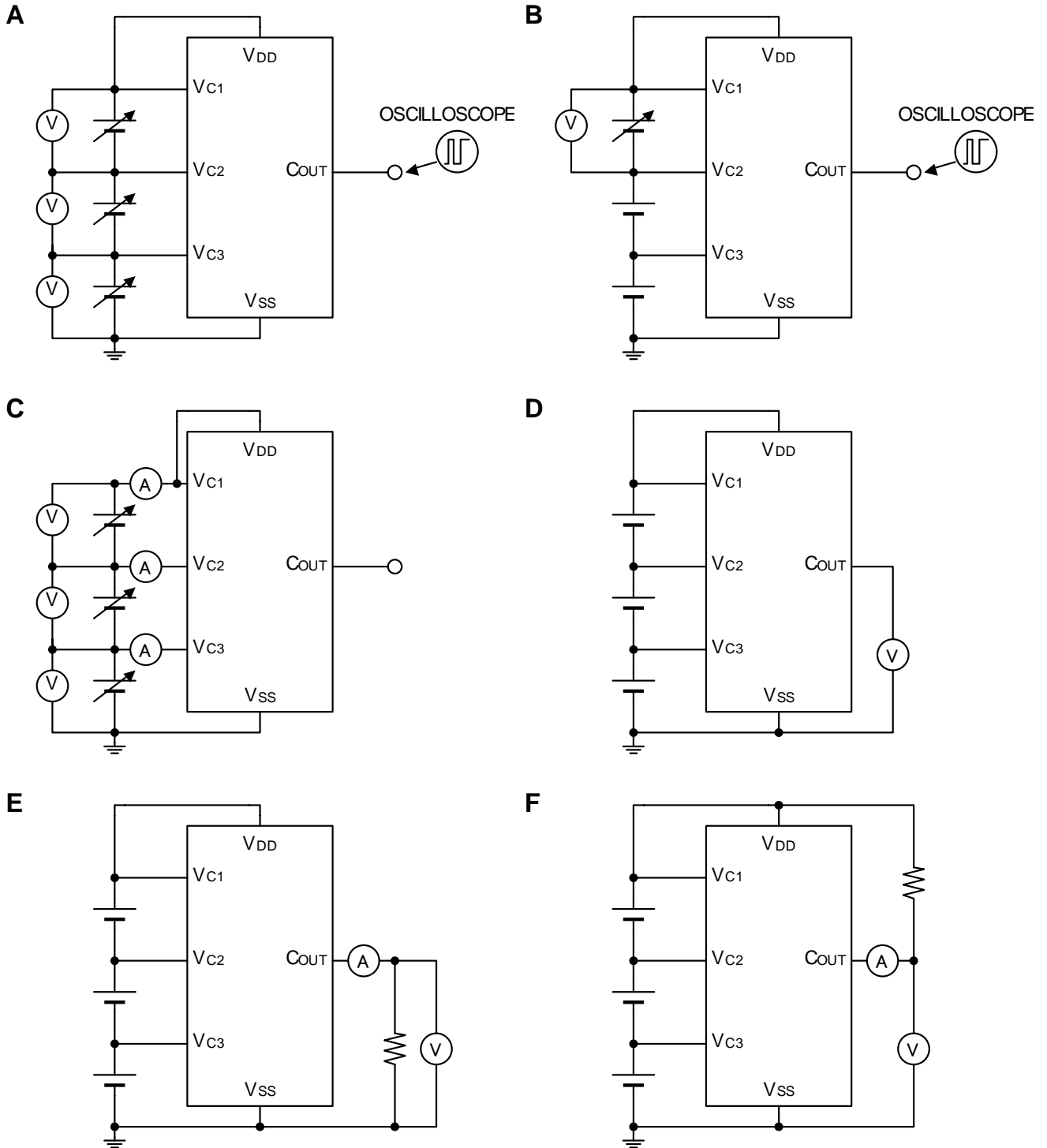
1-11-2 Osaki, Shinagawa, Tokyo

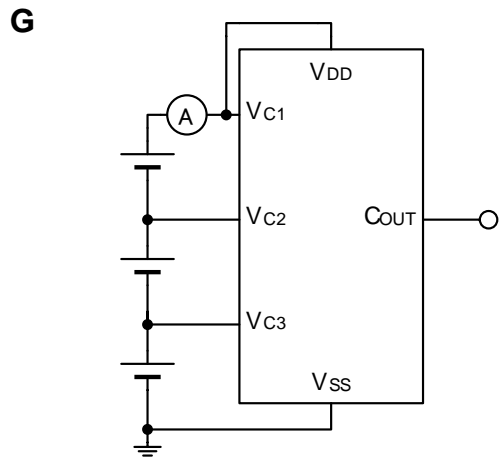
Gate-city Osaki East Tower 8F

Phone 03-5435-3946

<http://www.sonycid.jp>

TEST CIRCUITS





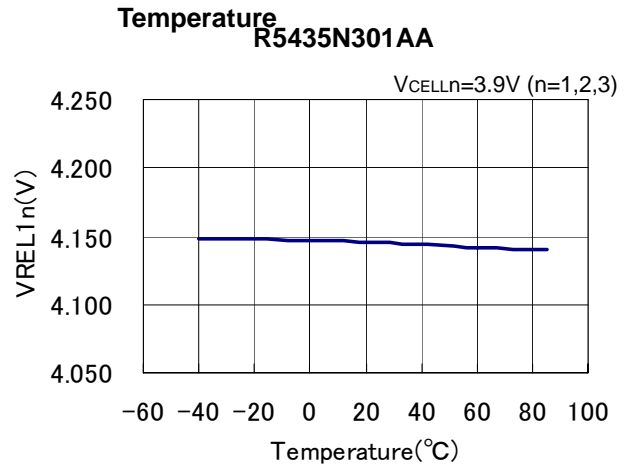
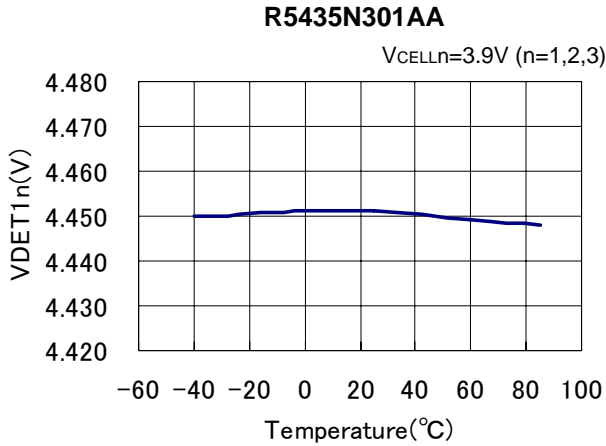
**Typical Characteristics were obtained with using those above circuits:**

- Test Circuit A: Typical characteristics 1), 2)
- Test Circuit B: Typical characteristics 3), 4), 6)
- Test Circuit C: Typical characteristics 5)
- Test Circuit D: Typical characteristics 7)
- Test Circuit E: Typical characteristics 8)
- Test Circuit F: Typical characteristics 9)
- Test Circuit G: Typical characteristics 10), 11)

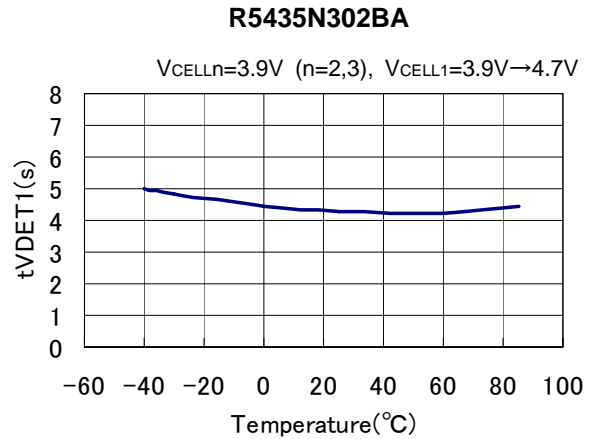
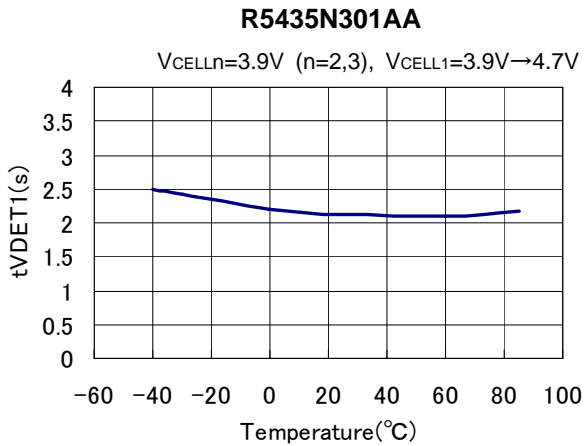
## TYPICAL CHARACTERISTICS

### Part1. vs. Temperature

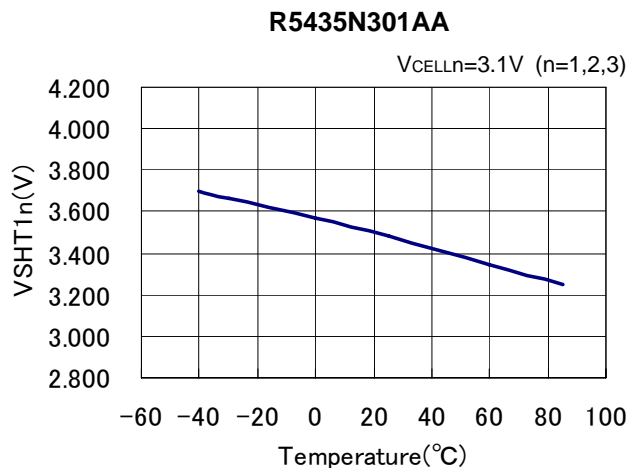
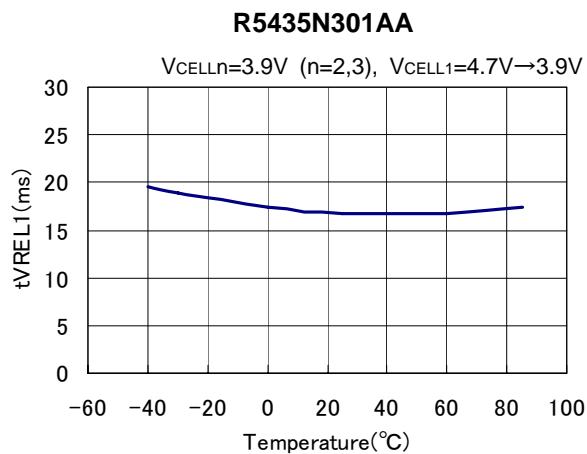
- 1) Over-charge voltage Threshold (CELLn) vs. Temperature    2) Over-charge Released Voltage (CELLn) vs. Temperature



- 3) Output Delay of Over-charge vs. Temperature



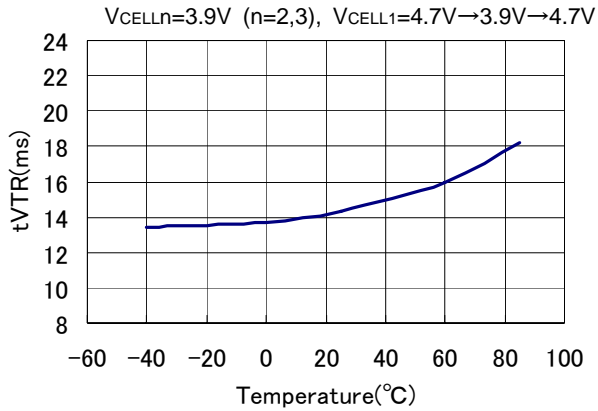
- 4) Output Delay of Release from Over-charge vs. Temperature    5) Shutdown Detector Threshold vs. Temperature



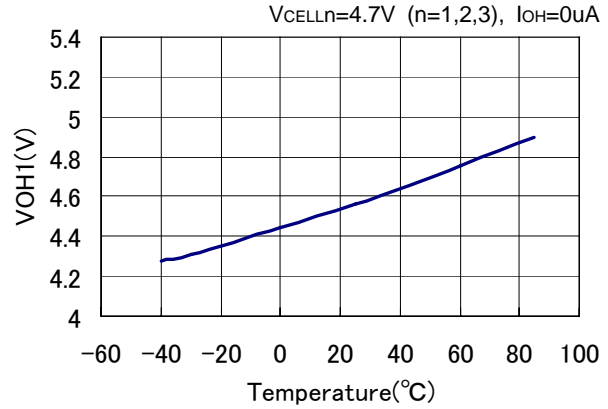


6) Output Delay of Over-charge Timer Reset vs. Temperature 7) C<sub>OUT</sub> Pch ON Voltage 1 vs. Temperature

R5435N301AA

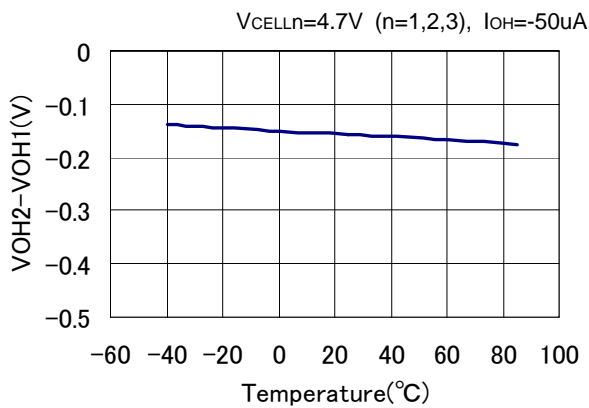


R5435N301AA



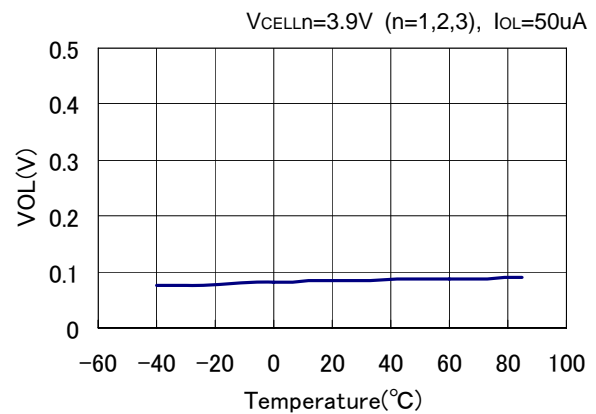
8) C<sub>OUT</sub> Pch ON Voltage 2 vs. Temperature

R5435N301AA



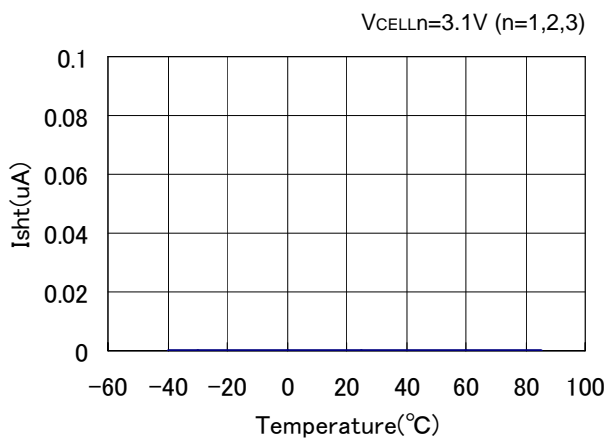
9) C<sub>OUT</sub> Nch ON Voltage vs. Temperature

R5435N301AA



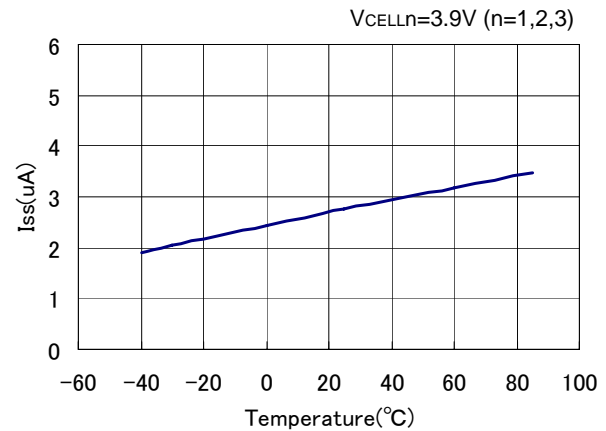
10) Shutdown Current vs. Temperature

R5435N301AA



11) Supply Current vs. Temperature

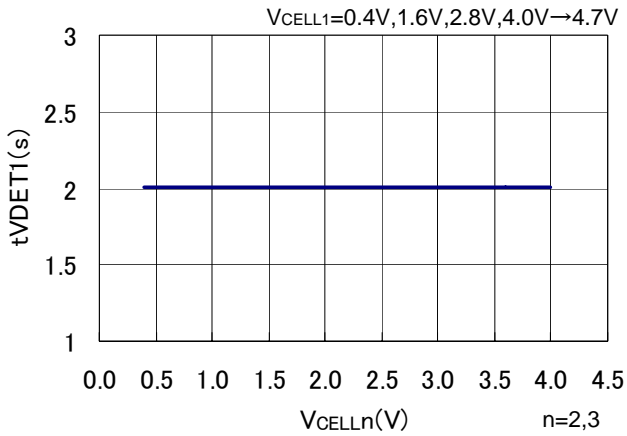
R5435N301AA



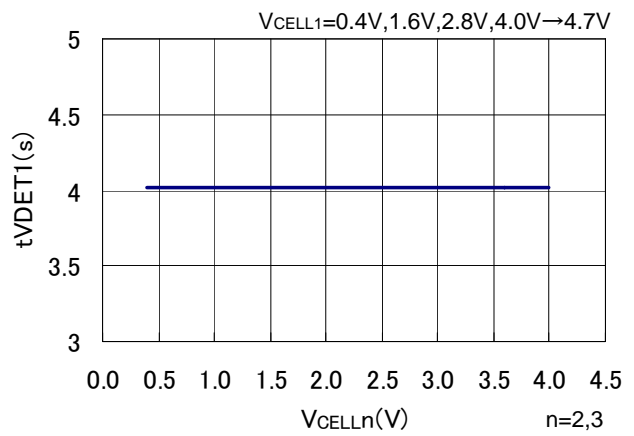
**Part2. Delay Time dependence on V<sub>DD</sub>**

**1) Output Delay of Over-charge vs. V<sub>DD</sub>**

**R5435N301AA**

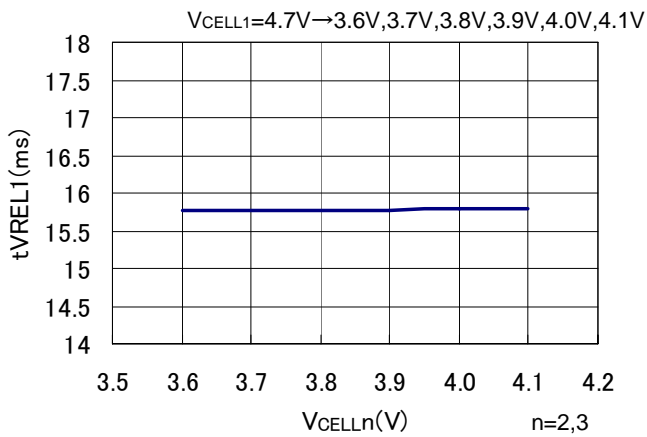


**R5435N302BA**



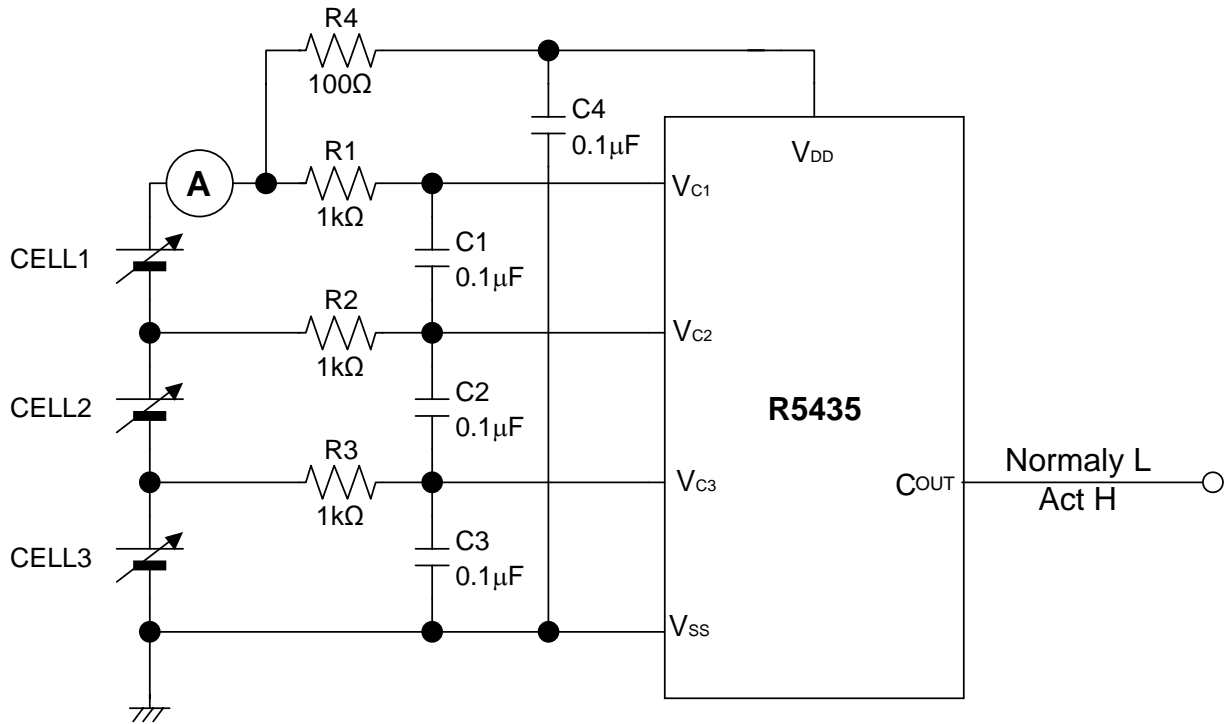
**2) Output Delay of Release from Over-charge vs. V<sub>DD</sub>**

**R5435N301AA**

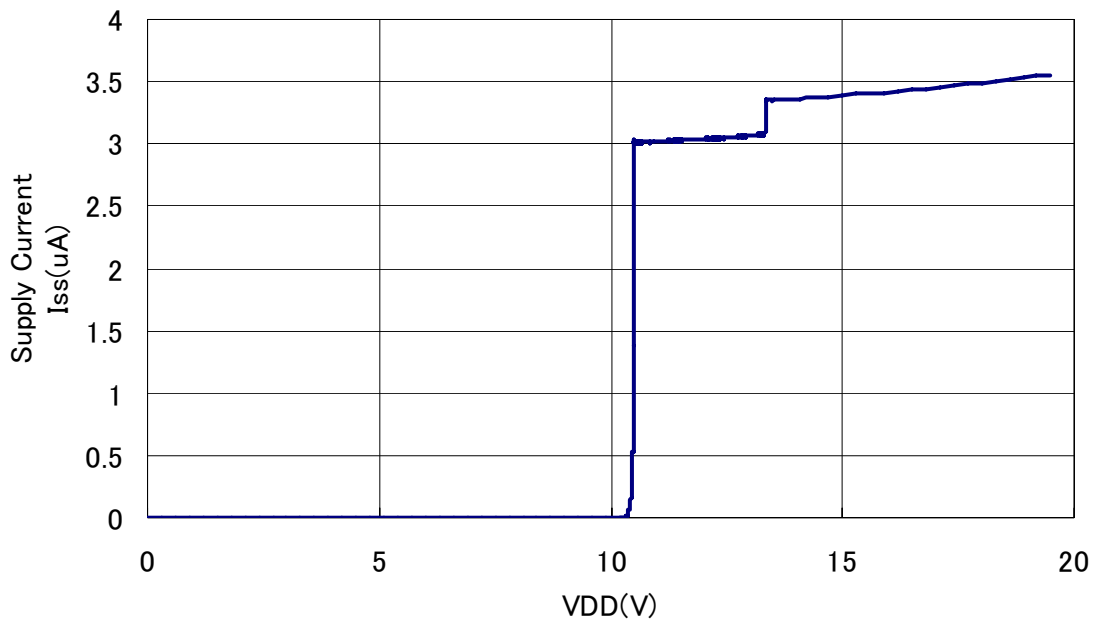


**Part3. Supply Current dependence on  $V_{DD}$  (R5435N301AA)**

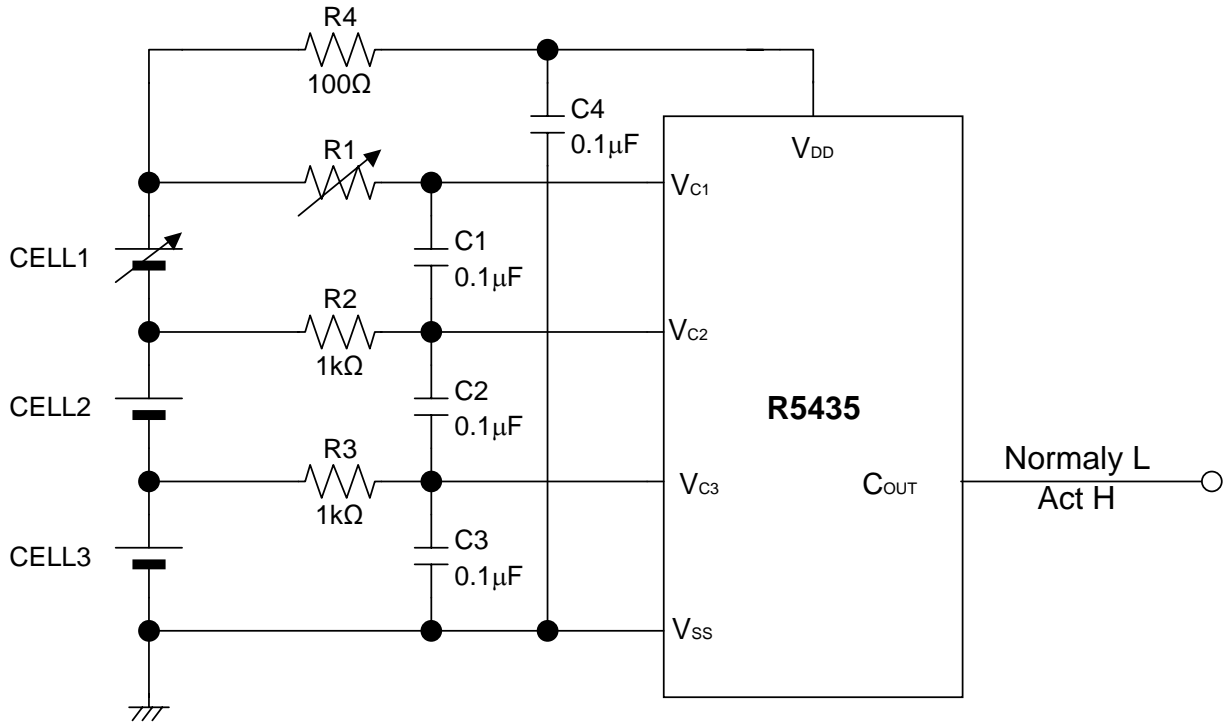
C1



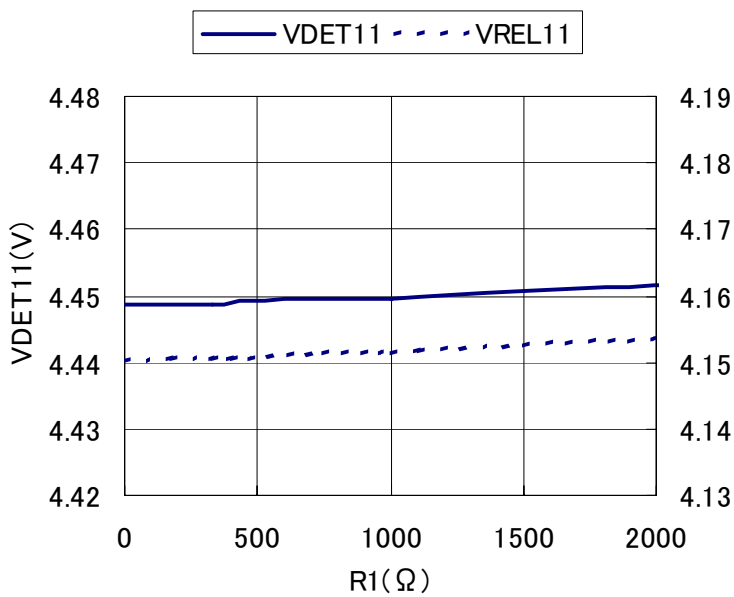
**3-cell protector Supply Current vs.  $V_{DD}$**



**Part4. Over-charge detector, Release voltage from Over-charge dependence on External Resistance value (R5435N301AA)**



**Over-charge Detector/Released Voltage from Over-charge vs. R1 (CELL1)**





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