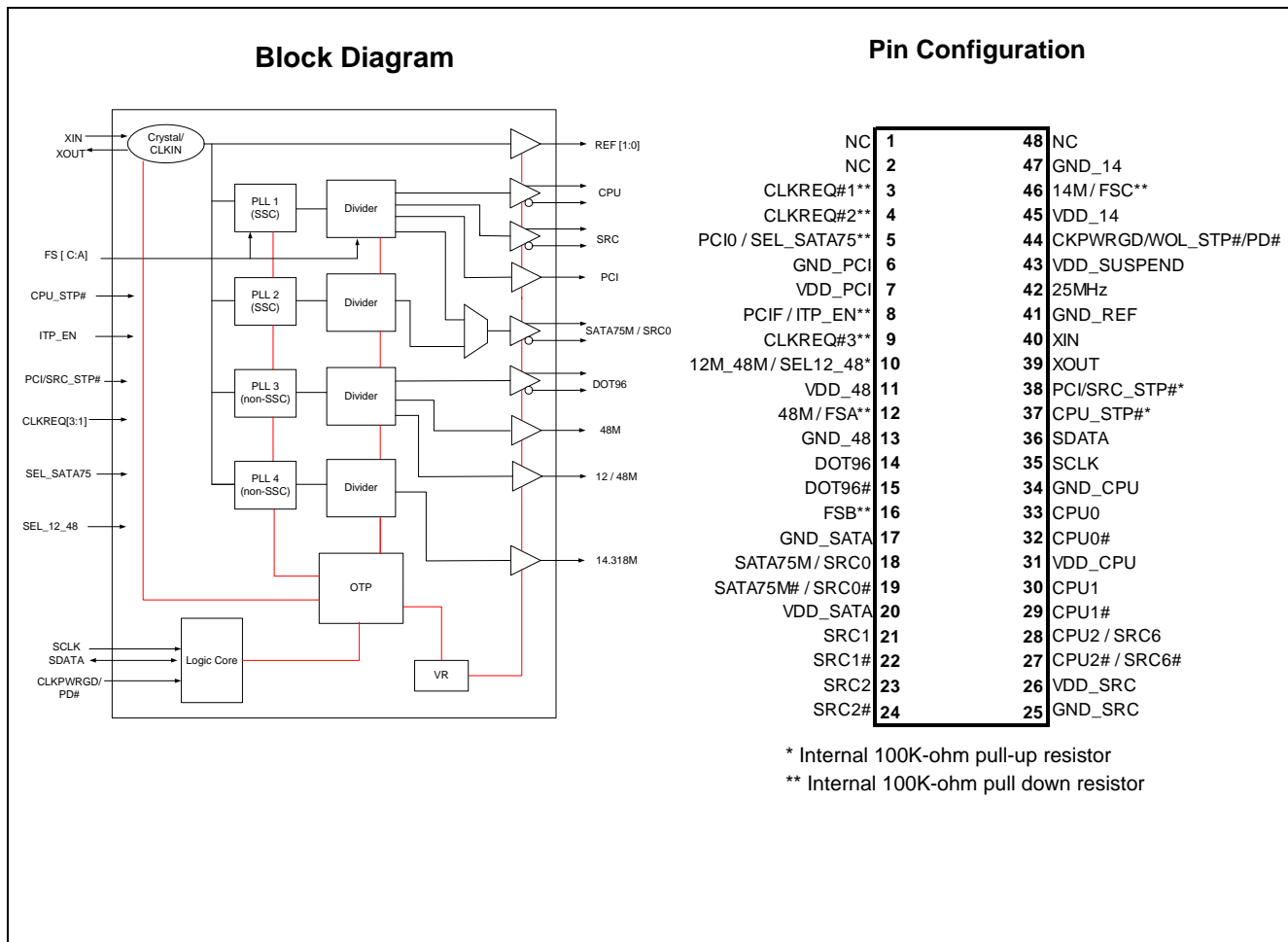


EProClock[®] Generator for Intel Tunnel Creek & Top Cliff

Features

- Compliant Intel CK505 Clock spec
- Low power push-pull type differential output buffers
- Integrated resistors on differential clocks
- Wireless friendly 3-bits slew rate control on single-ended clocks.
- Differential CPU clocks with selectable frequency
- 100MHz Differential SRC clocks
- 75MHz Differential SATA clocks
- 96MHz Differential DOT clock
- 48MHz USB clock
- Selectable 12 or 48MHz output
- 14.318MHz output
- Buffered Reference Clock 25MHz
- 25MHz Crystal Input or Clock input
- Support Wake-On-LAN (WOL)
- EProClock[®] Programmable Technology
- I²C support with readback capabilities
- Triangular Spread Spectrum profile for maximum electromagnetic interference (EMI) reduction
- Industrial Temperature -40°C to 85°C
- 3.3V Power supply
- 48-pin TSSOP package

| CPU | SRC | SATA75 | DOT96 | 48M | 48M/12M | 33M | 25M | 14.318M |
|-------|------|--------|-------|------|---------|-----|-----|---------|
| x2/x3 | x2/4 | x0/x1 | x 1 | x1/2 | x1 | x2 | x1 | x1 |



48-TSSOP Pin Definitions

| Pin No. | Name | Type | Description |
|---------|---------------------|----------------|---|
| 1 | NC | NC | No Connect. |
| 2 | NC | NC | No Connect. |
| 3 | CLKREQ#1** | I, PD | 3.3V clock request input (<i>internal 100K-ohm pull-down</i>) |
| 4 | CLKREQ#2** | I, PD | 3.3V clock request input (<i>internal 100K-ohm pull-down</i>) |
| 5 | PCI0 / SEL_SATA75** | I/O, SE PD | 33MHz clock output/3.3V LVTTTL input to enable 75MHz SATA (<i>internal 100K-ohm pull-down</i>) 0 = SATA75/SRC0 = 100MHz, 1 = SATA75/SRC0 = 75MHz |
| 6 | GND_PCI | GND | Ground for PCI clocks |
| 7 | VDD_PCI | PWR | 3.3V Power supply for PCI clocks |
| 8 | PCIF / ITP_EN** | I/O, SE, PD | 33 MHz free running clock output/3.3V LVTTTL input to enable SRC6 or CPU2_ITP (sampled on the CKPWRGD assertion) 0= SRC6, 1= CPU2 |
| 9 | CLKREQ#3** | I, PD | 3.3V clock request input (<i>internal 100K-ohm pull-down</i>) |
| 10 | 12_48M / SEL12_48* | I/O, SE PU | 12 MHz/ 48MHz Clock output/3.3V-tolerance input for 12MHz or 48MHz selection (Sampled at CKPWRGD assertion) (<i>internal 100K-ohm pull-up</i>) 0 = 48M, 1 = 12M |
| 11 | VDD_48 | PWR | 3.3V Power supply for 48MHz clocks |
| 12 | 48M / FSA** | I/O PD | Fixed 48 MHz clock output/3.3V-tolerant input for CPU frequency selection (<i>internal 100K-ohm pull-down</i>) Refer to DC Electrical Specifications table for Vil_FS and Vih_FS specifications. |
| 13 | GND_48 | GND | Ground for 48MHz clocks |
| 14 | DOT96 | O, DIF | Fixed true 96MHz clock output |
| 15 | DOT96# | O, DIF | Fixed complement 96MHz clock output |
| 16 | FSB** | I, PD | 3.3V-tolerant input for CPU frequency selection (<i>internal 100K-ohm pull-down</i>) Refer to DC Electrical Specifications table for Vil_FS and Vih_FS specifications. |
| 17 | GND_SATA | GND | Ground for SATA clock |
| 18 | SRC0 / SATA_75M | O, DIF | 75MHz or 100MHz True differential serial reference clock |
| 19 | SRC0# / SATA_75M# | O, DIF | 75MHz or 100MHz Complement differential serial reference clock |
| 20 | VDD_SATA | PWR | 3.3V Power supply for SATA clock |
| 21 | SRC1 | O, DIF | 100MHz True differential serial reference clock |
| 22 | SRC1# | O, DIF | 100MHz Complement differential serial reference clock |
| 23 | SRC2 | O, DIF | 100MHz True differential serial reference clock |
| 24 | SRC2# | O, DIF | 100MHz Complement differential serial reference clock |
| 25 | GND_SRC | GND | Ground for SRC clocks |
| 26 | VDD_SRC | PWR | 3.3V Power supply for SRC clocks |
| 27 | SRC6# / CPU2#_ITP | O, DIF | Selectable complementary differential CPU or SRC clock output. ITP_EN = 0 @ CK_PWRGD assertion = SRC6 ITP_EN = 1 @ CK_PWRGD assertion = CPU2 |
| 28 | SRC6 / CPU2_ITP, | O, DIF | Selectable True differential CPU or SRC clock output. ITP_EN = 0 @ CK_PWRGD assertion = SRC6 ITP_EN = 1 @ CK_PWRGD assertion = CPU2 |
| 29 | CPU1# | O, DIF | Complement differential CPU clock output |
| 30 | CPU1 | O, DIF | True differential CPU clock output |
| 31 | VDD_CPU | PWR | 3.3V Power supply for CPU clocks |
| 32 | CPU0# | O, DIF | Complement differential CPU clock output |
| 33 | CPU0 | O, DIF | True differential CPU clock output |
| 34 | GND_CPU | GND | Ground for clocks |

48-TSSOP Pin Definitions

| Pin No. | Name | Type | Description |
|---------|----------------------|---------|---|
| 35 | SCLK | I | SMBus compatible SCLOCK |
| 36 | SDATA | I/O | SMBus compatible SDATA |
| 37 | CPU_STOP#* | I, PU | 3.3V-tolerant input for stopping CPU outputs (<i>internal 100K-ohm pull-up</i>) |
| 38 | PCI_STOP#* | I, PU | 3.3V-tolerant input for stopping PCI and SRC outputs (<i>internal 100K-ohm pull-up</i>) |
| 39 | XOUT | O | 25.00MHz Crystal output |
| 40 | XIN | I | 25.00MHz Crystal input |
| 41 | GND_REF | GND | Ground for REF clock |
| 42 | 25MHz | O | 25MHz reference output clock |
| 43 | VDD_SUSPEND | PWR | 3.3V Power Supply for REF clock and power to support WOL |
| 44 | CKPWRGD/WOL_STP#/PD# | I | 3.3V LVTTTL input. This pin is a level sensitive strobe used to determine when latch inputs are valid and are ready to be sampled / Asynchronous active low input pin that stops all outputs except free running 25MHz when WOL_EN = "1" (<i>Byte 1 bit 1</i>) This pin becomes a real-time active low input for asserting power down (PD#) when WOL_EN = "0" (<i>Byte 1 bit 1</i>). |
| 45 | VDD_14 | PWR | 3.3V Power supply for 14.318MHz clock |
| 46 | 14.318M / FSC** | I/O, PD | Fixed 14.318MHz clock output/3.3V-tolerant input for CPU frequency selection (<i>internal 100K-ohm pull-down</i>) Refer to DC Electrical Specifications table for Vil_FS and Vih_FS specifications. |
| 47 | GND_14 | GND | Ground for 14.318MHz clock |
| 48 | NC | NC | No Connect. |

PC EProClock® Programmable Technology

PC EProClock® is the world's first non-volatile programmable PC clock. The PC EProClock® technology allows board designer to promptly achieve optimum compliance and clock signal integrity; historically, attainable typically through device and/or board redesigns.

PC EProClock® technology can be configured through SMBus or hard coded.

Features:

- > 4000 bits of configurations
- Can be configured through SMBus or hard coded

- Custom frequency sets
- Differential skew control on true or compliment or both
- Differential duty cycle control on true or compliment or both
- Differential amplitude control
- Differential and single-ended slew rate control
- Program Internal or External series resistor on single-ended clocks
- Program different spread profiles
- Program different spread modulation rate

Frequency Select Pin (FS)

| SEL_SATA | FSC | FSB | FSA | CPU | SRC | SATA | PCI |
|----------|-----|-----|-----|--------|--------|--------|-------|
| 0 | 0 | 0 | 0 | 100.00 | 100.00 | 100.00 | 33.33 |
| 0 | 0 | 0 | 1 | 100.00 | 100.00 | 100.00 | 33.33 |
| 0 | 0 | 1 | 0 | 83.33 | 100.00 | 100.00 | 33.33 |
| 0 | 0 | 1 | 1 | 83.33 | 100.00 | 100.00 | 33.33 |
| 0 | 1 | 0 | 0 | 133.33 | 100.00 | 100.00 | 33.33 |
| 0 | 1 | 0 | 1 | 133.33 | 100.00 | 100.00 | 33.33 |
| 0 | 1 | 1 | 0 | 166.67 | 100.00 | 100.00 | 33.33 |
| 0 | 1 | 1 | 1 | 166.67 | 100.00 | 100.00 | 33.33 |
| 1 | 0 | 0 | 0 | 100.00 | 100.00 | 75.00 | 33.33 |
| 1 | 0 | 0 | 1 | 100.00 | 100.00 | 75.00 | 33.33 |
| 1 | 0 | 1 | 0 | 83.33 | 100.00 | 75.00 | 33.33 |
| 1 | 0 | 1 | 1 | 83.33 | 100.00 | 75.00 | 33.33 |
| 1 | 1 | 0 | 0 | 133.33 | 100.00 | 75.00 | 33.33 |
| 1 | 1 | 0 | 1 | 133.33 | 100.00 | 75.00 | 33.33 |
| 1 | 1 | 1 | 0 | 166.67 | 100.00 | 75.00 | 33.33 |
| 1 | 1 | 1 | 1 | 166.67 | 100.00 | 75.00 | 33.33 |

Frequency Select Pin FS

Apply the appropriate logic levels to FS inputs before CKPWRGD assertion to achieve host clock frequency selection. When the clock chip sampled HIGH on CKPWRGD and indicates that VTT voltage is stable then FS input values are sampled. This process employs a one-shot functionality and once the CKPWRGD sampled a valid HIGH, all other FS, and CKPWRGD transitions are ignored except in test mode.

Wake-On-LAN (WOL) Support

When power is applied to the VDD_SUSPEND pin, the 25MHz reference clock output will be enabled under all conditions, unless the WOL_EN bit, Byte 1 bit 1, is set to "0". When the WOL_EN bit Byte 1 bit 1, is set to "0", the WOL_STP# pin will function as a PD# pin. By default, the WOL_EN bit is enabled and set to a "1". The clock device will support "out-of-the-box" WOL or after a power outage by enabling the 25MHz reference clock output when the clock device powers up for the very first time with only power applied to the VDD_SUSPEND pin and all other VDD pins power have not been applied.

Serial Data Interface

To enhance the flexibility and function of the clock synthesizer, a two-signal serial interface is provided. Through the Serial Data Interface, various device functions, such as individual clock output buffers are individually enabled or disabled. The registers associated with the Serial Data Interface initialize to their default setting at power-up. The use of this interface is optional. Clock device register changes are normally made at system initialization, if any are required. The interface cannot be used during system operation for power management functions.

Data Protocol

The clock driver serial protocol accepts byte write, byte read, block write, and block read operations from the controller. For block write/read operation, access the bytes in sequential order from lowest to highest (most significant bit first) with the ability to stop after any complete byte is transferred. For byte write and byte read operations, the system controller can access individually indexed bytes. The offset of the indexed byte is encoded in the command code described in *Table 1*.

The block write and block read protocol is outlined in *Table 2* while *Table 3* outlines byte write and byte read protocol. The slave receiver address is 11010010 (D2h).

Table 1. Command Code Definition

| Bit | Description |
|-------|--|
| 7 | 0 = Block read or block write operation, 1 = Byte read or byte write operation |
| (6:0) | Byte offset for byte read or byte write operation. For block read or block write operations, these bits should be '000000' |

Table 2. Block Read and Block Write Protocol

| Block Write Protocol | | Block Read Protocol | |
|----------------------|-------------------------------|---------------------|-------------------------------------|
| Bit | Description | Bit | Description |
| 1 | Start | 1 | Start |
| 8:2 | Slave address–7 bits | 8:2 | Slave address–7 bits |
| 9 | Write | 9 | Write |
| 10 | Acknowledge from slave | 10 | Acknowledge from slave |
| 18:11 | Command Code–8 bits | 18:11 | Command Code–8 bits |
| 19 | Acknowledge from slave | 19 | Acknowledge from slave |
| 27:20 | Byte Count–8 bits | 20 | Repeat start |
| 28 | Acknowledge from slave | 27:21 | Slave address–7 bits |
| 36:29 | Data byte 1–8 bits | 28 | Read = 1 |
| 37 | Acknowledge from slave | 29 | Acknowledge from slave |
| 45:38 | Data byte 2–8 bits | 37:30 | Byte Count from slave–8 bits |
| 46 | Acknowledge from slave | 38 | Acknowledge |
| | Data Byte /Slave Acknowledges | 46:39 | Data byte 1 from slave–8 bits |
| | Data Byte N–8 bits | 47 | Acknowledge |
| | Acknowledge from slave | 55:48 | Data byte 2 from slave–8 bits |
| | Stop | 56 | Acknowledge |
| | | | Data bytes from slave / Acknowledge |
| | | | Data Byte N from slave–8 bits |
| | | | NOT Acknowledge |
| | | | Stop |

Table 3. Byte Read and Byte Write Protocol

| Byte Write Protocol | | Byte Read Protocol | |
|---------------------|------------------------|--------------------|------------------------|
| Bit | Description | Bit | Description |
| 1 | Start | 1 | Start |
| 8:2 | Slave address–7 bits | 8:2 | Slave address–7 bits |
| 9 | Write | 9 | Write |
| 10 | Acknowledge from slave | 10 | Acknowledge from slave |
| 18:11 | Command Code–8 bits | 18:11 | Command Code–8 bits |
| 19 | Acknowledge from slave | 19 | Acknowledge from slave |
| 27:20 | Data byte–8 bits | 20 | Repeated start |
| 28 | Acknowledge from slave | 27:21 | Slave address–7 bits |
| 29 | Stop | 28 | Read |
| | | 29 | Acknowledge from slave |
| | | 37:30 | Data from slave–8 bits |
| | | 38 | NOT Acknowledge |
| | | 39 | Stop |

Control Registers

Byte 0: Control Register 0

| Bit | @Pup | Name | Description |
|-----|------|---------------|--|
| 7 | 0 | RESERVED | RESERVED |
| 6 | 0 | RESERVED | RESERVED |
| 5 | 0 | Spread Enable | Enable spread for CPU/SRC/PCI outputs 0=Disable, 1= -0.5% |
| 4 | HW | SEL_SATA | See Table 1 for SATA/SRC selection. |
| 3 | 0 | RESERVED | RESERVED |
| 2 | HW | FSC | See Table 1 for CPU Frequency selection Table |
| 1 | HW | FSB | |
| 0 | HW | FSA | |

Byte 1: Control Register 1

| Bit | @Pup | Name | Description |
|-----|------|----------------|--|
| 7 | 1 | DOT96_OE | Output enable for DOT96 0 = Output Disabled, 1 = Output Enabled |
| 6 | 1 | SATA75/SRC0_OE | Output enable for SATA75/SRC0 0 = Output Disabled, 1 = Output Enabled |
| 5 | 1 | CPU2/SRC6_OE | Output enable for CPU2/SRC6 0 = Output Disabled, 1 = Output Enabled |
| 4 | 1 | SRC2 | Output enable for SRC2 0 = Output Disabled, 1 = Output Enabled |
| 3 | 1 | SRC1 | Output enable for SRC1 0 = Output Disabled, 1 = Output Enabled |
| 2 | 1 | RESERVED | RESERVED |
| 1 | 1 | WOL_EN | Wake-On-LAN Enable bit 25MHz free running during VDD Suspend (S-states). If this bit is set to 0, the XTAL OSC will also be powered down in the Suspend States) |
| 0 | 0 | RESERVED | RESERVED |

Byte 2: Control Register 2

| Bit | @Pup | Name | Description |
|-----|------|-----------|---|
| 7 | 1 | 48M_OE | Output enable for 48M 0 = Output Disabled, 1 = Output Enabled |
| 6 | 0 | RESERVED | RESERVED |
| 5 | 1 | 14M_OE | Output enable for 14M 0 = Output Disabled, 1 = Output Enabled |
| 4 | 1 | 25M_OE | Output enable for 25M 0 = Output Disabled, 1 = Output Enabled |
| 3 | 1 | 12_48M_OE | Output enable for 12_48M 0 = Output Disabled, 1 = Output Enabled |
| 2 | 1 | PCI0_OE | Output enable for PCI0 0 = Output Disabled, 1 = Output Enabled |
| 1 | 1 | PCIF_OE | Output enable for PCIF 0 = Output Disabled, 1 = Output Enabled |
| 0 | 0 | RESERVED | RESERVED |

Byte 3: Control Register 3

| Bit | @Pup | Name | Description |
|-----|------|-----------|---|
| 7 | 1 | CPU1_OE | Output enable for CPU1 0 = Output Disabled, 1 = Output Enabled |
| 6 | 1 | CPU0_OE | Output enable for CPU0 0 = Output Disabled, 1 = Output Enabled |
| 5 | 0 | CLKREQ#_3 | Clock request for SRC2 0=Not controlled, 1= Controlled |
| 4 | 0 | CLKREQ#_3 | Clock request for SRC6 (does not apply to CPU clock) 0=Not controlled, 1= Controlled |
| 3 | 0 | CLKREQ#_2 | Clock request for SRC2 0=Not controlled, 1= Controlled |
| 2 | 0 | CLKREQ#_2 | Clock request for SATA75M/SRC0 0=Not controlled, 1= Controlled |
| 1 | 0 | CLKREQ#_1 | Clock request for SRC1 0=Not controlled, 1= Controlled |
| 0 | 0 | CLKREQ#_1 | Clock request for SATA75M/SRC0 0=Not controlled, 1= Controlled |

Byte 4: Control Register 4

| Bit | @Pup | Name | Description |
|-----|------|----------|--|
| 7 | 0 | RESERVED | RESERVED |
| 6 | 0 | CPU1 | CPU1 Free Run Control 0= Free Running, 1= Stoppable |
| 5 | HW | 12_48M | Selectable 12_48M status 0= 48M, 1=12M |
| 4 | 0 | CPU2 | CPU2 Free Run Control 0= Free Running, 1= Stoppable |
| 3 | HW | ITP_EN | SelectableCPUe_ITP/ SRC6 status 0= SRC6, 1=CPU2 |
| 2 | 0 | RESERVED | RESERVED |
| 1 | 0 | CPU0 | CPU0 Free Run Control 0= Free Running, 1= Stoppable |
| 0 | 0 | RESERVED | RESERVED |

Byte 5: Control Register 5

| Bit | @Pup | Name | Description |
|-----|------|-------------|---|
| 7 | 0 | RESERVED | RESERVED |
| 6 | 0 | RESERVED | RESERVED |
| 5 | 0 | RESERVED | RESERVED |
| 4 | 1 | SATA75/SRC0 | SATA75/SRC0 Free Run Control 0= Free Running, 1= Stoppable |
| 3 | 0 | SRC6 | SRC6 Free Run Control 0= Free Running, 1= Stoppable |
| 2 | 0 | SRC2 | SRC2 Free Run Control 0= Free Running, 1= Stoppable |
| 1 | 0 | SRC1 | SRC1 Free Run Control 0= Free Running, 1= Stoppable |
| 0 | 0 | RESERVED | RESERVED |

Byte 6: Control Register 6

| Bit | @Pup | Name | Description |
|-----|------|-----------|---|
| 7 | 0 | CPU_AMP | CPU amplitude adjustment 00= 700mV, 01=800mV, 10=900mV, 11= 1000mV |
| 6 | 1 | CPU_AMP | |
| 5 | 0 | SRC_AMP | SRC amplitude adjustment 00= 700mV, 01=800mV, 10=900mV, 11= 1000mV |
| 4 | 1 | SRC_AMP | |
| 3 | 0 | DOT96_AMP | DOT96 amplitude adjustment 00= 700mV, 01=800mV, 10=900mV, 11= 1000mV |
| 2 | 1 | DOT96_AMP | |
| 1 | 0 | SATA_AMP | SATA75/SRC0 amplitude adjustment 00= 700mV, 01=800mV, 10=900mV, 11= 1000mV |
| 0 | 1 | SATA_AMP | |

Byte 7: Vendor ID

| Bit | @Pup | Name | Description |
|-----|------|-----------------|---------------------|
| 7 | 0 | Rev Code Bit 3 | Revision Code Bit 3 |
| 6 | 0 | Rev Code Bit 2 | Revision Code Bit 2 |
| 5 | 0 | Rev Code Bit 1 | Revision Code Bit 1 |
| 4 | 0 | Rev Code Bit 0 | Revision Code Bit 0 |
| 3 | 1 | Vendor ID bit 3 | Vendor ID Bit 3 |
| 2 | 0 | Vendor ID bit 2 | Vendor ID Bit 2 |
| 1 | 0 | Vendor ID bit 1 | Vendor ID Bit 1 |
| 0 | 0 | Vendor ID bit 0 | Vendor ID Bit 0 |

Byte 8: Control Register 8

| Bit | @Pup | Name | Description |
|-----|------|------|---|
| 7 | 0 | BC7 | Byte count register for block read operation. The default value for Byte count is 15 In order to read beyond Byte 15, the user should change the byte count limit.to or beyond the byte that is desired to be read. |
| 6 | 0 | BC6 | |
| 5 | 0 | BC5 | |
| 4 | 0 | BC4 | |
| 3 | 1 | BC3 | |
| 2 | 1 | BC2 | |
| 1 | 1 | BC1 | |
| 0 | 1 | BC0 | |

Byte 9: Control Register 9

| Bit | @Pup | Name | Description |
|-----|------|----------|--|
| 7 | 1 | RESERVED | RESERVED |
| 6 | 1 | RESERVED | RESERVED |
| 5 | 1 | RESERVED | RESERVED |
| 4 | 0 | RESERVED | RESERVED |
| 3 | 0 | RESERVED | RESERVED |
| 2 | 0 | RESERVED | RESERVED |
| 1 | 0 | PCI0 | PCI0 Free Run Control 0= Free Running, 1= Stoppable |
| 0 | 1 | PCIF | PCIF Free Run Control 0= Free Running, 1= Stoppable |

Byte 10: Control Register 10

| Bit | @Pup | Name | Description |
|-----|------|----------|-------------|
| 7 | 0 | RESERVED | RESERVED |
| 6 | 0 | RESERVED | RESERVED |
| 5 | 0 | RESERVED | RESERVED |
| 4 | 0 | RESERVED | RESERVED |
| 3 | 0 | RESERVED | RESERVED |
| 2 | 0 | RESERVED | RESERVED |
| 1 | 0 | RESERVED | RESERVED |
| 0 | 0 | RESERVED | RESERVED |

Byte 11: Control Register 11

| Bit | @Pup | Name | Description | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-------------------|------|-------------|--|------|---------------------|------|------|-----------------|--|---|---|---|---------------------|--|---|---|---|--|---|---|---|--|---|---|---|--|---|---|---|---------|---|---|---|--|---|---|---|-------------------|---|---|---|
| 7 | 1 | 14M_Bit2 | Drive Strength Control - Bit[2:0] Normal mode default '101' Wireless Friendly Mode default to '111' <table border="1" style="margin-top: 10px;"> <thead> <tr> <th>Mode</th> <th>Bit2</th> <th>Bit1</th> <th>Bit0</th> <th>Buffer Strength</th> </tr> </thead> <tbody> <tr><td></td><td>0</td><td>0</td><td>0</td><td rowspan="8" style="text-align: center;"> Strong ↓ Weak </td></tr> <tr><td></td><td>0</td><td>0</td><td>1</td></tr> <tr><td></td><td>0</td><td>1</td><td>0</td></tr> <tr><td></td><td>0</td><td>1</td><td>1</td></tr> <tr><td></td><td>1</td><td>0</td><td>0</td></tr> <tr style="background-color: yellow;"><td>Default</td><td>1</td><td>0</td><td>1</td></tr> <tr><td></td><td>1</td><td>1</td><td>0</td></tr> <tr><td>Wireless Friendly</td><td>1</td><td>1</td><td>1</td></tr> </tbody> </table> | Mode | Bit2 | Bit1 | Bit0 | Buffer Strength | | 0 | 0 | 0 | Strong ↓ Weak | | 0 | 0 | 1 | | 0 | 1 | 0 | | 0 | 1 | 1 | | 1 | 0 | 0 | Default | 1 | 0 | 1 | | 1 | 1 | 0 | Wireless Friendly | 1 | 1 | 1 |
| Mode | Bit2 | Bit1 | | Bit0 | Buffer Strength | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | 0 | 0 | | 0 | Strong ↓ Weak | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | 0 | 0 | | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | 0 | 1 | | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | 0 | 1 | | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | 1 | 0 | | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Default | 1 | 0 | | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | 1 | 1 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Wireless Friendly | 1 | 1 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 6 | 0 | 14M_Bit1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 5 | 1 | 14M_Bit0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 4 | 1 | 25M_Bit2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 3 | 0 | 25M_Bit1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 2 | 1 | 25M_Bit0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | 12_48M_Bit2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 12_48M_Bit0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

Byte 12: Byte Count

| Bit | @Pup | Name | Description | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-------------------|------|-------------|--|------|---------------------|------|------|-----------------|--|---|---|---|---------------------|--|---|---|---|--|---|---|---|--|---|---|---|--|---|---|---|---------|---|---|---|--|---|---|---|-------------------|---|---|---|
| 7 | 1 | 48M_Bit2 | Drive Strength Control - Bit[2:0] Normal mode default '101' Wireless Friendly Mode default to '111' <table border="1" style="margin-top: 10px;"> <thead> <tr> <th>Mode</th> <th>Bit2</th> <th>Bit1</th> <th>Bit0</th> <th>Buffer Strength</th> </tr> </thead> <tbody> <tr><td></td><td>0</td><td>0</td><td>0</td><td rowspan="8" style="text-align: center;"> Strong ↓ Weak </td></tr> <tr><td></td><td>0</td><td>0</td><td>1</td></tr> <tr><td></td><td>0</td><td>1</td><td>0</td></tr> <tr><td></td><td>0</td><td>1</td><td>1</td></tr> <tr><td></td><td>1</td><td>0</td><td>0</td></tr> <tr style="background-color: yellow;"><td>Default</td><td>1</td><td>0</td><td>1</td></tr> <tr><td></td><td>1</td><td>1</td><td>0</td></tr> <tr><td>Wireless Friendly</td><td>1</td><td>1</td><td>1</td></tr> </tbody> </table> | Mode | Bit2 | Bit1 | Bit0 | Buffer Strength | | 0 | 0 | 0 | Strong ↓ Weak | | 0 | 0 | 1 | | 0 | 1 | 0 | | 0 | 1 | 1 | | 1 | 0 | 0 | Default | 1 | 0 | 1 | | 1 | 1 | 0 | Wireless Friendly | 1 | 1 | 1 |
| Mode | Bit2 | Bit1 | | Bit0 | Buffer Strength | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | 0 | 0 | | 0 | Strong ↓ Weak | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | 0 | 0 | | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | 0 | 1 | | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | 0 | 1 | | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | 1 | 0 | | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Default | 1 | 0 | | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | 1 | 1 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Wireless Friendly | 1 | 1 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 6 | 0 | 48M_Bit1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 5 | 1 | 48M_Bit0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 4 | 1 | PCI0_Bit2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 3 | 0 | PCI0_Bit1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 2 | 1 | PCI0_Bit0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | RESERVED | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 12_48M_Bit1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

Byte 13: Control Register 13

| Bit | @Pup | Name | Description | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-------------------|------|------------------------|---|--|------|------|------|-----------------|--|---|---|---|--|--|---|---|---|--|---|---|---|--|---|---|---|--|---|---|---|---------|---|---|---|--|---|---|---|-------------------|---|---|---|
| 7 | 1 | PCIF_Bit2 | Drive Strength Control - Bit[2:0] Normal mode default '101' Wireless Friendly Mode default to '111' | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 6 | 0 | PCIF_Bit1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 5 | 1 | PCIF_Bit0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | <table border="1"> <thead> <tr> <th>Mode</th> <th>Bit2</th> <th>Bit1</th> <th>Bit0</th> <th>Buffer Strength</th> </tr> </thead> <tbody> <tr> <td></td> <td>0</td> <td>0</td> <td>0</td> <td rowspan="7"> <div style="text-align: center;">Strong</div> <div style="text-align: center;">↓</div> <div style="text-align: center;">Weak</div> </td> </tr> <tr> <td></td> <td>0</td> <td>0</td> <td>1</td> </tr> <tr> <td></td> <td>0</td> <td>1</td> <td>0</td> </tr> <tr> <td></td> <td>0</td> <td>1</td> <td>1</td> </tr> <tr> <td></td> <td>1</td> <td>0</td> <td>0</td> </tr> <tr> <td style="background-color: yellow;">Default</td> <td style="background-color: yellow;">1</td> <td style="background-color: yellow;">0</td> <td style="background-color: yellow;">1</td> </tr> <tr> <td></td> <td>1</td> <td>1</td> <td>0</td> </tr> <tr> <td>Wireless Friendly</td> <td>1</td> <td>1</td> <td>1</td> </tr> </tbody> </table> | Mode | Bit2 | Bit1 | Bit0 | Buffer Strength | | 0 | 0 | 0 | <div style="text-align: center;">Strong</div> <div style="text-align: center;">↓</div> <div style="text-align: center;">Weak</div> | | 0 | 0 | 1 | | 0 | 1 | 0 | | 0 | 1 | 1 | | 1 | 0 | 0 | Default | 1 | 0 | 1 | | 1 | 1 | 0 | Wireless Friendly | 1 | 1 | 1 |
| Mode | Bit2 | Bit1 | Bit0 | Buffer Strength | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | 0 | 0 | 0 | <div style="text-align: center;">Strong</div> <div style="text-align: center;">↓</div> <div style="text-align: center;">Weak</div> | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | 0 | 0 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | 0 | 1 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | 0 | 1 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | 1 | 0 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Default | 1 | 0 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | 1 | 1 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Wireless Friendly | 1 | 1 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 4 | 0 | RESERVED | RESERVED | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 3 | 0 | RESERVED | RESERVED | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 2 | 0 | RESERVED | RESERVED | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | RESERVED | RESERVED | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | Wireless Friendly mode | Wireless Friendly Mode 0 = Disabled, Default all single-ended clocks slew rate config bits to '101' 1 = Enabled, Default all single-ended clocks slew rate config bits to '111' | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

Byte 14: Control Register 14

| Bit | @Pup | Name | Description |
|-----|------|----------|--|
| 7 | 1 | RESERVED | RESERVED |
| 6 | 0 | RESERVED | RESERVED |
| 5 | 1 | RESERVED | RESERVED |
| 4 | 0 | OTP_4 | OTP_ID Identification for programmed device |
| 3 | 0 | OTP_3 | |
| 2 | 0 | OTP_2 | |
| 1 | 0 | OTP_1 | |
| 0 | 0 | OTP_0 | |

Table 4. Output Driver Status during CPU_STP# & PCIS_STP#

| | | CPU_STP# Asserted | PCI_STP# Asserted | CLKREQ# Asserted | SMBus OE Disabled |
|---------------------|---------------|----------------------|----------------------|---------------------|-------------------|
| Single-ended Clocks | Stoppable | Running | Driven Low | Running | Driven low |
| | Non stoppable | Running | Running | Running | |
| Differential Clocks | Stoppable | Clock driven high | Clock driven high | Clock driven low | Clock driven low |
| | | Clock# driven low | Clock# driven low | Clock# driven low | |
| | Non stoppable | Running | Running | Running | |

Table 5. Output Driver Status

| | All Single-ended Clocks | | All Differential Clocks | |
|----------------------|-------------------------|----------|-------------------------|--------|
| | w/o Strap | w/ Strap | Clock | Clock# |
| PD# = 0 (Power down) | Low | Hi-z | Low | Low |

Table 6. Crystal Recommendations

| Frequency (Fund) | Cut | Loading | Load Cap | Drive (max.) | Shunt Cap (max.) | Motional (max.) | Tolerance (max.) | Stability (max.) | Aging (max.) |
|------------------|-----|----------|----------|--------------|------------------|-----------------|------------------|------------------|--------------|
| 25.000MHz | AT | Parallel | 20 pF | 0.1 mW | 5 pF | 0.016 pF | 35 ppm | 30 ppm | 5 ppm |

The SL28EB719 requires a Parallel Resonance Crystal. Substituting a series resonance crystal causes the SL28EB719 to operate at the wrong frequency and violates the ppm specification. For most applications there is a 300-ppm frequency shift between series and parallel crystals due to incorrect loading.

Crystal Loading

Crystal loading plays a critical role in achieving low ppm performance. To realize low ppm performance, use the total capacitance the crystal sees to calculate the appropriate capacitive loading (CL).

Figure 1 shows a typical crystal configuration using the two trim capacitors. It is important that the trim capacitors are in series with the crystal. It is not true that load capacitors are in parallel with the crystal and are approximately equal to the load capacitance of the crystal.

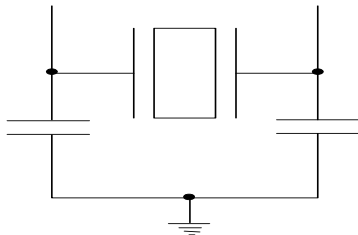


Figure 1. Crystal Capacitive Clarification

Calculating Load Capacitors

In addition to the standard external trim capacitors, consider the trace capacitance and pin capacitance to calculate the crystal loading correctly. Again, the capacitance on each side is in series with the crystal. The total capacitance on both side is twice the specified crystal load capacitance (CL). Trim capacitors are calculated to provide equal capacitive loading on both sides.

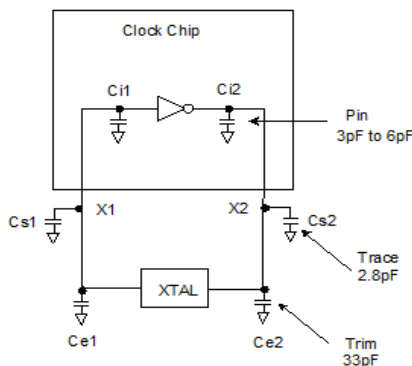


Figure 2. Crystal Loading Example

Use the following formulas to calculate the trim capacitor values for Ce1 and Ce2.

Load Capacitance (each side)

$$C_e = 2 * CL - (C_s + C_i)$$

Total Capacitance (as seen by the crystal)

$$CL_e = \frac{1}{\left(\frac{1}{C_{e1} + C_{s1} + C_{i1}} + \frac{1}{C_{e2} + C_{s2} + C_{i2}}\right)}$$

- CL.....Crystal load capacitance
- CL_e..... Actual loading seen by crystal using standard value trim capacitors
- C_e..... External trim capacitors
- C_s..... Stray capacitance (terraced)
- C_i Internal capacitance (lead frame, bond wires, etc.)

PD# (Power down) Clarification

The CKPWRGD/PD# pin is a dual-function pin. During initial power up, the pin functions as CKPWRGD. Once CKPWRGD has been sampled HIGH by the clock chip, the pin assumes PD# functionality. The PD# pin is an asynchronous active LOW input used to shut off all clocks cleanly before shutting off power to the device. This signal is synchronized internally to the device before powering down the clock synthesizer. PD# is also an asynchronous input for powering up the system. When PD# is asserted LOW, clocks are driven to a LOW value and held before turning off the VCOs and the crystal oscillator.

PD# (Power down) Assertion

When PD is sampled HIGH by two consecutive rising edges of CPUC, all single-ended outputs will be held LOW on their next HIGH-to-LOW transition and differential clocks must held LOW. When PD mode is desired as the initial power on state, PD must be asserted HIGH in less than 10 μs after asserting CKPWRGD.

PD# Deassertion

The power up latency is less than 1.8 ms. This is the time from the deassertion of the PD# pin or the ramping of the power supply until the time that stable clocks are generated from the clock chip. All differential outputs stopped in a three-state condition, resulting from power down are driven high in less than 300 μs of PD# deassertion to a voltage greater than 200 mV. After the clock chip's internal PLL is powered up and locked, all outputs are enabled within a few clock cycles of each clock. Figure 4 is an example showing the relationship of clocks coming up.

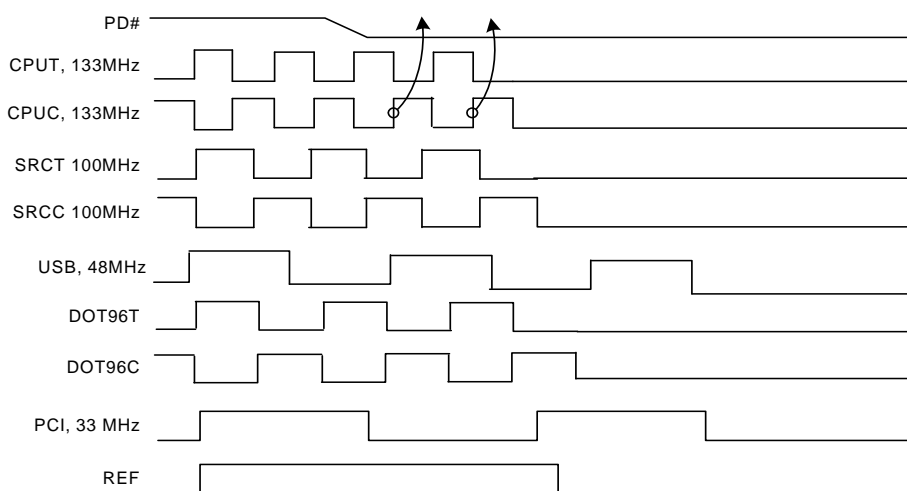


Figure 3. Power down Assertion Timing Waveform

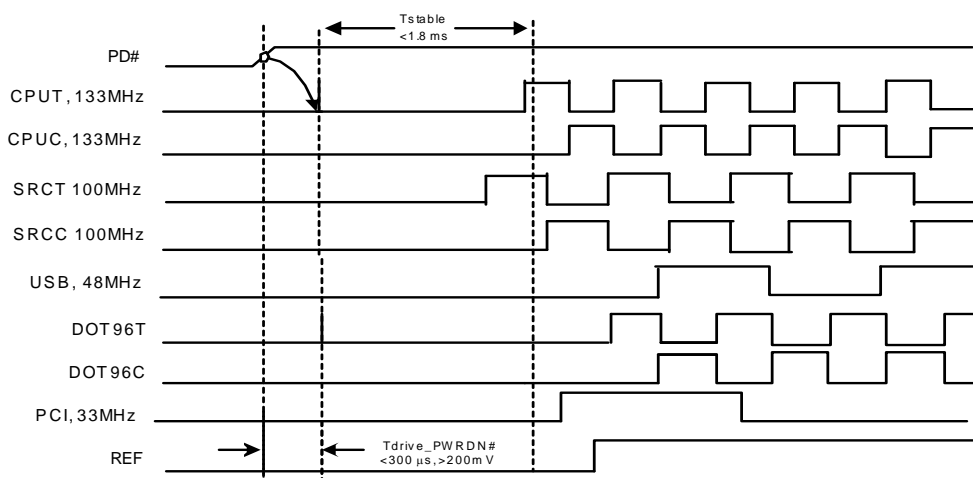


Figure 4. Power down Deassertion Timing Waveform

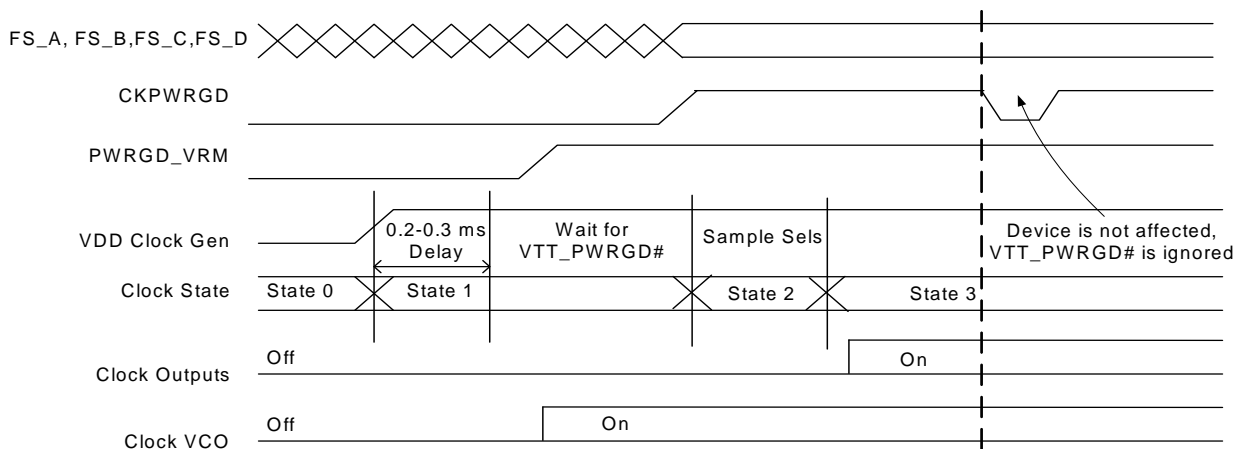


Figure 5. CKPWRGD Timing Diagram

CPU_STP# Assertion

The CPU_STP# signal is an active LOW input used for synchronous stopping and starting the CPU output clocks while the rest of the clock generator continues to function. When the CPU_STP# pin is asserted, all CPU outputs that are set with the SMBus configuration to be stoppable are stopped within two to six CPU clock periods after sampled by two rising edges of the internal CPUC clock. The final states of the stopped CPU signals are CPUT = HIGH and CPUC = LOW.

CPU_STP# Deassertion

The deassertion of the CPU_STP# signal causes all stopped CPU outputs to resume normal operation in a synchronous manner. No short or stretched clock pulses are produced when the clock resumes. The maximum latency from the deassertion to active outputs is no more than two CPU clock cycles.

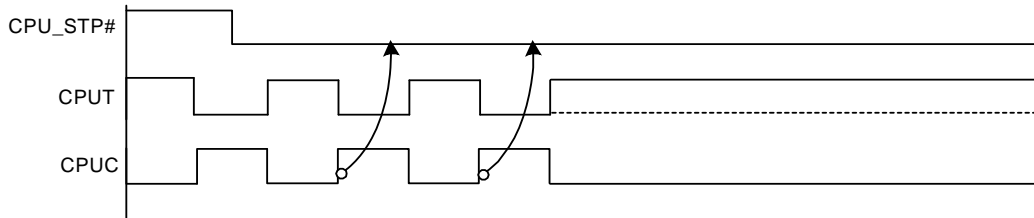


Figure 6. CPU_STP# Assertion Waveform

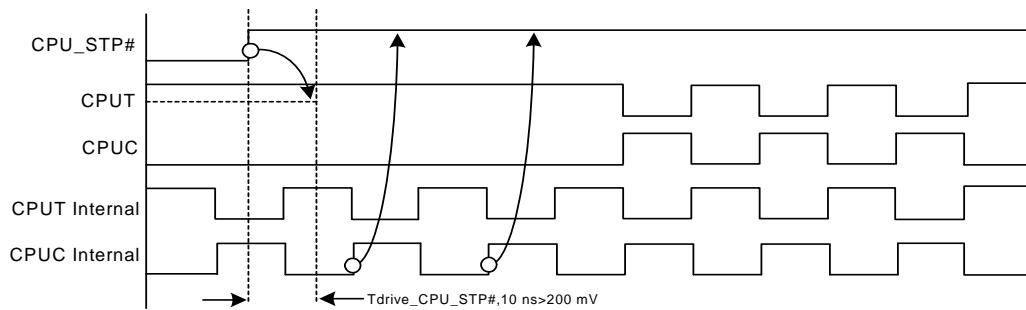


Figure 7. CPU_STP# Deassertion Waveform

PCI/SRC_STP# Assertion

The PCI/SRC_STP# signal is an active LOW input used for synchronously stopping and starting the PCI outputs while the rest of the clock generator continues to function. The set-up time for capturing PCI/SRC_STP# going LOW is 10 ns (t_{SU}). (See Figure 8.) The PCIF and SRC clocks are affected by this pin if their corresponding control bit in the SMBus register is set to allow them to be free running. For SRC clocks assertion description, please refer to CPU_STP# description.

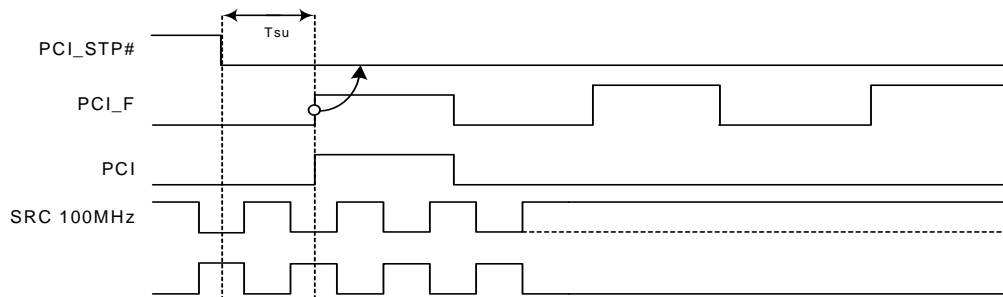


Figure 8. PCI_STP# Assertion Waveform

PCI/SRC_STP# Deassertion

The deassertion of the PCI/SRC_STP# signal causes all PCI and stoppable PCIF to resume running in a synchronous manner within two PCI clock periods, after PCI/SRC_STP# transitions to a HIGH level. Similarly, PCI/SRC_STP# deassertion will cause stoppable SRC clocks to resume running. For SRC clocks deassertion description, please refer to CPU_STP# description.

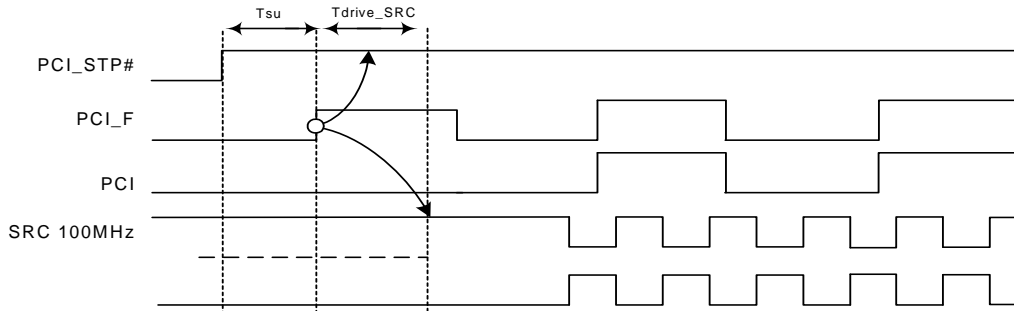


Figure 9. PCI_STP# Deassertion Waveform

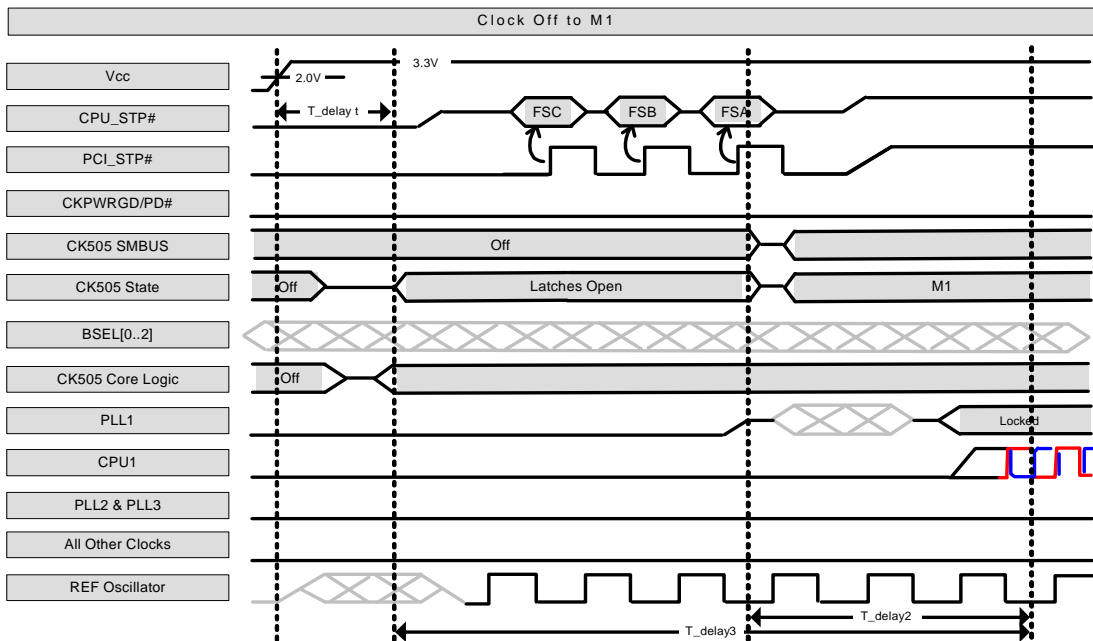


Figure 10. BSEL Serial Latching

Absolute Maximum Conditions

| Parameter | Description | Condition | Min. | Max. | Unit |
|----------------------|-----------------------------------|-----------------------------|------|------|-----------------|
| V _{DD_3.3V} | Main Supply Voltage | Functional | – | 4.6 | V |
| V _{IN} | Input Voltage | Relative to V _{SS} | –0.5 | 4.6 | V _{DC} |
| T _S | Temperature, Storage | Non-functional | –65 | 150 | °C |
| T _A | Temperature, Operating Ambient | Functional | –40 | 85 | °C |
| T _J | Temperature, Junction | Functional | – | 150 | °C |
| ∅ _{JC} | Dissipation, Junction to Case | JEDEC (JESD 51) | – | 20 | °C/W |
| ∅ _{JA} | Dissipation, Junction to Ambient | JEDEC (JESD 51) | – | 60 | °C/W |
| ESD _{HBM} | ESD Protection (Human Body Model) | JEDEC (JESD 22 - A114) | 2000 | – | V |
| UL-94 | Flammability Rating | UL (Class) | V-0 | | |

Multiple Supplies: The Voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.

DC Electrical Specifications

| Parameter | Description | Condition | Min. | Max. | Unit |
|----------------------|-------------------------------|--|-----------------------|-----------------------|------|
| VDD core | 3.3V Operating Voltage | 3.3 ± 5% | 3.135 | 3.465 | V |
| V _{IH} | 3.3V Input High Voltage (SE) | | 2.0 | V _{DD} + 0.3 | V |
| V _{IL} | 3.3V Input Low Voltage (SE) | | V _{SS} – 0.3 | 0.8 | V |
| V _{IHI2C} | Input High Voltage | SDATA, SCLK | 2.2 | – | V |
| V _{ILI2C} | Input Low Voltage | SDATA, SCLK | – | 1.0 | V |
| V _{IH_FS} | FS Input High Voltage | | 0.7 | VDD+0.3 | V |
| V _{IL_FS} | FS Input Low Voltage | | V _{SS} – 0.3 | 0.35 | V |
| I _{IH} | Input High Leakage Current | Except internal pull-down resistors, 0 < V _{IN} < V _{DD} | – | 5 | μA |
| I _{IL} | Input Low Leakage Current | Except internal pull-up resistors, 0 < V _{IN} < V _{DD} | –5 | – | μA |
| V _{OH} | 3.3V Output High Voltage (SE) | I _{OH} = –1 mA | 2.4 | – | V |
| V _{OL} | 3.3V Output Low Voltage (SE) | I _{OL} = 1 mA | – | 0.4 | V |
| I _{OZ} | High-impedance Output Current | | –10 | 10 | μA |
| C _{IN} | Input Pin Capacitance | | 1.5 | 5 | pF |
| C _{OUT} | Output Pin Capacitance | | | 6 | pF |
| L _{IN} | Pin Inductance | | – | 7 | nH |
| V _{XIH} | Xin High Voltage | | 0.7V _{DD} | V _{DD} | V |
| V _{XIL} | Xin Low Voltage | | 0 | 0.3V _{DD} | V |
| I _{DD_PD} | Power Down Current | | – | 1 | mA |
| I _{DD_3.3V} | Dynamic Supply Current | All outputs enabled. SE clocks with 8" traces. Differential clocks with 7" traces. Loading per CK505 spec. | – | 130 | mA |



AC Electrical Specifications

| Parameter | Description | Condition | Min. | Max. | Unit |
|---------------------------------|-------------------------------------|---|-----------|----------|------|
| Crystal | | | | | |
| T _{DC} | XIN Duty Cycle | The device will operate reliably with input duty cycles up to 30/70 but the REF clock duty cycle will not be within specification | 47.5 | 52.5 | % |
| T _{PERIOD} | XIN Period | When XIN is driven from an external clock source | 69.841 | 71.0 | ns |
| T _R /T _F | XIN Rise and Fall Times | Measured between 0.3V _{DD} and 0.7V _{DD} | – | 10.0 | ns |
| T _{CCJ} | XIN Cycle to Cycle Jitter | As an average over 1-μs duration | – | 500 | ps |
| L _{ACC} | Long-term Accuracy | Measured at VDD/2 differential | – | 250 | ppm |
| L _{ACC} | Long-term Accuracy | Measured at VDD/2 differential | – | 250 | ppm |
| Clock Input | | | | | |
| T _{DC} | CLKIN Duty Cycle | Measured at VDD/2 | 47 | 53 | % |
| T _R /T _F | CLKIN Rise and Fall Times | Measured between 0.2V _{DD} and 0.8V _{DD} | 0.5 | 4.0 | V/ns |
| T _{CCJ} | CLKIN Cycle to Cycle Jitter | Measured at VDD/2 | – | 250 | ps |
| T _{LTJ} | CLKIN Long Term Jitter | Measured at VDD/2 | – | 350 | ps |
| V _{IL} | Input Low Voltage | XIN / CLKIN pin | – | 0.8 | V |
| V _{IH} | Input High Voltage | XIN / CLKIN pin | 2 | VDD+0.3 | V |
| I _{IL} | Input LowCurrent | XIN / CLKIN pin, 0 < VIN <0.8 | – | 20 | uA |
| I _{IH} | Input HighCurrent | XIN / CLKIN pin, VIN = VDD | – | 35 | uA |
| CPU at 0.7V | | | | | |
| T _{DC} | CPU Duty Cycle | Measured at 0V differential | 45 | 55 | % |
| T _{PERIOD} | 83.33 MHz CPU Period | Measured at 0V differential at 0.1s | 11.99880 | 12.00120 | ns |
| T _{PERIODSS} | 83.33 MHz CPU Period, SSC | Measured at 0V differential at 0.1s | 12.028872 | 12.03128 | ns |
| T _{PERIODAbs} | 83.33 MHz CPU Absolute Period | Measured at 0V differential at 1clock | 11.18969 | 12.16344 | ns |
| T _{PERIODSSAbs} | 83.33 MHz CPU Absolute Period, SSC | Measured at 0V differential at 1 clock | 11.89687 | 12.16344 | ns |
| T _{PERIOD} | 100 MHz CPU Period | Measured at 0V differential at 0.1s | 9.99900 | 10.0010 | ns |
| T _{PERIODSS} | 100 MHz CPU Period, SSC | Measured at 0V differential at 0.1s | 10.02406 | 10.02607 | ns |
| T _{PERIODAbs} | 100 MHz CPU Absolute Period | Measured at 0V differential at 1clock | 9.87400 | 10.1260 | ns |
| T _{PERIODSSAbs} | 100 MHz CPU Absolute Period, SSC | Measured at 0V differential at 1 clock | 9.87406 | 10.1762 | ns |
| T _{PERIOD} | 133 MHz CPU Period | Measured at 0V differential at 0.1s | 7.49925 | 7.50075 | ns |
| T _{PERIODSS} | 133 MHz CPU Period, SSC | Measured at 0V differential at 0.1s | 7.51804 | 7.51955 | ns |
| T _{PERIODAbs} | 133 MHz CPU Absolute period | Measured at 0V differential at 1 clock | 7.41425 | 7.58575 | ns |
| T _{PERIODSSAbs} | 133 MHz CPU Absolute period, SSC | Measured at 0V differential at1 clock | 7.41430 | 7.62340 | ns |
| T _{PERIOD} | 166 MHz CPU Period | Measured at 0V differential at 0.1s | 5.99940 | 6.00060 | ns |
| T _{PERIODSS} | 166 MHz CPU Period, SSC | Measured at 0V differential at 0.1s | 6.01444 | 6.01564 | ns |
| T _{PERIODAbs} | 166 MHz CPU Absolute period | Measured at 0V differential at 1 clock | 5.91440 | 6.08560 | ns |
| T _{PERIODSSAbs} | 166 MHz CPU Absolute period, SSC | Measured at 0V differential at 1 clock | 5.91444 | 6.11572 | ns |
| T _{CCJ} | CPU Cycle to Cycle Jitter | Measured at 0V differential | – | 85 | ps |
| T _{CCJ (CPU2)} | CPU Cycle to Cycle Jitter for CPU 2 | Measured at 0V differential | – | 125 | ps |
| Skew | CPU0 to CPU1 skew | Measured at 0V differential | – | 100 | ps |
| L _{ACC} | Long-term Accuracy | Measured at 0V differential | – | 100 | ppm |
| T _R / T _F | CPU Rising/Falling Slew rate | Measured differentially from ±150 mV | 2.5 | 8 | V/ns |
| T _{RFM} | Rise/Fall Matching | Measured single-endedly from ±75 mV | – | 20 | % |
| V _{HIGH} | Voltage High | | | 1.15 | V |
| V _{LOW} | Voltage Low | | –0.3 | – | V |



AC Electrical Specifications (continued)

| Parameter | Description | Condition | Min. | Max. | Unit |
|---------------------------------|--|--|----------|----------|------|
| V _{OX} | Crossing Point Voltage at 0.7V Swing | | 300 | 550 | mV |
| SRC at 0.7V | | | | | |
| T _{DC} | SRC Duty Cycle | Measured at 0V differential | 45 | 55 | % |
| T _{PERIOD} | 100 MHz SRC Period | Measured at 0V differential at 0.1s | 9.99900 | 10.0010 | ns |
| T _{PERIODSS} | 100 MHz SRC Period, SSC | Measured at 0V differential at 0.1s | 10.02406 | 10.02607 | ns |
| T _{PERIODAbs} | 100 MHz SRC Absolute Period | Measured at 0V differential at 1 clock | 9.87400 | 10.1260 | ns |
| T _{PERIODSSAbs} | 100 MHz SRC Absolute Period, SSC | Measured at 0V differential at 1 clock | 9.87406 | 10.1762 | ns |
| T _{SKEW(window)} | Any SRC Clock Skew from the earliest bank to the latest bank | Measured at 0V differential | – | 3.0 | ns |
| T _{CCJ} | SRC Cycle to Cycle Jitter | Measured at 0V differential | – | 125 | ps |
| L _{ACC} | SRC Long Term Accuracy | Measured at 0V differential | – | 100 | ppm |
| T _R / T _F | SRC Rising/Falling Slew Rate | Measured differentially from ±150 mV | 2.5 | 8 | V/ns |
| T _{RFM} | Rise/Fall Matching | Measured single-endedly from ±75 mV | – | 20 | % |
| V _{HIGH} | Voltage High | | | 1.15 | V |
| V _{LOW} | Voltage Low | | –0.3 | – | V |
| V _{OX} | Crossing Point Voltage at 0.7V Swing | | 300 | 550 | mV |
| DOT96 at 0.7V | | | | | |
| T _{DC} | DOT96 Duty Cycle | Measured at 0V differential | 45 | 55 | % |
| T _{PERIOD} | DOT96 Period | Measured at 0V differential at 0.1s | 10.4156 | 10.4177 | ns |
| T _{PERIODAbs} | DOT96 Absolute Period | Measured at 0V differential at 0.1s | 10.1656 | 10.6677 | ns |
| T _{CCJ} | DOT96 Cycle to Cycle Jitter | Measured at 0V differential at 1 clock | – | 250 | ps |
| L _{ACC} | DOT96 Long Term Accuracy | Measured at 0V differential at 1 clock | – | 100 | ppm |
| T _R / T _F | DOT96 Rising/Falling Slew Rate | Measured differentially from ±150 mV | 2.5 | 8 | V/ns |
| T _{RFM} | Rise/Fall Matching | Measured single-endedly from ±75 mV | – | 20 | % |
| V _{HIGH} | Voltage High | | | 1.15 | V |
| V _{LOW} | Voltage Low | | –0.3 | – | V |
| V _{OX} | Crossing Point Voltage at 0.7V Swing | | 300 | 550 | mV |
| SATA75M at 0.7V | | | | | |
| T _{DC} | SATA75M Duty Cycle | Measured at 0V differential | 45 | 55 | % |
| T _{CCJ} | SATA75M Cycle to Cycle Jitter | Measured at 0V differential at 1 clock | – | 125 | ps |
| L _{ACC} | SATA75M Long Term Accuracy | Measured at 0V differential at 1 clock | – | 100 | ppm |
| T _R / T _F | SATA75M Rising/Falling Slew Rate | Measured differentially from ±150 mV | 2.5 | 8 | V/ns |
| T _{RFM} | Rise/Fall Matching | Measured single-endedly from ±75 mV | – | 20 | % |
| V _{HIGH} | Voltage High | | | 1.15 | V |
| V _{LOW} | Voltage Low | | –0.3 | – | V |
| V _{OX} | Crossing Point Voltage at 0.7V Swing | | 300 | 550 | mV |
| PCI/PCIF at 3.3V | | | | | |
| T _{DC} | PCI Duty Cycle | Measurement at 1.5V | 45 | 55 | % |
| T _{PERIOD} | Spread Disabled PCIF/PCI Period | Measurement at 1.5V | 29.99700 | 30.00300 | ns |
| T _{PERIODSS} | Spread Enabled PCIF/PCI Period | Measurement at 1.5V | 30.08421 | 30.23459 | ns |
| T _{PERIODAbs} | Spread Disabled PCIF/PCI Period | Measurement at 1.5V | 29.49700 | 30.50300 | ns |
| T _{PERIODSSAbs} | Spread Enabled PCIF/PCI Period | Measurement at 1.5V | 29.56617 | 30.58421 | ns |
| T _{HIGH} | Spread Enabled PCIF and PCI high time | Measurement at 2V | 12.27095 | 16.27995 | ns |
| T _{LOW} | Spread Enabled PCIF and PCI low time | Measurement at 0.8V | 11.87095 | 16.07995 | ns |

AC Electrical Specifications (continued)

| Parameter | Description | Condition | Min. | Max. | Unit |
|--|--|--------------------------------|----------|----------|------|
| T _{HIGH} | Spread Disabled PCIF and PCI high time | Measurement at 2.0V | 12.27365 | 16.27665 | ns |
| T _{LOW} | Spread Disabled PCIF and PCI low time | Measurement at 0.8V | 11.87365 | 16.07665 | ns |
| T _R / T _F | PCIF/PCI Rising/Falling Slew Rate | Measured between 0.8V and 2.0V | 1.0 | 4.0 | V/ns |
| T _{SKEW} | Any PCI clock to Any PCI clock Skew | Measurement at 1.5V | – | 250 | ps |
| T _{CCJ} | PCIF and PCI Cycle to Cycle Jitter | Measurement at 1.5V | – | 300 | ps |
| L _{ACC} | PCIF/PCI Long Term Accuracy | Measurement at 1.5V | – | 100 | ppm |
| 48M, 12_48M at 3.3V | | | | | |
| T _{DC} | Duty Cycle | Measurement at 1.5V | 45 | 55 | % |
| T _{PERIOD} | 48MHz Period | Measurement at 1.5V | 20.83125 | 20.83542 | ns |
| T _{PERIODAbs} | 48MHz Absolute Period | Measurement at 1.5V | 20.48125 | 21.18542 | ns |
| T _{HIGH} | 48MHz High time | Measurement at 2V | 8.216563 | 11.15198 | ns |
| T _{LOW} | 48MHz Low time | Measurement at 0.8V | 7.816563 | 10.95198 | ns |
| T _R / T _F (48M) | Rising and Falling Edge Rate | Measured between 0.8V and 2.0V | 1.0 | 2.0 | V/ns |
| T _R / T _F (12_48M) | Rising and Falling Edge Rate | Measured between 0.8V and 2.0V | 1.0 | 2.0 | V/ns |
| T _{CCJ} | Cycle to Cycle Jitter | Measurement at 1.5V | – | 300 | ps |
| L _{ACC} | Long Term Accuracy | Measurement at 1.5V | – | 100 | ppm |
| 25M at 3.3V | | | | | |
| T _{DC} | Duty Cycle | Measurement at 1.5V | 45 | 55 | % |
| T _{PERIOD} | Period | Measurement at 1.5V | 39.996 | 40.004 | ns |
| T _{PERIODAbs} | Absolute Period | Measurement at 1.5V | 39.32360 | 40.67640 | ns |
| T _R / T _F | Rising and Falling Edge Rate | Measured between 0.8V and 2.0V | 1.0 | 4.0 | V/ns |
| T _{CCJ} | Cycle to Cycle Jitter | Measurement at 1.5V | – | 300 | ps |
| L _{ACC} | Long Term Accuracy | Measured at 1.5V | – | 100 | ppm |
| 14.318M, at 3.3V | | | | | |
| T _{DC} | Duty Cycle | Measurement at 1.5V | 45 | 55 | % |
| T _{PERIOD} | Period | Measurement at 1.5V | 69.82033 | 69.86224 | ns |
| T _{PERIODAbs} | Absolute Period | Measurement at 1.5V | 68.83429 | 70.84826 | ns |
| T _{HIGH} | High time | Measurement at 2V | 29.97543 | 38.46654 | ns |
| T _{LOW} | Low time | Measurement at 0.8V | 29.57543 | 38.26654 | ns |
| T _R / T _F | Rising and Falling Edge Rate | Measured between 0.8V and 2.0V | 1.0 | 4.0 | V/ns |
| T _{CCJ} | Cycle to Cycle Jitter | Measurement at 1.5V | – | 500 | ps |
| L _{ACC} | Long Term Accuracy | Measurement at 1.5V | – | 100 | ppm |
| ENABLE/DISABLE and SET-UP | | | | | |
| T _{STABLE} | Clock Stabilization from Power-up | | – | 1.8 | ms |
| T _{SS} | Stopclock Set-up Time | | 10.0 | – | ns |

Test and Measurement Set-up

For Single Ended Clocks

The following diagram shows the test load configurations for the single-ended output signals.

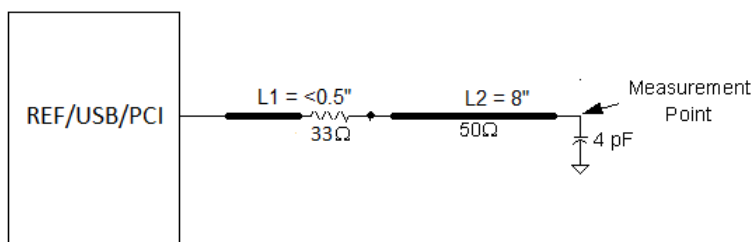


Figure 11. Single-ended clocks Single Load Configuration

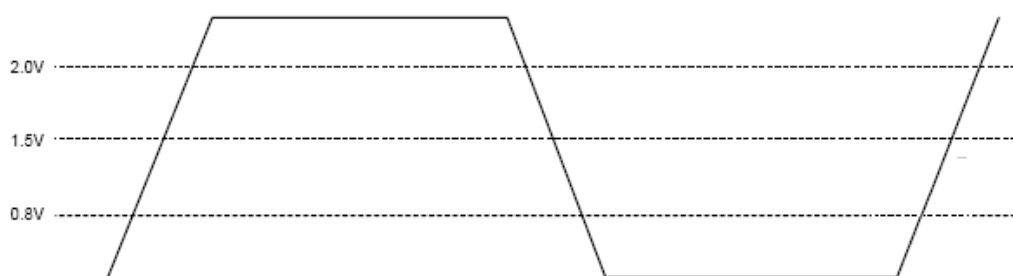


Figure 12. Single-ended Output Signals (for AC Parameters Measurement)

For Differential Clock Signals

This diagram shows the test load configuration for the differential clock signals

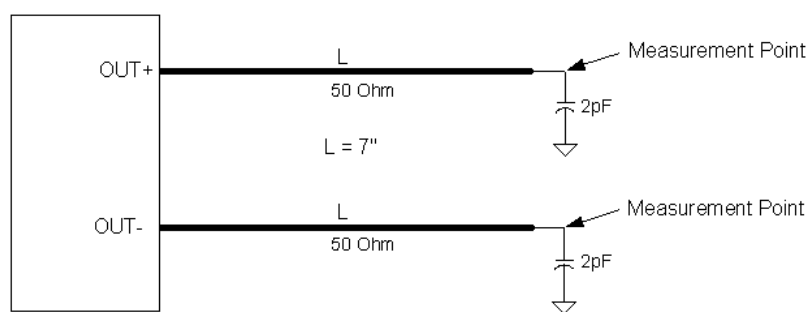


Figure 13. 0.7V Differential Load Configuration

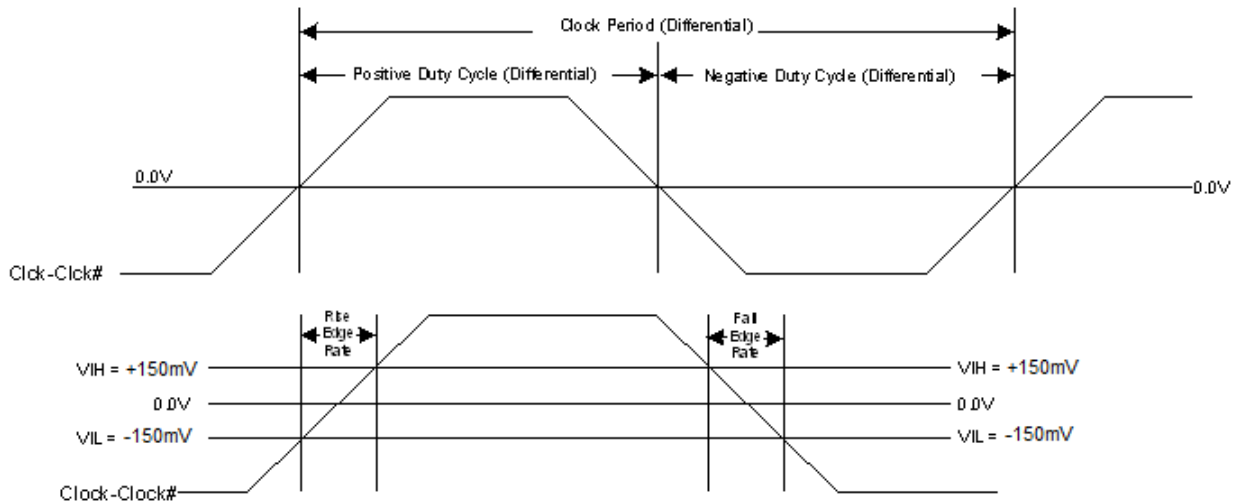


Figure 14. Differential Measurement for Differential Output Signals (for AC Parameters Measurement)

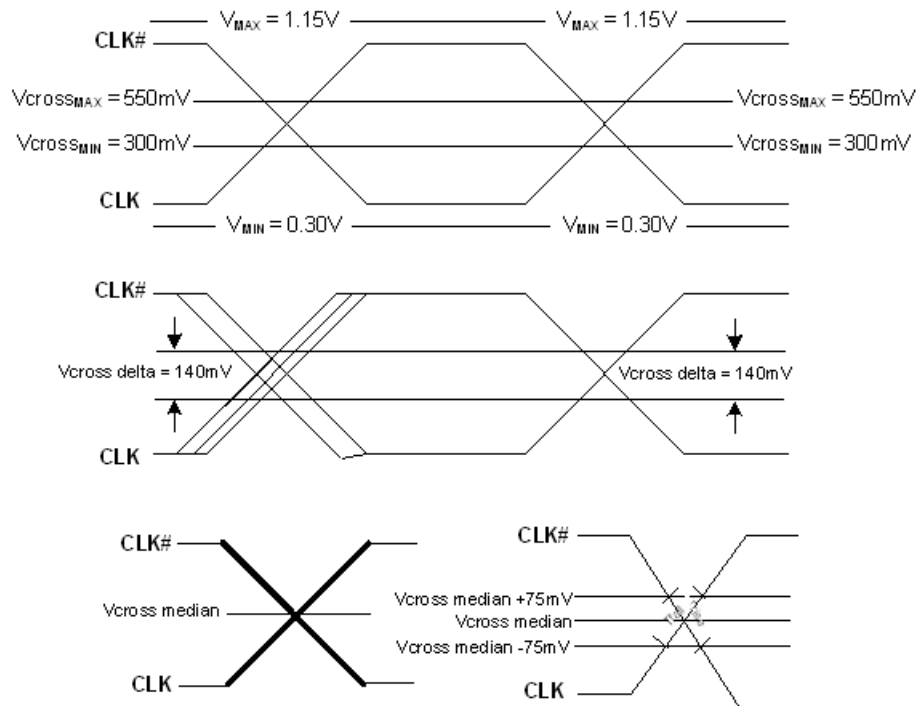


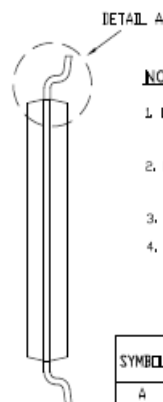
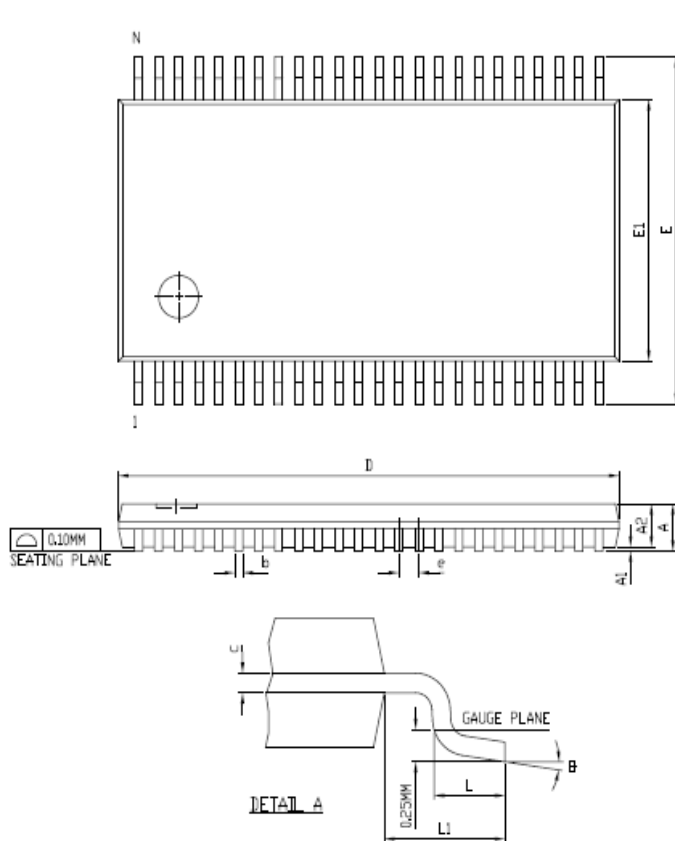
Figure 15. Single-ended Measurement for Differential Output Signals (for AC Parameters Measurement)

Ordering Information

| Part Number | Package Type | Product Flow |
|------------------|-----------------------------|--------------------------|
| Lead-free | | |
| SL28EB719ALI | 48-pin TSSOP | Industrial, -40° to 85°C |
| SL28EB719ALIT | 48-pin TSSOP– Tape and Reel | Industrial, -40° to 85°C |

Package Diagrams

48-Lead TSSOP



NOTES

1. LEAD WIDTH AND LEAD THICKNESS EXCLUSIVE OF SOLDER PLATE
2. PACKAGE OUTLINE EXCLUSIVE OF MOLD FLASHES AND BURR DIMENSIONS
3. ALLOWABLE MOLD FLASH IS 5 MILS PER SIDE.
4. LEAD COPLANARITY IS 0.003 INCH MAX.

| SYMBOL | DIMENSION IN MM | | | DIMENSION IN INCH | | |
|--------|---------------------------|-------|-------|-------------------|------|------|
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A | | | 1.20 | | | .047 |
| A1 | 0.05 | | 0.15 | .002 | | .006 |
| A2 | 0.80 | 1.00 | 1.05 | .031 | .039 | .041 |
| D | 12.40 | 12.50 | 12.60 | .488 | .492 | .496 |
| E | 8.00 | 8.10 | 8.20 | .315 | .319 | .323 |
| E1 | 6.00 | 6.10 | 6.20 | .236 | .240 | .244 |
| L | 0.45 | 0.60 | 0.75 | .018 | .024 | .030 |
| L1 | 1.00 REF. | | | .039 REF. | | |
| b | 0.10 | 0.20 | 0.25 | .007 | .008 | .010 |
| e | 0.50 BSC. | | | .020 BSC. | | |
| c | 0.09 | | 0.20 | .004 | | .008 |
| Φ | 0 | | 8 | 0 | | 8 |
| N | 48 | | | | | |
| REF | JEDEC MO-153 VARIATION ED | | | | | |

Document History Page

| Document Title: SL28EB719 PC EProClock® Generator for Intel Tunnel Creek & Top Cliff | | | | |
|---|-------------|-------------------|------------------------|--|
| DOC#: SP-AP-0005 (Rev. AB) | | | | |
| REV. | ECR# | Issue Date | Orig. of Change | Description of Change |
| AA | 1458 | 03/17/10 | JMA | Initial Release |
| AB | 1640 | 06/23/10 | JMA | <ol style="list-style-type: none"> 1. Added CLKIN feature 2. Added Period Spec for CPU, SRC, and DOT96 3. Added Cycle-to-cycle jitter spec for CPU2/SRC5 (ITP clock) 4. Removed REF wording from 14.318MHz 5. Reduced IDD to 130mA from 200mA 6. Reduced PCI clocks cycle-to-cycle jitter to 300ps from 500ps 7. Reduced 25MHzclock cycle-to-cycle jitter to 300ps from 500ps 8. Reduced 48/12MHz clocks cycle-to-cycle jitter to 300ps from 350ps 9. Reduced 14.318MHz clock cycle-to-cycle jitter to 500ps from 1000ps 10. Reduced SATA75 clock cycle-to-cycle jitter to 125ps from 250ps 11. Removed skew for 14MHz 12. Updated CPU2 Cycle-to-cycle jitter to be 125ps from 85ps 13. Updated Package information 14. Added PD# label to pin configuration on page 1 15. Updated MIL-STD to JEDEC 16. Removed Preliminary wording 17. Added period spec for 83.33, 133, and 166MHz 18. Updated block diagram |

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